DESIGNER'S REFERENCE MANUAL

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Analog Switches & Multiplexers

Comparators

D/A Converters

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Introduction

Analog Devices is a semiconductor company with over one billion dollars in annual sales that designs, manufactures and sells worldwide sophisticated integrated circuits, electronic components and subsystems for use in real-world signal processing. More than one thousand standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several forms of CMOS, BiCMOS, bipolar, and hybrid integrated circuits, each optimized for specific attributes—as well as several types of assembled subsystem products.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional through-hole and surface-mount packages (SOIC, LCC, SOT, SSOP, PLCC, and others) as well as some of the newer high density power surface-mount packages. Over thirty years of successful applications experience and continuing vertical integration ensure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the creation of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and also make us strong contenders in high performance mixed-signal ICs for advanced computing and communications applications.

MAJOR PROGRESS

Since the publication of the selection guides in the *Design-In Reference Manual* in late 1994, Analog Devices has introduced more than 150 new products; they cover the range from brand new product and market categories and technologies to standard products (with improvements in price, performance, or design) to augmented performance second source products. The greatest emphasis has been in the area of single-supply design for 3- and 5-volt requirements at lower and lower power levels, while continuing to push the performance and adding critical features. All of our newest products from all of the product areas of the company are included in this volume.

Examples of the variety, performance, and innovation of the outstanding new linear, data converter, and DSP products to be found in this volume include the:

ADP1148 family of high efficiency, synchronous step-down switching regulators that function properly down to a 3.5 volt input voltage and provide very low dropout operation.

AD815 high output current differential driver amplifiers with 900 V/μs slew rate and 200 mA output drive from a thermally enhanced SOIC—ideal for ADSL and HDSL line interface drive applications.

AD215 low distortion isolation amplifiers with 120 kHz bandwidth and full isolation to 1500 volts and –80 dB harmonic distortion.

ADSP-21060/ADSP-21062 SHARC Super Harvard Architecture Computer with 4 MBit/2 MBit on-chip SRAM and 40 MIPS/ 80 MFLOPS performance for high performance signal processing.

AD1843 16-bit serial-port SoundComm™ Codec integrated speech, audio, fax and modem codec for computer audio, V.34, and voice over data applications.

AD9220 complete 12-bit 10 MSPS ADC that works on a +5 V supply with only 250 mW—other family members use only 60 mW at 1 MHz.

AD9830 complete 50 MHz direct digital synthesizer (DDS) with numerically controlled oscillator and 10-bit DAC.

ADM207E Family of EMI/EMC compliant, ±15 kV ESD protected, RS-232 line drivers and receivers with 230 kbits/sec guaranteed data rate.

AD8402/8403 two- and four-channel digital potentiometers in 10 kΩ, 50 kΩ, and 100 kΩ formats and 2.7 volt supply operation.

AD7896 12-bit serial-interface, 100 kHz sampling ADC in 8-pin SOIC with 2.7 V supply operation using 9 mW.

DESIGNER'S REFERENCE MANUAL

This volume provides technical data on the product features and specifications on all the products we recommend for new design requirements for all of the markets we serve. This is a companion volume and update to the series of Reference Manuals we began publishing in 1992. These manuals include the two-volume *Data Converter Reference Manual, Amplifier Reference Manual, Special Linear Reference Manual, Applications Reference Manual, Military/ Aerospace Reference Manual, DSP/MSP Products Reference Manual,* and *Design-In Reference Manual (1994)*. All of the data sheets in this volume are two pages in length, containing information on the key features and specifications on each product, but not the detailed applications information. On products introduced prior to 1995, this information is contained in those previously released reference manuals. As a result, it is important to retain the entire set of Reference Manuals to have the complete applications information about these products. For our newer products, the longer data sheets with all of the details about these products are available on the CD-ROM Catalog, which is a companion to this volume. This information is also available from our World Wide Web site at http://www.analog.com and from *AnalogFax*™, our automated fax retrieval system. The most up-to-date data sheets on all of our currently available products are also available on all three of these media. Any of our previous reference manuals or the CD-ROM can be ordered from our Literature Center or any sales office worldwide.

In the approximately 1200 pages of this volume you will find:

- A two-page data sheet for all products that we currently recommend for new system design requirements. These data sheets provide information on the key features, pinouts, block diagrams, and specifications for these products.
- Advance technical information on upcoming new products which may prompt you to seek more up-to-date information on the product.
- Selection guides and product function trees for finding products rapidly.
- Faxcodes on every product referenced that allow you to get a full-length data sheet with complete applications information on the product from AnalogFax.

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- A representative list of available Analog Devices technical publications on real-world analog and digital signal processing.
- A complete set of drawings of all of the packages presently in use by Analog Devices for our products and references to these packages in each of the data sheets in this volume.
- Our Worldwide Sales Directory.
- The complete Product Index to all Analog Devices products referenced in this manual including those soon to be released.

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, existing and available products that offer little if any unique advantage over newer products in future designs are not listed in the Index; their data sheets are still available separately through our CD-Catalog or *AnalogFax* system—but they are not published in this book.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our reference manuals, we offer application notes, application guides, technical handbooks (at reasonable prices), and several free serial publications. For example, *Analog Briefings*® provides current information about products for military/avionics applications, and *Analog Dialogue,* our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, test, and communications. *DSPatch*® is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to reference manuals and general short form selection guides, we also publish several short form catalogs and selection guides on specific product families.

Analog Devices also provides in-depth technical support through field applications engineers, our sales offices and a network of applications engineers available at our factory locations to discuss our products and your applications. A call to our central number in Norwood, Massachusetts, at 1-800-ANALOGD will be directed to the engineer most closely associated with your interests. We have also installed a World Wide Web site on the Internet and several fax-on-demand systems around the world to provide current in-depth technical information fast.

SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices, representatives, and distributors throughout the United States and the world staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, current as of the publication date, appears on pages 30–14 and 30–15 at the back of the book.

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RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is the companywide commitment to Total Quality Management (TQM). In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the United States and MIL-STD-1772 for hybrids. Our major facilities have also been certified to ISO-9000 and QS9000.

Many of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process of qualification. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military/Aerospace Reference Manual* for designers who specify ICs and hybrids for military programs. The 1994 issue contains data on 378 product families. A newsletter, *Analog Briefings*, provides current information about the status of reliability at ADI.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to standard products most likely to be used for the design of new circuits and systems. These products represent about half of the total product offerings that we manufacture and sell. Omission of a product from the current selection guides in no way indicates that such a product is nearing the end of its life cycle, most are likely to be manufactured for years to come. If the model number of a product you are interested in is not in the Table of Contents or selection guides, turn to page 30–4 where you will find a list of older products that are still currently manufactured. Data sheets for these products are available on request or can be found through AnalogFax, our Web site, or the CD-Catalog. On page 30–5 you will find a guide to substitutions (where possible) for products that are no longer available.

OBSOLETE GRADES OF ACTIVE PRODUCT FAMILIES

Due to changes in demand for particular grades of an active product family, it is occasionally necessary to discontinue grades and/or package combinations of that product family without discontinuing the entire family. The timing of these occurrences precludes this catalog from necessarily having the most accurate production status information. The user should therefore not assume that every grade and package combination listed for a given family is currently available. For the most current availability information, consult our current price list or an Analog Devices sales office or distributor.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors.

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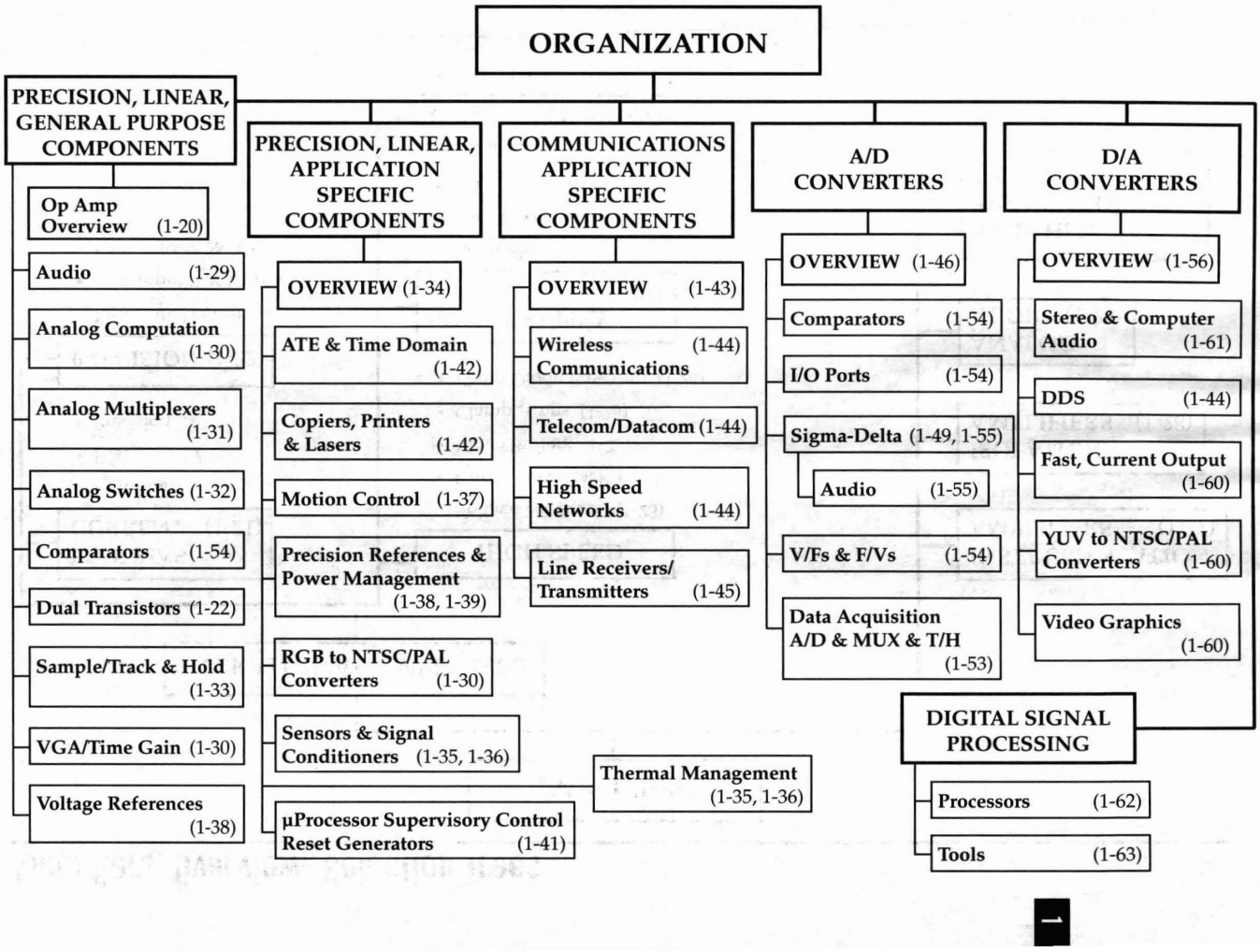
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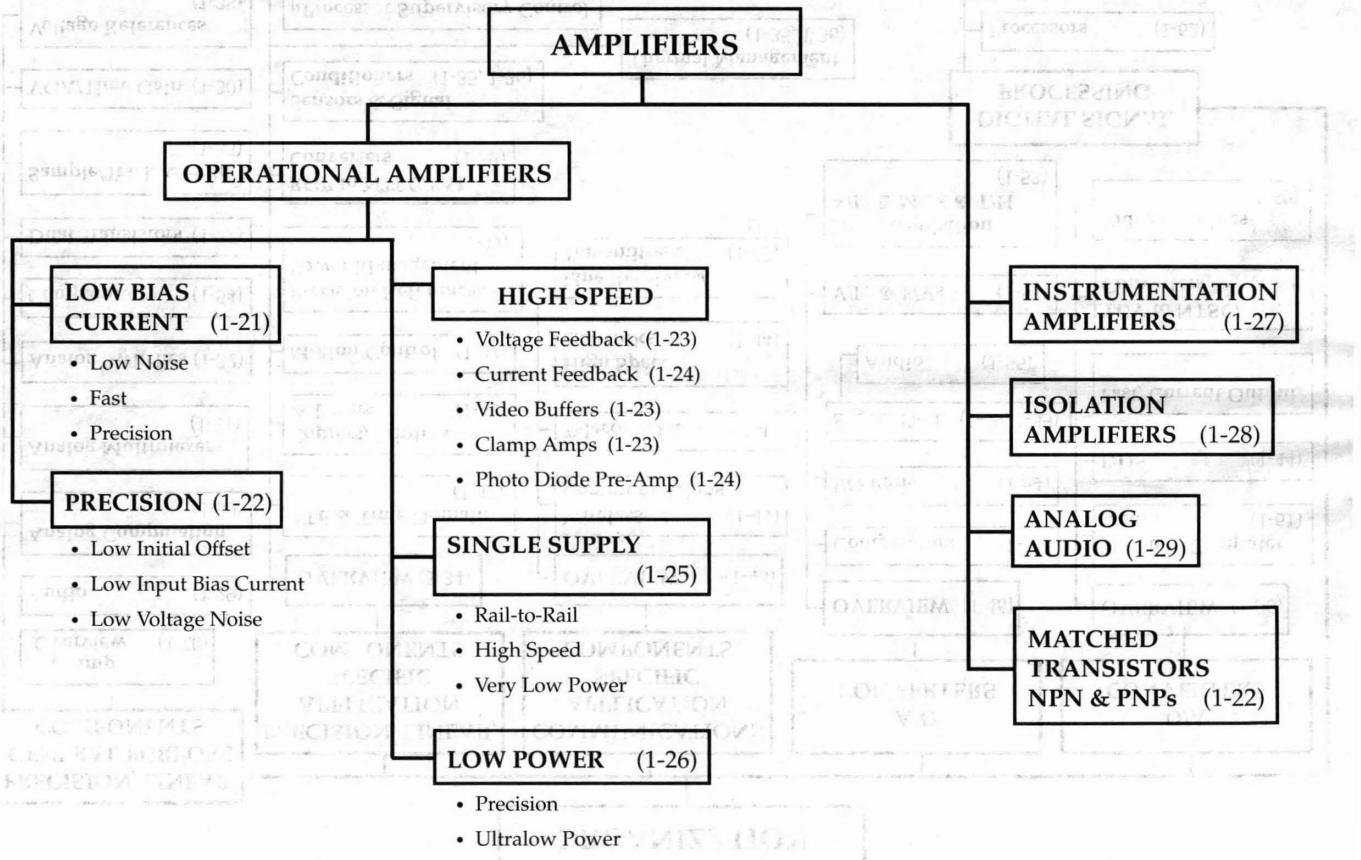

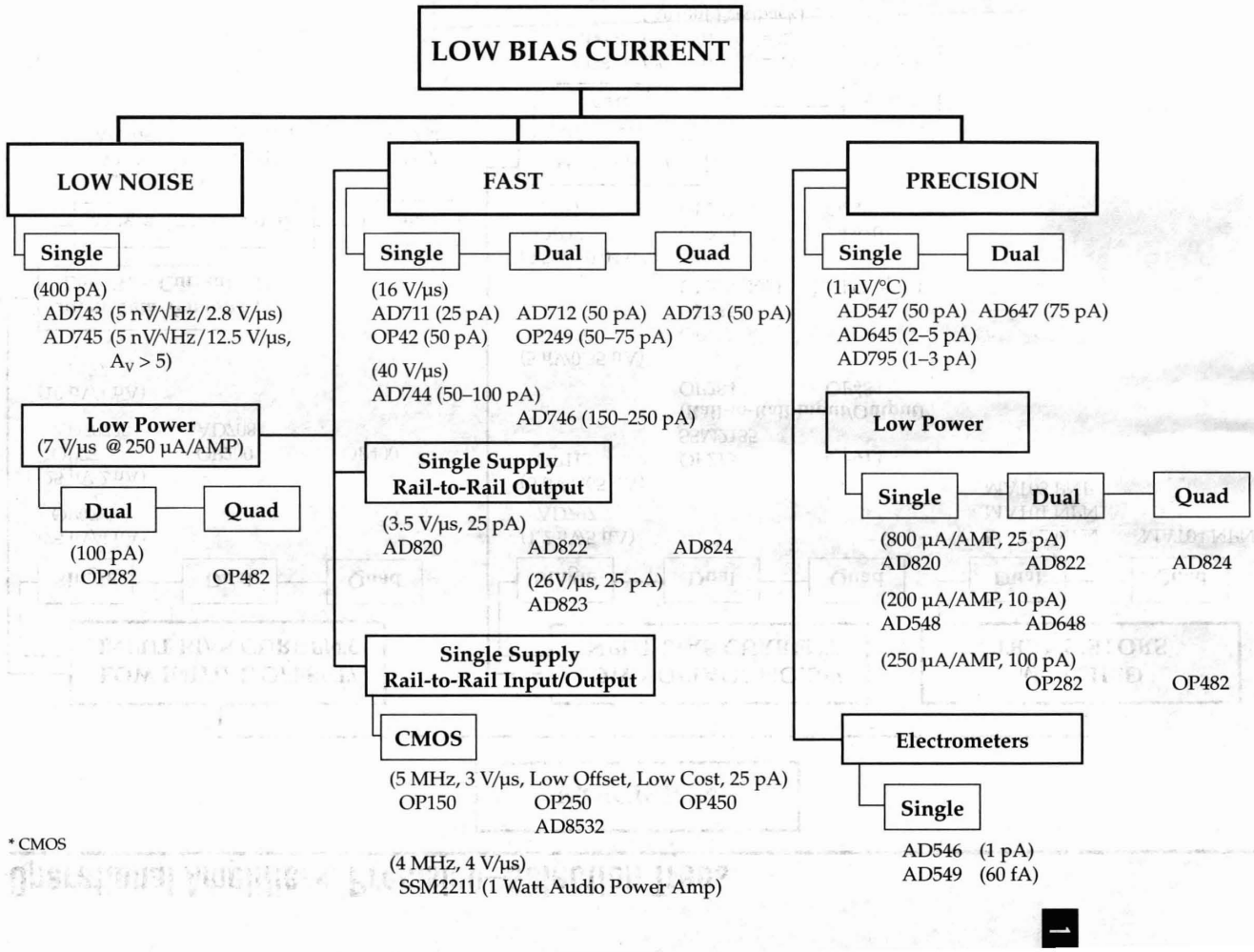
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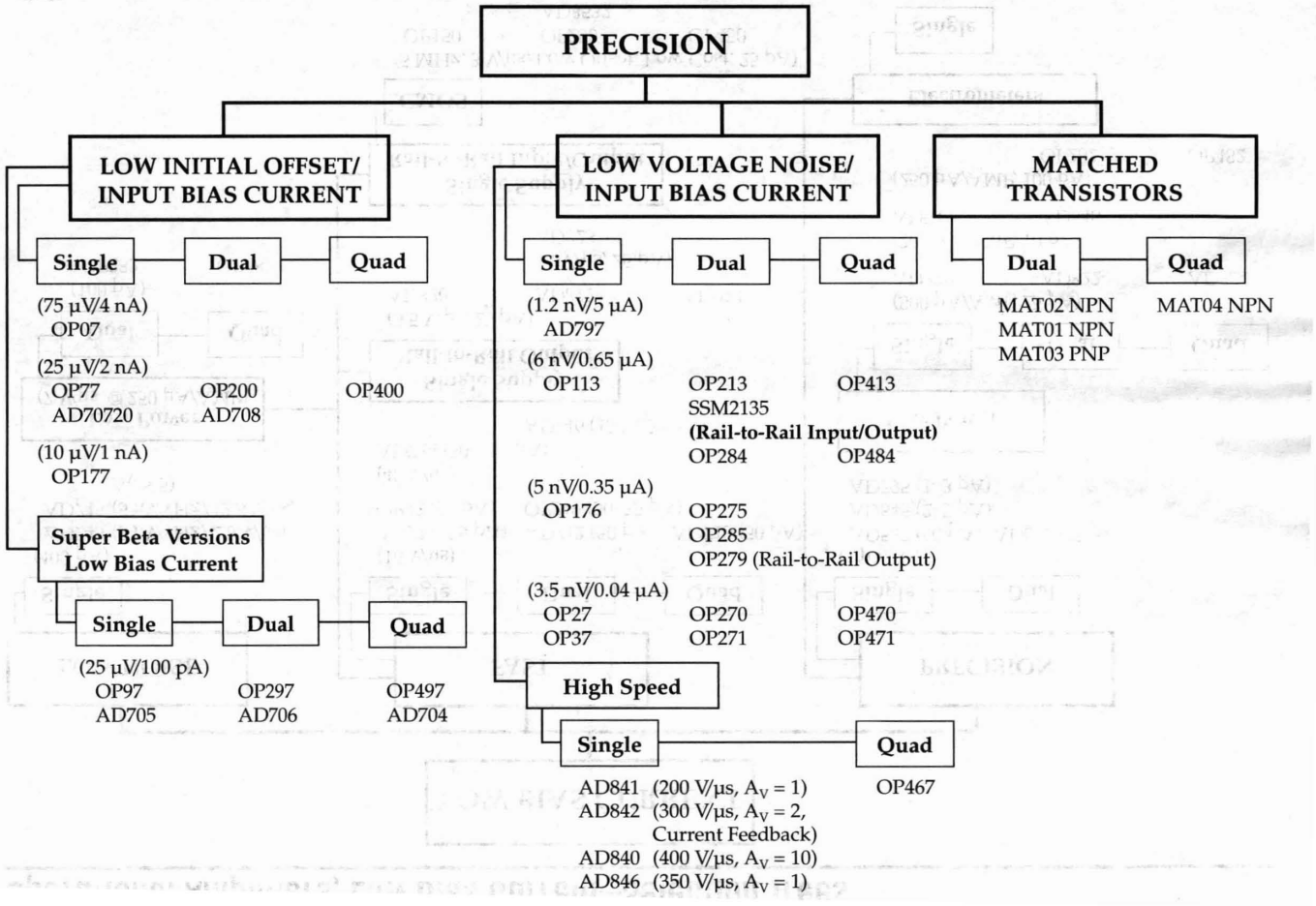
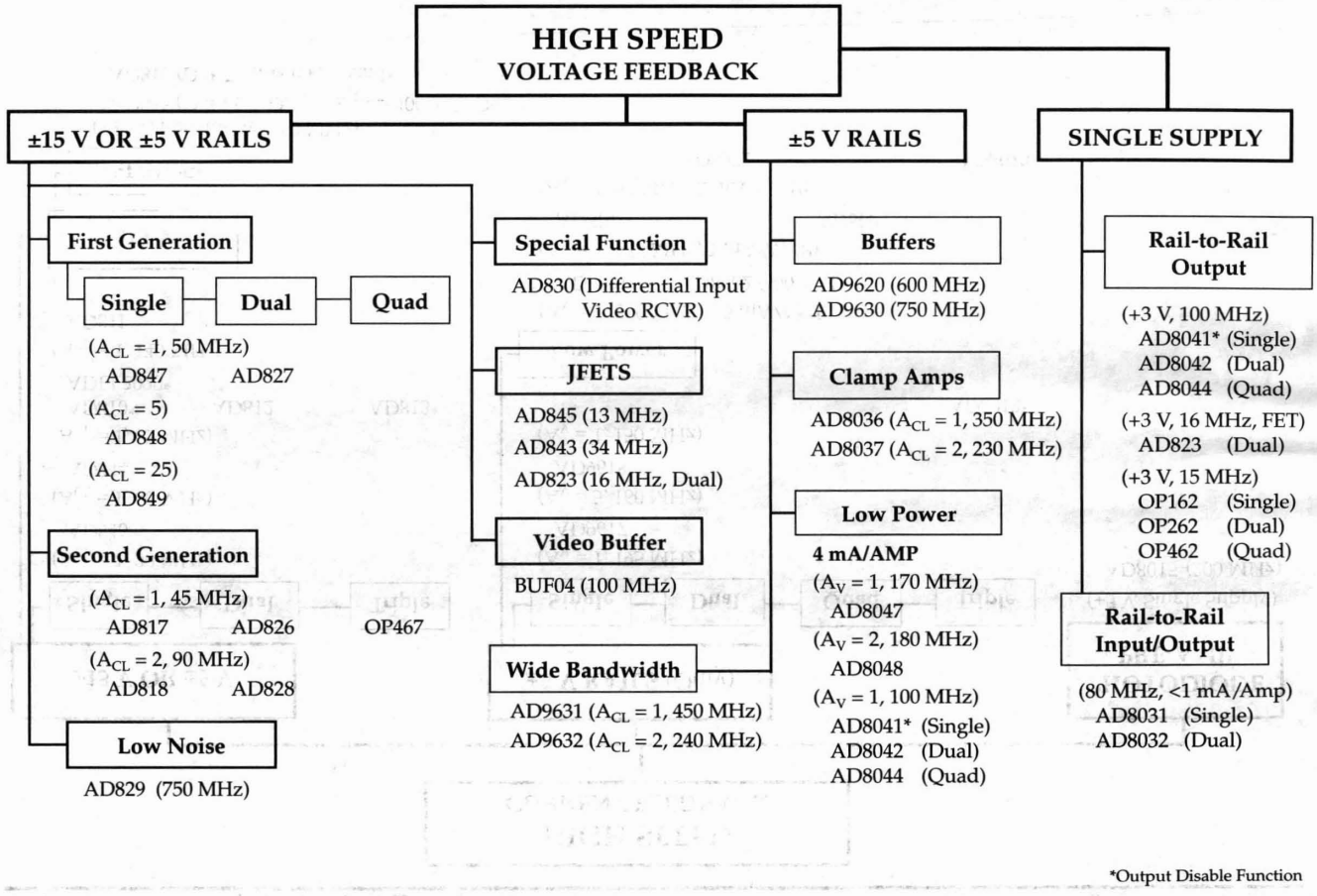
Single
(400 pA)
AD743 (5 nV/√Hz/2.8 V/µs)
AD745 (5 nV/√Hz/12.5 V/µs, A_V > 5)
Low Power
(7 V/µs @ 250 µA/AMP)
Dual
Quad
(100 pA)
OP282
OP482
FAST
Single
Dual
Quad
(16 V/µs)
AD711 (25 pA)
AD712 (50 pA)
AD713 (50 pA)
OP42 (50 pA)
OP249 (50–75 pA)
(40 V/µs)
AD744 (50–100 pA)
AD746 (150–250 pA)
Single Supply Rail-to-Rail Output
(3.5 V/µs, 25 pA)
AD820
AD822
AD824
(26V/µs, 25 pA)
AD823
Single Supply Rail-to-Rail Input/Output
CMOS
(5 MHz, 3 V/µs, Low Offset, Low Cost, 25 pA)
OP150
OP250
OP450
AD8532
(4 MHz, 4 V/µs)
SSM2211 (1 Watt Audio Power Amp)
PRECISION
Single
Dual
(1 µV/°C)
AD547 (50 pA)
AD647 (75 pA)
AD645 (2–5 pA)
AD795 (1–3 pA)
Low Power
Single
Dual
Quad
(800 µA/AMP, 25 pA)
AD820
AD822
AD824
(200 µA/AMP, 10 pA)
AD548
AD648
(250 µA/AMP, 100 pA)
OP282
OP482
Electrometers
Single
AD546 (1 pA)
AD549 (60 fA)
* CMOS

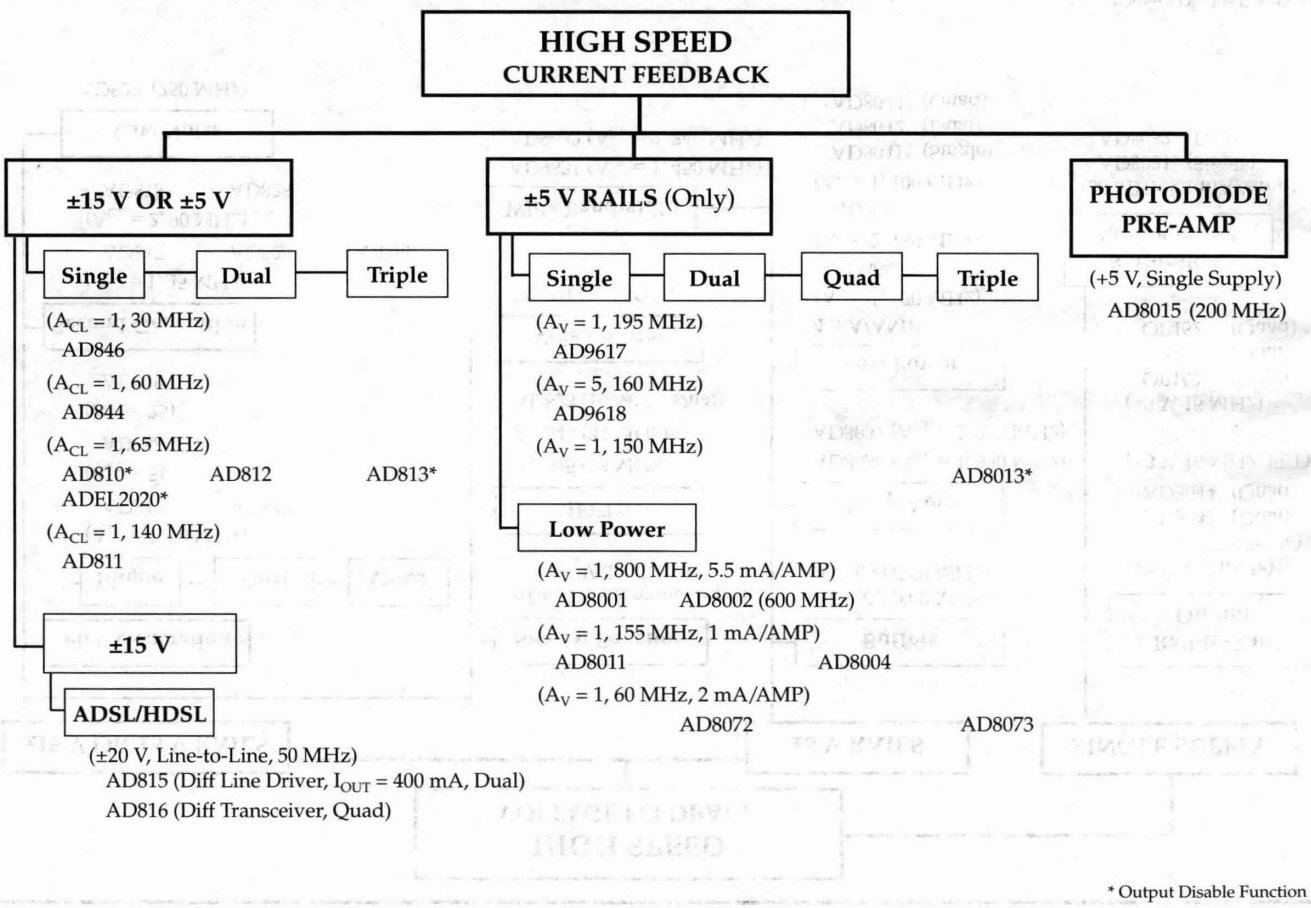
Operational Amplifiers, Precision–Selection Trees





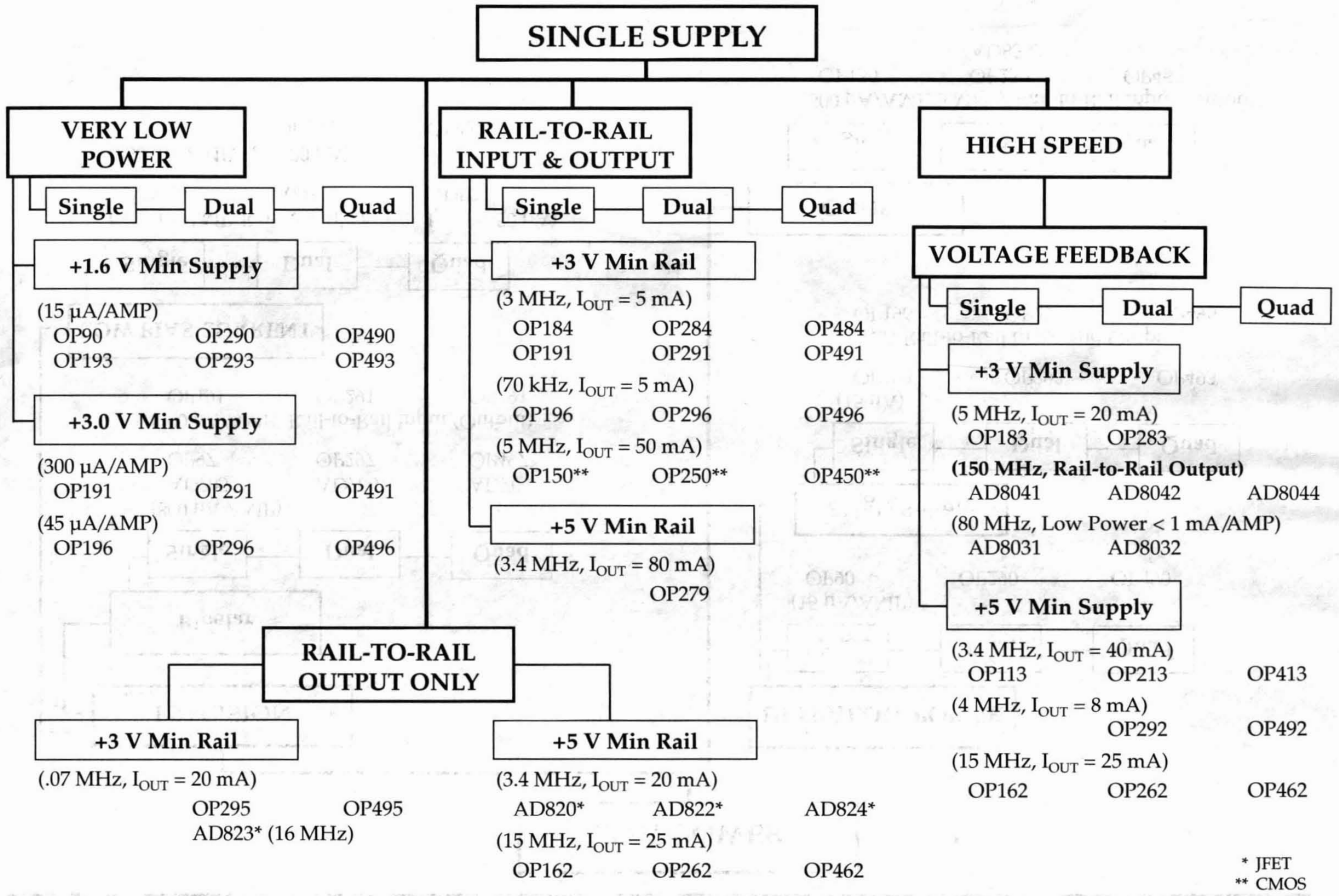
*Output Disable Function

Operational Amplifiers, High Speed–Selection Trees

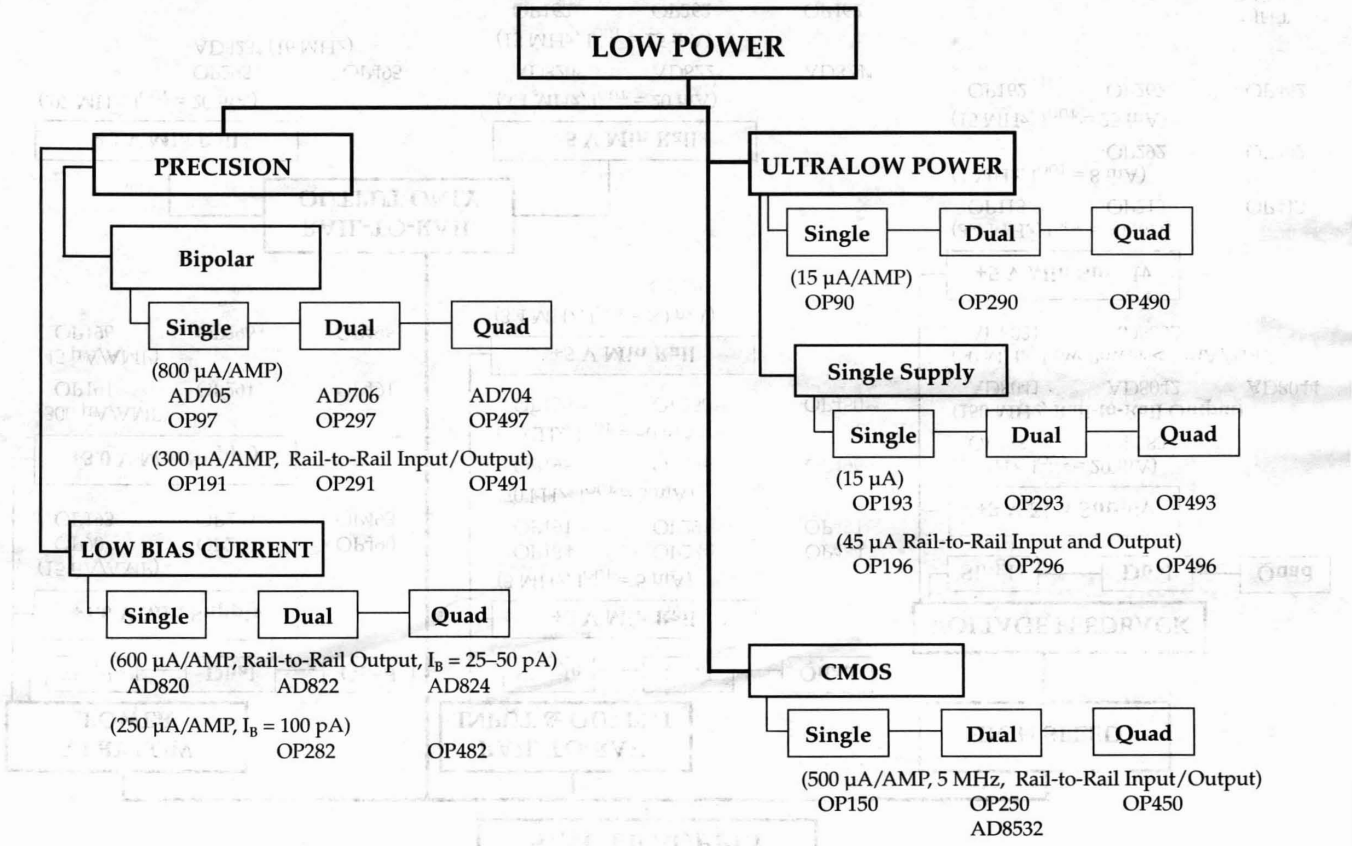


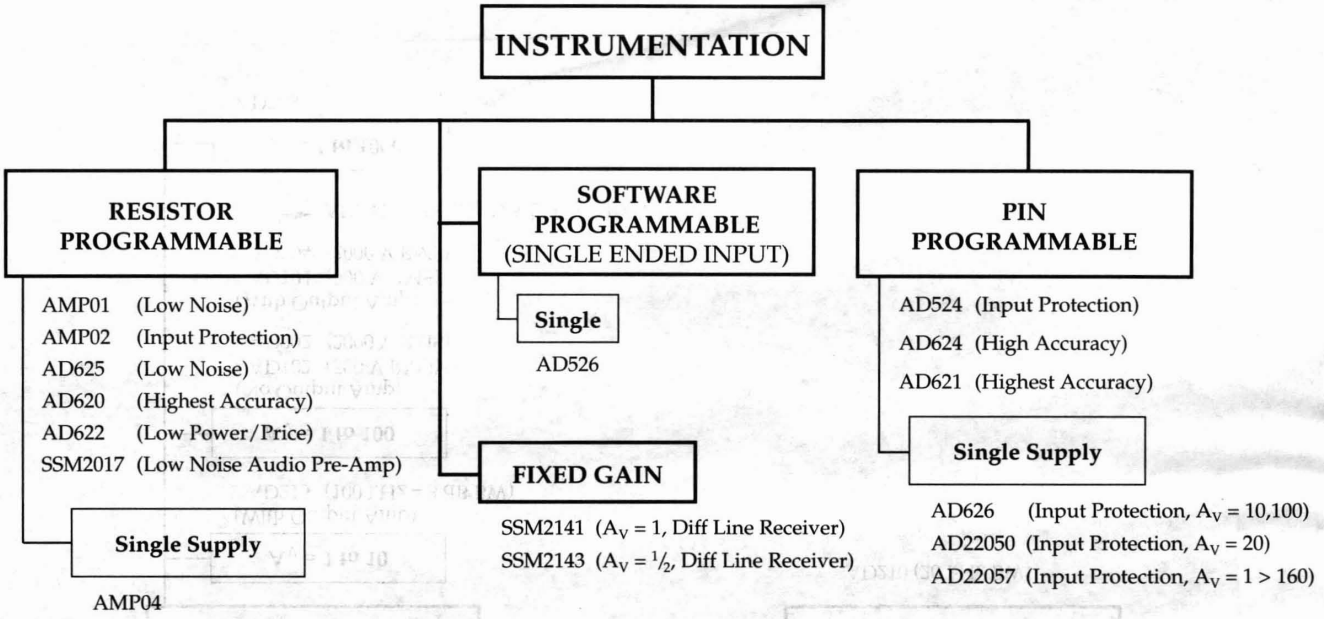
* Output Disable Function

Operational Amplifiers, Single Supply—Selection Trees

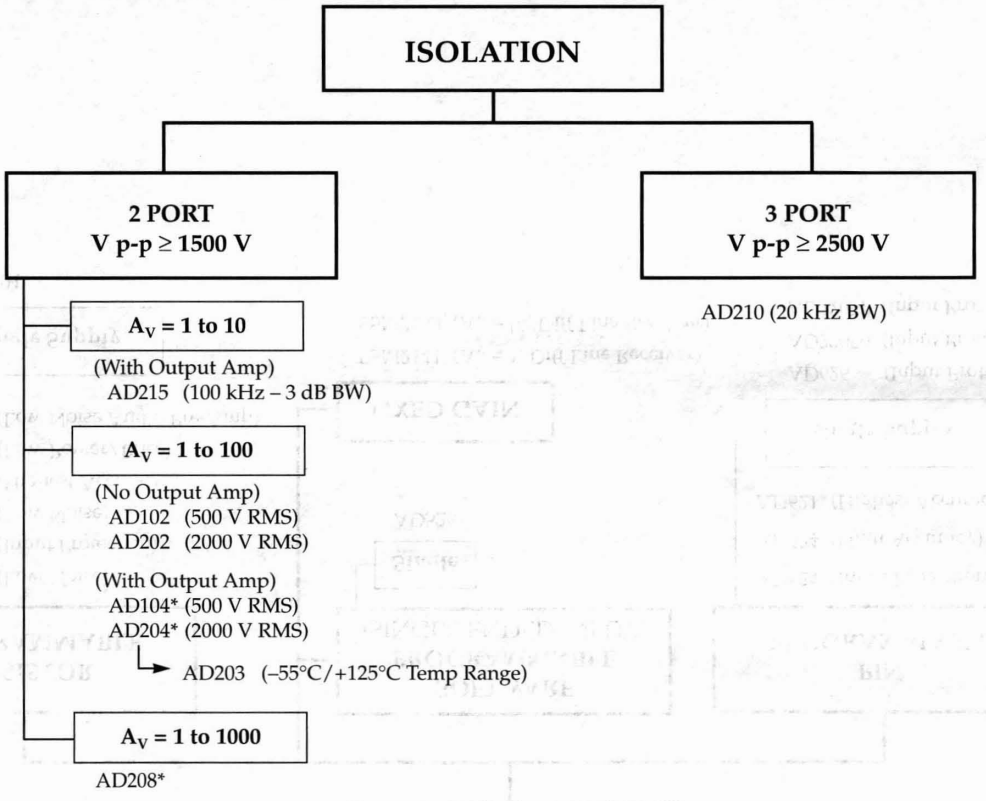


Operational Amplifiers, Low Power–Selection Trees



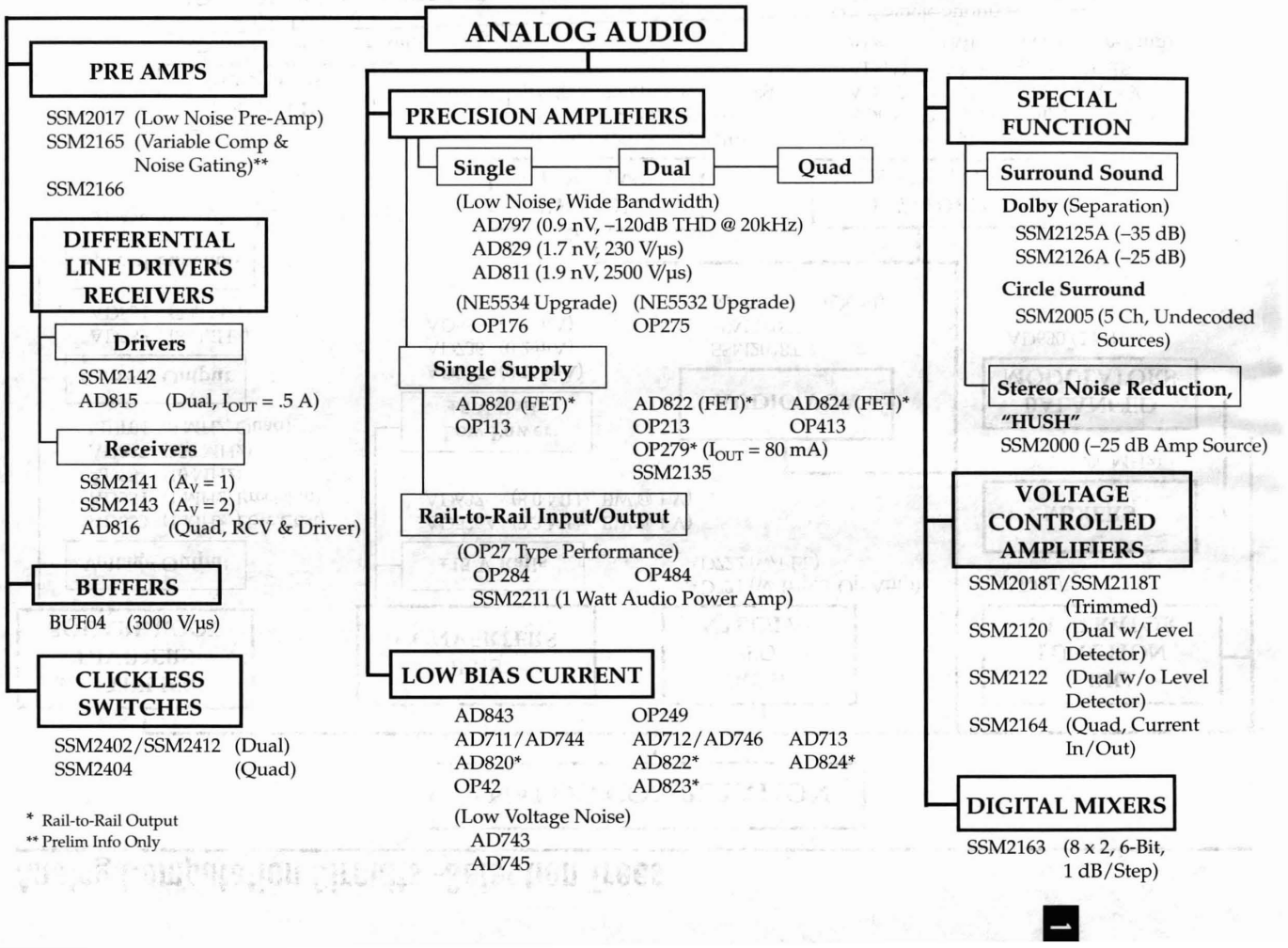

INSTRUMENTATION
RESISTOR PROGRAMMABLE
AMP01 (Low Noise)
AMP02 (Input Protection)
AD625 (Low Noise)
AD620 (Highest Accuracy)
AD622 (Low Power/Price)
SSM2017 (Low Noise Audio Pre-Amp)
Single Supply
AMP04
SOFTWARE PROGRAMMABLE (SINGLE ENDED INPUT)
Single
AD526
FIXED GAIN
SSM2141 (A_V = 1, Diff Line Receiver)
SSM2143 (A_V = ½, Diff Line Receiver)
PIN PROGRAMMABLE
AD524 (Input Protection)
AD624 (High Accuracy)
AD621 (Highest Accuracy)
Single Supply
AD626 (Input Protection, A_V = 10,100)
AD22050 (Input Protection, A_V = 20)
AD22057 (Input Protection, A_V = 1 > 160)

Isolation Amplifiers–Selection Trees

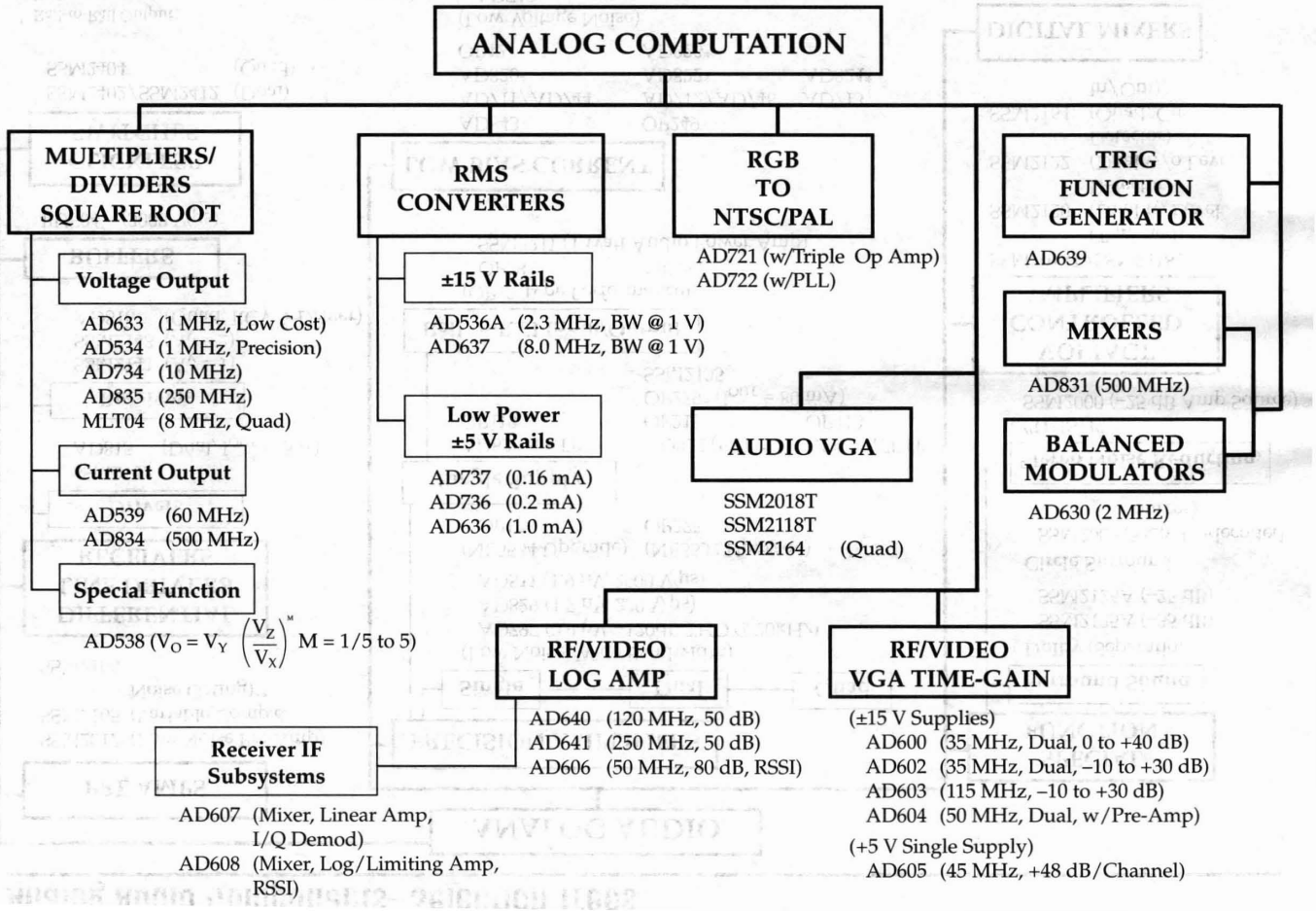


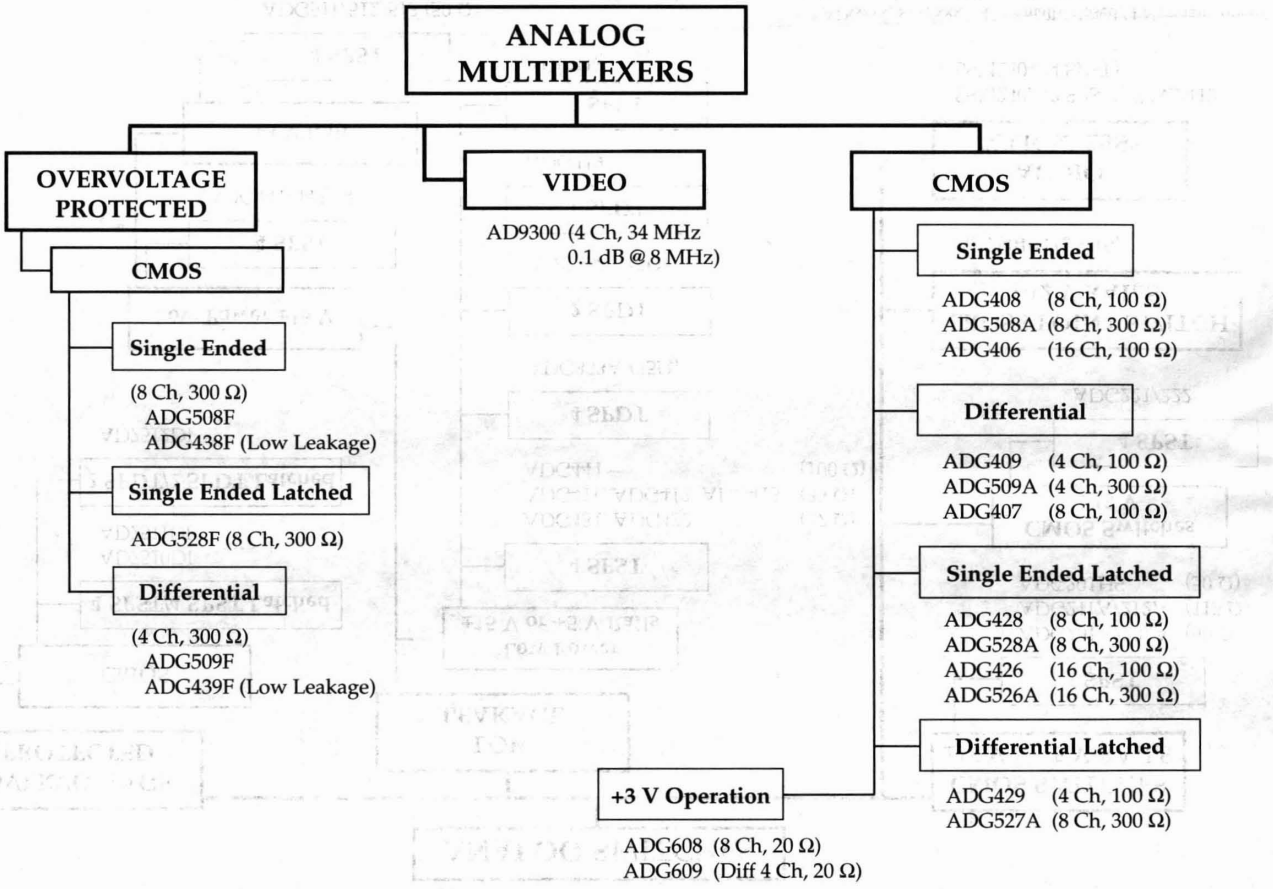
*Multichannel: Requires Clock Driver AD246

Analog Audio Components—Selection Trees

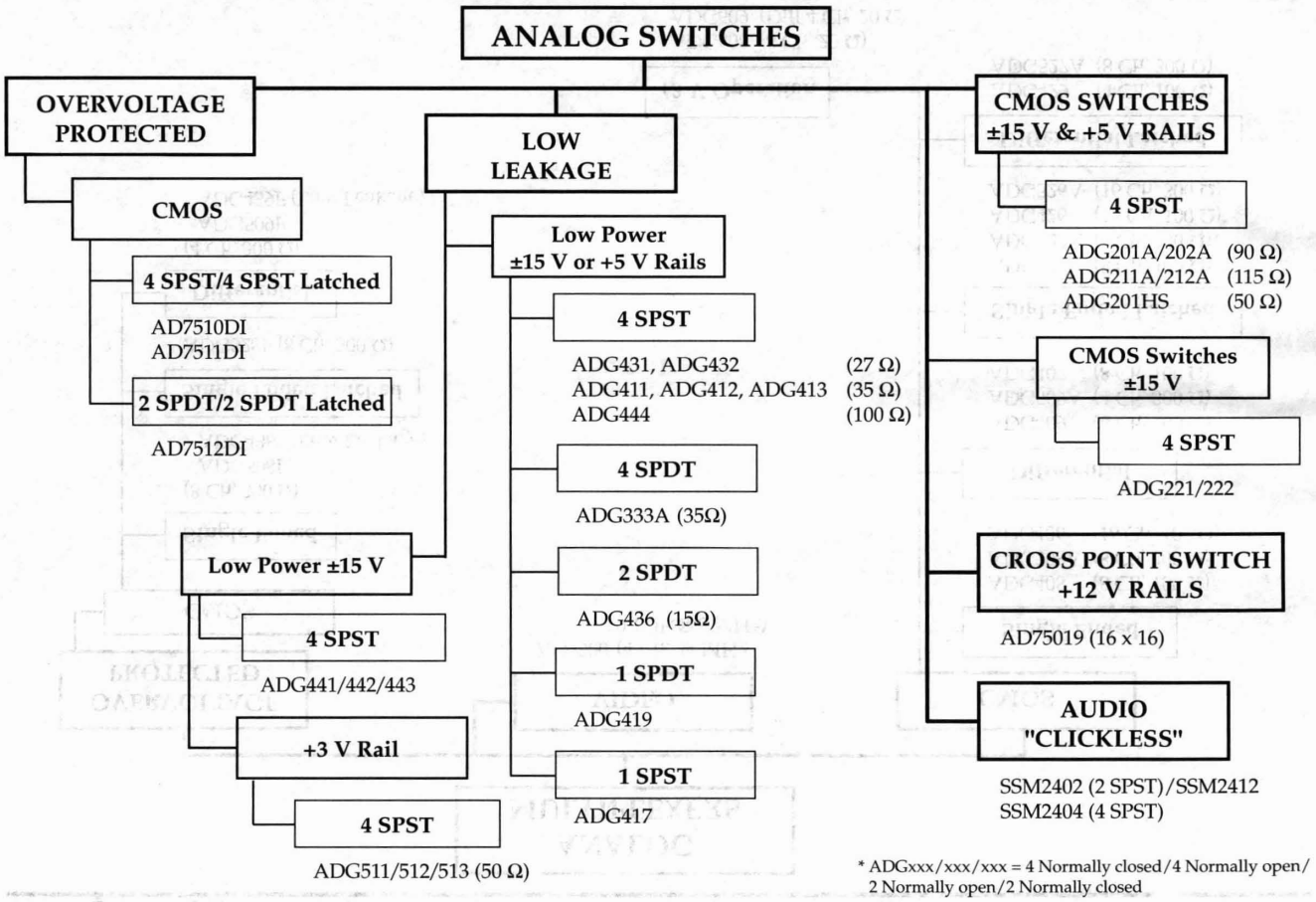


Analog Computation Circuits—Selection Trees

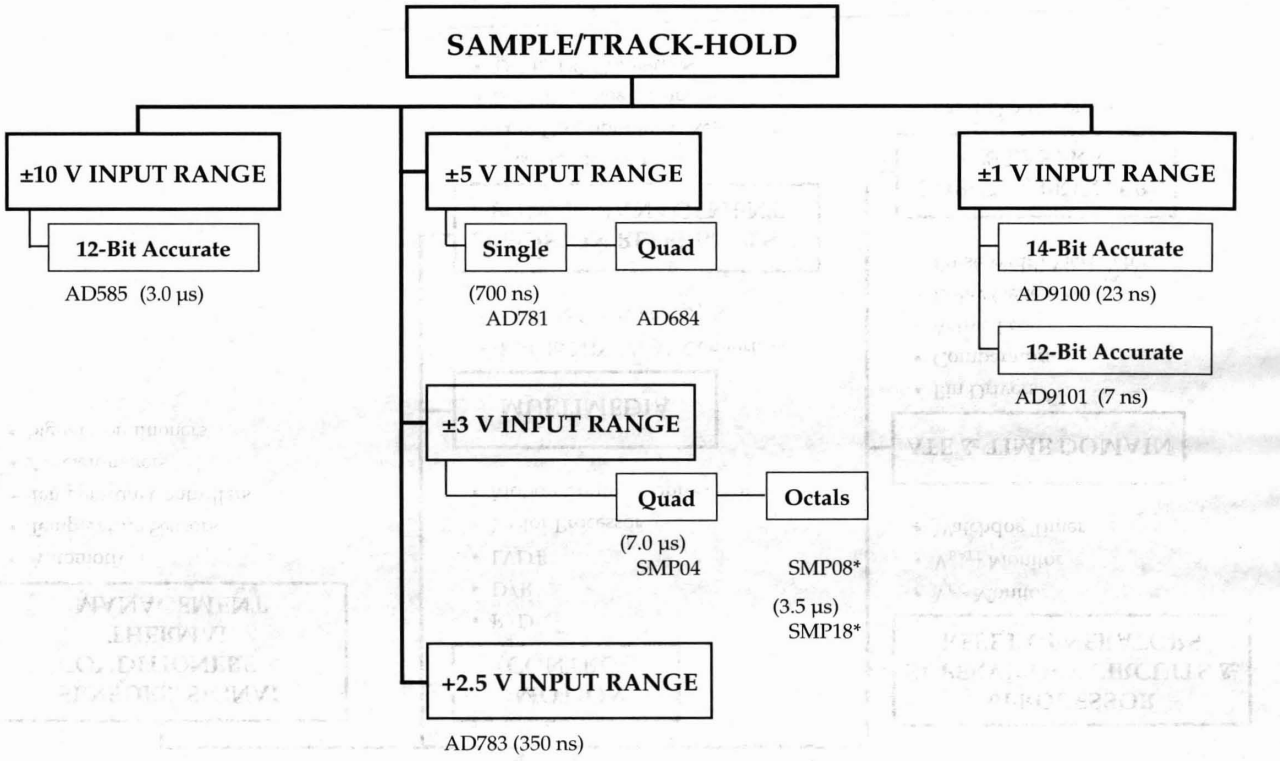



ANALOG MULTIPLEXERS
OVERVOLTAGE PROTECTED
CMOS
Single Ended
(8 Ch, 300 Ω)
ADG508F
ADG438F (Low Leakage)
Single Ended Latched
ADG528F (8 Ch, 300 Ω)
Differential
(4 Ch, 300 Ω)
ADG509F
ADG439F (Low Leakage)
VIDEO
AD9300 (4 Ch, 34 MHz
0.1 dB @ 8 MHz)
CMOS
Single Ended
ADG408 (8 Ch, 100 Ω)
ADG508A (8 Ch, 300 Ω)
ADG406 (16 Ch, 100 Ω)
Differential
ADG409 (4 Ch, 100 Ω)
ADG509A (4 Ch, 300 Ω)
ADG407 (8 Ch, 100 Ω)
Single Ended Latched
ADG428 (8 Ch, 100 Ω)
ADG528A (8 Ch, 300 Ω)
ADG426 (16 Ch, 100 Ω)
ADG526A (16 Ch, 300 Ω)
Differential Latched
ADG429 (4 Ch, 100 Ω)
ADG527A (8 Ch, 300 Ω)
+3 V Operation
ADG608 (8 Ch, 20 Ω)
ADG609 (Diff 4 Ch, 20 Ω)

Analog Switches–Selection Trees

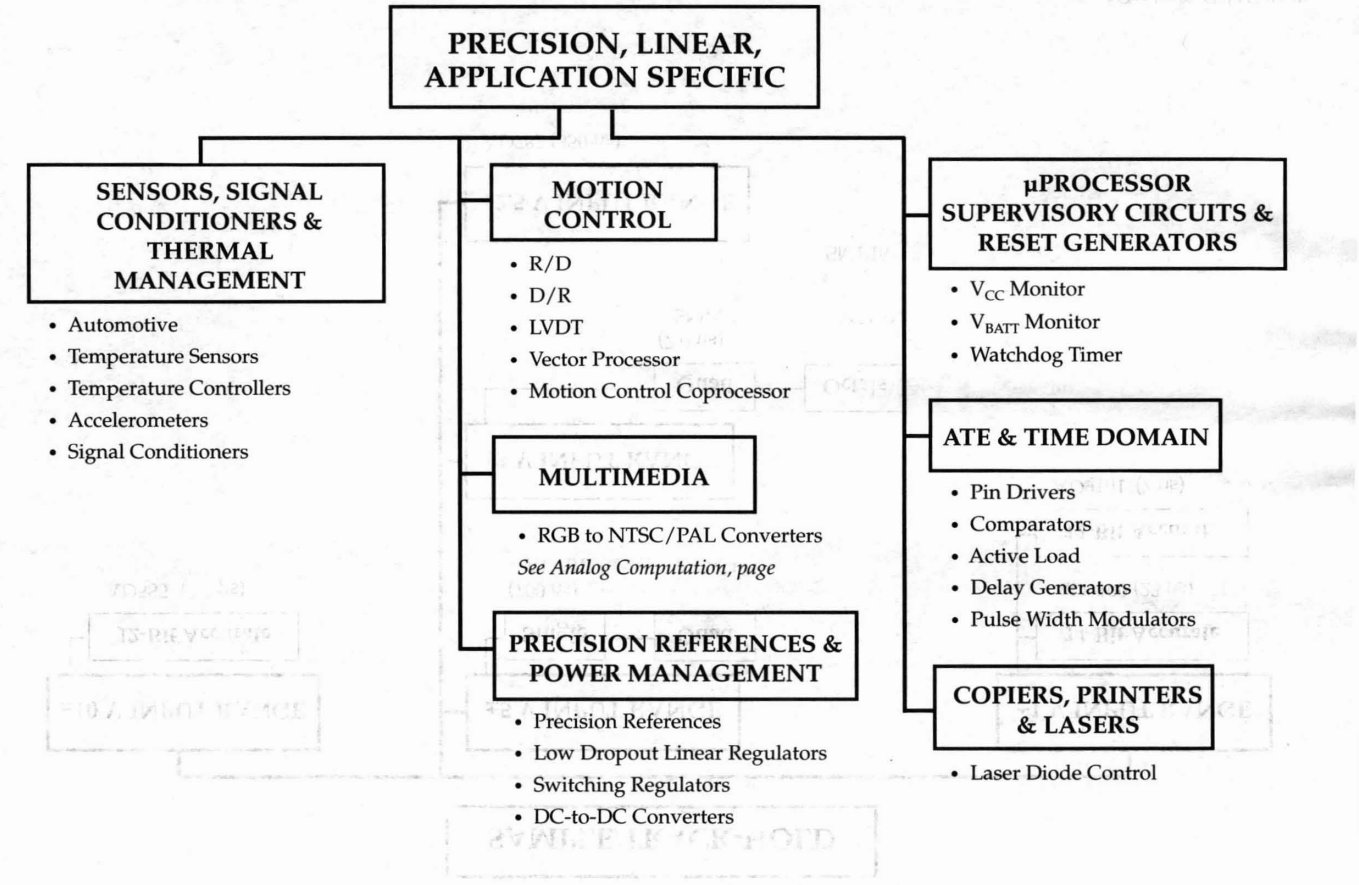


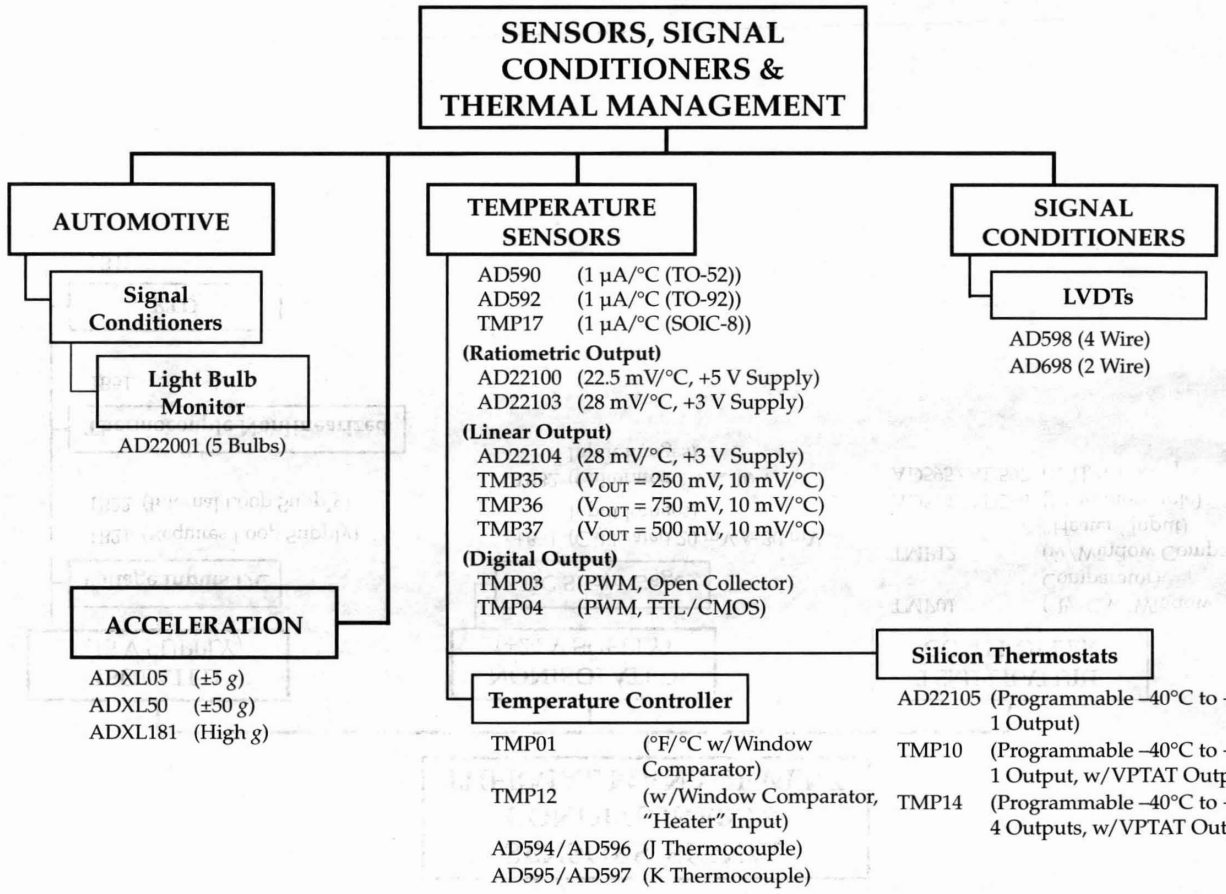
Sample/Track-Hold Amplifiers—Selection Trees



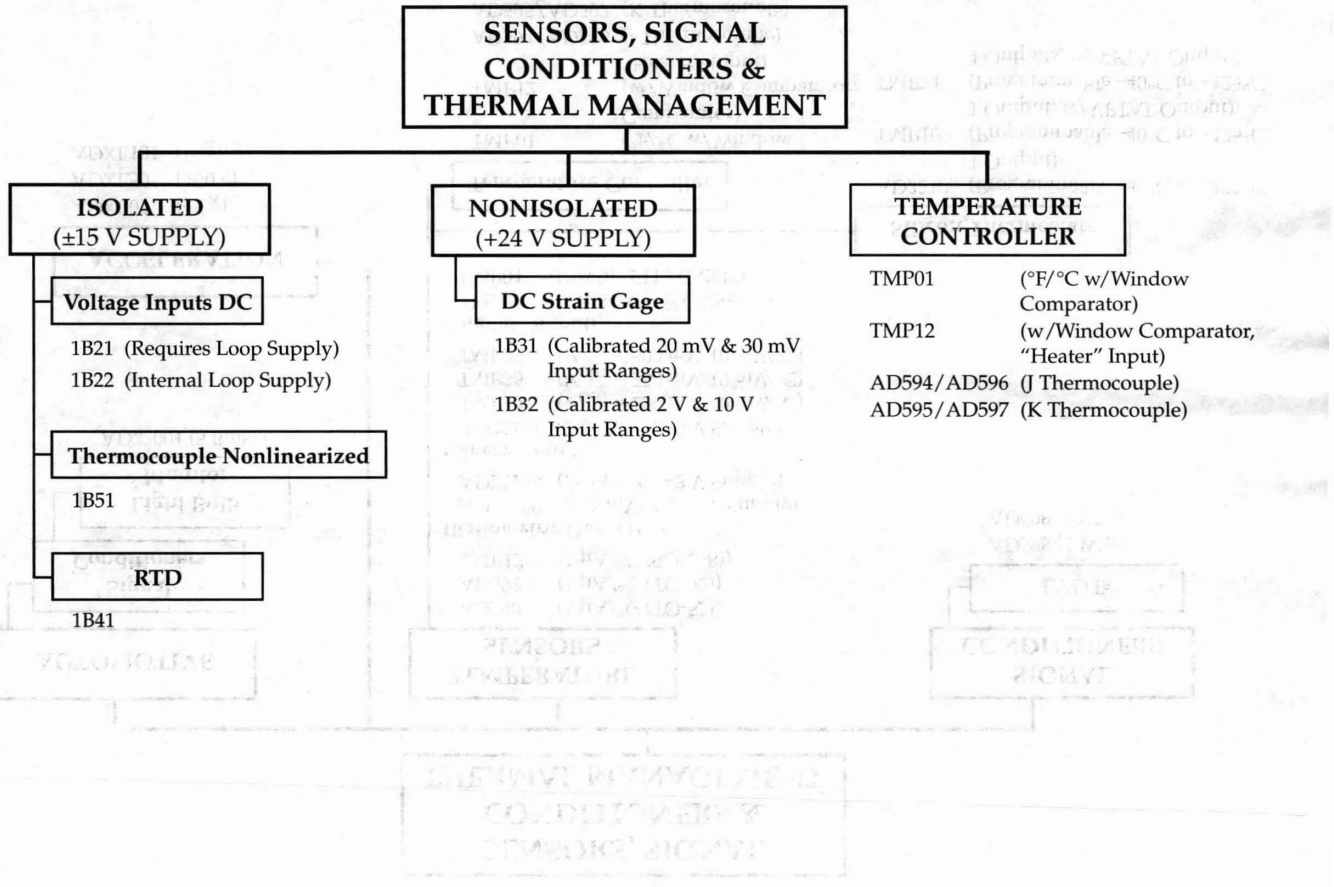
* One Input, Eight Outputs

Precision, Linear, Application Specific Components, Overview–Selection Trees

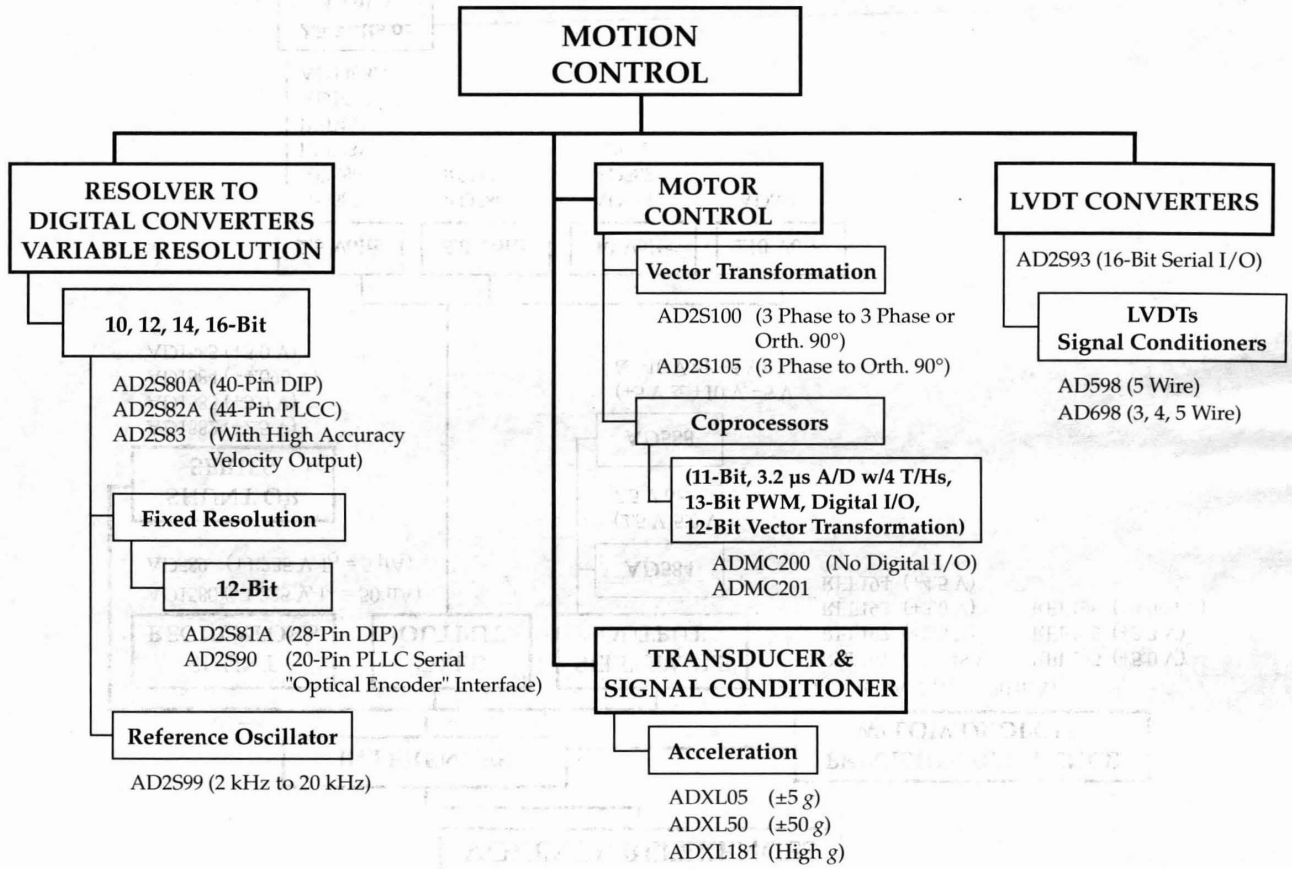



SENSORS, SIGNAL CONDITIONERS & THERMAL MANAGEMENT
AUTOMOTIVE
Signal Conditioners
Light Bulb Monitor
AD22001 (5 Bulbs)
ACCELERATION
ADXL05 (±5 g)
ADXL50 (±50 g)
ADXL181 (High g)
TEMPERATURE SENSORS
AD590 (1 µA/°C (TO-52))
AD592 (1 µA/°C (TO-92))
TMP17 (1 µA/°C (SOIC-8))
(Ratiometric Output)
AD22100 (22.5 mV/°C, +5 V Supply)
AD22103 (28 mV/°C, +3 V Supply)
(Linear Output)
AD22104 (28 mV/°C, +3 V Supply)
TMP35 (V_{OUT} = 250 mV, 10 mV/°C)
TMP36 (V_{OUT} = 750 mV, 10 mV/°C)
TMP37 (V_{OUT} = 500 mV, 10 mV/°C)
(Digital Output)
TMP03 (PWM, Open Collector)
TMP04 (PWM, TTL/CMOS)
Temperature Controller
TMP01 (°F/°C w/Window Comparator)
TMP12 (w/Window Comparator, "Heater" Input)
AD594/AD596 (J Thermocouple)
AD595/AD597 (K Thermocouple)
Silicon Thermostats
AD22105 (Programmable –40°C to +125°C, 1 Output)
TMP10 (Programmable –40°C to +125°C, 1 Output, w/VPTAT Output)
TMP14 (Programmable –40°C to +125°C, 4 Outputs, w/VPTAT Output)
SIGNAL CONDITIONERS
LVDTs
AD598 (4 Wire)
AD698 (2 Wire)

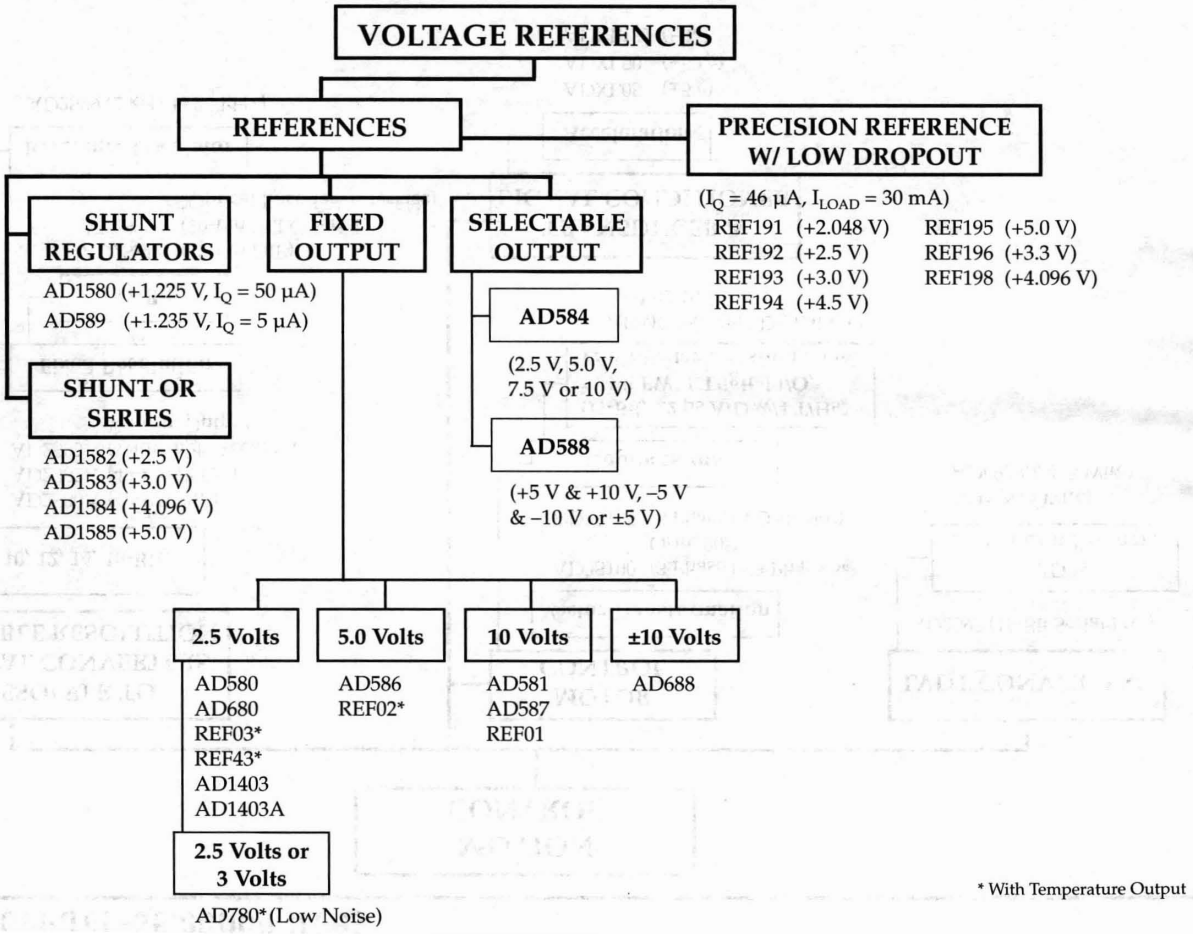
Sensors, Signal Conditioners & Thermal Management–Selection Trees



Motion Control—Selection Trees



Voltage References–Selection Trees



* With Temperature Output

POWER MANAGEMENT

LINEAR LOW DROPOUT REGULATORS

Single Output, Switched Capacitor

(I_{OUT} = 40 mA)

ADM663 (Fixed +5 V; +1.6 V to +16 Adj.)
ADM666 (Fixed +5 V; +1.6 V to +16 Adj. w/Low Battery Monitor)

(I_{OUT} = 100 mA)

ADM663A (Fixed +3.3 V or +5 V; +1.6 V to +16 Adj.)
ADM663A (Fixed +3.3 V or +5 V; +1.6 V to +16 Adj. w/Low Battery Monitor)
ADP3301 (Fixed +2.7 V, +3.0 V, +3.2 V, +3.3 V, +5 V or Adj.; 200 mV Dropout, w/Shutdown)

(I_{OUT} = 200 mA)

ADP667 (Fixed +5 V, +3.5 to +16 Adj.)
ADP3367 (Fixed +5 V, +3.5 to +16 Adj., 300 mV Dropout)

Single Output, Switched Capacitor

(100 mA, Regulated Output)

ADP3302 (+2.7 V & +5.0 V)
(+3.0 V & +5.0 V)
(+3.2 V & +3.2 V)
(+2.7 V & +3.3 V)
(+3.3 V & +5.0 V)

SWITCHING REGULATORS

Step-Down

(Continuous Offtime)

(400 kHz, P Channel Drive Output)

ADP1147 (+3.5 V > +16 V Input, +3 V or +5 V Output)

(Synchronous)

(250 kHz, N & P Channel Drive Outputs)

ADP1148 (+3.3 V > +20 V Input, +3 V or +5 V Output or Adjustable)
ADP1149 (+3.3 V > +48 V Input, +3.3 V, +5 V or Adj. Output)

Step-Up

ADP1109 (+2 V > +12 V Input, +5 V, +12 V or Adj. Output, I_Q = 550 µA, +5 V @ 100 mA from +3 V)

Step-Up or Step-Down

(+2 V > +12.6 V Input Step-Up Mode to +30 V Step-Down Mode)

ADP1108 (19 kHz, +3.3 V, +5 V, +12 V or Adj. Output, I_Q = 110 µA; +5 V @ 150 mA from +3 V Input, +5 V @ 300 mA +9 V Input)
ADP1173 (24 kHz, +5 V, +12 V or Adj. Output, I_Q = 110 µA; +5 V @ 80 mA from +8 V)
ADP1111 (7 kHz, +5 V, +12 V or Adj. Output; +5 V @ 100 mA from +3 V Input, +5 V @ 200 mA +12 V Input)

(+1.15 V to +12.6 V Step-Up Mode to +30 V Step-Down Mode)

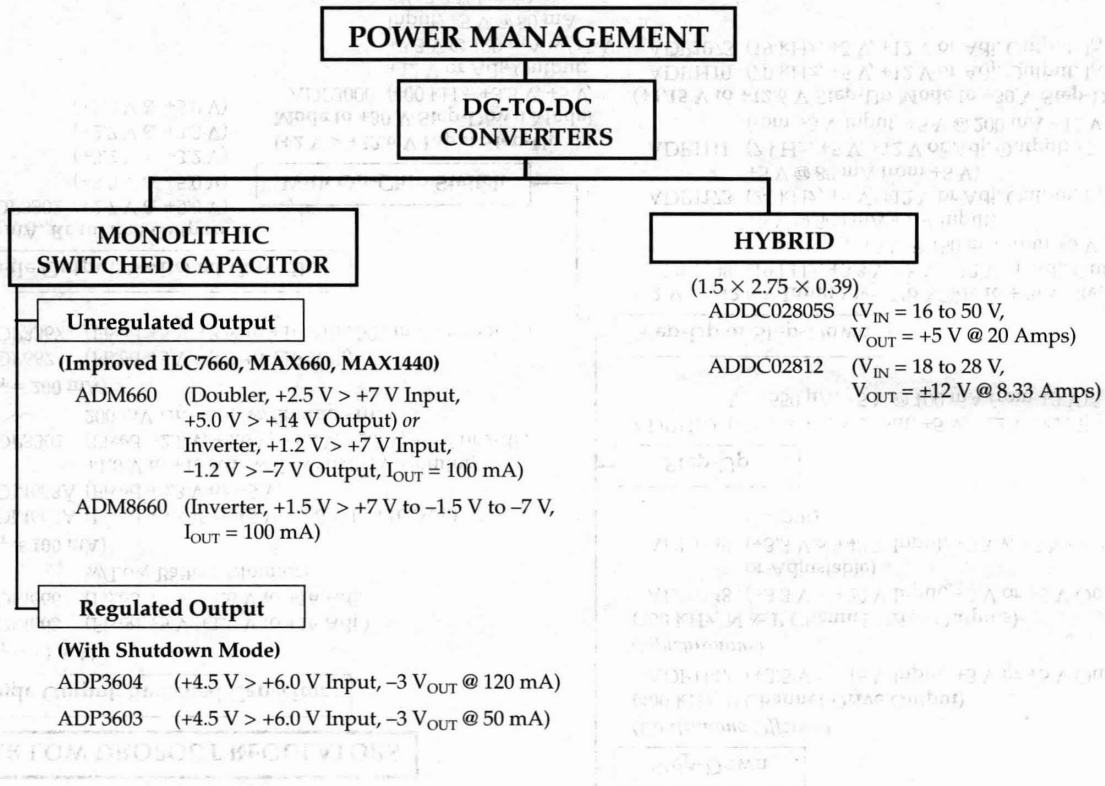
ADP1110 (70 kHz, +5 V, +12 V or Adj. Output, I_Q = 300 µA)
ADP1073 (19 kHz, +5 V, +12 V or Adj. Output; I_Q = 95 µA)

With On-Chip Switch

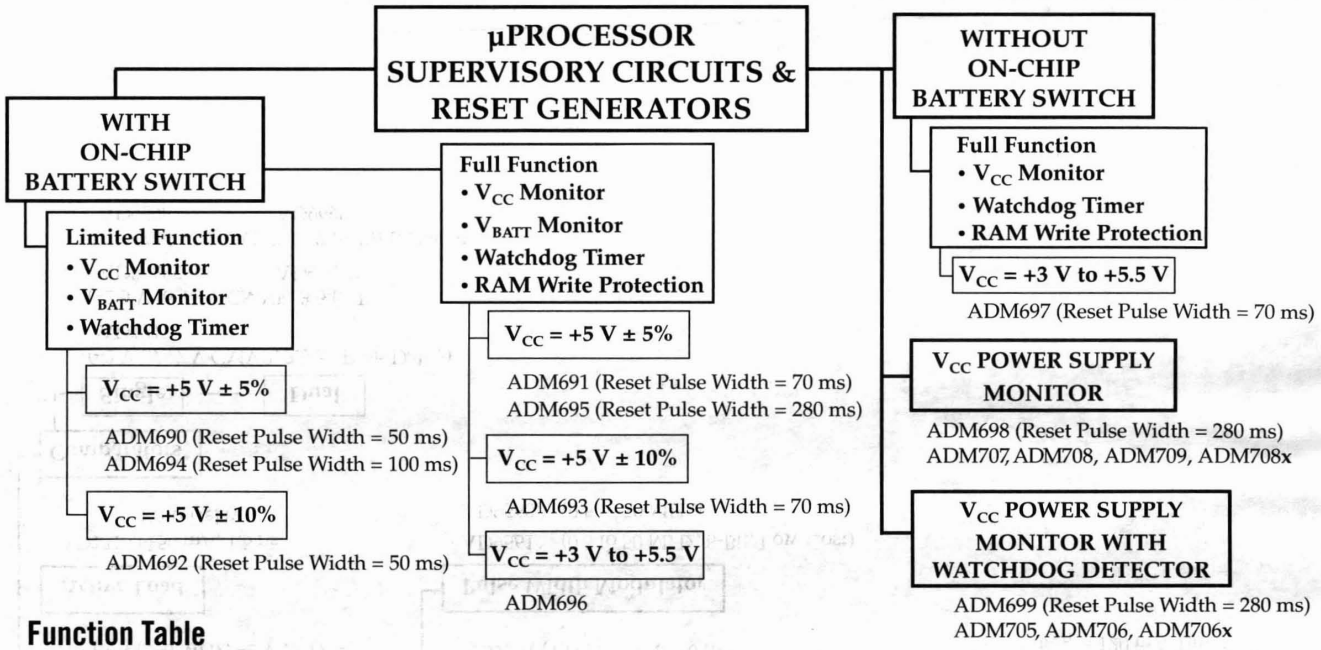
(+2 V > +12.6 V Input Step-Up Mode to +30 V Step-Down Mode)

ADP3000 (400 kHz, +3.3 V, +5 V, +12 V or Adj. Output; +3.3 V @ 120 mA w/+5 V Input, +5 V @ 80 mA w/+3.3 V Input)

Power Management, DC-to-DC Converters–Selection Trees


POWER MANAGEMENT
DC-TO-DC CONVERTERS
MONOLITHIC SWITCHED CAPACITOR
Unregulated Output
(Improved ILC7660, MAX660, MAX1440)
ADM660 (Doubler, +2.5 V > +7 V Input, +5.0 V > +14 V Output) or Inverter, +1.2 V > +7 V Input, –1.2 V > –7 V Output, I_{OUT} = 100 mA)
ADM8660 (Inverter, +1.5 V > +7 V to –1.5 V to –7 V, I_{OUT} = 100 mA)
Regulated Output
(With Shutdown Mode)
ADP3604 (+4.5 V > +6.0 V Input, –3 V_{OUT} @ 120 mA)
ADP3603 (+4.5 V > +6.0 V Input, –3 V_{OUT} @ 50 mA)
HYBRID
(1.5 × 2.75 × 0.39)
ADDC02805S (V_{IN} = 16 to 50 V, V_{OUT} = +5 V @ 20 Amps)
ADDC02812 (V_{IN} = 18 to 28 V, V_{OUT} = ±12 V @ 8.33 Amps)

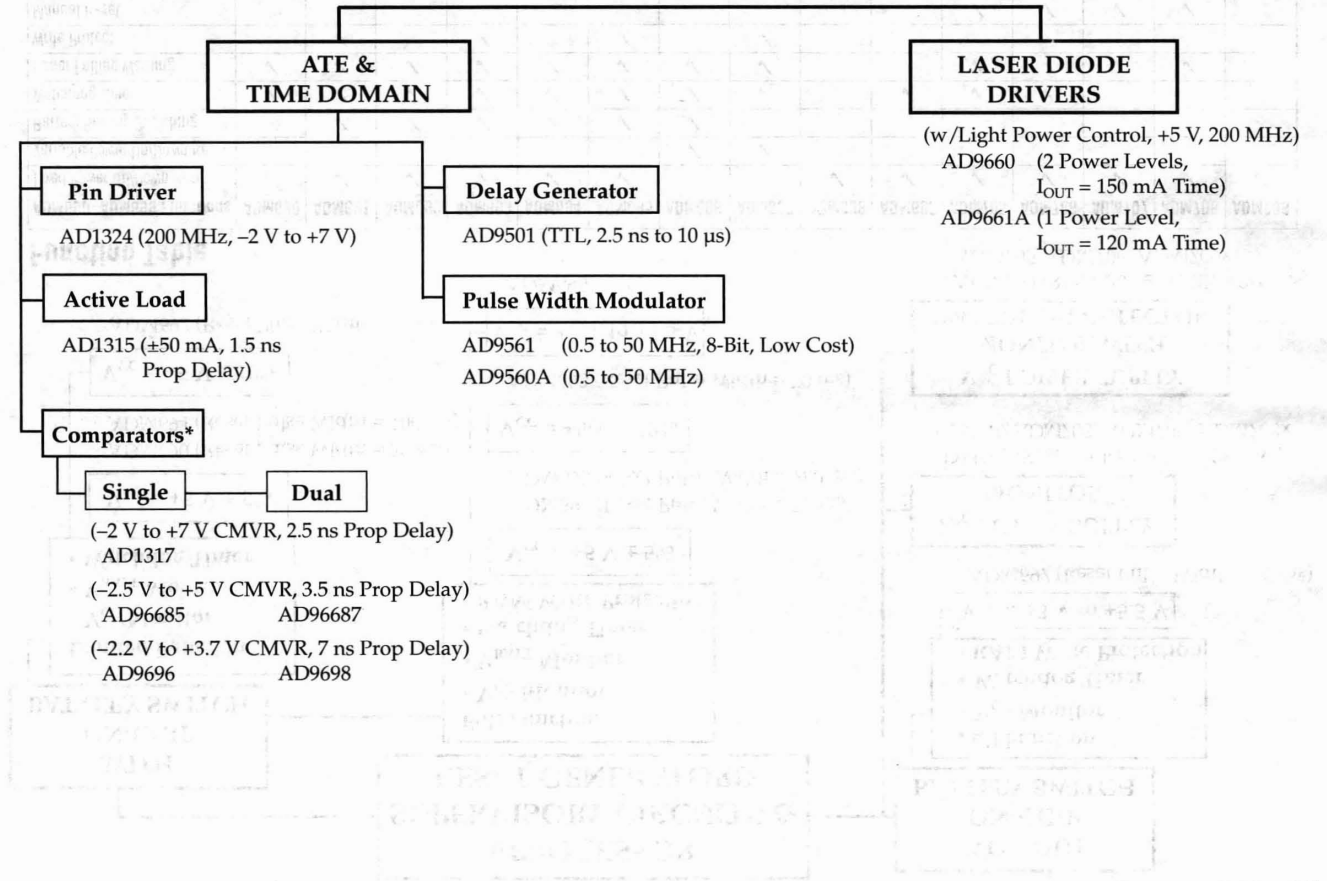
µProcessor Supervisory Circuits & Reset Generators—Selection Trees


µPROCESSOR SUPERVISORY CIRCUITS & RESET GENERATORS
WITH ON-CHIP BATTERY SWITCH
Limited Function
• V_{CC} Monitor
• V_{BATT} Monitor
• Watchdog Timer
V_{CC} = +5 V ± 5%
ADM690 (Reset Pulse Width = 50 ms)
ADM694 (Reset Pulse Width = 100 ms)
V_{CC} = +5 V ± 10%
ADM692 (Reset Pulse Width = 50 ms)
Full Function
• V_{CC} Monitor
• V_{BATT} Monitor
• Watchdog Timer
• RAM Write Protection
V_{CC} = +5 V ± 5%
ADM691 (Reset Pulse Width = 70 ms)
ADM695 (Reset Pulse Width = 280 ms)
V_{CC} = +5 V ± 10%
ADM693 (Reset Pulse Width = 70 ms)
V_{CC} = +3 V to +5.5 V
ADM696
WITHOUT ON-CHIP BATTERY SWITCH
Full Function
• V_{CC} Monitor
• Watchdog Timer
• RAM Write Protection
V_{CC} = +3 V to +5.5 V
ADM697 (Reset Pulse Width = 70 ms)
V_{CC} POWER SUPPLY MONITOR
ADM698 (Reset Pulse Width = 280 ms)
ADM707, ADM708, ADM709, ADM708x
V_{CC} POWER SUPPLY MONITOR WITH WATCHDOG DETECTOR
ADM699 (Reset Pulse Width = 280 ms)
ADM705, ADM706, ADM706x

Function Table

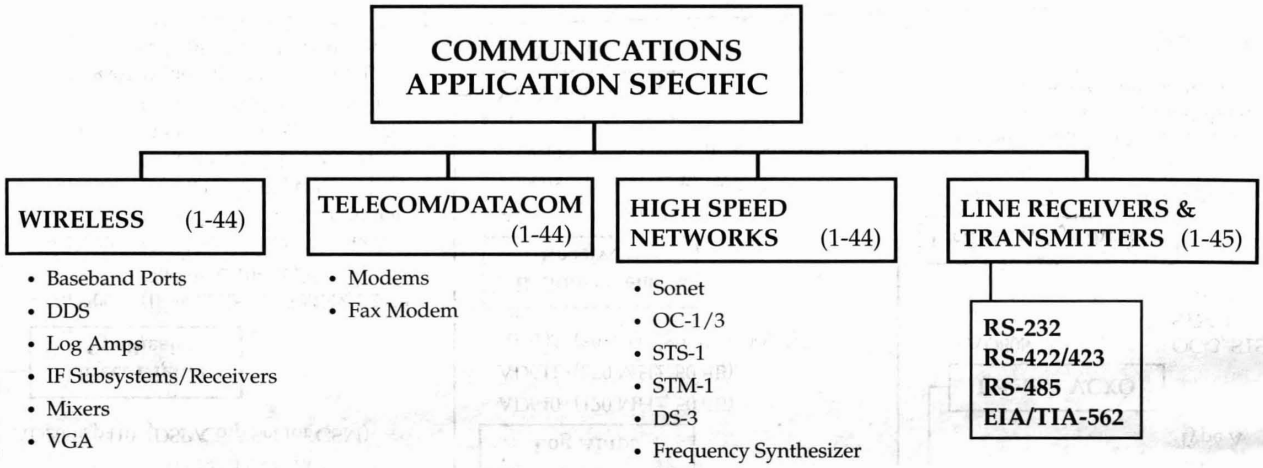
ADM690–ADM699 Functions	ADM690	ADM691	ADM692	ADM693	ADM694	ADM695	ADM696	ADM697	ADM698	ADM699	ADM705	ADM706	ADM707	ADM708	ADM709
Fixed Power Up/Down Reset	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓
Variable Power Up/Down Reset							✓	✓							
Battery Backup Switching	✓	✓	✓	✓	✓	✓	✓								
Watchdog Timer	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓			
Power Failing Warning	✓	✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	
Write Protect		✓		✓		✓		✓							
Manual Reset											✓	✓	✓	✓	
+3 V Systems												✘		✘	✓

ATE, Time Domain & Laser Diode Driver–Selection Trees

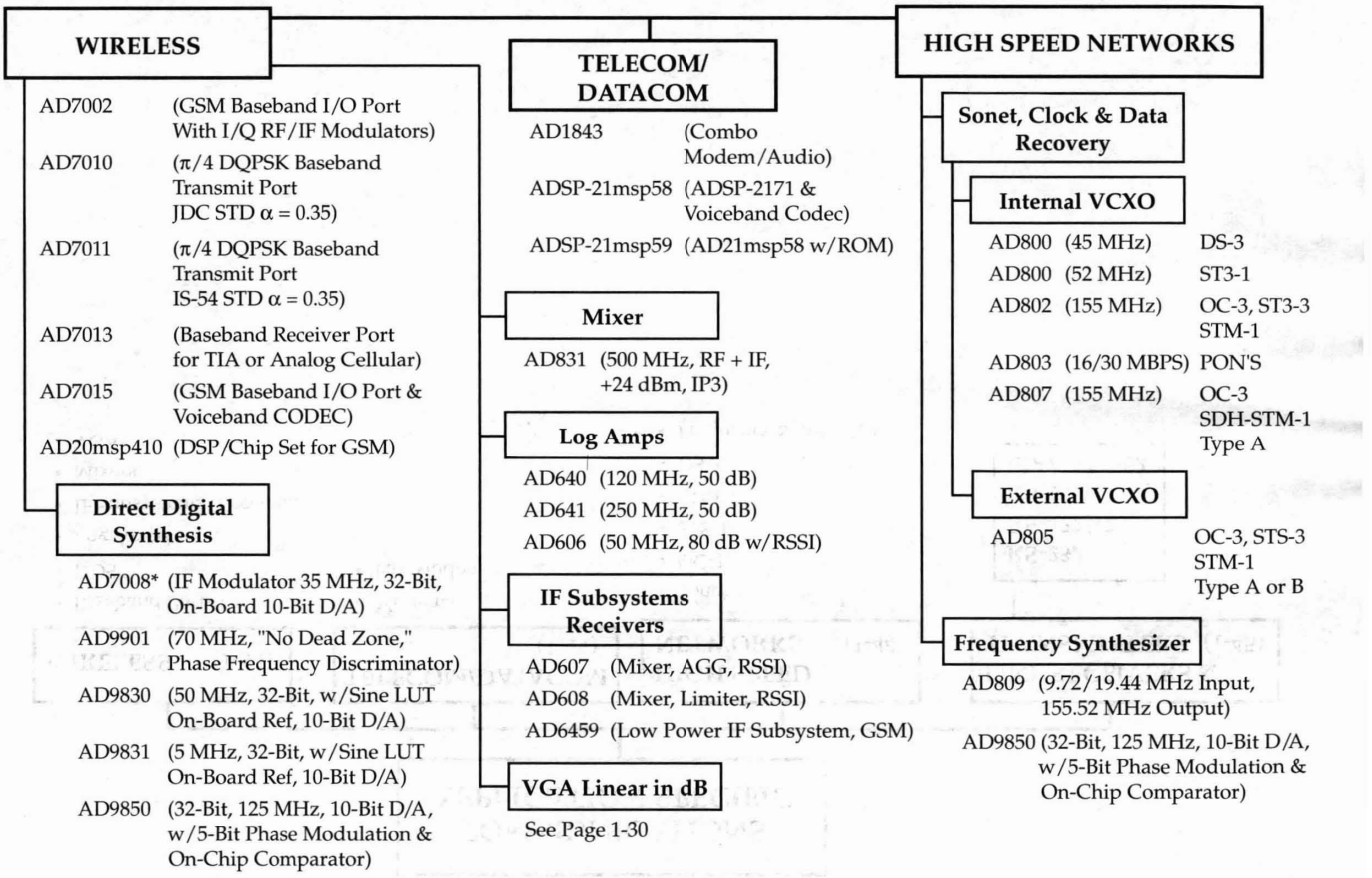

ATE & TIME DOMAIN
LASER DIODE DRIVERS
(w/Light Power Control, +5 V, 200 MHz)
AD9660 (2 Power Levels, I_{OUT} = 150 mA Time)
AD9661A (1 Power Level, I_{OUT} = 120 mA Time)
Pin Driver
AD1324 (200 MHz, –2 V to +7 V)
Delay Generator
AD9501 (TTL, 2.5 ns to 10 µs)
Active Load
AD1315 (±50 mA, 1.5 ns Prop Delay)
Pulse Width Modulator
AD9561 (0.5 to 50 MHz, 8-Bit, Low Cost)
AD9560A (0.5 to 50 MHz)
Comparators*
Single
Dual
(–2 V to +7 V CMVR, 2.5 ns Prop Delay)
AD1317
(–2.5 V to +5 V CMVR, 3.5 ns Prop Delay)
AD96685 AD96687
(–2.2 V to +3.7 V CMVR, 7 ns Prop Delay)
AD9696 AD9698

* For Precision Comparators See Page 1-54

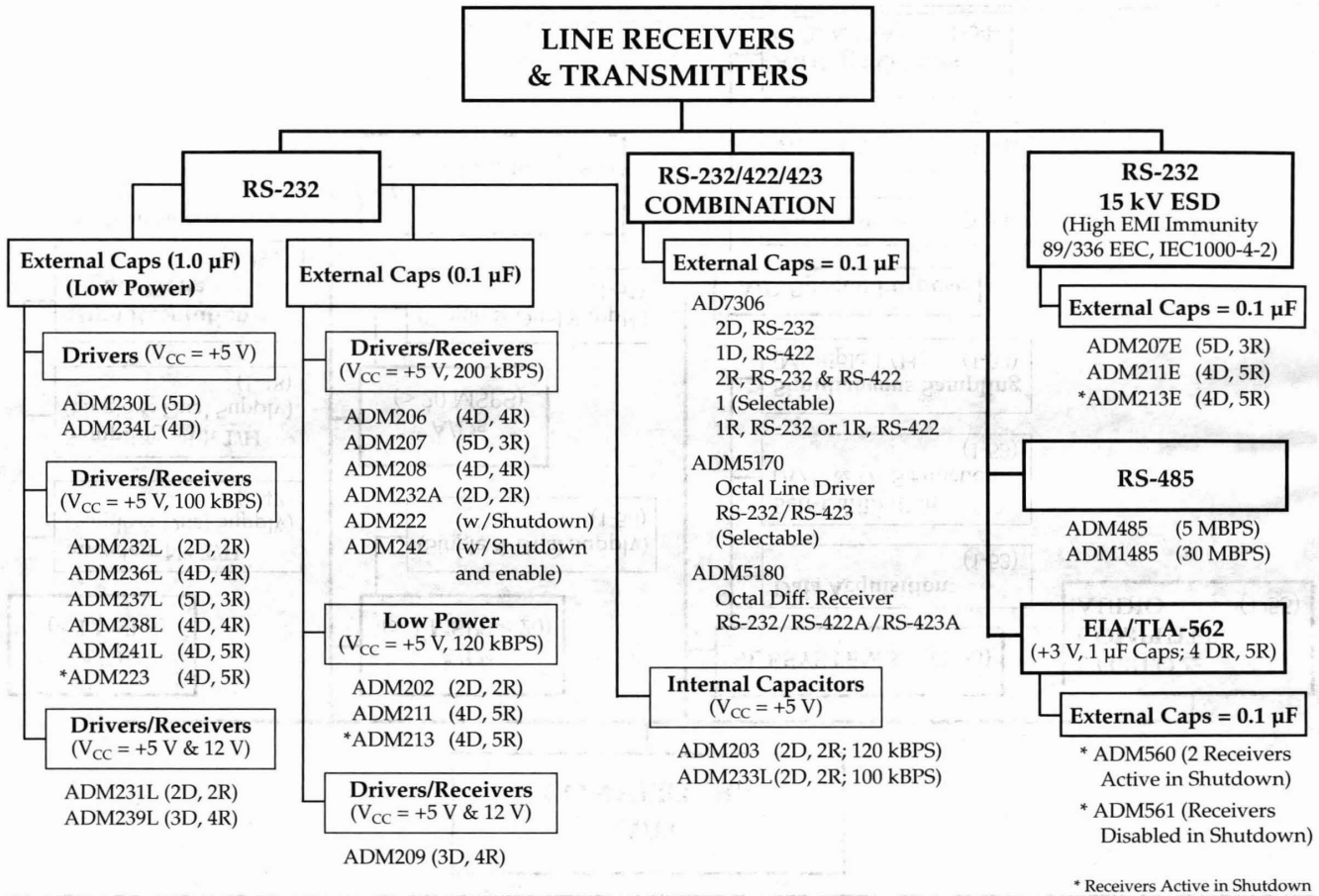
Communications, Application Specific Components, Overview—Selection Trees



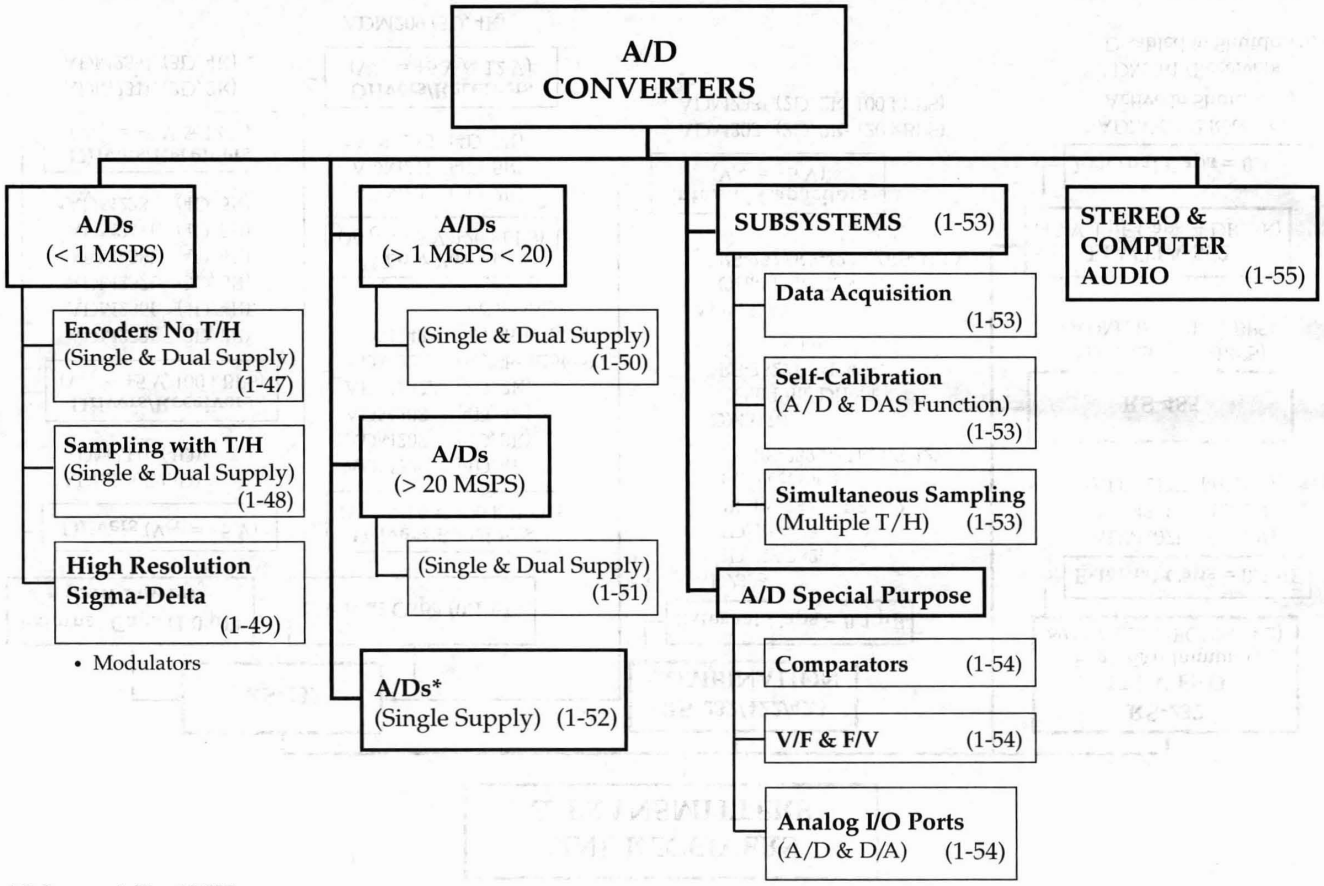
Communications, Wireless, Telecom/Datacom & High Speed Networks–Selection Trees


WIRELESS
AD7002 (GSM Baseband I/O Port With I/Q RF/IF Modulators)
AD7010 (π/4 DQPSK Baseband Transmit Port JDC STD α = 0.35)
AD7011 (π/4 DQPSK Baseband Transmit Port IS-54 STD α = 0.35)
AD7013 (Baseband Receiver Port for TIA or Analog Cellular)
AD7015 (GSM Baseband I/O Port & Voiceband CODEC)
AD20msp410 (DSP/Chip Set for GSM)
Direct Digital Synthesis
AD7008* (IF Modulator 35 MHz, 32-Bit, On-Board 10-Bit D/A)
AD9901 (70 MHz, "No Dead Zone," Phase Frequency Discriminator)
AD9830 (50 MHz, 32-Bit, w/Sine LUT On-Board Ref, 10-Bit D/A)
AD9831 (5 MHz, 32-Bit, w/Sine LUT On-Board Ref, 10-Bit D/A)
AD9850 (32-Bit, 125 MHz, 10-Bit D/A, w/5-Bit Phase Modulation & On-Chip Comparator)
TELECOM/ DATACOM
AD1843 (Combo Modem/Audio)
ADSP-21msp58 (ADSP-2171 & Voiceband Codec)
ADSP-21msp59 (AD21msp58 w/ROM)
Mixer
AD831 (500 MHz, RF + IF, +24 dBm, IP3)
Log Amps
AD640 (120 MHz, 50 dB)
AD641 (250 MHz, 50 dB)
AD606 (50 MHz, 80 dB w/RSSI)
IF Subsystems Receivers
AD607 (Mixer, AGG, RSSI)
AD608 (Mixer, Limiter, RSSI)
AD6459 (Low Power IF Subsystem, GSM)
VGA Linear in dB
See Page 1-30
HIGH SPEED NETWORKS
Sonet, Clock & Data Recovery
Internal VCXO
AD800 (45 MHz) DS-3
AD800 (52 MHz) ST3-1
AD802 (155 MHz) OC-3, ST3-3 STM-1
AD803 (16/30 MBPS) PON'S
AD807 (155 MHz) OC-3 SDH-STM-1 Type A
External VCXO
AD805 OC-3, STS-3 STM-1 Type A or B
Frequency Synthesizer
AD809 (9.72/19.44 MHz Input, 155.52 MHz Output)
AD9850 (32-Bit, 125 MHz, 10-Bit D/A, w/5-Bit Phase Modulation & On-Chip Comparator)

Communications, Line Receivers & Transmitters—Selection Trees

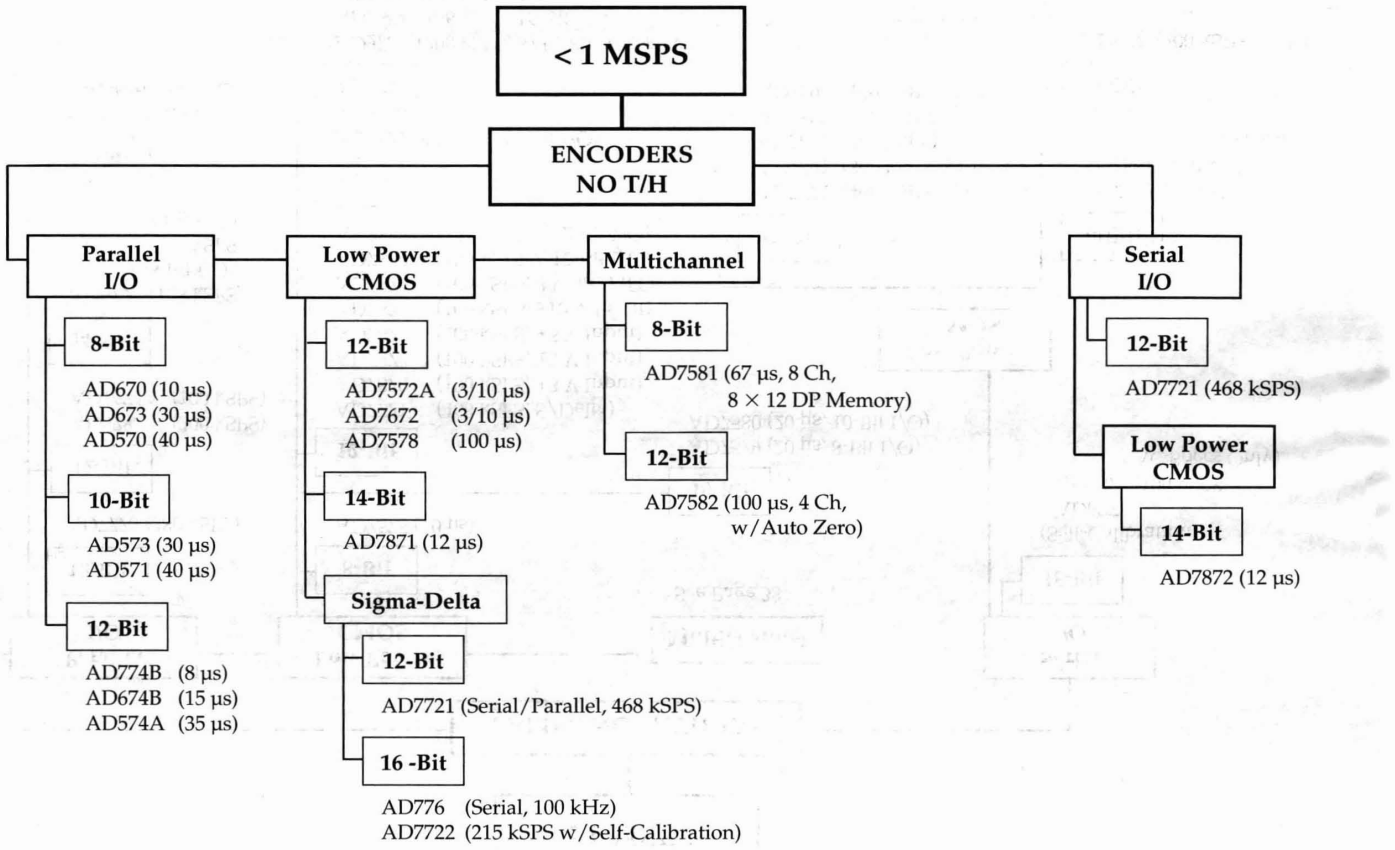


A/D Converters, Overview—Selection Trees

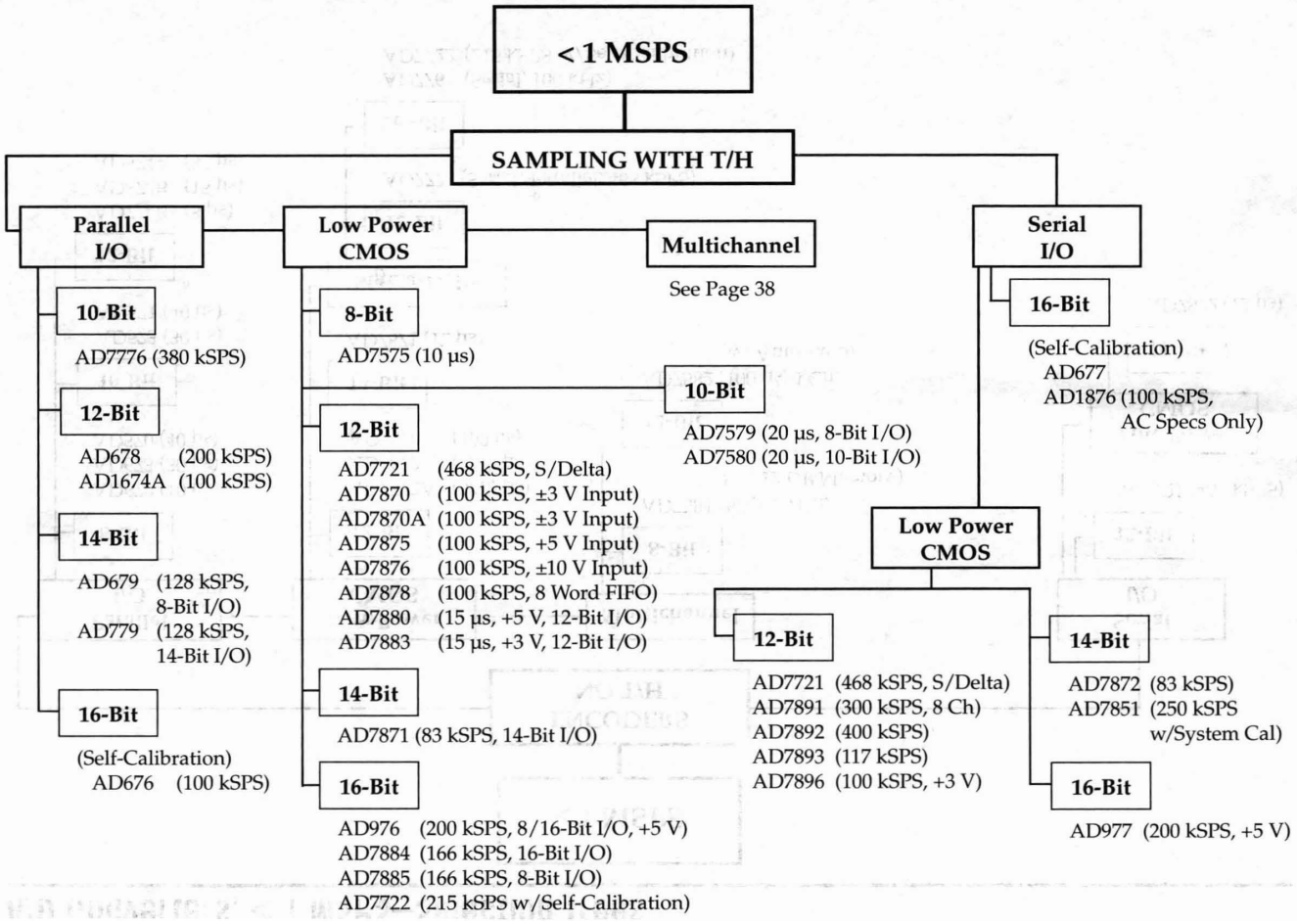


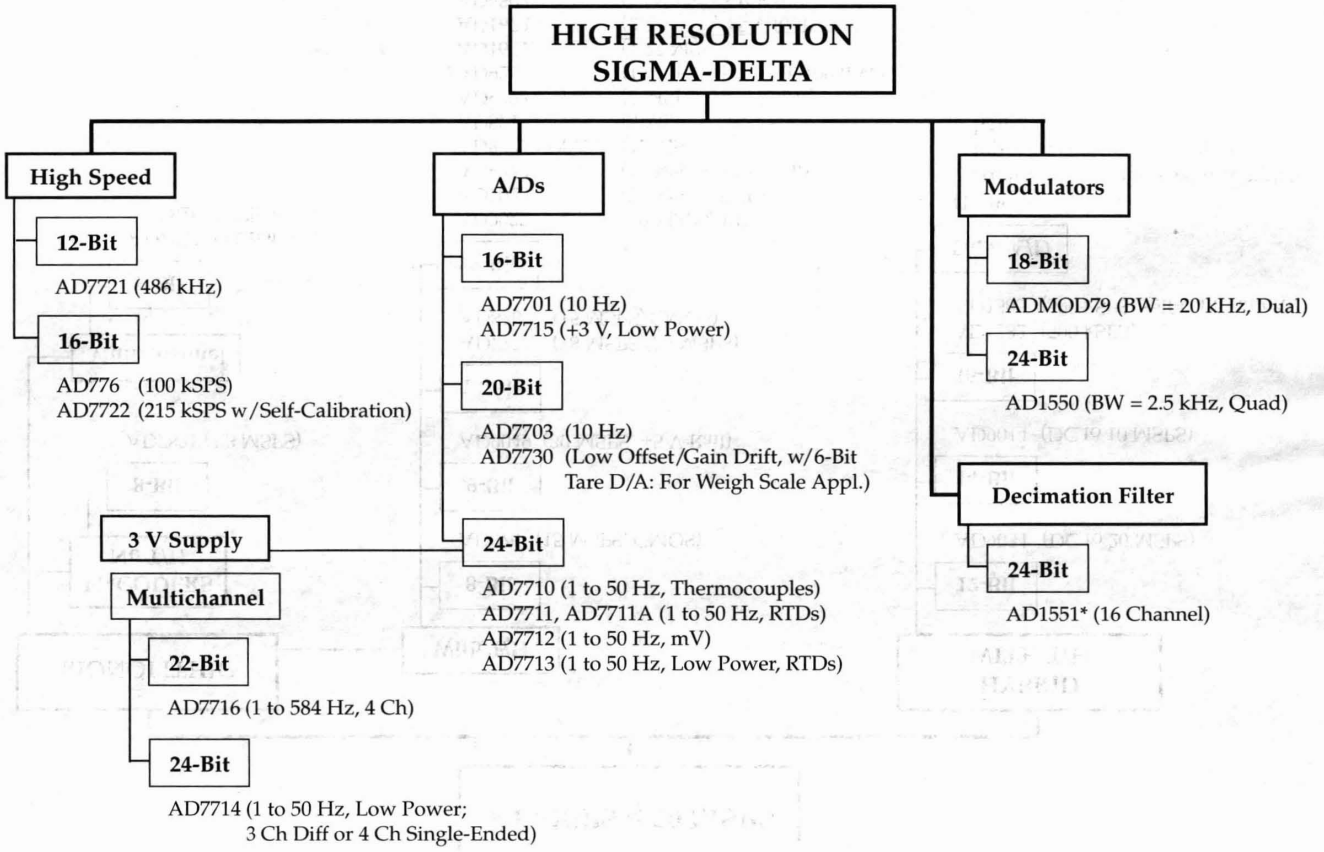
* Only covers A/Ds < 1 MSPS.

A/D Converters, < 1 MSPS—Selection Trees



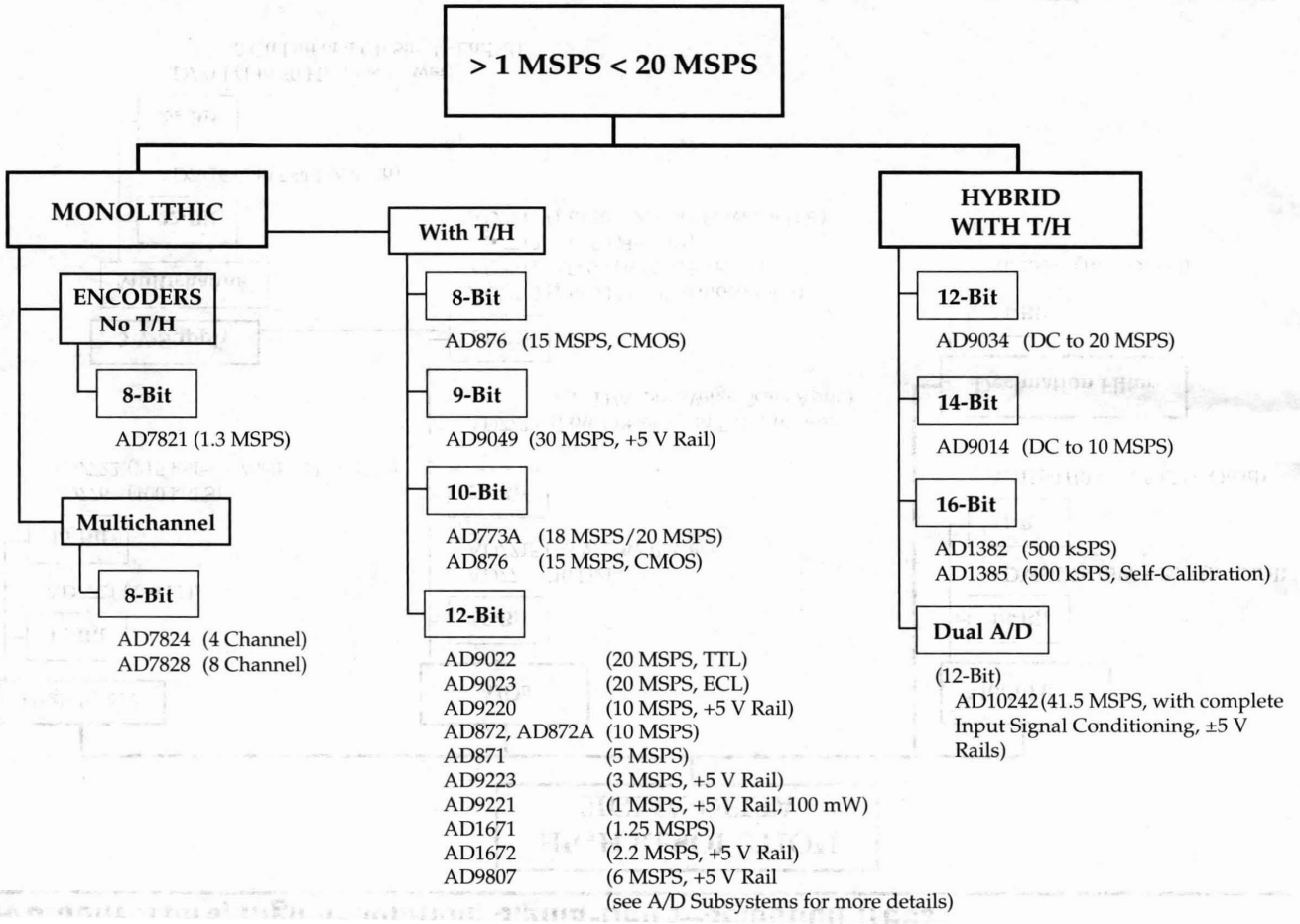
A/D Converters, < 1 MSPS—Selection Trees



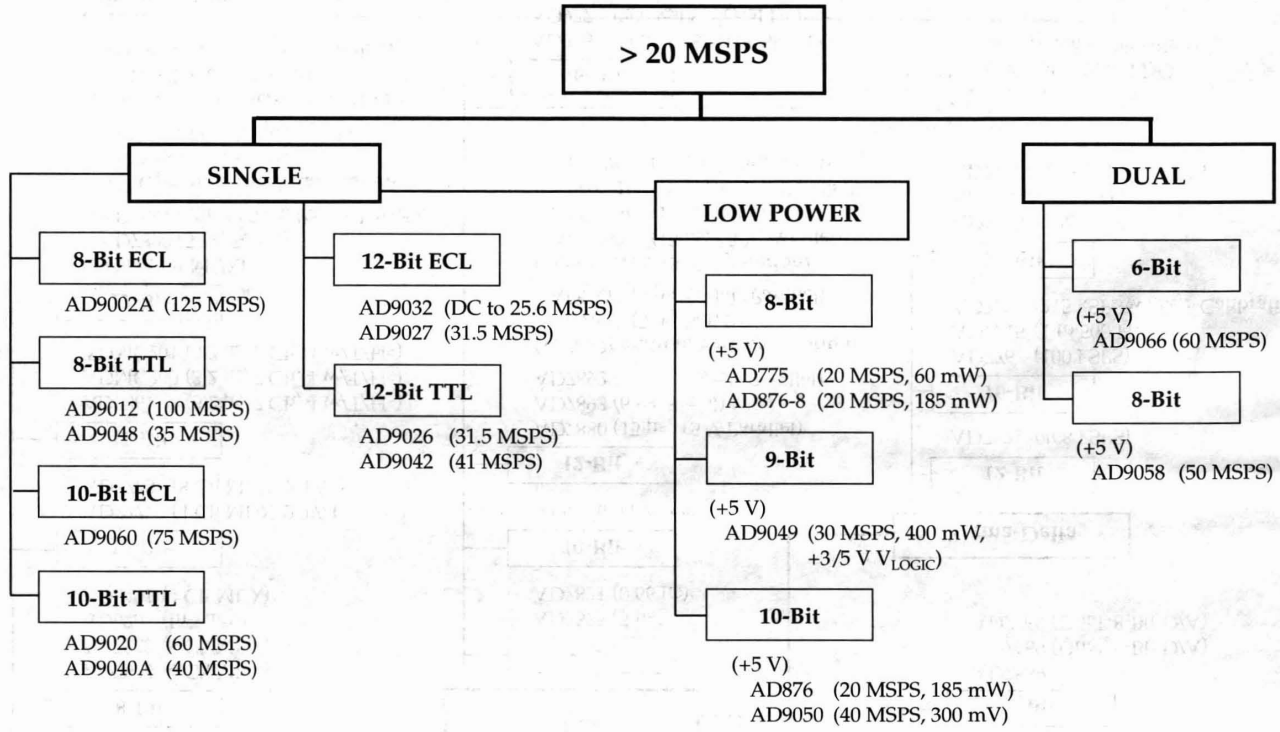


*One AD1551 Can Service Four AD1550s

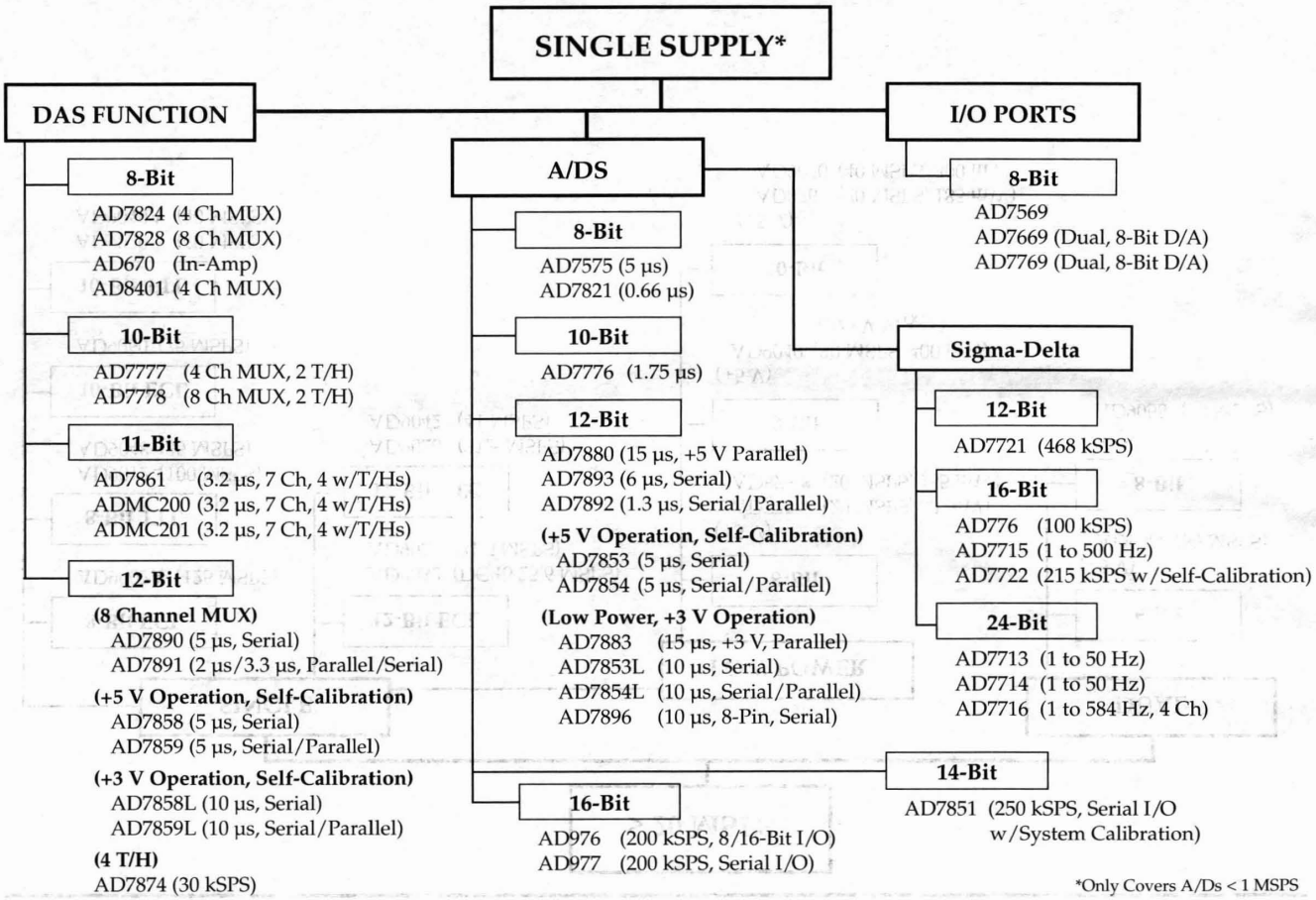
A/D Converters, > 1 MSPS–Selection Trees



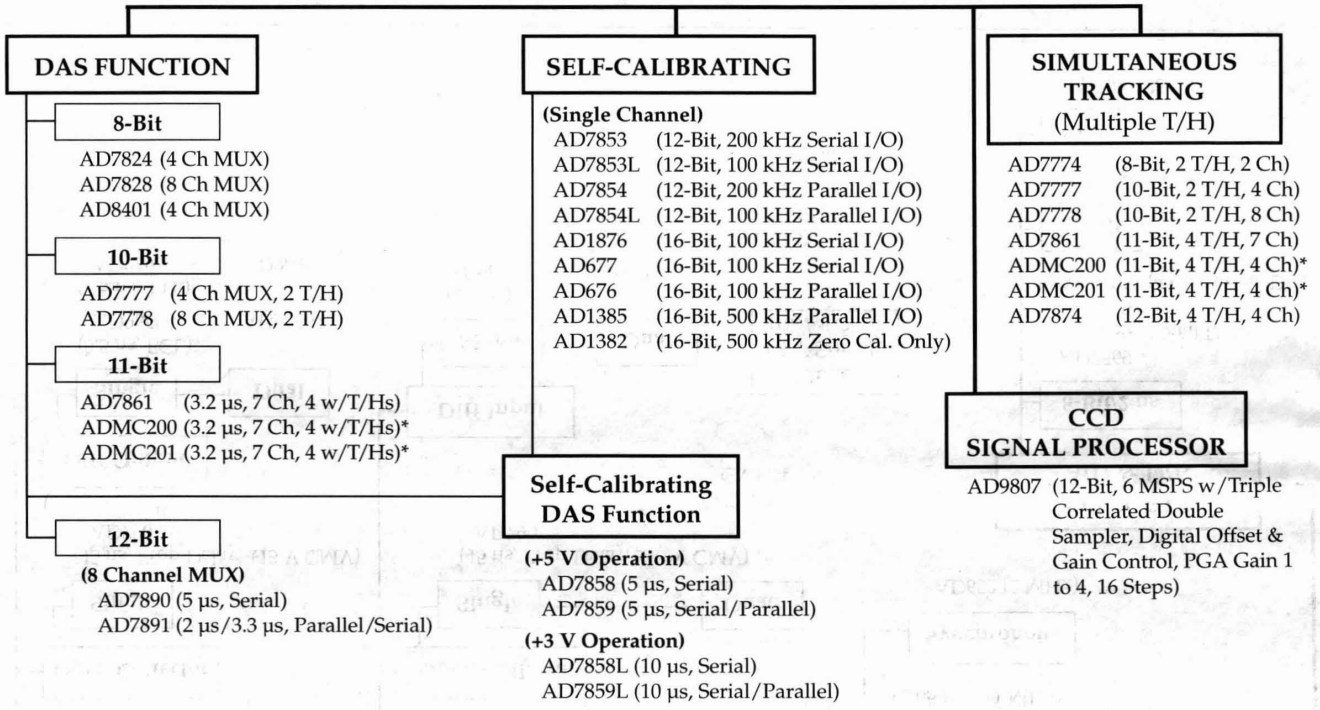
A/D Converters, > 20 MSPS—Selection Trees



A/D Converters, Single Supply–Selection Trees

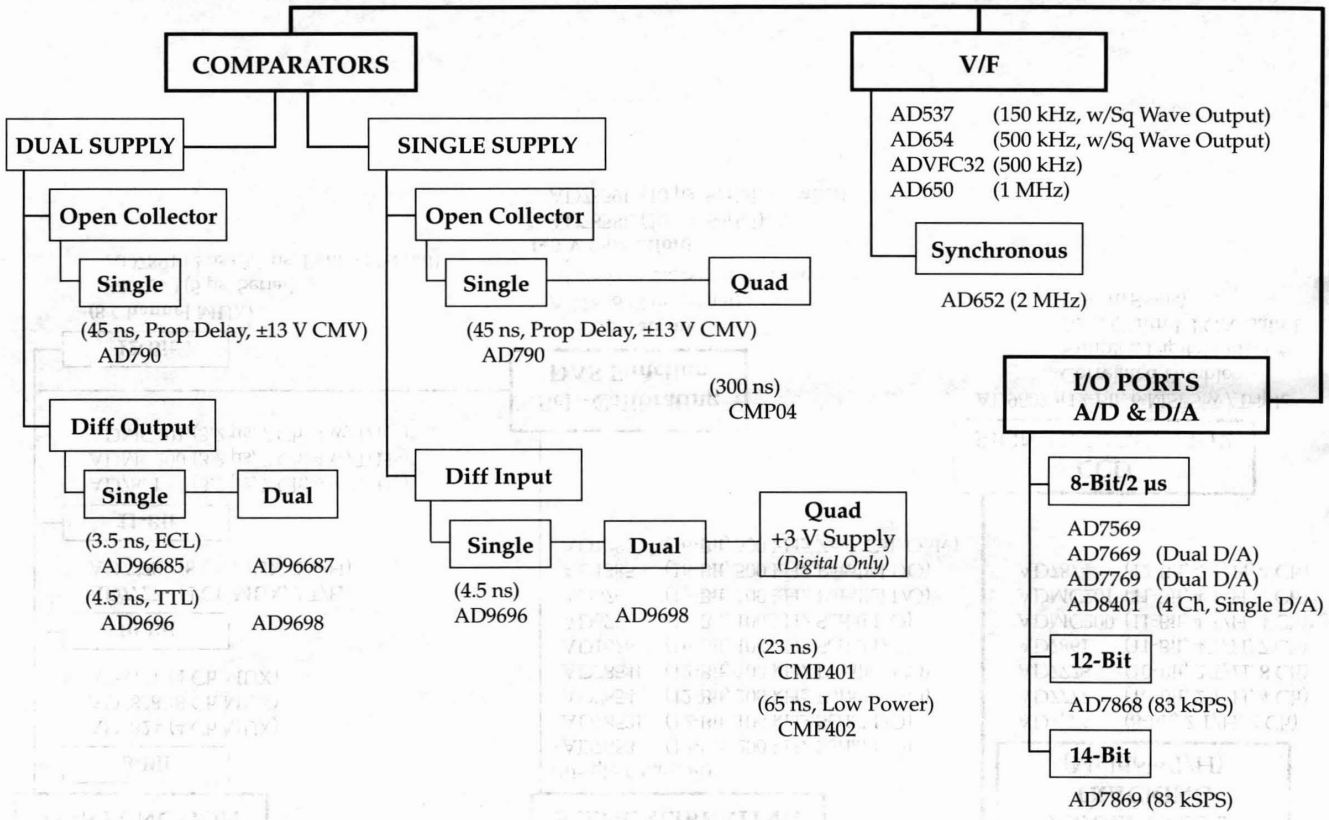


A/D Converters, Subsystems—Selection Trees

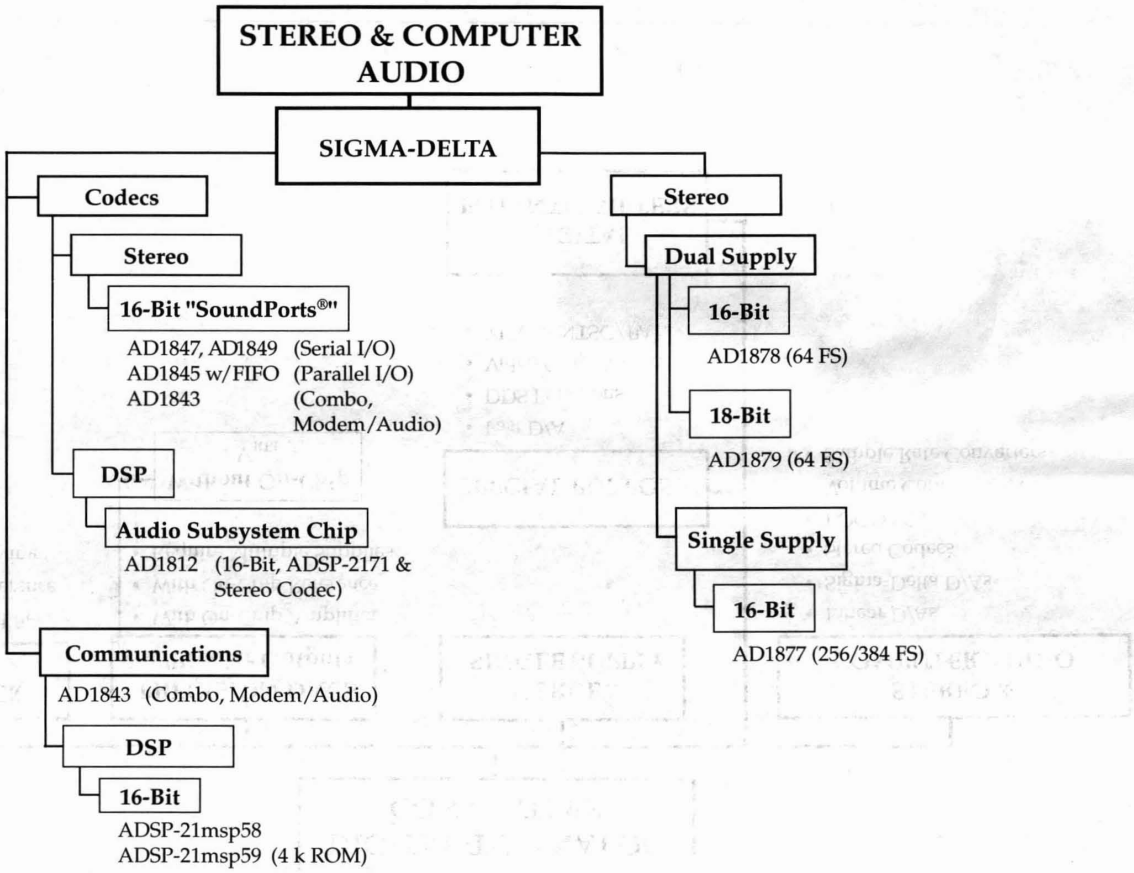

DAS FUNCTION
8-Bit
AD7824 (4 Ch MUX)
AD7828 (8 Ch MUX)
AD8401 (4 Ch MUX)
10-Bit
AD7777 (4 Ch MUX, 2 T/H)
AD7778 (8 Ch MUX, 2 T/H)
11-Bit
AD7861 (3.2 µs, 7 Ch, 4 w/T/Hs)
ADMC200 (3.2 µs, 7 Ch, 4 w/T/Hs)*
ADMC201 (3.2 µs, 7 Ch, 4 w/T/Hs)*
12-Bit
(8 Channel MUX)
AD7890 (5 µs, Serial)
AD7891 (2 µs/3.3 µs, Parallel/Serial)
SELF-CALIBRATING
(Single Channel)
AD7853 (12-Bit, 200 kHz Serial I/O)
AD7853L (12-Bit, 100 kHz Serial I/O)
AD7854 (12-Bit, 200 kHz Parallel I/O)
AD7854L (12-Bit, 100 kHz Parallel I/O)
AD1876 (16-Bit, 100 kHz Serial I/O)
AD677 (16-Bit, 100 kHz Serial I/O)
AD676 (16-Bit, 100 kHz Parallel I/O)
AD1385 (16-Bit, 500 kHz Parallel I/O)
AD1382 (16-Bit, 500 kHz Zero Cal. Only)
Self-Calibrating DAS Function
(+5 V Operation)
AD7858 (5 µs, Serial)
AD7859 (5 µs, Serial/Parallel)
(+3 V Operation)
AD7858L (10 µs, Serial)
AD7859L (10 µs, Serial/Parallel)
SIMULTANEOUS TRACKING
(Multiple T/H)
AD7774 (8-Bit, 2 T/H, 2 Ch)
AD7777 (10-Bit, 2 T/H, 4 Ch)
AD7778 (10-Bit, 2 T/H, 8 Ch)
AD7861 (11-Bit, 4 T/H, 7 Ch)
ADMC200 (11-Bit, 4 T/H, 4 Ch)*
ADMC201 (11-Bit, 4 T/H, 4 Ch)*
AD7874 (12-Bit, 4 T/H, 4 Ch)
CCD SIGNAL PROCESSOR
AD9807 (12-Bit, 6 MSPS w/Triple Correlated Double Sampler, Digital Offset & Gain Control, PGA Gain 1 to 4, 16 Steps)

* See Motion Control Section for More Detail

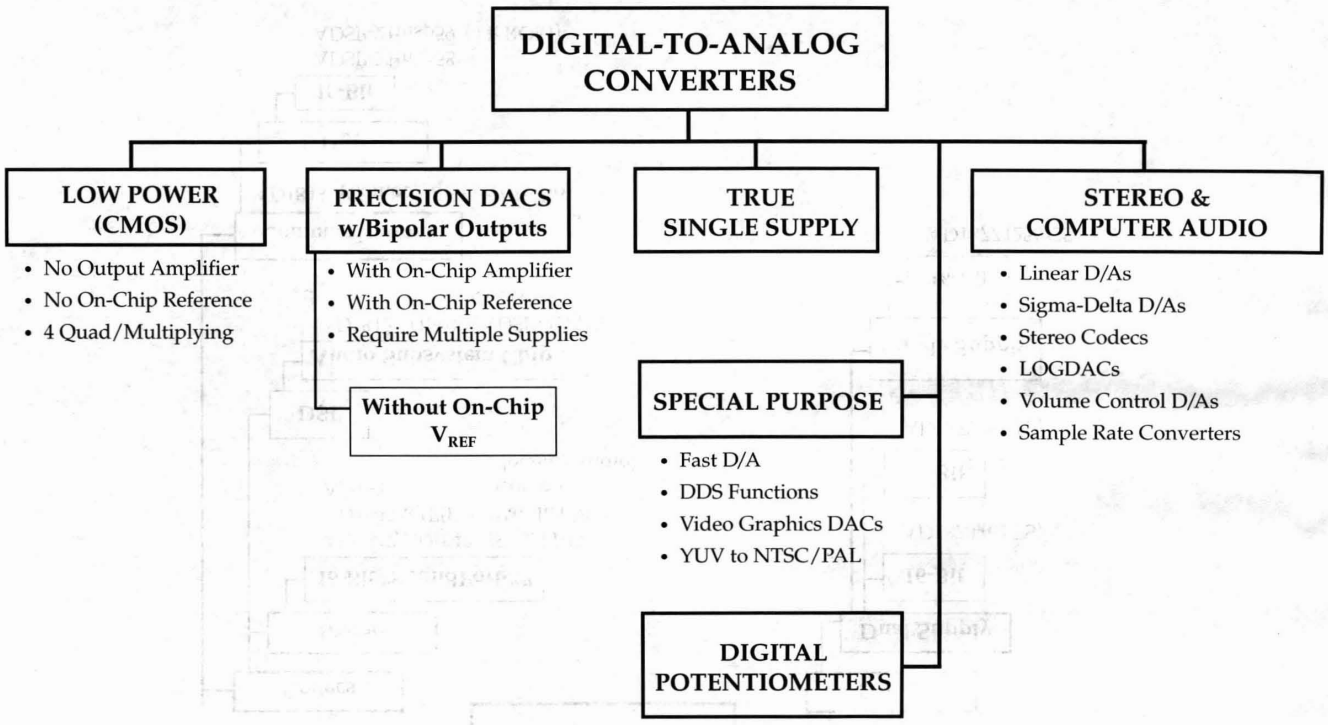
A/D Converters, Special Purpose—Selection Trees

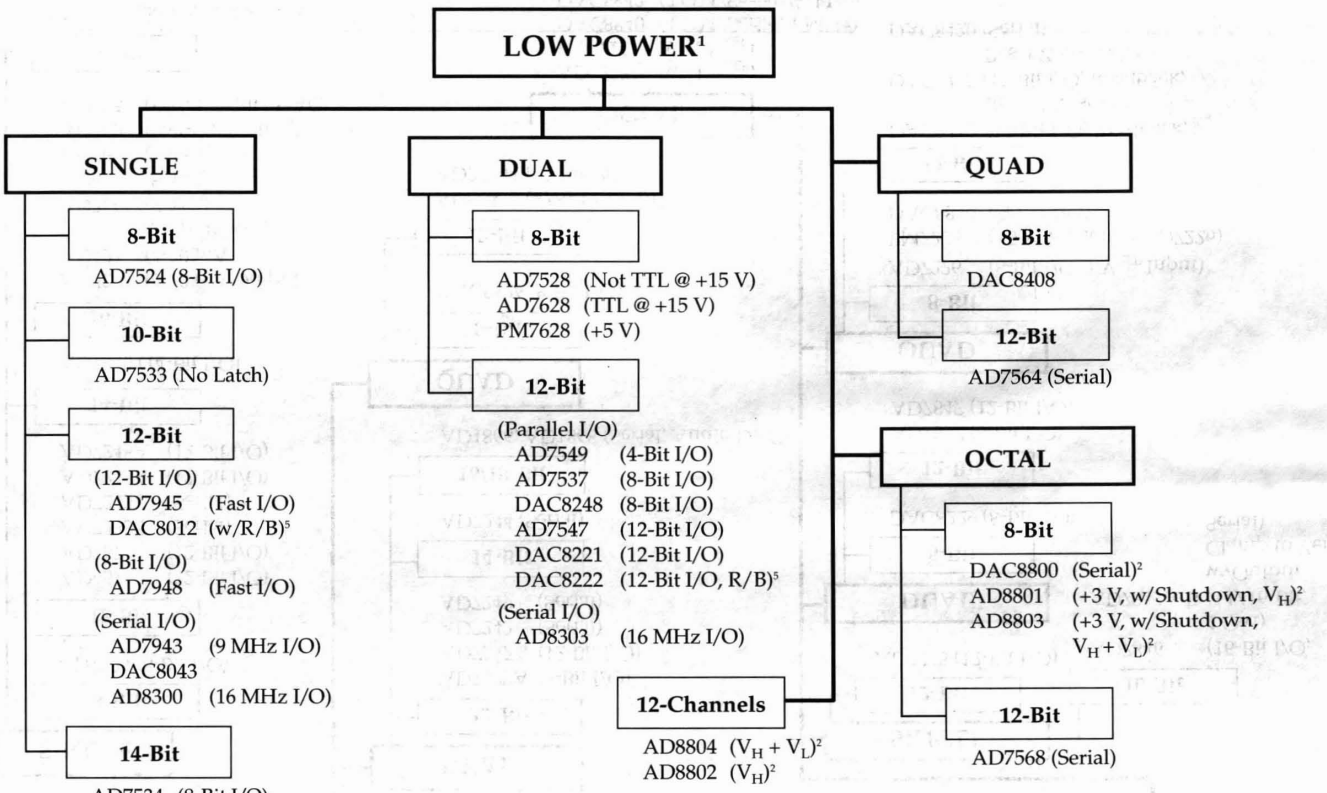


A/D Converters, Stereo & Computer Audio—Selection Trees



D/A Converters-Overview–Selection Trees

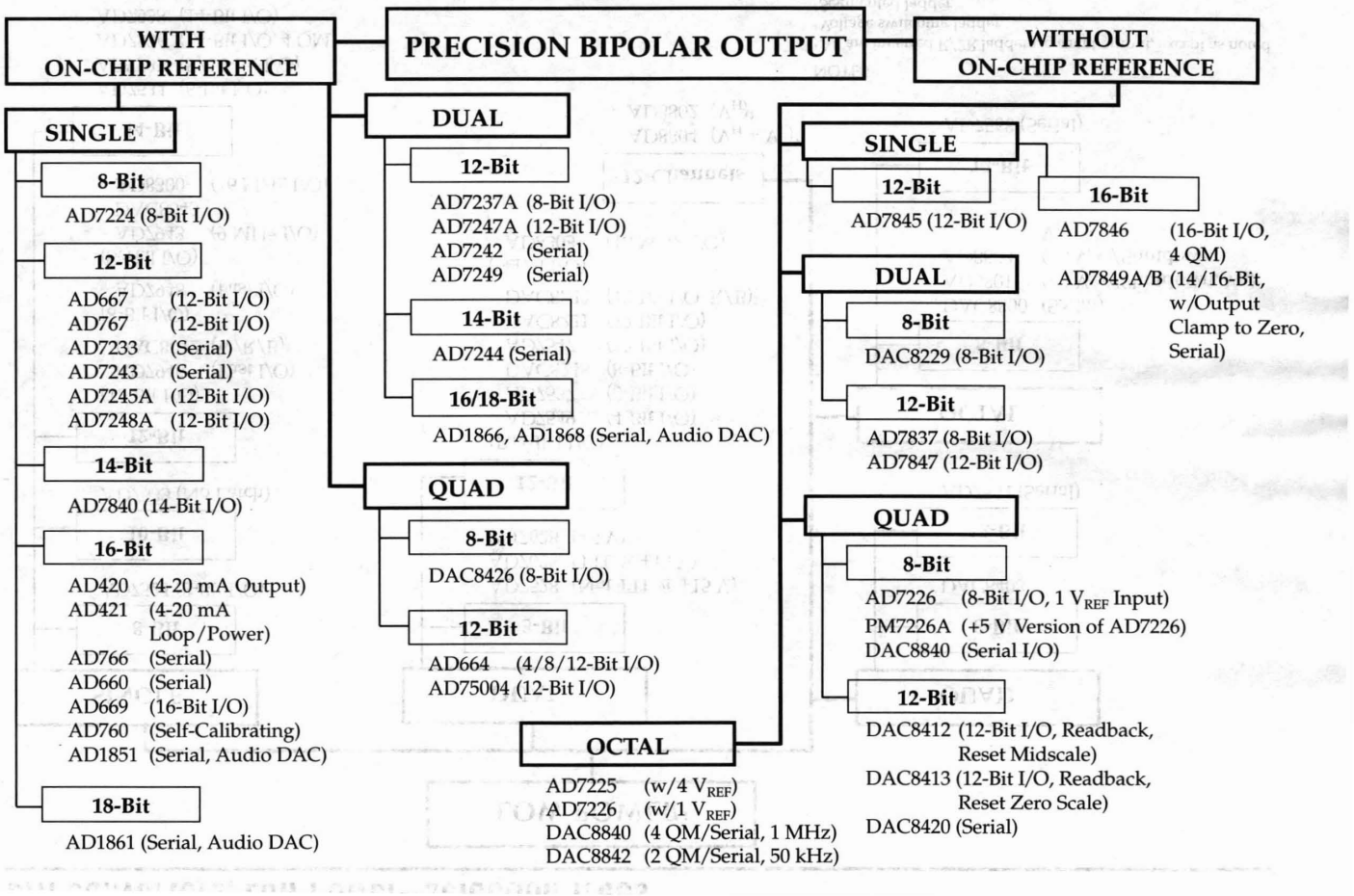




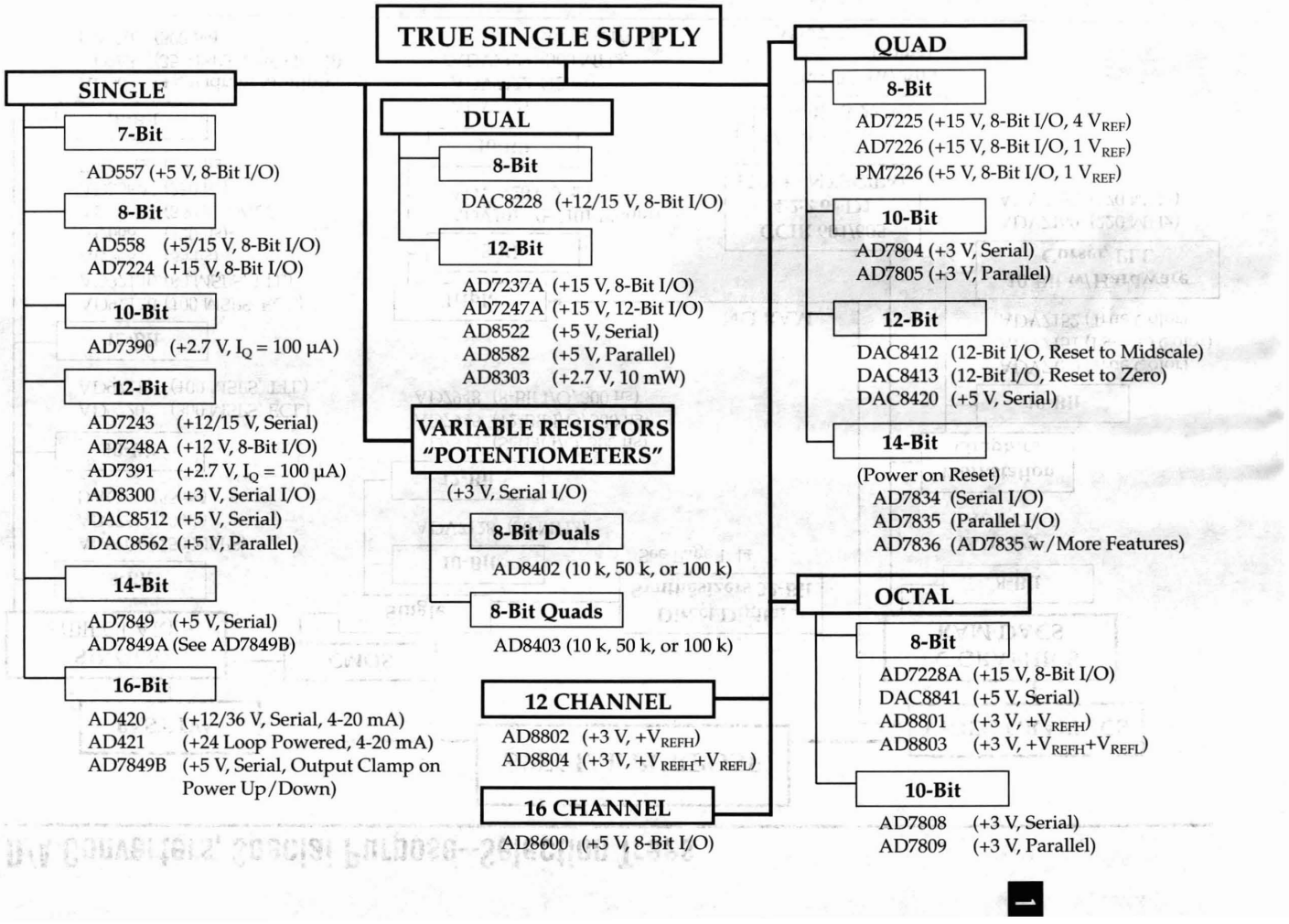
NOTES

[1] All are inverted R/2R ladders, current output, except as noted.
[2] Voltage switching ladder.
[3] Segmented ladder.
[4] 4 QM = 4 quadrant multiplying on-chip resistors.
[5] R/B = Readback feature.

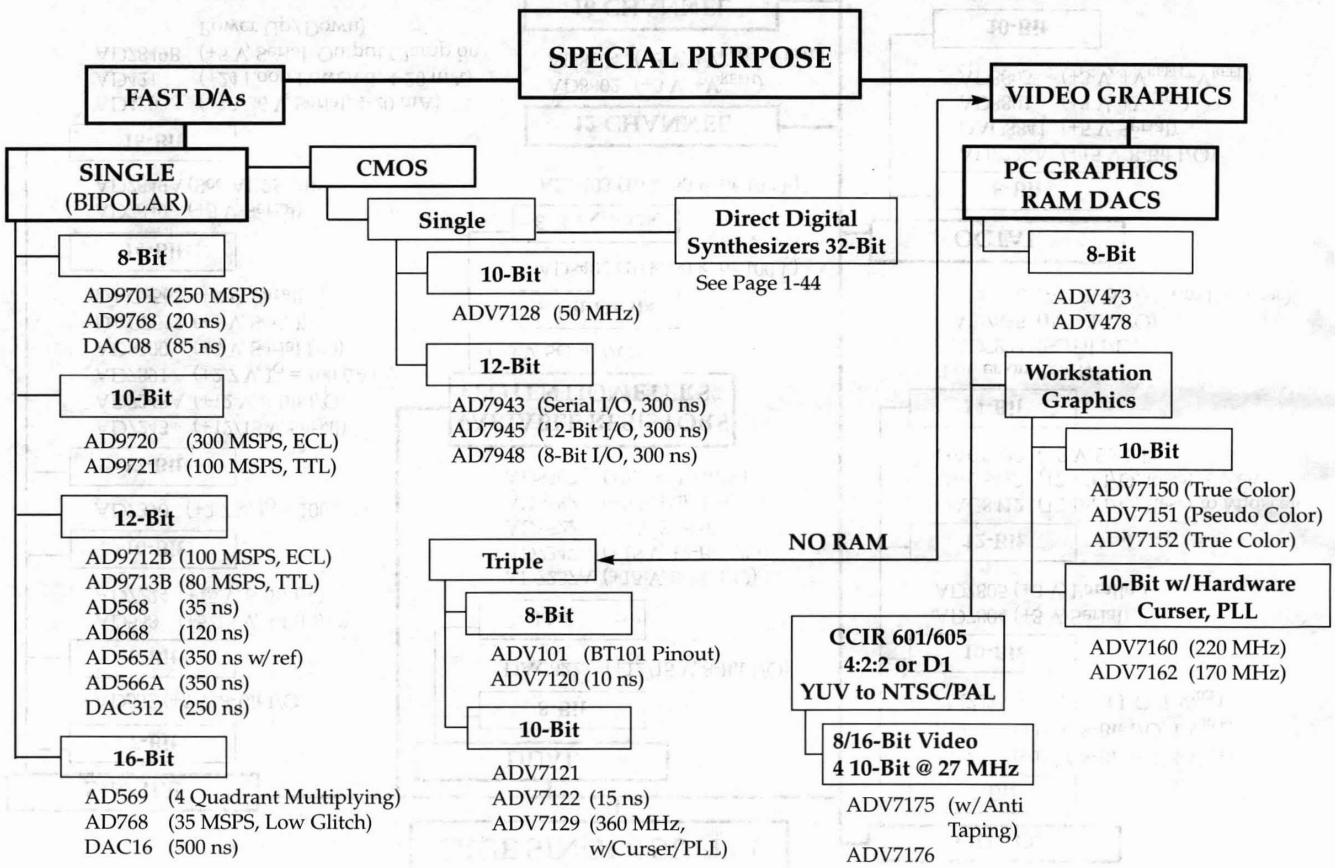
D/A Converters, Precision–Selection Trees

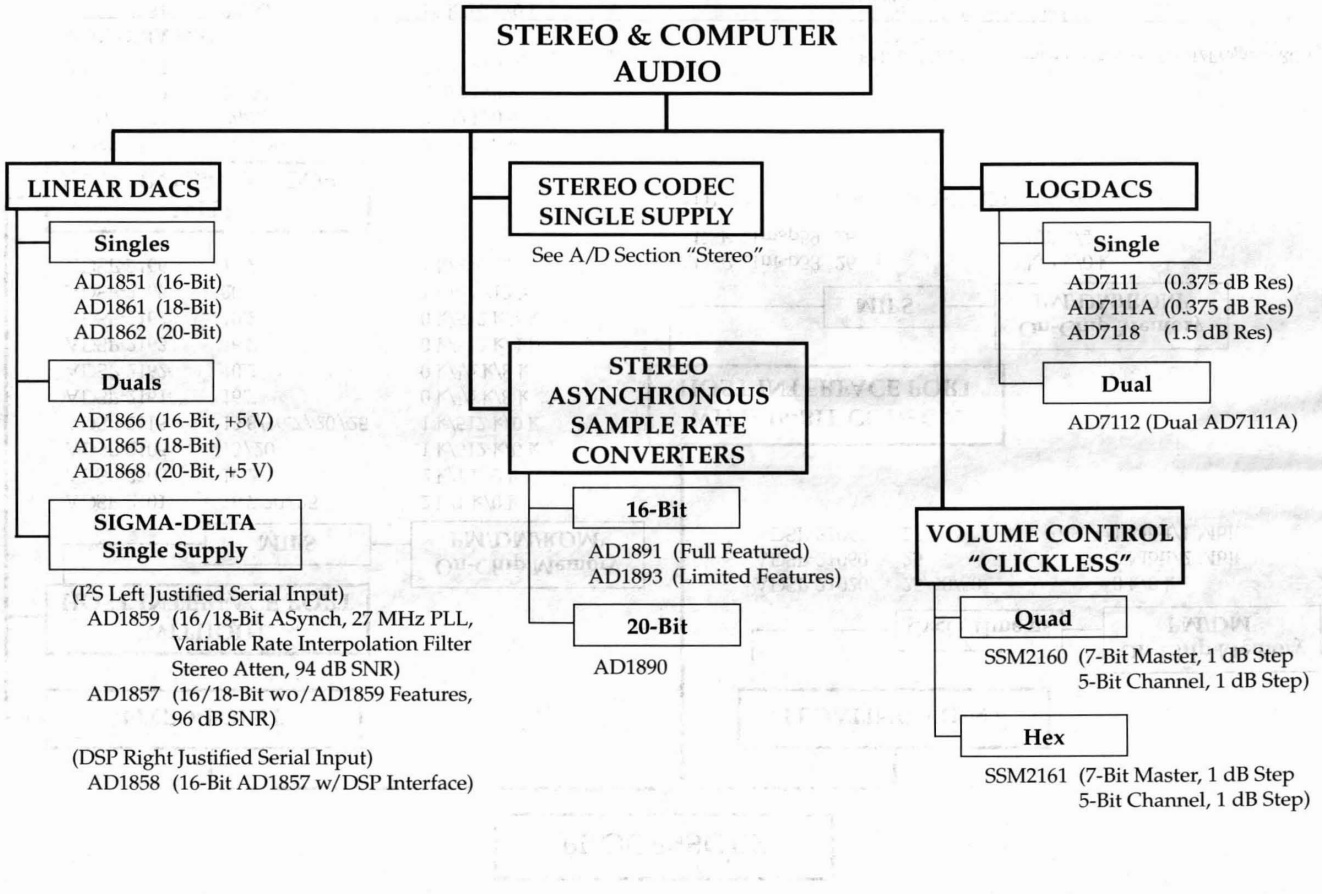


D/A Converters, True Single Supply—Selection Trees

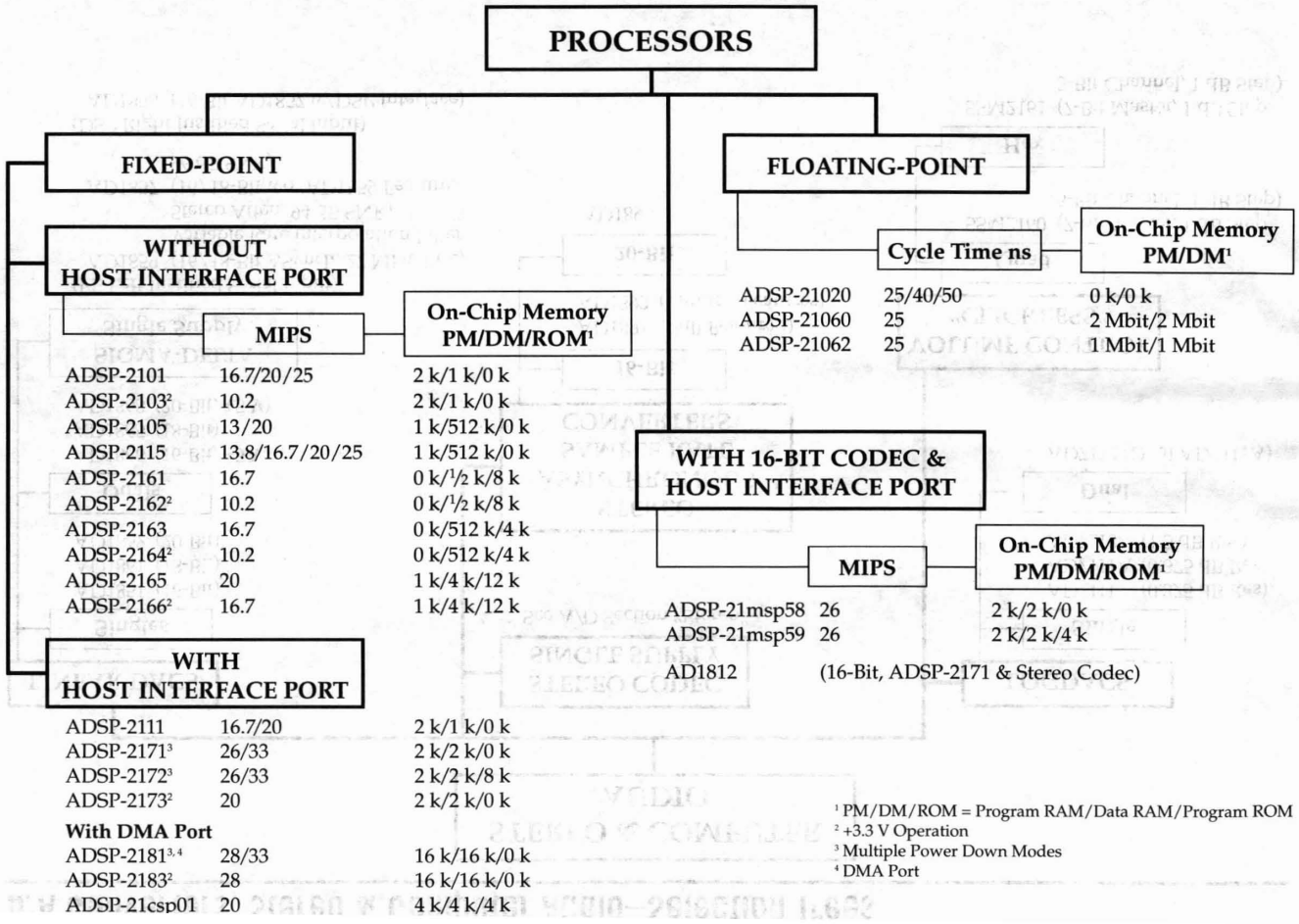


D/A Converters, Special Purpose–Selection Trees

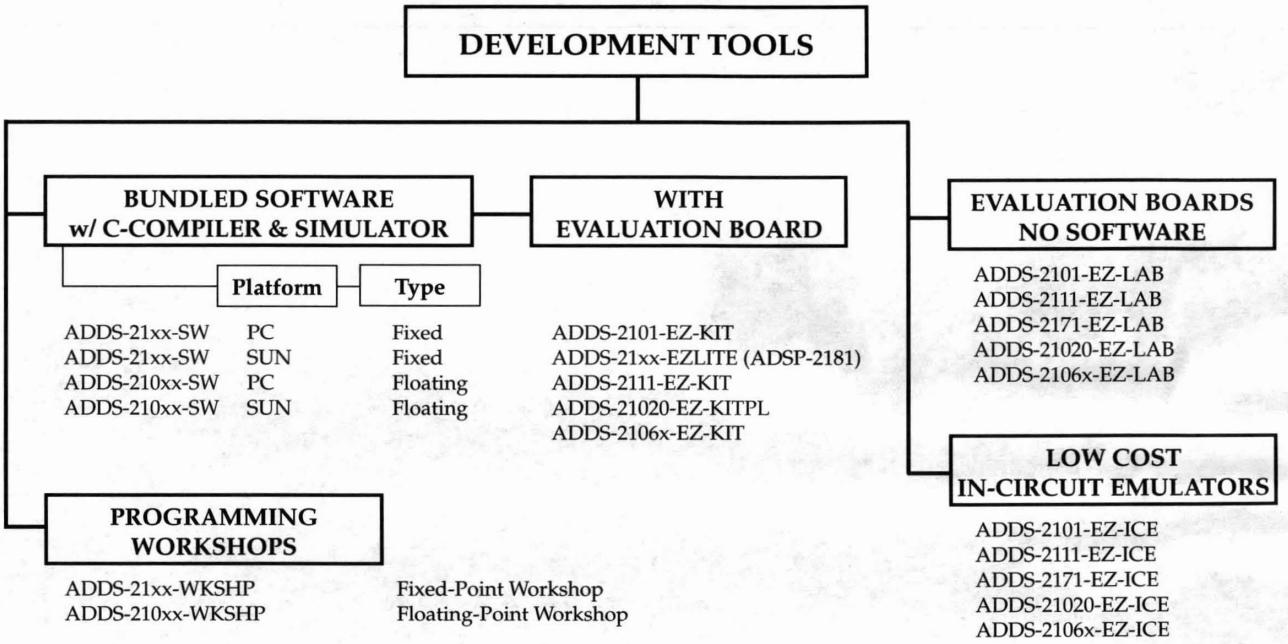



STEREO & COMPUTER AUDIO
LINEAR DACS
Singles
AD1851 (16-Bit)
AD1861 (18-Bit)
AD1862 (20-Bit)
Duals
AD1866 (16-Bit, +5 V)
AD1865 (18-Bit)
AD1868 (20-Bit, +5 V)
SIGMA-DELTA Single Supply
(I²S Left Justified Serial Input)
AD1859 (16/18-Bit ASynch, 27 MHz PLL, Variable Rate Interpolation Filter Stereo Atten, 94 dB SNR)
AD1857 (16/18-Bit wo/AD1859 Features, 96 dB SNR)
(DSP Right Justified Serial Input)
AD1858 (16-Bit AD1857 w/DSP Interface)
STEREO CODEC SINGLE SUPPLY
See A/D Section "Stereo"
STEREO ASYNCHRONOUS SAMPLE RATE CONVERTERS
16-Bit
AD1891 (Full Featured)
AD1893 (Limited Features)
20-Bit
AD1890
LOGDACS
Single
AD7111 (0.375 dB Res)
AD7111A (0.375 dB Res)
AD7118 (1.5 dB Res)
Dual
AD7112 (Dual AD7111A)
VOLUME CONTROL "CLICKLESS"
Quad
SSM2160 (7-Bit Master, 1 dB Step 5-Bit Channel, 1 dB Step)
Hex
SSM2161 (7-Bit Master, 1 dB Step 5-Bit Channel, 1 dB Step)

Digital Signal Processing, Processors—Selection Trees


PROCESSORS
FIXED-POINT
WITHOUT HOST INTERFACE PORT
MIPS
On-Chip Memory PM/DM/ROM[1]
ADSP-2101 16.7/20/25 2 k/1 k/0 k
ADSP-2103[2] 10.2 2 k/1 k/0 k
ADSP-2105 13/20 1 k/512 k/0 k
ADSP-2115 13.8/16.7/20/25 1 k/512 k/0 k
ADSP-2161 16.7 0 k/½ k/8 k
ADSP-2162[2] 10.2 0 k/½ k/8 k
ADSP-2163 16.7 0 k/512 k/4 k
ADSP-2164[2] 10.2 0 k/512 k/4 k
ADSP-2165 20 1 k/4 k/12 k
ADSP-2166[2] 16.7 1 k/4 k/12 k
WITH HOST INTERFACE PORT
ADSP-2111 16.7/20 2 k/1 k/0 k
ADSP-2171[3] 26/33 2 k/2 k/0 k
ADSP-2172[3] 26/33 2 k/2 k/8 k
ADSP-2173[2] 20 2 k/2 k/0 k
With DMA Port
ADSP-2181[3,4] 28/33 16 k/16 k/0 k
ADSP-2183[2] 28 16 k/16 k/0 k
ADSP-21csp01 20 4 k/4 k/4 k
FLOATING-POINT
Cycle Time ns
On-Chip Memory PM/DM[1]
ADSP-21020 25/40/50 0 k/0 k
ADSP-21060 25 2 Mbit/2 Mbit
ADSP-21062 25 1 Mbit/1 Mbit
WITH 16-BIT CODEC & HOST INTERFACE PORT
MIPS
On-Chip Memory PM/DM/ROM[1]
ADSP-21msp58 26 2 k/2 k/0 k
ADSP-21msp59 26 2 k/2 k/4 k
AD1812 (16-Bit, ADSP-2171 & Stereo Codec)

[1] PM/DM/ROM = Program RAM/Data RAM/Program ROM
[2] +3.3 V Operation
[3] Multiple Power Down Modes
[4] DMA Port



Note:
ADSP-21csp01: Compliers/Software/Evaluation Boards & Emulators Are Under Development

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<1 MSPS, without T/H

Single Supply

Model	# Bits	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Convert Time µs	Linearity LSBs +25°C	Voltage Reference Int	I/O	# Pins	Page No.	Comments	Fax-code
AD670	8	+5 @ 45 mA	255 mV/+2.5	10	1/4–1/2	Yes	P8	20	*	Pin Strap Full-Scale Options	1222
AD7821	8	+5 @ 5 mA	V_{REF}	0.66	1	No	P8	20	2–71		1358
AD7581	8	+5 @ 5 mA	$\pm V_{REF}$	128	1/2–1 7/8	No	P8	28	*	8 × 8 Dual Ported RAM	1321
AD7580	10	+5 @ 10 mA	2.5	18	1/2–1	No	P10	24	*		1321

Multiple Supply

Model	# Bits	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Convert Time µs	Linearity LSBs +25°C	Voltage Reference Int	I/O	# Pins	Page No.	Comments	Fax-code
AD570	8	+5, –12–15 @ 15 mA	10, ±5	40	1/2	Yes	P8	18	*		1168
AD673	8	+5, –12–15 @ 15 mA	All	30	1/2	Yes	P10	20	*		1224
AD571	10	+5, –12–15 @ 15 mA	10, ±5	40	1/2–1	Yes	P10	18	*		1169
AD573	10	+5, –12–15 @ 25 mA	10, ±5	30	1/2–1	Yes	P10	20	*		1171
AD574A	12	+5, –12–15 @ 30 mA	All	35	1/2–1	Yes	P4/8/12	28	2–13	Industry Standard	1172
AD674B	12	+5, –12–15 @ 7 mA	All	15	1/2–1	Yes	P4/8/12	28	*	Industry Standard	1226
AD774B	12	+5, –12–15 @ 7 mA	All	8	1/2	Yes	P4/8/12	28	*	Industry Standard	1226

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

A/D Converters & Data Acquisition Subsystems–Selection Guides

<1 MSPS, with T/H

Multiple Supply

Model	# Bits	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Pins	Page No.	Comments	Fax-code
AD1674A	12	±/12 @ 12 mA, +5 @ 8 mA	All	100	1/2–1	+10		P8/16	28	2–41	Industry Standard	1060
AD7870A	12	±/5 @ 13 mA	±3	100	1/2–1	+3		P12	24	2–91	Mode 1 Oper, CS/RS Control Bus	1898
AD7870	12	±/5 @ 13 mA	±3	100	1/2–1	+3		P12	24	2–91		1375
AD7875	12	±/5 @ 13 mA	+5	100	1/2–1	+3		P12	24	2–91		1375
AD7876	12	±/5 @ 13 mA	±10	100	1/2–1	+3		P12	24	2–91		1375
AD7878	12	±/5 @ 5 mA	±3	100	NS	+3		P12	28	*	With 8 × 12 FIFO Memory	1376
AD678	12	±/12 @ 25 mA, +5 @ 12 mA	+10, ±5	200	1/2–1	+5		P8/16	28	*		1229
AD7886	12	±/5 @ 35 mA	+5/10	666	1.5–2		+5	P12	28	*		1381
AD7871	14	±/5 @ 13 mA	±3	83	1	+3		P14	28	2–93		1371
AD7872	14	±/5 @ 13 mA	±3	83	1	+3		S	16	2–93		1372
AD679	14	±/12 @ 25 mA, +5 @ 12 mA	+10, ±5	100	2	+5		P14	S	*		1230
AD779	14	±/12 @ 25 mA, +5 @ 12 mA	+10, ±5	100	2	+5		P14	S	*		1354
AD1380	16	±/15 @ 30 mA, +5 @ 15 mA	All	50	4	+10		P16	32	*		1054
AD1876	16	±12 @ 12 mA	$+V_{REF}$	100	NS		+3 –10	S	16	2–43	Self-Calibration	1073
AD676	16	±12 @ 12 mA	±10	100	1 1/2		+5 –10	P16	24	2–15	Self-Calibration	1227
AD677	16	±12 @ 12 mA	±10	100	1 1/2		+5 –10	S	16	2–17	Self-Calibration	1228
AD7884	16	±/5 @ 13 mA	±5/+3	166	4 1/2		+3	P16	40/44	2–103		1379
AD7885	16	±/5 @ 13 mA	±5/+3	166	4 1/2		+3	P8	28/44	2–103		1380
AD1382	16	±/15 @ 65 mA, +5 @ 160 mA	±5/10	500	4	+10		P16	DH48	2–35	Self-Calibration, Zero Only	1055
AD1385	16	±/15 @ 75 mA, +5 @ 160 mA	±5/10	500	4	+10		P16	DH48	2–37	Self-Calibration, Zero and Linearity	1056

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Sigma Delta <1 MSPS

Model	# Bits	Power Supply $+V_{CC}$ Volts	f_{CLOCK} MHz	Sample Rate	Resolution vs. Update Rate Min/Max Bits	Linearity LSBs % FS	# Pins	Page No.	Comments	Fax-code
Clock Programmable Filter, –3 dB Cutoff & Update Rate										
AD7701	16	±5 @ 4 mA	4.096	$f_{CLK}/256$	16	0.0015–0.003	20	2–47	5-Pole Brickwall Filter	1336
AD7703	20	±5 @ 4 mA	4.096	$f_{CLK}/256$	20	0.0015–0.003	20	2–49	5-Pole Brickwall Filter	1337
Software Programmable Filter, –3 dB Cutoff & Update Rate†										
AD7710	24	±5 @ 7/1.5 mA	10	$f_{CLK}/512$	21.5/11	0.0045	24	2–51	Optimized for T/Couples	1338
AD7711	24	±5 @ 7/1.5 mA	10	$f_{CLK}/512$	21.5/11	0.0045	24	2–53	Optimized for 4 Wire RTD	1339
AD7711A	24	±5 @ 7/1.5 mA	10	$f_{CLK}/512$	21.5/12	0.0045	24	2–55	Optimized for 2 Wire RTD	1828
AD7712	24	±5 @ 7/1.5 mA	10	$f_{CLK}/512$	21.5/11	0.0045	24	2–51	Optimized for mV Inputs	1340
AD7713	24	+5 @ 1 mA	2.46	$f_{CLK}/512$	22/12	0.0045	24	2–53	Optimized for 4 Wire RTD and T/Couples	1341
AD7714	24	+3–+5 @ 0.5 mA	2.46	$f_{CLK}/512$	21.5/11	0.0015	24	2–57	Optimized for 4 Wire RTD, and Low Power Transmitters	1812
AD7715	16	+3–+5 @ 0.5/2 mA	2.46	$f_{CLK}/512$	21.5/11	0.0015	16	2–59	Buffered Input, mV Input	1813
AD7730	19	+5 @ 10 mA	TBD	TBD	TBD	TBD	24	2–65	W/DAC for Offset/Tare Removal	TBD
Quad A/D										
AD7716	16	±5 @ 5/2.5 mA	8	$f_{CLK}/512$	22/16	0.0015	44	2–61	Wide Bandwidth, 99 dBc 584 Hz	1342

†$SIN(x)^3$ filter response

Features That Differentiate the AD7701–AD7730 Family

Singles	# Bits	Current Sources	PGA 1–128	+3 V Operation	100 nA I_{SOURCE} OpenT/Couple	Int +2.5 V Reference	Read/Write Coefficient	Software Powerdown	Hardware Powerdown
AD7701	16					X			X
AD7703	16					X			X
AD7710	24	20 µA	X		X	X	X	X	
AD7711	24	2 200 µA	X			X	X	X	
AD7711A	24	1 400 µA	X			X	X	X	
AD7712	24		X		X	X	X	X	X
AD7713	24	2 200 µA	X		X		X	X	X
AD7714	24		X	X			X		X
AD7715	16		X	X					
AD7730	19		1 to 8		X		X	X	X

Note: All specifications after calibration

A/D Converters & Data Acquisition Subsystems–Selection Guides

Sigma-Delta <1 MSPS

Single Channel Wide Bandwidth Sigma-Delta Converters

Model	# Bits	Over Sample Rate	Power Supply Requirements $+V_{CC}$ Volts	Analog Input BW kHz	THD Plus Noise dB	SINAD dB	# Pins	Page No.	Comments	Fax-code
AD7721	12	468	+5 @ 35 mA	229.2	80	74	28	2–63	12-Bit Mode	1829
AD7721	16	312	+5 @ 35 mA	152	78	70	28	2–63	16-Bit Mode	1829
AD776	16	100	+5 @ 40 mA	45	80	88	20	2–23		1346

>1 MSPS AC Specs Only

Model	# Bits	Sample Rate MSPS	Input BW MHz	SNR No. Harmonics	SFDR –dB	SINAD S(N+D) dB	Test Conditions F_{IN} MHz	F_{SAMPLE} MHz	# Pins	Page No.	Comments	Fax-code
Single Supply												
AD9066	6	60	NS	NS	NS	34	15	60	28	2–141	Dual A/D	1905
AD775	8	20	NS	NS	NS	41	5	20	24	2–21	F_{SAMPLE} Rate Min = DC	1345
AD9059	8	60	120	47	NS	46	10.3	60	28	*	Dual A/D	
AD9054-100	8	100	200	49	NS	46	2.3	100	44	*		1937
AD9054-200	8	200	300	49	NS	46	2.3	200	44	*		1937
AD9049	9	30	100	51	NS	50	10.3	30	28	2–133	400 mW, –60 dBc 2nd & 3rd	1976
AD876	10	20	NS	NS	NS	55	3.58	20	48	2–29	I/O = +3 V or +5 V	1838
AD9050	10	40	100	53.5	NS	53	10.3	40	28	2–135		1843
AD9221	12	1	35	NS	83	70	0.5	1	28	2–145	50 mW	1936
AD9223	12	3	10	NS	76	68	1.5	3	28	2–147	100 mW	1936
AD1672	12	3	20	66	65	63	0.5	3	28	2–39		1880
AD9220	12	10	35	69	77.5	70	1	10	28	2–143	280 mW	1936
AD9042	12	41	140	70	81	69	9.6	41	28	2–129	SFDR = 90 dB with Dither	1922
AD9243	14	3	15		75	72	1.5	3	28	2–149	–72 dB THD @ 1.5 MHz	1976
Dual Supply												
AD9048	8	35	NS	NS	NS	45	1.248	20	28	2–131	F_{SAMPLE} Rate Min = DC	1454
AD9058	8	40	175	46	NS	45	2.3	40	44	2–137	Dual A/D	1455
AD9012	8	100	160	46	NS	NS	1.23	100	28	2–117	TTL	1445
AD9002	8	125	160	NS	NS	46	1.23	12.5	28	2–115	F_{SAMPLE} Rate Min = DC	1440
AD773A	10	20	NS	50/51	54	50/51	10	20	28	2–19	SFDR @ 1 MHz FIN	1899
AD9020	10	40	175	51	NS	50	10.3	40	68	2–119	F_{SAMPLE} Rate Min = DC	1448
AD9040A	10	40.5	48	53	NS	51	10.3	32	28	2–127		1453
AD9060	10	75	175	46	NS	44	29.3	75	68	2–139	ECL	1456
AD1671	12	1	12	NS	NS	68	0.1	1	28	*		1059
AD871	12	5	15	NS	70	63	1	5	28	2–25		1430
AD872A	12	10	70	NS	72	63	4.99	10	28	2–27		1891
AD9022	12	20	110	65	85	64	1.2	20	28	2–121	TTL	1840
AD9023	12	20		64	75	63	9.6	20	28	2–123	ECL	1841
AD9026	12	25.6	150	60	70	59	9.6	31	28	*	TTL	1842
AD9027	12	25.6	150	61	70	60	9.6	31	28	*	ECL	1842
AD9034	12	20.48	150	63	NS	NS	9.6	20.48	DH40	*	F_{SAMPLE} Rate Min = DC	1451
AD9032	12	2.5	150	62	NS	NS	9.6	25.6	DH40	2–125		1450
AD10242	12	41	TBD	NS	65	63	9.6	41	68	2–153	Dual w/Input Signal Cond.	1450
AD1385	16	0.5	NS	80	NS	NS	0.1 @ –0.05 dB	0.5	DH48	2–37	With Self-Calibration	1056

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

A/D Converters & Data Acquisition Subsystems–Selection Guides

Single Supply†

Model	# Bits	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Pins	Page No.	Comments	Fax-code
AD7776	10	+5 @ 10 mA	$V_{BIAS} - V_{SWING}$	380	1	+2		P12	24	2–69	I_Q = 1 mA w/CMOS Logic	1351
AD7883	12	+3 @ 2.5 mA	All	50	2	+2.5		P12	24	2–101	With Powerdown, Three State	1946
AD7880	12	+5 @ 10 mA	$\pm V_{REF}$	66	1		V_{DD}	P12	24	2–97	With Powerdown	1377
AD7853L	12	+3 @ 1.3 mA	$\pm/+V_{REF}/2$	100	1/2–1	+2.5		S	24	2–77	With Powerdown, Self-Calibration	1814
AD7854L	12	+3 @ 1.6 mA	$\pm/+V_{REF}/2$	100	1/2–1	+2.5		P12	24	2–79	With Powerdown, Self-Calibration	1874
AD7890	12	+5 @ 10 mA	±10/+4/2.5	100	1		+2.5	S	24	2–105	With 8 Channel Mux	1382
AD7858L	12	+3 @ 5.5 mA	$V_{REF}/2$	100	1/2–1	+2.5		S	24	2–81	With 8 Channel Mux & Self-Calibration	1814
AD7859L	12	+3 @ 5.5 mA	$V_{REF}/2$	100	1/2–1	+2.5		P12	24	2–83	With 8 Channel Mux & Self-Calibration	1874
AD7896	12	+3 @ 4.5 mA	0 to V_{CC}	117	1/2–1		V_{DD}	S	8	2–113	With Powerdown I_Q = 10 µA	1816
AD7893	12	+5 @ 10 mA	±10/+/5/2.5	117	1/2–1		V_{DD}	P12	8	2–111	With Powerdown	1385
AD7853	12	+5 @ 5.5 mA	$\pm/+V_{REF}/2$	200	1/2–1	+2.5		P8/12	24	2–77	With Powerdown, Self-Calibration	1814
AD7854	12	+5 @ 5.5 mA	$\pm/+V_{REF}/2$	200	1/2–1	+2.5		P12	24	2–79	With Powerdown, Self-Calibration	1874
AD7858	12	+5 @ 6 mA	$V_{REF}/2$	200	1/2–1	+2.5		S	24	2–81	With 8 Channel Mux & Self-Calibration	1814
AD7859	12	+5 @ 6 mA	$V_{REF}/2$	200	1/2–1	+2.5		P12	44	2–83	With 8 Channel Mux & Self-Calibration	1874
AD7892	12	+5 @ 10 mA	±10/+/5/2.5	400	1/2–1	+2.5		P12	24	2–109		1829
AD7721	12	+5 @ 80 mA	±1.25/+2.5	468	1		+2.5	P12	28	2–63	Sigma Delta/12-Bit Mode	1829
AD7891	12	+5 @ 10 mA	All	500	1		+2.5	S/P12	44	2–107	With 8 Channel Mux	1383
AD7851	14	+3 @ 10 mA	$\pm/+V_{REF}/2$	250	1–2	+4.096		S	24	2–75	Self- & System Calibration	1873
AD977	16	+5 @ 10 mA	All	200	1 1/2–3	+2.5		S	20	2–33	Self-Calibration	1958
AD976	16	+5 @ 10 mA	All	200	1 1/2–3	+2.5		P8/16	28	2–31	Self-Calibration	1953
AD7721	16	+5 @ 80 mA	±1.25/+2.5	312	1		+2.5	P12	28	2–63	Sigma Delta/16-Bit Mode	1829

†Only covers A/Ds < 1 MSPS

Model	# Bits	# Ch	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C ± Bits	Voltage Reference–Volts Int	Ext	I/O	# Pins	Page No.	Comments	Fax-code
AD8401	8	4	+5 @ 13 mA	+3	500	1	+1.25		P8	28	*	Three-State Output, 18-Bit D/A	1417
AD7824	8	4	+5 @ 20 mA	2.5	1000	1		+5	P8	24	2–73	Three-State Output	1359
AD7828	8	8	+5 @ 20 mA	2.5	1000	1		+5	P8	28	2–73	Three-State Output	1359
AD7858L	12	8	+3 @ 5.5 mA	$V_{REF}/2$	100	1/2–1	+2.5		S	24	2–81	With Powerdown, Self-Calibration	1814
AD7859L	12	8	+3 @ 5.5 mA	$V_{REF}/2$	100	1/2–1	+2.5		P12	44	2–83	With Powerdown, Self-Calibration, Three State	1874
AD7890	12	8	+5 @ 10 mA	±10/+4/2.5	100	1		+2.5	S	24	2–105	With Powerdown	1382
AD7858	12	8	+5 @ 6 mA	$V_{REF}/2$	200	1/2–1	+2.5		S	24	2–81	With Powerdown, Self-Calibration	1814
AD7859	12	8	+5 @ 6 mA	$V_{REF}/2$	200	1/2–1	+2.5		P12	44	2–83	With Powerdown, Self-Calibration, Three State	1874
AD7891	12	8	+5 @ 10 mA	All	500	1		+2.5	S/P12	44	2–107	With Powerdown	1383

CCD Signal Processor

Model	# Bits	# Ch	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C ± Bits	Voltage Reference–Volts Int	Ext	I/O	# Pins	Page No.	Comments	Fax-code
AD9807	12	3	+5 @ 100 mA	+4	6000	1	+2		P12	64	2–151	With PGA, Digital Gain & Offset Correction, Triple CDS	2021

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

A/D Converters & Data Acquisition Subsystems–Selection Guides

Subsystems: Self-Calibrating

Multichannel

Model	# Bits	# Ch	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Pins	Page No.	Comments	Fax-code
AD7858L	12	8	+3 @ 5.5 mA	$V_{REF}/2$	100	1/2–1	+2.5		S	24	2–81	With Powerdown, Self-Calibration	1814
AD7859L	12	8	+3 @ 5.5 mA	$V_{REF}/2$	100	1/2–1	+2.5		P12	44	2–83	With Powerdown, Self-Calibration, Three State	1874
AD7858	12	8	+5 @ 6 mA	$V_{REF}/2$	200	1/2–1	+2.5		S	24	2–81	With Powerdown, Self-Calibration	1814
AD7859	12	8	+5 @ 6 mA	$V_{REF}/2$	200	1/2–1	+2.5		P12	44	2–83	With Powerdown, Self-Calibration, Three State	1874

Single Channel

Model	# Bits	# Ch	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Pins	Page No.	Comments	Fax-code
AD7853L	12	1	+3 @ 1.3 mA	$\pm/+V_{REF}/2$	100	1/2–1	+2.5		S	24	2–77	With Powerdown, Self-Calibration	1814
AD7854L	12	1	+3 @ 1.6 mA	$\pm/+V_{REF}/2$	100	1/2–1	+2.5		P12	24	2–79	With Powerdown, Three State	1874
AD7853	12	1	+5 @ 5.5 mA	$\pm/+V_{REF}/2$	200	1/2–1	+2.5		P8/12	24	2–77	With Powerdown, Self-Calibration	1814
AD7854	12	1	+5 @ 5.5 mA	$\pm/+V_{REF}/2$	200	1/2–1	+2.5		P12	24	2–79	With Powerdown, Three State	1874
AD1876	16	1	±12 @ 12 mA	–12	100			+5	S	16	2–43	Specified for AC Performance Only	1073
AD676	16	1	±12 @ 12 mA	±10	100	1 1/2		+5	P16	24	2–15		1227
AD677	16	1	±12 @ 12 mA	±10	100	1 1/2			S	16	2–17		1228
AD7882	16	1	±5 @ 13 mA	±2.5	200	2	+2.5		P14	44	2–99	Self- & System Cal, With Powerdown	1832
AD1382	16	1	±/15 @ 65 mA, +5 @ 160	±5/10	500	4	+10		P16	DH48	2–35	Self-Calibration, Zero Only	1055
AD1385	16	1	±/15 @ 75 mA, +5 @ 160	±5/10	500	4	+10		P16	DH48	2–37	Self-Calibration, Zero + Linearity	1056

Subsystems: Multiple T/H

Model	# Bits	# CH	# TH	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Conversion Rate kSPS	Linearity +25°C	Voltage Reference Int–Volts	I/O	# Pins	Page No.	Comments	Fax-code
AD7774	8	2	2	±/5 @ 5 mA	±2.5	277	1	+1.2	P8	28	*	2 PGAs, 3 8-Bit, 1 11-Bit D/A	1349
AD7777	10	4	2	+5 @ 10 mA	$V_{BIAS} - V_{SWING}$	380	1	+2	P10	24	2–69	I_Q = 1 mA with CMOS Levels	1351
AD7778	10	8	2	+5 @ 10 mA	$V_{BIAS} - V_{SWING}$	380	1	+2	P10	24	2–69	I_Q = 1 mA with CMOS Levels	1351
AD7861	11	7	4	+5 @ 10 mA	+2.5	200	2	+2.5	P12	44	2–85	4 × 12 Output Register	1962
ADMC200	11	4	4	+5 @ 20 mA	+5	100	±2	+2.5	P11	44	15–17	12-Bit Three Phase Center Based PWM Timer with PRGM Deadtime & Pulse Deletion. 2.5–25 kHz PWM Range, 12-Bit Vector Transformation	1960
ADMC201	11	7	4	+5 @ 20 mA	+5	100	±2	+2.5	P11	44	15–17	12-Bit Three Phase Center Based PWM Timer with PRGM Deadtime & Pulse Deletion. 2.5–25 kHz PWM Range, 12-Bit Vector Transformation, 6-Bit Configurable Digital I/O with Change of State Interrupt Support	1961
AD7874	12	4	4	±/5 @ 18 mA	±10	30	1/2–1	+3	P12	28	2–95	4 × 12 Output Register	1374

Analog I/O Ports

Model	# Bits	Power Supply Requirements $+V_{CC}$ Volts	Input Voltage Range Volts	Sample Rate kSPS	Linearity +25°C ± Bits	Voltage Reference Int–Volts	I/O	# Pins	Page No.	Comments	Fax-code
AD7569	8	±/5 @ 13/4 mA	±2.5	500	1/2–1	+1.2	P8	24	2–45	With 1, 8-Bit D/A	1315
AD7669	8	±/5 @ 18/6 mA	±2.5	500	1	+1.2	P8	28	2–45	With 2, 8-Bit D/A	1315
AD7769	8	+12 @ 20 mA +5 @ 5 mA	V_{BIAS}– V_{SWING}	400	1	Ext	P8	28	2–67	With 2, 8-Bit D/A	1347
AD7774	8	±/5 @ 5 mA	±2.5	277	1	+1.2	P8	28	*	2 PGAs, 2 T/H, 3 8-Bit , 1 11-Bit D/A	1349
AD7868	12	±/5 @ 12/27 mA	±3	83	1	+3	S	24	2–87	With 1, 12-Bit D/A	1368
AD7869	14	±/5 @ 22/12 mA	±3	83	1–2	+3	S	24	2–89	With 1, 14-Bit D/A	1369

*Product not recommended for new designs; for complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

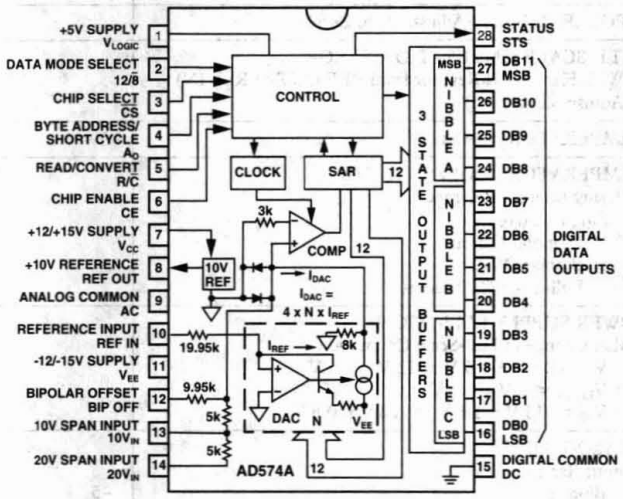
Complete 12-Bit A/D Converter

AD574A*

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- 8- and 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
  - 0°C to +70°C – AD574AJ, K, L
  - –55°C to +125°C – AD574AS, T, U
- No Missing Codes Over Temperature
- 35 μs Maximum Conversion Time
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10 ppm/°C max AD574AL
  12.5 ppm/°C max AD574AU
- Ceramic DIP, Plastic DIP or PLCC Package
- Available in Higher Speed, Pinout-Compatible Versions (15 μs AD674B, 80 μs AD774B; 10 μs (with SHA) AD1674)
- Available in Versions Compliant with MIL-STD-883 and JAN QPL

BLOCK DIAGRAM AND PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8- or 16-bit microprocessor bus. A high precision voltage reference and clock are included on-chip, and the circuit guarantees full-rated performance without external circuitry or clock signals.

The AD574A design is implemented using Analog Devices' Bipolar/I^2L process, and integrates all analog and digital functions on one chip. Offset, linearity and scaling errors are minimized by active laser-trimming of thin-film resistors at the wafer stage. The voltage reference uses an implanted buried Zener for low noise and low drift. On the digital side, I^2L logic is used for the successive-approximation register, control circuitry and 3-state output buffers.

The AD574A is available in six different grades. The AD574AJ, K, and L grades are specified for operation over the 0°C to +70°C temperature range. The AD574AS, T, and U are specified for the –55°C to +125°C range. All grades are available in a 28-pin hermetically-sealed ceramic DIP. Also, the J, K, and L grades are available in a 28-pin plastic DIP and PLCC, and the J and K grades are available in ceramic LCC.

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413; RE 28,633.

The S, T, and U grades in ceramic DIP or LCC are available with optional processing to MIL-STD-883C Class B; the T and U grades are available as JAN QPL. The Analog Devices' Military Products Databook should be consulted for details on /883B testing of the AD574A.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most 8- or 16-bit microprocessors. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 volts to +10 volts and 0 volts to +20 volts unipolar, –5 volts to +5 volts and –10 volts to +10 volts bipolar. Typical bipolar offset and full-scale calibration errors of ±0.1% can be trimmed to zero with one external component each.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max (T_{MIN} to T_{MAX})	Resolution No Missing Codes (T_{MIN} to T_{MAX})	Max Full Scale T.C. (ppm/°C)
AD574AJ(X)	0°C to +70°C	±1 LSB	11 Bits	50.0
AD574AK(X)	0°C to +70°C	±1/2 LSB	12 Bits	27.0
AD574AL(X)	0°C to +70°C	±1/2 LSB	12 Bits	10.0
AD574AS(X)[2]	–55°C to +125°C	±1 LSB	11 Bits	50.0
AD574AT(X)[2]	–55°C to +125°C	±1 LSB	12 Bits	25.0
AD574AU(X)[2]	–55°C to +125°C	±1 LSB	12 Bits	12.5

NOTES
[1]X = Package designator. Available packages are: D (D-28) for all grades. E (E-28A) for J and K grades and /883B processed S, T and U grades. N (N-28) for J, K, and L grades. P (P-28A) for PLCC in J, K grades. Example: AD574AKN is K grade in plastic DIP.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to Analog Devices Military Products Databook.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD574A–SPECIFICATIONS (@ +25°C with V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, V_{EE} = –15 V or –12 V unless otherwise noted)

Model	AD574AJ Min	AD574AJ Typ	AD574AJ Max	AD574AK Min	AD574AK Typ	AD574AK Max	AD574AL Min	AD574AL Typ	AD574AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR @ +25°C			±1			±1/2			±1/2	LSB
T_{MIN} to T_{MAX}			±1			±1/2			±1/2	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum Resolution for Which No Missing Codes are Guaranteed) T_{MIN} to T_{MAX}	11			12			12			Bits
UNIPOLAR OFFSET (Adjustable to Zero)			±2			±1			±1	LSB
BIPOLAR OFFSET (Adjustable to Zero)			±4			±4			±2	LSB
FULL-SCALE CALIBRATION ERROR (With Fixed 50 Ω Resistor from REF OUT to REF IN) (Adjustable to Zero)			0.25			0.25			0.125	% of FS
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using Internal Reference) T_{MIN} to T_{MAX}										
Unipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Bipolar Offset			±2 (10)			±1 (5)			±1 (5)	LSB (ppm/°C)
Full-Scale Calibration			±9 (50)			±5 (27)			±2 (10)	LSB (ppm/°C)
POWER SUPPLY REJECTION Max Change in Full-Scale Calibration										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	–5		+5	–5		+5	–5		+5	Volts
	–10		+10	–10		+10	–10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20	0		+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
DIGITAL CHARACTERISTICS[1] (T_{MIN}–T_{MAX})										
Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)										
Logic "1" Voltage	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	Volts
Logic "0" Voltage	–0.5		+0.8	–0.5		+0.8	–0.5		+0.8	Volts
Current	–20		+20	–20		+20	–20		+20	μA
Capacitance		5			5			5		pF
Output (DB11–DB0, STS)										
Logic "1" Voltage (I_{SOURCE} ≤ 500 μA)	+2.4			+2.4			+2.4			Volts
Logic "0" Voltage (I_{SINK} ≤ 1.6 mA)			+0.4			+0.4			+0.4	Volts
Leakage (DB11–DB0, High-Z State)	–20		+20	–20		+20	–20		+20	μA
Capacitance		5			5			5		pF
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	–11.4		–16.5	–11.4		–16.5	–11.4		–16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.98	10.0	10.02	9.98	10.0	10.02	9.99	10.0	10.01	Volts
Output Current (Available for External Loads)[3] (External Load Should not Change During Conversion)			1.5			1.5			1.5	mA
PACKAGE OPTIONS[4]										
Ceramic (D-28)		AD574ASD			AD574AKD			AD574ALD		
Plastic (N-28)		AD574AJN			AD574AKN			AD574ALN		
PLCC (P-28A)		AD574AJP			AD574AKP					
LCC (E-28A)		AD574AJE			AD574AKE					

NOTES

[1]Detailed Timing Specifications appear in the Timing Section.

[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard wired to V_{LOGIC} or Digital Common.

[3]The reference should be buffered for operation on ±12 V supplies.

[4]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

Specifications subject to change without notice.

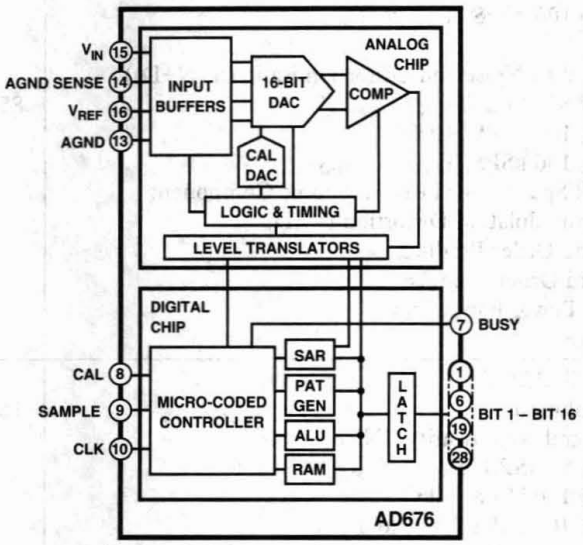
ANALOG DEVICES

16-Bit 100 kSPS Sampling ADC

AD676

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Parallel Output Format
16 Bits No Missing Codes
±1 LSB INL
–97 dB THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD676 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

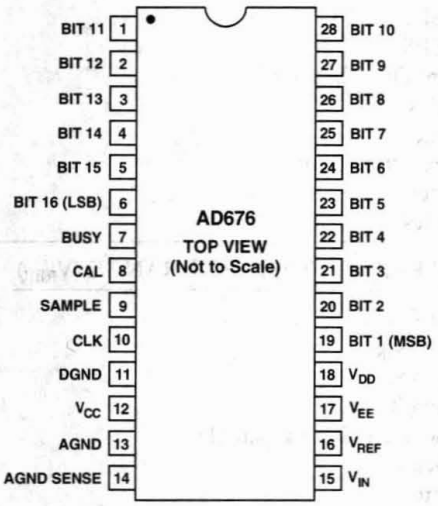
The AD676 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD676 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD676 operates from +5 V and ±12 V supplies and typically consumes 360 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD676 is available in a 28-pin plastic DIP or 28-pin side-brazed ceramic package. A serial-output version, the AD677, is available in a 16-pin 300 mil wide ceramic or plastic package.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range[1]	S/(N+D)	Max INL	Package Description	Package Option[2]
AD676JD	0°C to +70°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676KD	0°C to +70°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28
AD676AD	–40°C to +85°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676BD	–40°C to +85°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the AD676/883 data sheet.
[2]D = Ceramic DIP. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD676–SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
Total Harmonic Distortion (THD)							
@ 83 kSPS, T_{MIN} to T_{MAX}		–96	–88		–97	–90	dB
		0.0016	0.004		0.0014	0.003	%
@ 100 kSPS, +25°C		–96			–97		dB
		0.0016			0.0014		%
@ 100 kSPS, T_{MIN} to T_{MAX}		–92			–92		dB
		0.0025			0.0025		%
Signal-to-Noise and Distortion Ratio (S/(N+D))							
@ 83 kSPS, T_{MIN} to T_{MAX}	85	89		87	90		dB
@ 100 kSPS, +25°C		89			90		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		86			86		dB
Peak Spurious or Peak Harmonic Component		–98			–98		dB
Intermodulation Distortion (IMD)							
2nd Order Products		–102			–102		dB
3rd Order Products		–98			–98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		μV rms
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			±1		LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)–No Missing Codes		16		16			Bits
Bipolar Zero Error (at Nominal Supplies)		0.005			0.005		% FSR
Gain Error (at Nominal Supplies)							
@ 83 kSPS		0.005			0.005		% FSR
@ 100 kSPS, +25°C		0.005			0.005		% FSR
@ 100 kSPS		0.01			0.01		% FSR
Temperature Drift, Bipolar Zero							% FSR
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
Temperature Drift, Gain							
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
VOLTAGE REFERENCE INPUT RANGE (V_{REF})	5		10	5		10	V
ANALOG INPUT							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		*			*		
Input Settling Time		2			2		μs
Input Capacitance During Sample			50*			50*	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
DIGITAL SPECIFICATIONS							
TTL/CMOS Compatible							
POWER SUPPLIES							
Operating Current							
I_{CC}		14.5	18		14.5	18	mA
I_{EE}		14.5	18		14.5	18	mA
I_{DD}		2	5		2	5	mA
Power Consumption		360	480		360	480	mW

Specifications subject to change without notice.

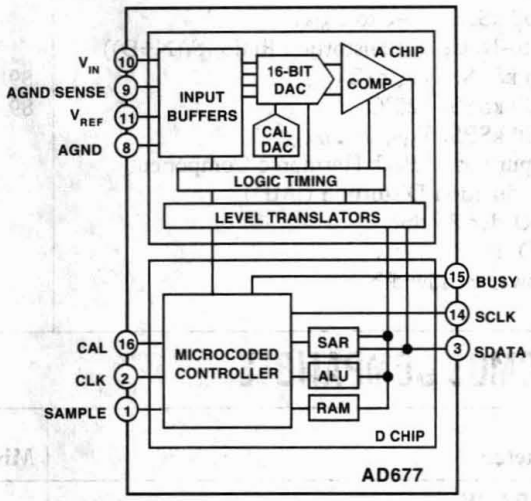
ANALOG DEVICES

16-Bit 100 kSPS Sampling ADC

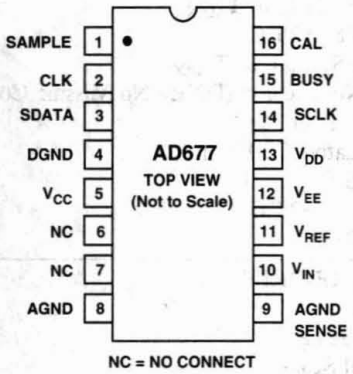
AD677

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Serial Output
16 Bits No Missing Codes
±1 LSB INL
–99 dB THD
92 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD677 is a multipurpose 16-bit serial output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD677 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD677 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD677 operates from +5 V and ±12 V supplies and typically consumes 450 mW using a 10 V reference (360 mW with 5 V reference) during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided to remotely sense the ground potential of the signal source. This can be useful if the signal has to be carried some distance to the A/D converter. Separate analog and digital grounds are also provided.

The AD677 is available in a 16-pin narrow plastic DIP, 16-pin narrow side-brazed ceramic package, or 28-lead SOIC. A parallel output version, the AD676, is available in a 28-pin ceramic or plastic DIP. All models operate over a commercial temperature range of 0°C to +70°C or an industrial range of –40°C to +85°C.

ORDERING GUIDE

Model	Temperature Range	S/(N+D)	Max INL	Package Description	Package Option*
AD677JN	0°C to +70°C	89 dB	Typ Only	Plastic 16-Pin DIP	N-16
AD677KN	0°C to +70°C	90 dB	±1.5 LSB	Plastic 16-Pin DIP	N-16
AD677JD	0°C to +70°C	89 dB	Typ Only	Ceramic 16-Pin DIP	D-16
AD677KD	0°C to +70°C	90 dB	±1.5 LSB	Ceramic 16-Pin DIP	D-16
AD677JR	0°C to +70°C	89 dB	Typ Only	Plastic 28-Lead SOIC	R-28
AD677KR	0°C to +70°C	90 dB	±1.5 LSB	Plastic 28-Lead SOIC	R-28
AD677AD	–40°C to +85°C	89 dB	Typ Only	Ceramic 16-Pin DIP	D-16
AD677BD	–40°C to +85°C	90 dB	±1.5 LSB	Ceramic 16-Pin DIP	D-16

*D = Ceramic DIP; N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

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AD677–SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter	AD677J/A Min	AD677J/A Typ	AD677J/A Max	AD677K/B Min	AD677K/B Typ	AD677K/B Max	Units
Total Harmonic Distortion (THD)							
@ 83 kSPS, T_{MIN} to T_{MAX}		–97	–92		–99	–95	dB
@ 100 kSPS, +25°C		–97	–92		–99	–95	dB
@ 100 kSPS, T_{MIN} to T_{MAX}		–93			–95		dB
Signal-to-Noise and Distortion Ratio (S/(N+D))							
@ 83 kSPS, T_{MIN} to T_{MAX}	89	91		90	92		dB
@ 100 kSPS, +25°C	89	91		90	92		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		89			90		dB
Peak Spurious or Peak Harmonic Component		–101			–101		dB
Intermodulation Distortion (IMD)							
2nd Order Products		–102			–102		dB
3rd Order Products		–98			–98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		μV rms

TTL/CMOS COMPATIBLE

Parameter	AD677J/A Min	AD677J/A Typ	AD677J/A Max	AD677K/B Min	AD677K/B Typ	AD677K/B Max	Units
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			+1	±1.5	LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)–No Missing Codes		16		16			Bits
Bipolar Zero Error		±2	±4		±1	±3	LSB
Positive, Negative FS Errors							
@ 83 kSPS		±2	±4		±1	±3	LSB
@ 100 kSPS, +25°C		±2	±4		±1	±3	LSB
@ 100 kSPS		±4			±4		LSB
TEMPERATURE DRIFT							
Bipolar Zero		±0.5			±0.5		LSB
Postive Full Scale		±0.5			±0.5		LSB
Negative Full Scale		±0.5			±0.5		LSB
VOLTAGE REFERENCE INPUT RANGE (V_{REF})	5		10	5		10	V
ANALOG INPUT							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		*			*		
Input Settling Time		2			2		μs
Input Capacitance During Sample			50*			50*	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER CONSUMPTION							
V_{REF} = 5 V		360	480		360	480	mW
V_{REF} = 10 V		450	630		450	630	mW

Specifications subject to change without notice.

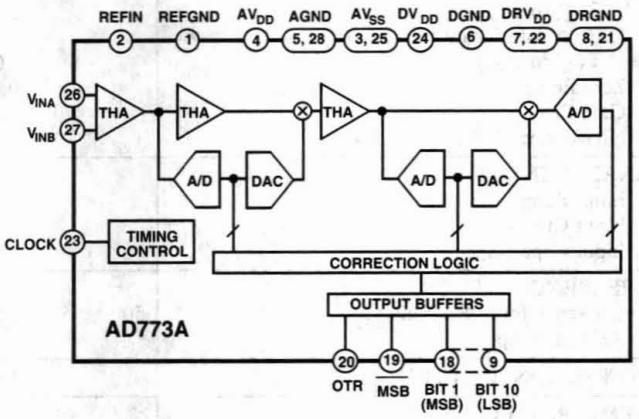
10-Bit, 20 MSPS Monolithic A/D Converter

AD773A

FEATURES

- Monolithic 10-Bit, 20 MSPS A/D Converter
- Signal-to-Noise Plus Distortion Ratio
  - f_{IN} = 1 MHz: 51 dB
- Guaranteed No Missing Codes
- On-Chip Track-and-Hold Amplifier
- 100 MHz Full Power Bandwidth
- High Impedance Reference Input
- Out of Range Output
- Twos Complement and Binary Output Data
- Available in Commercial and Military Temperature Ranges (See Military/Aerospace Reference Manual for Specifications)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD773A is a monolithic 10-bit, 20 Msps analog-to-digital converter incorporating an on-board, high performance track-and-hold amplifier (THA). The AD773A converts video bandwidth signals without the use of an external THA. The AD773A implements a multistage differential pipelined architecture with output error correction logic. The AD773A offers accurate performance and guarantees no missing codes over the full operating temperature range.

Output data is presented in binary and twos complement format. An out of range (OTR) signal indicates the analog input voltage is beyond the specified input range. OTR can be decoded with the MSB/$\overline{\text{MSB}}$ pins to signal an underflow or overflow condition. The high impedance reference input allows multiple AD773As to be driven in parallel from a single reference.

The combined dc precision and dynamic performance of the AD773A is useful in a variety of applications. Typical applications include: video enhancement, HDTV, ghost cancellation, ultrasound imaging, radar and high speed data acquisition.

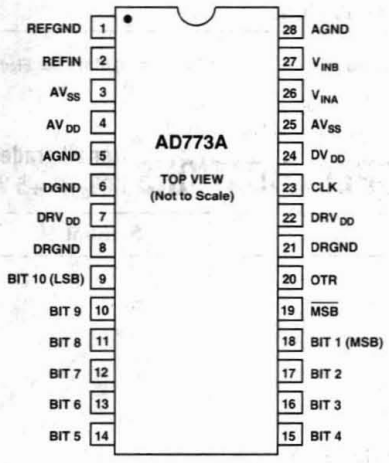
The AD773A was designed using Analog Devices' ABCMOS-1 process which utilizes high speed bipolar and 2-micron CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits. Laser trimmed thin film resistors are used to optimize accuracy and temperature stability.

The AD773A is packaged in a 28-pin ceramic DIP and is available in military (–55°C to +125°C) grade.

PRODUCT HIGHLIGHTS

1. On-board THA
   The high impedance differential input THA eliminates the need for external buffering or sample and hold amplifiers. The THA offers the choice of differential or single-ended inputs. Input current is typically 5 μA.
2. High Impedance Reference Input
   The high impedance reference input (200 kΩ) allows direct connection with standard +2.5 V references, such as the AD680, AD580 and REF43.
3. Output Data Flexibility
   Output data is available in bipolar offset and bipolar twos complement binary format.
4. Out of Range (OTR)
   The OTR output bit indicates when the input signal is beyond the AD773A's input range.
5. Military Temperature Range

PIN CONFIGURATION



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AD773A–SPECIFICATIONS

DC SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = –5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise noted)

Parameter	AD773AJ Min	AD773AJ Typ	AD773AJ Max	AD773AK Min	AD773AK Typ	AD773AK Max	Units
RESOLUTION	10			10			Bits
DC ACCURACY							
Integral Nonlinearity							LSB
T_{MIN} to T_{MAX}		±0.75			±0.75	±2	LSB
Differential Linearity Error							LSB
T_{MIN} to T_{MAX}		±0.75			±0.75	±1	LSB
Zero Error		0.5			0.5	3.5	% FSR
Gain Error		0.5			0.5	3.0	% FSR
No Missing Codes					GUARANTEED		
ANALOG INPUT							
Input Range		1			1		V p-p
Input Current		5	20		5	20	µA
Input Capacitance			10			10	pF
REFERENCE INPUT							
Reference Input Resistance	50	200		50	200		kΩ
Reference Input		2.5			2.5		Volts
POWER CONSUMPTION[2]		1.0	1.2		1.0	1.2	W
TEMPERATURE RANGE							
Specified (J/K)	0		+70	0		+70	°C

NOTES
[1]C_L = 15 pF.
[2]100% production tested.
Specifications subject to change without notice. See Definition of Specifications for additional information.

AC SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = –5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise noted, f_{SAMPLE} = 20 MSPS, f_{IN} amplitude = –0.5 dB)

Parameter	AD773AJ Min	AD773AJ Typ	AD773AJ Max	AD773AK Min	AD773AK Typ	AD773AK Max	Units
DYNAMIC PERFORMANCE[1]							
Signal-to-Noise plus Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz	52	56		54	56		dB
f_{IN} = 10 MHz	50	54		51	54		dB
Effective Number of Bits (ENOB)							
f_{IN} = 1 MHz		9.0			9.0		Bits
f_{IN} = 10 MHz		8.7			8.7		Bits
Total Harmonic Distortion (THD)							
f_{IN} = 1 MHz		–67	–57		–67	–59	dB
f_{IN} = 10 MHz		–65	–54		–65	–55	dB
Spurious Free Dynamic Range[2]		70			70		dB
Full Power Bandwidth		100			100		MHz
Intermodulation Distortion (IMD)[3]							
Second Order Products		–69			–69		dB
Third Order Products		–64			–64		dB

NOTES
[1]For typical dynamic performance curves at f_{SAMPLE} = 20 MSPS see Figures 2 through 7.
[2]f_{IN} = 1 MHz.
[3]fa = 1.0 MHz, fb = 1.05 MHz.
Specifications subject to change without notice.

TIMING SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX} with AV_{DD} = +5 V ± 5%, AV_{SS} = –5 V ± 5%, DV_{DD} = +5 V ± 5%, DRV_{DD} = +5 V ± 5%, V_{REF} = +2.500 V unless otherwise noted, f_{SAMPLE} = 20 MSPS)

	Symbol	Min	Typ	Max	Units
Conversion Rate				20	Msps
Clock Period	t_{CLK}	50			ns
Clock High	t_{CH}	24.5			ns
Clock Low	t_{CL}	24.5			ns
Output Delay	t_{OD}		20		ns
Aperture Delay			7		ns
Aperture Jitter			9		ps
Pipeline Delay (Latency)				4	Clock Cycles

Specifications subject to change without notice.

8-Bit 20 MSPS, 60 mW Sampling A/D Converter

AD775

FEATURES

CMOS 8-Bit 20 MSPS Sampling A/D Converter
Low Power Dissipation: 60 mW
+5 V Single Supply Operation
Differential Nonlinearity: 0.3 LSB
Differential Gain: 1%
Differential Phase: 0.5 Degrees
Three-State Outputs
On-Chip Reference Bias Resistors
Adjustable Reference Input
Video Industry Standard Pinout
Small Packages:
24-Pin, 300 Mil SOIC Surface Mount
24-Pin, 400 Mil Plastic DIP

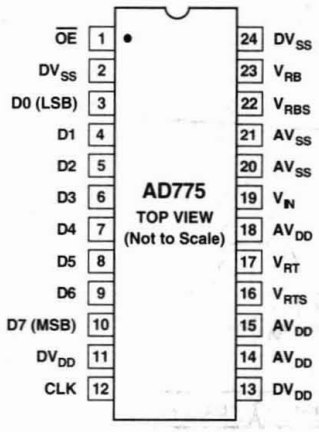
PRODUCT DESCRIPTION

The AD775 is a CMOS, low power, 8-bit, 20 MSPS sampling analog-to-digital converter (ADC). The AD775 features a built-in sampling function and on-chip reference bias resistors to provide a complete 8-bit ADC solution. The AD775 utilizes a pipelined/ping pong two-step flash architecture to provide high sampling rates (up to 35 MHz) while maintaining very low power consumption (60 mW).

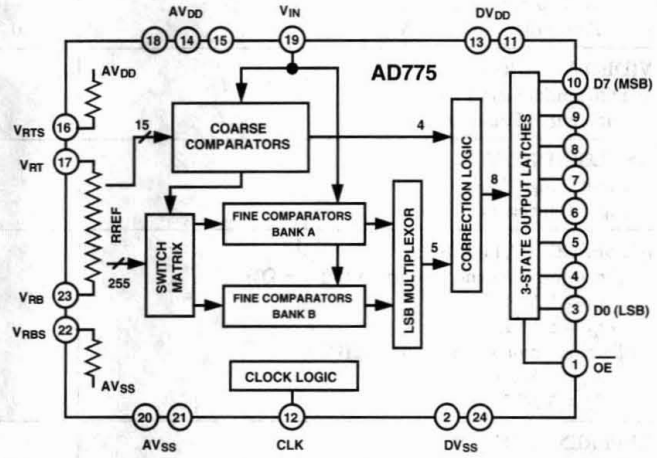
Its combination of excellent DNL, fast sampling rate, low differential gain and phase errors, extremely low power dissipation, and single +5 V supply operation make it ideally suited for a variety of video and image acquisition applications, including portable equipment. The AD775's reference ladder may be connected in a variety of configurations to accommodate different input ranges. The low input capacitance (11 pF typical) provides an easy-to-drive input load compared to conventional flash converters.

The AD775 is offered in both 300 mil SOIC and 400 mil DIP plastic packages, and is designed to operate over an extended commercial temperature range (–20°C to +75°C).

PIN CONFIGURATION (DIP and SOIC)



FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

Low Power: The AD775 has a typical supply current of 12 mA, for a power consumption of 60 mW. Reference ladder current is also low: 6.6 mA typical, minimizing the reference power consumption.

Complete Solution: The AD775's switched capacitor design features an inherent sample/hold function: no external SHA is required. On-chip reference bias resistors are included to allow a supply-based reference to be generated without any external resistors.

Excellent Differential Nonlinearity: The AD775 features a typical DNL of 0.3 LSBs, with a maximum limit of 0.5 LSBs. No missing codes is guaranteed.

Single +5 V Supply Operation: The AD775 is designed to operate on a single +5 V supply, and the reference ladder may be configured to accommodate analog inputs inclusive of ground.

Low Input Capacitance: The 11 pF input capacitance of the AD775 can significantly decrease the cost and complexity of input driving circuitry, compared with conventional 8-bit flash ADCs.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD775JN	–20°C to +75°C	24-Pin 400 Mil Plastic DIP	N-24B
AD775JR	–20°C to +75°C	24-Pin 300 Mil SOIC	R-24A

*For outline information see Package Information section.

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AD775–SPECIFICATIONS

(T_A = +25°C with AV_{DD}, DV_{DD} = +5 V, AV_{SS}, DV_{SS} = 0 V, V_{RT} = 2.6 V, V_{RB} = +0.6 V, CLOCK = 20 MHz unless otherwise noted)

Parameter	AD775J Min	Typ	Max	Units
RESOLUTION	8			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		+0.5	1.3	LSB
Differential Nonlinearity (DNL)		±0.3	±0.5	LSB
No Missing Codes		GUARANTEED		
Offset				
To Top of Ladder V_{RT}	–10	–35	–60	mV
To Bottom of Ladder V_{RB}	0	+15	+45	mV
VIDEO ACCURACY				
Differential Gain Error		1.0		%
Differential Phase Error		0.5		Degrees
ANALOG INPUT				
Input Range (V_{RT}–V_{RB})		2.0		V p-p
Input Capacitance		11		pF
AC SPECIFICATIONS				
Signal-to-Noise and Distortion (S/(N + D))				
f_{IN} = 1 MHz		47		dB
f_{IN} = 5 MHz		41		dB
Total Harmonic Distortion (THD)				
f_{IN} = 1 MHz		–51		dB
f_{IN} = 5 MHz		–42		dB
REFERENCE INPUT				
Reference Input Resistance (R_{REF})	230	300	450	Ω
Case 1: V_{RT} = V_{RTS}, V_{RB} = V_{RBS}				
Reference Bottom Voltage (V_{RB})	0.60	0.64	0.68	V
Reference Span (V_{RT}–V_{RB})	1.96	2.09	2.21	V
Reference Ladder Current (I_{REF})	4.4	7.0	9.6	mA
Case 2: V_{RT} = V_{RTS}, V_{RB} = AV_{SS}				
Reference Span (V_{RT}–V_{RB})	2.25	2.39	2.53	V
Reference Ladder Current (I_{REF})	5	8	11	mA
POWER CONSUMPTION		60	85	mW
TEMPERATURE RANGE				
Operating	–20		+75	°C

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate		20	35		MHz
Clock Period	t_C	50			ns
Clock High	t_{CH}	25			ns
Clock Low	t_{CL}	25			ns
Output Delay	t_{OD}		18	30	ns
Pipeline Delay (Latency)				2.5	Clock Cycles
Sampling Delay	t_{DS}		4		ns
Aperture Jitter			30		ps

Specifications subject to change without notice.

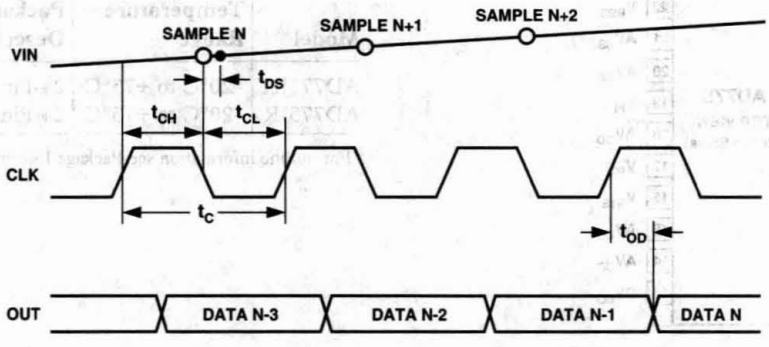


Figure 1. AD775 Timing Diagram

ANALOG DEVICES

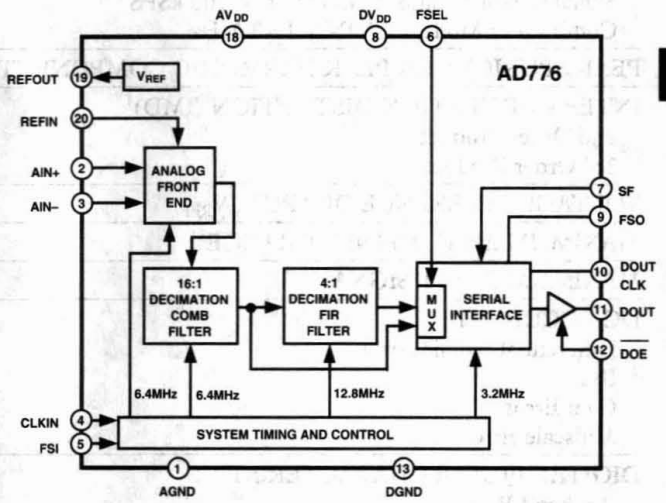
16-Bit 100 kSPS Oversampling ADC

AD776

FEATURES
Monolithic 16-Bit Sigma-Delta ADC
Third-Order Noise Shaping
96 dB Dynamic Range
90 dB SNR
16-Bit 100 kHz Output from FIR Filter
12-Bit 400 kHz Output from Comb Filter
No Missing Codes
<0.001 dB In-Band Ripple

APPLICATIONS
Digital Audio Disk/Tape
Voice Bandwidth Communications
ADC Support for ADSP-21xx
High Accuracy Measurement Systems

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD776 is a 16-bit sigma-delta oversampled ADC, incorporating a 1-bit third-order modulator and digital decimation filter. An on-chip voltage reference circuit is also included.

The AD776 does not generally require the use of sample-hold circuits or complex antialiasing filters as a result of its sigma-delta architecture. The output is available both before and after the final Finite Impulse Response (FIR) decimation filter. This provides the flexibility of optimizing conversion speed or dynamic range: 12-bit/400 kHz (from the comb filter) or 16-bit/100 kHz (from the FIR filter). The serial port provides easy interface with a variety of standard processors including the ADSP-21xx.

The AD776 is specified for ac (or "dynamic") parameters such as SNR, THD and IMD which are important in signal processing and audio applications. Third order noise shaping is employed using 64 times oversampling to provide 90 dB SNR and –100 dB peak spurious component for signal bandwidths up to 45 kHz.

The AD776 operates from a single +5 V supply and typically consumes 350 mW during conversion. The device is packaged in 20-pin ceramic DIP (cerdip) and is offered in an industrial temperature grade (–40°C to +85°C).

PRODUCT HIGHLIGHTS

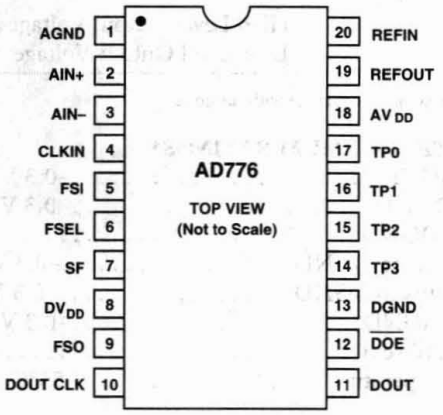
1. Analog Front End. The analog input is differential providing increased signal swing, increased power supply rejection ratio, and reduced sensitivity to clock jitter. Since the input signal is oversampled by a factor of 64, a complex antialiasing filter is not needed.
2. Flexible Digital Interface. The AD776 has three output pins for the serial interface: 1) serial data out (DOUT), 2) frame sync out (FSO), and 3) serial clock out (DOUT CLOCK). The serial port can interface with general purpose DSPs such as the ADSP-21xx, TMS320xx, and DSP56001/2 without additional "glue" logic.
3. Inherently Self-Sampling. The AD776 needs no external sample-and-hold amplifier to capture and freeze the analog input while the conversion takes place.
4. Speed/Performance Options. In addition to the standard 16-bit resolution at 100 kHz, the output of the comb filter can be accessed to provide 12-bit resolution at 400 kHz.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD776AQ	–40°C to +85°C	20-Pin Cerdip	Q-20

*For outline information see Package Information section.

PIN CONFIGURATION



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AD776–SPECIFICATIONS (T_{MIN} to T_{MAX}; AV_{DD}, DV_{DD} = +5 V, FIR filter output mode unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
TEMPERATURE RANGE	–40		+85	°C
TOTAL HARMONIC DISTORTION (THD)[1, 2, 3]	–80	–83		dB
	0.01	0.003		%
SIGNAL-TO-NOISE RATIO (SNR)[1, 2], f_S = 48 kSPS	88	90		dB
Signal to Noise Ratio (SNR)[1, 2], f_S = 100 kSPS		86		dB
Comb Filter Mode, CLKIN = 12.8 MHz		72		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		–100		dB
INTERMODULATION DISTORTION (IMD)[4]				
2nd Order Products		–102		dB
3rd Order Products		–98		dB
VOLTAGE REFERENCE OUTPUT (V_{REF})	(AV_{DD} × 0.4) – 4%	AV_{DD} × 0.4 V	(AV_{DD} × 0.4) + 4%	V
MAXIMUM ANALOG INPUT RANGE[5]		2 × V_{REF} – 0.5		V p-p
MAXIMUM INPUT SIGNAL[6]		±0.5 V_{REF}		V p-p
DC ACCURACY[1]				
Differential Nonlinearity		±0.5		LSB
INL		2		LSB
Gain Error		1.0		%
Midscale Error		0.5		%
DIGITAL FILTER CHARACTERISTICS				
Passband Ripple		0.001		dB
Stopband Attenuation		–96		dB
POWER SUPPLY REQUIREMENTS[7]				
Analog Supply Voltage (AV_{DD})	4.5	5.0	5.5	V
Digital Supply Voltage (DV_{DD})	4.5		AV_{DD}	V
Analog Supply Current		20		mA
Digital Supply Current		20		mA
Power Consumption[8]		300	400	mW
Power Supply Rejection[9]		70		dB

DIGITAL SPECIFICATIONS

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		–0.5		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{DD}		1		µA
I_{IL}	Low Level Input Current	V_{IL} = 0 V		1		µA
C_{IN}	Input Capacitance			10		pF
I_Z	Hi-Z Input Current for SDO				10	µA
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.4 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.0 mA			0.5	V

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

AV_{DD} to AGND ..... –0.3 V to +7.0 V
DV_{DD} to DGND ..... –0.3 V to +7.0 V
AGND to DGND ..... ±0.3 V
Digital Inputs to DGND ..... –0.3 V to DV_{DD}
Analog Inputs to AGND ..... –0.3 V to AV_{DD}
REFIN to AGND ..... –0.3 V to +2.5 V
Soldering (10 sec) ..... +300°C
Storage Temperature ..... –55°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

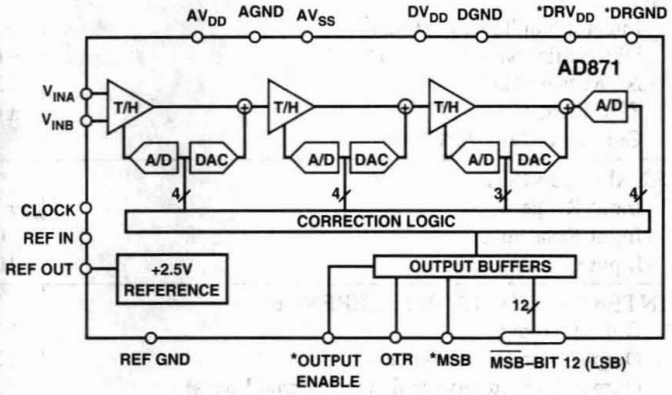
Complete 12-Bit 5 MSPS Monolithic A/D Converter

AD871

FEATURES

- Monolithic 12-Bit 5 MSPS A/D Converter
- Low Noise: 0.17 LSB RMS Referred to Input
- No Missing Codes Guaranteed
- Differential Nonlinearity Error: 0.5 LSB
- Signal-to-Noise and Distortion Ratio: 68 dB
- Spurious-Free Dynamic Range: 73 dB
- Power Dissipation: 1.03 W
- Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
- Pin Compatible with the AD872
- Twos Complement Binary Output Data
- Out of Range Indicator
- 28-Pin Ceramic DIP or 44-Pin Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



*ONLY AVAILABLE ON 44-PIN SURFACE MOUNT PACKAGE.

PRODUCT DESCRIPTION

The AD871 is a monolithic 12-bit, 5 MSPS analog to digital converter with an on-chip, high performance track-and-hold amplifier and voltage reference. The AD871 uses a multistage differential pipelined architecture with error correction logic to provide 12-bit accuracy at 5 MSPS data rates and guarantees no missing codes over the full operating temperature range. The AD871 is a redesigned variation of the AD872A 12-bit, 10 MSPS ADC, optimized for lower noise in applications requiring sampling rates of 5 MSPS or less. The AD871 is pin compatible with the AD872A, allowing the parts to be used interchangeably as system requirements change.

The low-noise input track-and-hold (T/H) of the AD871 is ideally suited for high-end imaging applications. In addition, the T/H's high input impedance and fast settling characteristics allow the AD871 to easily interface with multiplexed systems that switch multiple signals through a single A/D converter. The dynamic performance of the input T/H also renders the AD871 suitable for sampling single channel inputs at frequencies up to and beyond the Nyquist rate. The AD871 provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in twos complement binary output format. An out-of-range signal indicates an overflow condition, and can be used with the most significant bit to determine low or high overflow.

The AD871 is fabricated on Analog Devices ABCMOS-1 process which utilizes high speed bipolar and CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits.

The AD871 is packaged in a 28-pin ceramic DIP and a 44-pin leadless ceramic surface mount package and is specified for operation from 0°C to +70°C and –55°C to +125°C.

PRODUCT HIGHLIGHTS

The AD871 offers a complete single-chip sampling 12-bit, 5 MSPS analog-to-digital conversion function in a 28-pin DIP or 44-pin leadless ceramic surface mount package (LCC).

Low Noise—The AD871 features 0.17 LSB referred-to-input noise, producing essentially a "1 code wide" histogram for a code-centered dc input.

Low Power—The AD871 at 1.03 W consumes a fraction of the power of presently available hybrids.

On-Chip Track-and-Hold (T/H)—The low noise, high impedance T/H input eliminates the need for external buffers and can be configured for single ended or differential inputs.

Ease of Use—The AD871 is complete with T/H and voltage reference and is pin-compatible with the AD872A (12-bit, 10 MSPS monolithic ADC).

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD871's input range.

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AD871–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 5 MHz, unless otherwise noted)

Parameter	J Grade[1]	S Grade[1]	Units
RESOLUTION	12	12	Bits min
MAX CONVERSION RATE	5	5	MHz min
INPUT REFERRED NOISE	0.17	0.17	LSB rms typ
ACCURACY			
Integral Nonlinearity (INL)	±1.5	±1.5	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	12	12	Bits Guaranteed
Zero Error (@ +25°C)[2]	±0.75	±0.75	% FSR max
Gain Error (@ +25°C)[2]	±1.25	±1.25	% FSR max
ANALOG INPUT			
Input Range	±1	±1	Volts max
Input Resistance	50	50	kΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	Volts typ
Output Voltage Tolerance	±20	±40	mV max
Output Current (Available for External Loads) (External load should not change during conversion.)	2.0	2.0	mA typ
REFERENCE INPUT RESISTANCE	5	5	kΩ typ
POWER CONSUMPTION	1.03 1.25	1.03 1.3	W typ W max

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 5 MSPS, unless otherwise noted)[1]

	J Grade	S Grade	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)			
f_{INPUT} = 750 kHz	68	68	dB typ
f_{INPUT} = 1 MHz	66	66	dB typ
	63	62	dB min
f_{INPUT} = 2.49 MHz	60	60	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 750 kHz	–72	–72	dB typ
f_{INPUT} = 1 MHz	–69	–69	dB typ
	–64	–63	dB max
f_{INPUT} = 2.49 MHz	–62	–62	dB typ
SPURIOUS FREE DYNAMIC RANGE (SFDR)			
f_{INPUT} = 750 kHz	73	73	dB typ
f_{INPUT} = 1 MHz	70	70	dB typ
f_{INPUT} = 2.49 MHz	62	62	dB typ
INTERMODULATION DISTORTION (IMD)[2]			
Second Order Products	–80	–80	dB typ
Third Order Products	–73	–73	dB typ
FULL POWER BANDWIDTH	15	15	MHz typ
SMALL SIGNAL BANDWIDTH	15	15	MHz typ
APERTURE DELAY	6	6	ns typ
APERTURE JITTER	16	16	ps rms typ
ACQUISITION TO FULL-SCALE STEP	80	80	ns typ
OVERVOLTAGE RECOVERY TIME	80	80	ns typ

Specifications subject to change without notice.

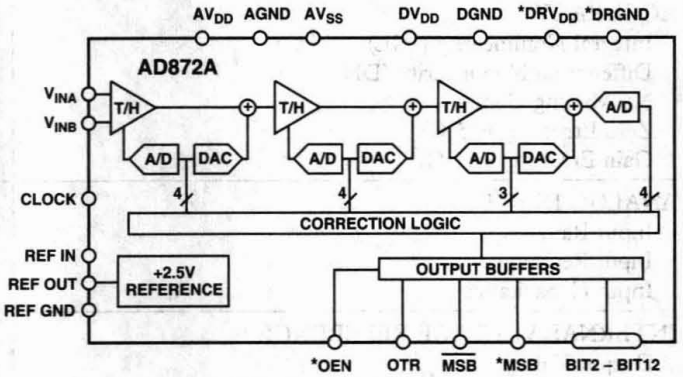
Complete 12-Bit 10 MSPS Monolithic A/D Converter

AD872A

FEATURES

- Monolithic 12-Bit 10 MSPS A/D Converter
- Low Noise: 0.26 LSB RMS Referred-to-Input
- No Missing Codes Guaranteed
- Differential Nonlinearity Error: 0.5 LSB
- Signal-to-Noise and Distortion Ratio: 68 dB
- Spurious-Free Dynamic Range: 75 dB
- Power Dissipation: 1.03 W
- Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
- Twos Complement Binary Output Data
- Out-of-Range Indicator
- 28-Pin Ceramic DIP or 44-Pin Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



*ONLY AVAILABLE ON 44-PIN SURFACE MOUNT PACKAGE

PRODUCT DESCRIPTION

The AD872A is a monolithic 12-bit, 10 MSPS analog-to-digital converter with an on-chip, high performance track-and-hold amplifier and voltage reference. The AD872A uses a multistage differential pipelined architecture with error correction logic to provide 12-bit accuracy at 10 MSPS data rates and guarantees no missing codes over the full operating temperature range. The AD872A is a redesigned version of the the AD872 which has been optimized for lower noise. The AD872A is pin compatible with the AD872, allowing the parts to be used interchangeably as system requirements change.

The low noise input track-and-hold (T/H) of the AD872A is ideally suited for high-end imaging applications. In addition, the T/H's high input impedance and fast settling characteristics allow the AD872A to easily interface with multiplexed systems that switch multiple signals through a single A/D converter. The dynamic performance of the T/H also renders the AD872A suitable for sampling single channel inputs at frequencies up to and beyond the Nyquist rate. The AD872A provides both reference output and reference input pins, allowing the on-board reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in twos complement binary output format. An out-of-range signal indicates an overflow condition, and can be used with the most significant bit to determine low or high overflow.

The AD872A is fabricated on Analog Devices' ABCMOS-1 process that utilizes high speed bipolar and CMOS transistors on a single chip.

The AD872A is packaged in a 28-pin ceramic DIP and a 44-pin leadless ceramic surface mount package (LCC). Operation is specified from 0°C to +70°C and –55°C to +125°C.

PRODUCT HIGHLIGHTS

The AD872A offers a complete single-chip sampling, 12-bit 10 MSPS analog-to-digital conversion function in a 28-pin DIP or 44-pin LCC.

Low Noise—The AD872A features 0.26 LSB rms referred to-input noise.

Low Power—The AD872A at 1.03 W consumes a fraction of the power of presently available hybrids.

On-Chip Track-and-Hold (T/H)—The low noise, high impedance T/H input eliminates the need for external buffers and can be configured for single-ended or differential inputs.

Ease of Use—The AD872A is complete with T/H and voltage reference and is pin-compatible with the AD872.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD872A's input range.

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD872AJD	0°C to +70°C	D-28
AD872AJE	0°C to +70°C	E-44A
AD872ASD[2]	–55°C to +125°C	D-28
AD872ASE[2]	–55°C to +125°C	E-44A

NOTES
[1]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.
[2]MIL-STD-883 version will be available; contact factory.

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AD872A–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AV_{DD} = + 5 V, DV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 10 MHz unless otherwise noted)

Parameter	J Grade[1]	S Grade[1]	Units
RESOLUTION	12	12	Bits min
MAX CONVERSION RATE	10	10	MHz min
INPUT REFERRED NOISE	0.26	0.26	LSB rms typ
ACCURACY			
Integral Nonlinearity (INL)	±1.75	±1.75	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	12	12	Bits Guaranteed
Zero Error (@ +25°C)[2]	±0.75	±0.75	% FSR max
Gain Error (@ +25°C)[2]	±1.25	±1.25	% FSR max
ANALOG INPUT			
Input Range	±1.0	±1.0	V max
Input Resistance	50	50	kΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	V typ
Output Voltage Tolerance	±20	±40	mV max
Output Current (Available for External Loads) (External Load Should Not Change During Conversion)	2.0	2.0	mA typ
REFERENCE INPUT RESISTANCE	5	5	kΩ
POWER CONSUMPTION	1.03 1.25	1.03 1.3	W typ W max

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, AV_{DD} = + 5 V, DV_{DD} = +5 V, AV_{SS} = –5 V, f_{SAMPLE} = 10 MHz unless otherwise noted)[1]

Parameter	J Grade	S Grade	Units
SIGNAL-TO-NOISE & DISTORTION RATIO (S/N+D)			
f_{INPUT} = 1 MHz	68	68	dB typ
	61	61	dB min
f_{INPUT} = 4.99 MHz	66	66	dB typ
SIGNAL-TO-NOISE RATIO (SNR)			
f_{INPUT} = 1 MHz	69	69	dB typ
f_{INPUT} = 4.99 MHz	67	67	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 1 MHz	–74	–74	dB typ
	–63	–62	dB max
f_{INPUT} = 4.99 MHz	–72	–72	dB typ
SPURIOUS-FREE DYNAMIC RANGE (SFDR)			
f_{INPUT} = 1 MHz	75	75	dB typ
f_{INPUT} = 4.99 MHz	74	74	dB typ
INTERMODULATION DISTORTION (IMD)[2]			
Second Order Products	–80	–80	dB typ
Third Order Products	–73	–73	dB typ
FULL POWER BANDWIDTH	35	35	MHz typ
SMALL SIGNAL BANDWIDTH	35	35	MHz typ
APERTURE DELAY	6	6	ns typ
APERTURE JITTER	16	16	ps rms typ
ACQUISITION TO FULL-SCALE STEP	40	40	ns typ
OVERVOLTAGE RECOVERY TIME	40	40	ns typ

Specifications subject to change without notice.

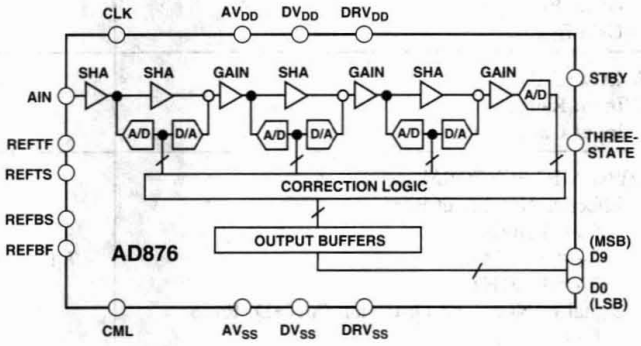
10-Bit 20 MSPS 160 mW CMOS A/D Converter

AD876

FEATURES

CMOS 10-Bit 20 MSPS Sampling A/D Converter
Pin-Compatible 8-Bit Option
Power Dissipation: 160 mW
+5 V Single Supply Operation
Differential Nonlinearity: 0.5 LSB
Guaranteed No Missing Codes
Power Down (Stand-By) Mode
Three-State Outputs
Digital I/Os Compatible with +5 V or +3.3 V Logic
Adjustable Reference Input
Small Size: 28-Pin SOIC or 48-Pin Thin Quad Flatpack (TQFP)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD876 is a CMOS, 160 mW, 10-bit, 20 MSPS analog-to-digital converter (ADC). The AD876 has an on-chip input sample-and-hold amplifier. By implementing a multistage pipelined architecture with output error correction logic, the AD876 offers accurate performance and guarantees no missing codes over the full operating temperature range. Force and sense connections to the reference inputs minimize external voltage drops.

The AD876 can be placed into a stand-by mode of operation reducing the power below 50 mW. The AD876's digital I/O interfaces to either +5 V or +3.3 V logic. Digital output pins can be placed in a high impedance state; the format of the output is straight binary coding.

The AD876's speed, resolution and single-supply operation ideally suit a variety of applications in video, multimedia, imaging, high speed data acquisition and communications. The AD876's low power and single-supply operation satisfy requirements for high speed portable applications. Its speed and resolution ideally suit charge coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras and camcorders.

The AD876 comes in a space saving 28-pin SOIC and 48-pin thin quad flatpack (TQFP) and is specified over the commercial (0°C to +70°C) temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description*
AD876JR	0°C to +70°C	28-Pin SOIC
AD876JST-Reel	0°C to +70°C	48-Pin TQFP (Tape and Reel 13")
AD876JR-8	0°C to +70°C	28-Pin SOIC
AD876AR	–40°C to +85°C	28-Pin SOIC
AD876AR-Reel		28-Pin SOIC
AD876JRS	0°C to +70°C	28-Pin SSOP

*For outline information see Package Information section.

PRODUCT HIGHLIGHTS

Low Power

The AD876 at 160 mW consumes a fraction of the power of presently available 8- or 10-bit, video speed converters. Power-down mode and single-supply operation further enhance its desirability in low power, battery operated applications such as electronic still cameras, camcorders and communication systems.

Very Small Package

The AD876 comes in both a 28-pin SOIC and 48-pin surface mount, thin quad flat package. The TQFP package is ideal for very tight, low headroom designs.

Digital I/O Functionality

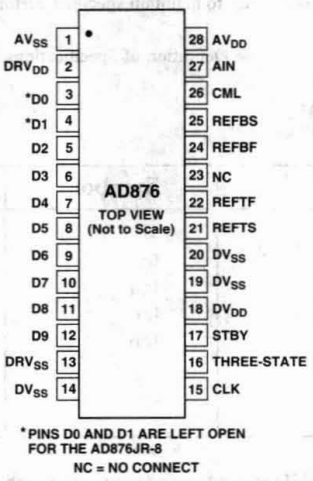
The AD876 offers three-state output control.

Pin Compatible Upgrade Path

The AD876 offers the option of laying out designs for eight bits and migrating to 10-bit resolution if prototype results warrant.

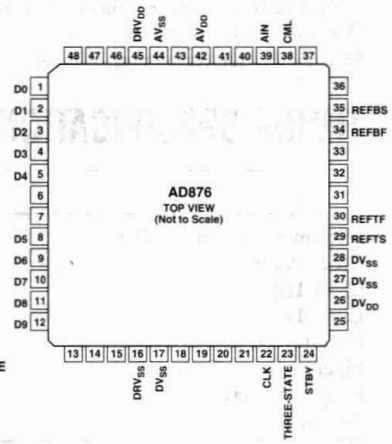
PIN CONFIGURATIONS

SOIC



*PINS D0 AND D1 ARE LEFT OPEN FOR THE AD876JR-8
NC = NO CONNECT

TQFP



AD876–SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFB} = +4.0 V, V_{REFB} = +2.0 V, f_{CLOCK} = 20 MSPS, unless otherwise noted)

Parameter	AD876JR-8 Min	AD876JR-8 Typ	AD876JR-8 Max	AD876 Min	AD876 Typ	AD876 Max	Units
RESOLUTION		8			10		Bits
DC ACCURACY							
Integral Nonlinearity (INL)		±0.3	±1.0		±1.0		LSB
Differential Nonlinearity (DNL)		±0.1	±0.75		±0.5	±1	LSB
No Missing Codes		GUARANTEED			GUARANTEED		
Offset Error		0.1			0.4		% FSR
Gain Error		0.1			0.2		% FSR
ANALOG INPUT							
Input Range		2			2		V p-p
Input Capacitance		5.0			5.0		pF
DYNAMIC PERFORMANCE							
Effective Number of Bits							
f_{IN} = 1 MHz		7.8			9.0		Bits
f_{IN} = 3.58 MHz	7.4	7.8		8.2	9.0		Bits
f_{IN} = 10 MHz		7.5			8.2		Bits
Signal-to-Noise and Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz		49			56		dB
f_{IN} = 3.58 MHz	46	49		51	56		dB
f_{IN} = 10 MHz		47			51		dB
Total Harmonic Distortion (THD)							
f_{IN} =1 MHz		–62			–62		dB
f_{IN} = 3.58 MHz		–62	–56		–62	–56	dB
f_{IN} =10 MHz		–60			–60		dB
Spurious Free Dynamic Range[2]		–65			–65		dB
Full Power Bandwidth		150			150		MHz
Differential Phase		0.5			0.5		Degree
Differential Gain		1			1		%
POWER SUPPLIES							
Operating Voltage							
AV_{DD}[1]	+4.5		+5.25	+4.5		+5.25	Volts
DV_{DD}[1]	+4.5		+5.25	+4.5		+5.25	Volts
DRV_{DD}	+3.0		+5.25	+3.0		+5.25	Volts
Operating Current							
IAV_{DD}		20	25		20	25	mA
IDV_{DD}		12	16		12	16	mA
$IDRV_{DD}$		0.1	1		0.1	1	mA
POWER CONSUMPTION		160	190		160	190	mW
TEMPERATURE RANGE							
Specified	0		+70	0		+70	°C

NOTES

[1]AV_{DD} and DV_{DD} must be within 0.5 V of each other to maintain specified performance levels.

[2]3.58 MHz Input Frequency.

Specifications subject to change without notice. See Definition of Specifications for additional information.

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate[1]		20			MHz
Clock Period	t_C		50		ns
Clock High	t_{CH}	23	25		ns
Clock Low	t_{CL}	23	25		ns
Output Delay	t_{OD}	10	20		ns
Pipeline Delay (Latency)				3.5	Clock Cycles
Aperture Delay Time			4		ns
Aperture Jitter			22		ps

NOTE

[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.

Specifications subject to change without notice.

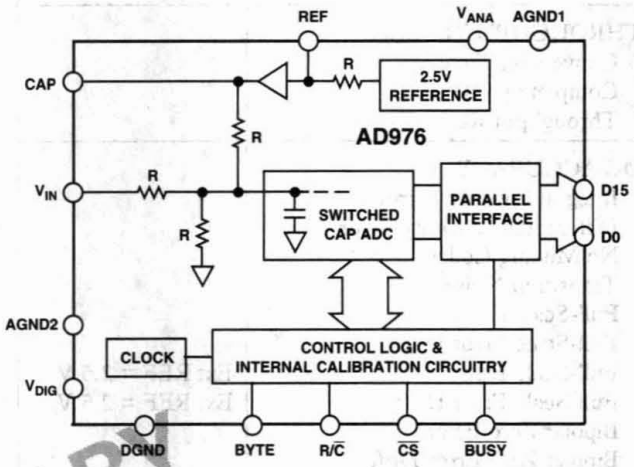
16-Bit, 200 kSPS BiCMOS A/D Converter

AD976

FEATURES

Fast 16-Bit ADC with 200 kSPS Throughput
Single 5 V Supply Operation
Input Range: ±10 V
100 mW Max Power Dissipation
Choice of External or Internal 2.5 V Reference
High Speed Parallel Interface
On-Chip Clock
28-Pin Skinny DIP, SOIC or SSOP Packages

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD976 is a high speed, low power 16-bit A/D converter that operates from a single 5 V supply. The part contains a successive approximation, switched capacitor ADC, an internal 2.5 V reference, and a high speed parallel interface. The ADC is factory calibrated to minimize all linearity errors. The analog full scale input is the standard industrial range of ±10 V.

The AD976 is comprehensively tested for ac parameters such as SNR and THD, as well as the more traditional parameters of offset, gain, and linearity.

The AD976 is fabricated on Analog Devices' BiCMOS process which has high performance bipolar devices along with CMOS transistors.

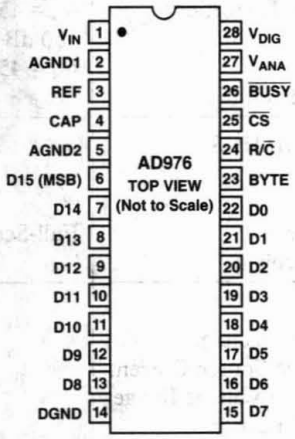
The AD976 is available in skinny 28-pin DIP, SOIC, and SSOP packages.

PRODUCT HIGHLIGHTS

1. Fast 200 kSPS Throughput.
   The AD976 is a high speed, 16-bit ADC based on aswitched capacitor architecture which is factory calibrated.
2. Single-Supply Operation.
   The AD976 operates from a single 5 V supply and dissipates only 100 mW max.
3. Comprehensive DC and AC Specifications.
   As well as the traditional specifications of offset, gain, and linearity, the AD976 is fully tested for SNR and THD.
4. Complete A/D Solution.
   The AD976 offers a highly integrated solution containing an accurate A/D, reference and on-chip clock.

PIN CONFIGURATION

DIP, SOIC and SSOP Packages



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD976–SPECIFICATIONS (T_{MIN} to T_{MAX}, F_S = 200 kHz, V_{DIG} = +5 V ± 10%, V_{ANA} = +5 V ± 5% unless otherwise noted)

Parameter	Conditions	AD976A Min	AD976A Typ	AD976A Max	AD976B Min	AD976B Typ	AD976B Max	Units
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range			±10			±10		V
Impedance			23			23		kΩ
Capacitance			35			35		pF
THROUGHPUT SPEED								
Conversion Time			3.2	3.5		3.2	3.5	µs
Complete Cycle				5			5	µs
Throughput Rate		200			200			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, –2			+1.5, –1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			1.3		LSB
Full-Scale Error[3, 4]				±0.50			±0.25	%
Full-Scale Error Drift			±7			±5		ppm/°C
Full-Scale Error	Ext REF = 2.5 V			±0.50			±0.25	%
Full-Scale Error Drift	Ext REF = 2.5 V		±2			±2		ppm/°C
Bipolar Zero Error[3]				±10			±10	mV
Bipolar Zero Error Drift			±2			±2		ppm/°C
Power Supply Sensitivity								
$V_{ANA} = V_{DIG} = V_D$	V_D = 5 V ± 5%			±8			±8	LSB
V_{DIG} = 5 V ± 10%	V_{ANA} = 5 V		TBD			TBD		LSB
AC ACCURACY								
Spurious Free Dynamic Range	f_{IN} = 45 kHz	90			96			dB[5]
Total Harmonic Distortion	f_{IN} = 45 kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 45 kHz	83			86			dB
	–60 dB Input		30			32		
Signal-to-Noise	f_{IN} = 45 kHz	83			86			dB
Full Power Bandwidth[6]			250			250		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			40		ns
Aperture Jitter			Sufficient to Meet AC Specs					
Transient Response	Full-Scale Step			2			2	µs
Over Voltage Recovery[7]			150			150		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	2.48	2.5	2.52	V
Internal Reference Source Current			1			1		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
External Reference Current Drain	Ext REF = 2.5 V			100			100	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	–0.3		+0.8	V
V_{IH}		+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	V
I_{IL}				±10			±10	µA
I_{IH}				±10			±10	µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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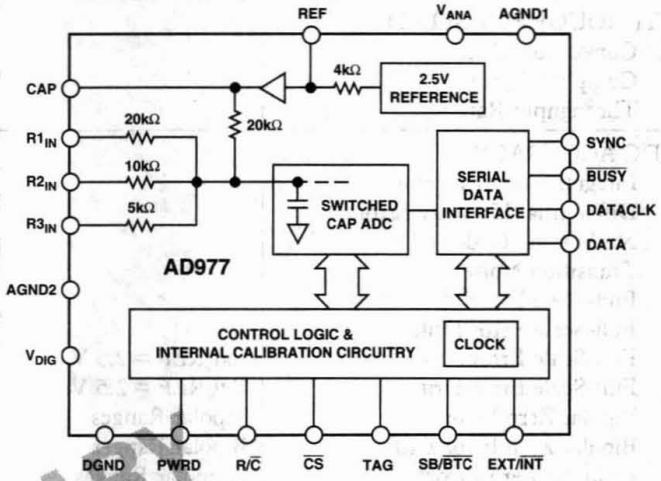
16-Bit, 200 kSPS BiCMOS A/D Converter

AD977

FEATURES

Fast 16-Bit ADC with 200 kSPS Throughput
Single 5 V Supply Operation
Power Dissipation: 100 mW max
Power Down Mode: 50 μW
Input Ranges:
Unipolar: 0–10 V, 0–5 V, and 0–4 V
Bipolar: ±10 V, ±5 V, and ±3.3 V
Choice of External or Internal 2.5 V Reference
High Speed Serial Interface
On-Chip Clock
20-Pin Skinny DIP, SOIC Packages & 28-Lead SSOP Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD977 is a high speed, low power 16-bit A/D converter that operates from a single 5 V supply. The part contains a successive approximation, switched capacitor ADC, an internal 2.5 V reference, and a high speed serial interface. The ADC is factory calibrated to minimize all linearity errors. The AD977 provides full scale bipolar input ranges of ±10 V, ±5 V, and ±3.3 V and unipolar ranges of 0 V to 10 V, 0 V to 5 V, and 0 V to 4 V.

The AD977 is comprehensively tested for ac parameters such as SNR and THD, as well as the more traditional dc parameters of offset, gain, and linearity.

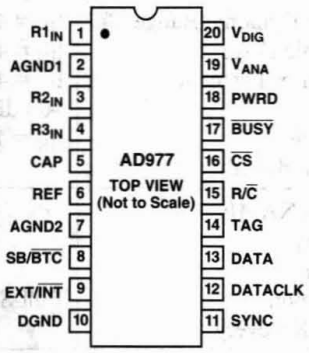
The AD977 is fabricated on Analog Devices' BiCMOS process which has high performance bipolar devices along with CMOS transistors.

The AD977 is available in skinny 20-pin DIP and SOIC packages and a 28-lead SSOP package.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION

SOIC & DIP Packages



PRODUCT HIGHLIGHTS

1. Fast 200 kSPS Throughput.
   The AD977 is a high speed, 16-bit ADC based on a switched capacitor architecture which is factory calibrated.
2. Single-Supply Operation.
   The AD977 operates from a single 5 V supply and dissipates only 100 mW max.
3. Comprehensive DC and AC Specifications.
   As well as the traditional specifications of offset, gain, and linearity, the AD977 is fully tested for SNR and THD.
4. Complete A/D Solution.
   The AD977 offers a highly integrated solution containing an accurate A/D, reference and on-chip clock.

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AD977–SPECIFICATIONS (T_{MIN} to T_{MAX}, F_S = 200 kHz, V_{DIG} = +5 V ± 10%, V_{ANA} = +5 V ± 5% unless otherwise noted)

Parameter	Conditions	AD977A Min	AD977A Typ	AD977A Max	AD977B Min	AD977B Typ	AD977B Max	Units
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range			±10 V, 0 V to 5 V, (See Table I)					
Impedance			See Table I					
Capacitance			35			35		pF
THROUGHPUT SPEED								
Conversion Time			3.2	3.5		3.2	3.5	µs
Complete Cycle				5			5	µs
Throughput Rate		200			200			kHz
DC ACCURACY								
Integral Linearity Error				±3			±1.5	LSB[1]
Differential Linearity Error				+3, –2			+1.5, –1	LSB
No Missing Codes		15			16			Bits
Transition Noise			1.3			1.3		LSB
Full-Scale Error[3, 4]				±0.50			±0.25	%
Full-Scale Error Drift			±7			±5		ppm/°C
Full-Scale Error	Ext REF = 2.5 V			±0.50			±0.25	%
Full-Scale Error Drift	Ext REF = 2.5 V		±2			±2		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10			±10	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2			±2		ppm/°C
Unipolar Zero Error[3]	Unipolar Ranges			±3			±3	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			±2		ppm/°C
Recovery to Rated Accuracy after Power Down	1 µF Capacitor to CAP		1			1		ms
Power Supply Sensitivity								
$V_{ANA} = V_{DIG} = V_D$	V_D = 5 V ± 5%			±8			±8	LSB
V_{DIG} = 5 V ± 10%	V_{ANA} = 5 V		TBD			TBD		LSB
AC ACCURACY								
Spurious Free Dynamic Range	f_{IN} = 45 kHz	90			96			dB[5]
Total Harmonic Distortion	f_{IN} = 45 kHz			–90			–96	dB
Signal-to-(Noise+Distortion)	f_{IN} = 45 kHz	83			86			dB
	–60 dB Input		30			32		
Signal-to-Noise	f_{IN} = 45 kHz	83			86			dB
Full Power Bandwidth[6]			250			250		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			40		ns
Aperture Jitter			Sufficient to meet ac specs.					
Transient Response	Full-Scale Step			2			2	µs
Over Voltage Recovery[7]			150			150		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	2.48	2.5	2.52	V
Internal Reference Source Current			1			1		µA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
External Reference Current Drain	Ext REF = 2.5 V			100			100	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	–0.3		+0.8	V
V_{IH}		+2.0		V_{DIG} + 0.3	+2.0		V_{DIG} + 0.3	V
I_{IL}				±10			±10	µA
I_{IH}				±10			±10	µA

Specifications subject to change without notice.

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PRELIMINARY TECHNICAL DATA

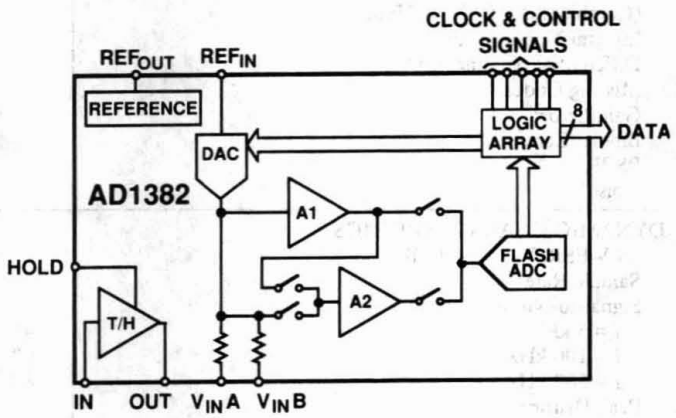
16-Bit 500 kHz Sampling ADC

AD1382

PRODUCT FEATURES
Single Package
16-Bit Resolution
500 kHz Sampling Rate
SNR 90 dB @ 100 kHz (min)
THD –88 dB @ 100 kHz (min)
0.0015% FSR INL (typ)
±5, ±10 V Bipolar Input
Zero Offset Autocalibration

APPLICATIONS
Medical Imaging
CAT
Magnetic Resonance
Vibration Analysis
Parametric Measurement Unit (ATE)
Waveform/Transient Recorders
Analytical Instruments
Sonar
Radar

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1382 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. This high resolution, high speed converter offers outstanding noise and distortion performance along with excellent INL and DNL performance, all in a single dual-in-line package.

The AD1382 guarantees outstanding noise and distortion performance for both ±5 V and ±10 V input ranges. The AD1382 architecture includes a low noise and low distortion track/hold with a three-pass digitally corrected subranging ADC. Precision thin film resistors and a new proprietary DAC provide for outstanding dynamic and static performance. Output data is multiplexed over an eight-bit CMOS/TTL compatible data bus.

The AD1382 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.8 W. Two user selectable bipolar input ranges, ±5 V and ±10 V are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1382KD	10°C to 40°C Ambient (40°C to 70°C Case)	DH-48A

*DH-48A = Hermetic Ceramic DIP. For outline information see Package Information section.

AD1382–SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = –5 V, 10 MHz External Clock, 5 Minute Warm-up, unless otherwise noted)

Parameter	AD1382KD Min	Typ	Max	Units
RESOLUTION	16			Bits
ANALOG INPUT				
Input Ranges		±5, ±10		V
Input Impedance	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS				
(Combined ADC/Track/Hold)				
Integral Nonlinearity[1]		±0.0015		% FSR[2]
Differential Nonlinearity[1]		±0.0006	±0.0015	% FSR
Missing Codes			None	
Gain Error[3]		±0.07	±0.15	% FSR
Bipolar Zero[3]		±0.03	±0.10	% FSR
PSRR		±0.006	±0.10	% FSR/V
Noise[4]		55		μV rms
DYNAMIC CHARACTERISTICS				
±5 V FSR, V_{IN} = –0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	93		dB
f = 100 kHz	90	92		dB
f = 200 kHz	88	91		dB
Peak Distortion				
f = 5 kHz	–90	–98		dB
f = 100 kHz	–88	–93		dB
f = 200 kHz	–82	–85		dB
Total Harmonic Distortion[6]				
f = 5 kHz	–90	–96		dB
f = 100 kHz	–88	–92		dB
f = 200 kHz	–82	–85		dB
DYNAMIC CHARACTERISTICS				
±10 V FSR, V_{IN} = –0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	95		dB
f = 100 kHz	90	94		dB
f = 200 kHz	88	93		dB
Peak Distortion				
f = 5 kHz	–90	–98		dB
f = 100 kHz	–80	–87		dB
f = 200 kHz	–74	–81		dB
Total Harmonic Distortion[6]				
f = 5 kHz	–90	–96		dB
f = 100 kHz	–80	–87		dB
f = 200 kHz	–74	–81		dB
DIGITAL INPUTS[9]				
Input Voltage				
V_{IL}			0.8	V
V_{IH}	2.0			V
Input Current			±200	μA
Input Capacitance		2		pF
Start Command				
Setup Time, t_{SCS}	10	3		ns
Hold Time, t_{SCH}	10	0		ns
Autozero				
Setup Time, t_{AZS}	10	0		ns
Hold Time, t_{AZH}	20	6		ns
Clock				
Frequency	2.5		10	MHz
Duty Cycle	40		60	%

Specifications subject to change without notice.

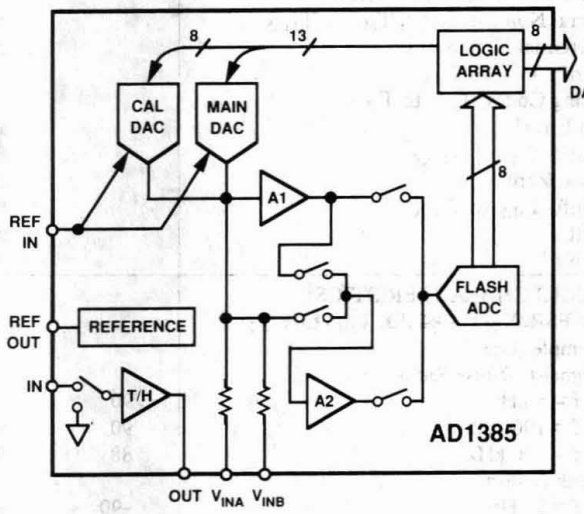
16-Bit 500 kHz Wide Temperature Range Sampling ADC

AD1385

FEATURES
- 16-Bit Resolution
- 500 kHz Sampling Rate
- Differential Linearity Autocalibration
- Specified over –55°C to +125°C Range
- SNR 90 dB @ 100 kHz (min)
- THD –88 dB @ 100 kHz (min)
- 0.0006% FSR DNL (typ)
- 0.0015% FSR INL (typ)
- No Missing Codes
- ±5, ±10 V Bipolar Input Ranges
- Zero Offset Autocalibration

APPLICATIONS
- Medical Imaging
  - CAT
  - Magnetic Resonance
- Radar
- Vibration Analysis
- Parametric Measurement Unit (ATE)
- Digital Storage Oscilloscopes
- Waveform Recorders
- Analytical Instruments

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1385 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. Its differential linearity autocalibration feature allows this high resolution, high speed converter to offer outstanding noise and distortion performance, as well as excellent INL and DNL specifications, over the full military temperature range. Autocalibration effectively eliminates DNL drift over temperature.

The AD1385 architecture includes a low noise, low distortion track/hold, a three pass digitally corrected subranging ADC, and linearity calibration circuitry. A complete linearity calibration requires only 15 ms. Precision thin-film resistors and a proprietary DAC contribute to the part's outstanding dynamic and static performance.

The AD1385 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.76 W. Two user selectable bipolar input ranges, ±5 V and ±10 V, are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

The AD1385's pinout is nearly identical to that of the AD1382, a factory calibrated 16-bit, 500 kHz SADC. Just two additional connections, to enable and monitor autocalibration, are required. This commonality provides an easy upgrade path to extend system performance and operating temperature range.

ORDERING GUIDE

Model	Temperature Range (Case)	Package Option*
AD1385KD	0°C to +70°C	DH-48A
AD1385TD	–55°C to +125°C	DH-48A
AD1385TD/883B	–55°C to +125°C	DH-48A

*DH-48A = Bottom Brazed Ceramic DIP. For outline information see Package Information section.

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AD1385–SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = –5 V, 10 MHz External Clock, unless otherwise noted)

Parameter	AD1385KD Min	AD1385KD Typ	AD1385KD Max	AD1385TD Min	AD1385TD Typ	AD1385TD Max	Units
RESOLUTION	16			16			Bits
ANALOG INPUT							
Input Ranges		±5, ±10			±5, ±10		V
Input Impedance	2.45	2.5	2.55	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS (Combined ADC/Track/Hold)							
Integral Nonlinearity[1, 2], T_{MIN} to T_{MAX}		±0.0015			±0.0015		% FSR[3]
Differential Nonlinearity[1]		±0.0006	±0.0015		±0.0006	±0.0015	% FSR
Drift, T_{MIN} to T_{MAX}		0.3			0.3		ppm/°C
Missing Codes, T_{MIN} to T_{MAX}			None			None	
Gain Error[4]		±0.05	±0.15		±0.05	±0.15	% FSR
Drift, T_{MIN} to T_{MAX}		8	15		8	15	ppm/°C
Bipolar Zero[4]		±0.05	±0.10		±0.05	±0.10	% FSR
Drift, T_{MIN} to T_{MAX}		5	15		5	15	ppm/°C
PSRR		±0.006	±0.10		±0.006	±0.10	% FSR/V
Noise		70			70		µV rms
DYNAMIC CHARACTERISTICS[2] ±5 V FSR, V_{IN} = –0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	93		90	93		dB
f = 100 kHz	90	92		90	92		dB
f = 200 kHz	88	91		88	91		dB
Peak Distortion							
f = 5 kHz	–90	–107		–90	–107		dB
f = 100 kHz	–88	–95		–88	–95		dB
f = 200 kHz	–82	–88		–82	–88		dB
Total Harmonic Distortion[6]							
f = 5 kHz	–90	–105		–90	–105		dB
f = 100 kHz	–88	–95		–88	–95		dB
f = 200 kHz	–82	–88		–82	–88		dB
DYNAMIC CHARACTERISTICS[2] ±10 V FSR, V_{IN} = –0.4 dB, T_{MIN} to T_{MAX}							
Sample Rate			500			500	kHz
Signal-to-Noise Ratio[5]							
f = 5 kHz	90	95		90	95		dB
f = 100 kHz	90	94		90	94		dB
f = 200 kHz	88	93		88	93		dB
Peak Distortion							
f = 5 kHz	–90	–108		–90	–108		dB
f = 100 kHz	–80	–87		–80	–87		dB
f = 200 kHz	–74	–82		–74	–82		dB
Total Harmonic Distortion[6]							
f = 5 kHz	–90	–105		–90	–105		dB
f = 100 kHz	–80	–87		–80	–87		dB
f = 200 kHz	–74	–82		–74	–82		dB
DIGITAL INPUTS							
Input Voltage							
V_{IL}			0.8			0.8	V
V_{IH}	2.25			2.25			V
Input Current			±200			±200	µA
Input Capacitance		2			2		pF
Clock							
Frequency		2.5–10			2.5–10		MHz
Duty Cycle		40-60			40-60		%
Aperture Delay[7]		7			7		ns
DIGITAL OUTPUTS							
Output Voltage							
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4		0.2	0.4	V
V_{OH} @ I_{OH} = –3.2 mA	2.4	4.5		2.4	4.5		V
Output Capacitance		4			4		pF
Leakage, Outputs Disabled			±200			±200	µA

Specifications subject to change without notice.

Complete 12-Bit, 3 MSPS Monolithic A/D Converter

AD1672AP

FEATURES

Single Supply
Pin Configurable Input Voltage Ranges
Power Dissipation: 240 mW
No Missing Codes Guaranteed
Differential Nonlinearity Error: 0.5 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 68 dB
Spurious-Free Dynamic Range: –77 dB
Out of Range Indicator
Binary Output Data
Digital I/Os Compatible with +5 V or +3.3 V Logic
28-Pin PLCC Package

PRODUCT DESCRIPTION

The AD1672 is a monolithic, single supply 12-bit, 3 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier (SHA) and voltage reference. The AD1672 uses a multistage pipelined architecture with output error correction logic to provide 12-bit accuracy at 3 MSPS data rates and guarantees no missing codes over the full operating temperature range. The AD1672 combines a high performance BiCMOS process and a novel architecture to achieve its high performance levels.

The fast settling input SHA is equally suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to the Nyquist rate. The AD1672's wideband input combined with the power and cost savings over previously available solutions will enable new designs in communications, imaging and medical applications. The AD1672 provides both reference output and reference input pins allowing the onboard reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. The digital output data is presented in a straight binary output format for the unipolar input ranges of 0 V to 2.5 V and 0 V to 5.0 V. For the bipolar input range of –2.5 V to +2.5 V, the digital output data is presented in an offset binary format. An out-of-range (OTR) signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The AD1672 is packaged in a 28-pin PLCC package and is specified for operation from –40°C to +85°C.

PRODUCT HIGHLIGHT

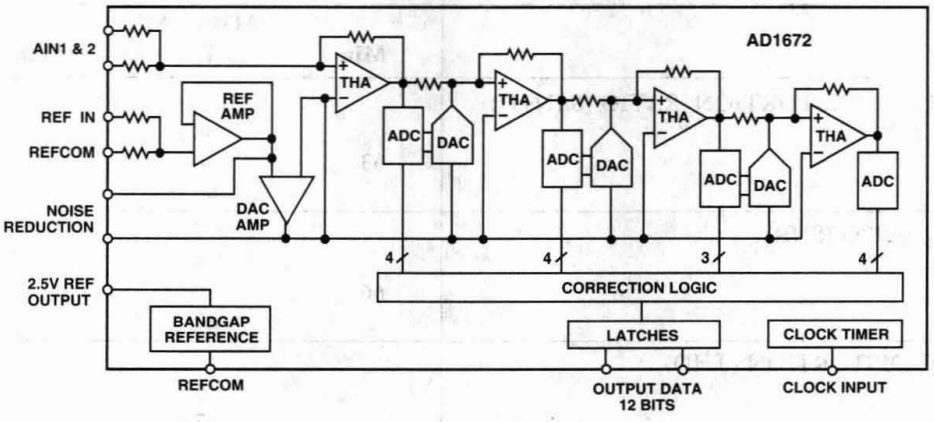
The AD1672 offers a complete single-chip sampling 12-bit, 3 MSPS analog-to-digital conversion function in a 28-pin PLCC package.

The AD1672 at 240 mW consumes a fraction of the power of presently available solutions and provides exceptional performance relative to other monolithic solutions.

OUT OF RANGE (OTR)—The OTR output bit indicates when the input signal is beyond the AD1672's input range.

Ease-of-Use—The single supply AD1672 is complete with SHA voltage reference and pin strappable input ranges. It is compatible with a wide range of amplifiers.

FUNCTIONAL BLOCK DIAGRAM



AD1672AP–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5.0 V, V_{DD} = +5.0 V, DRV_{DD} = +5.0 V, f_{SAMPLE} = 3 MHz unless otherwise noted)

Parameter	AD1672AP Min	Typ	Max	Units
RESOLUTION	12			Bits
MAX CONVERSION RATE	3			MHz
ACCURACY				
Integral Nonlinearity (INL)	–2.5	±1.0	2.5	LSB
Differential Nonlinearity (DNL)	–1.0	±0.5	1.5	LSB
No Missing Codes		12 Bits Guaranteed		
Offset Error	–0.75	±0.20	0.75	% FSR
Zero Error[1]	–0.75	±0.20	0.75	% FSR
Gain Error[2]	–1.50	±0.30	1.50	% FSR
ANALOG INPUT				
Input Ranges				
2.5 V Range Unipolar	0.0		2.5	Volts
5.0 V Range Unipolar	0.0		5.0	Volts
5.0 V Bipolar	–2.5		2.5	Volts
Input Resistance				
2.5 V Input Range	1.5	2.0	2.5	kΩ
5.0 V Input Ranges	3.0	4.0	5.0	kΩ
Input Capacitance		10		pF
INTERNAL VOLTAGE REFERENCE				
Output Voltage	2.475	2.5	2.525	Volts
Output Current[3]	0.5			mA
REFERENCE INPUT RESISTANCE	6.0	8.0	10.0	kΩ
POWER CONSUMPTION		240	363	mW
TEMPERATURE RANGE	–40	25	85	°C

NOTES
[1]Bipolar Mode.
[2]Includes internal reference error.
[3]Current available for external loads. External load should not change during conversion.
Specification subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5.0 V, V_{DD} = +5.0 V, DRV_{DD} = +5.0 V, f_{SAMPLE} = 3 MHz, AIN = 0.5 dB in bipolar –2.5 V to +2.5 V configuration unless otherwise noted)

Parameter	AD1672AP Min	Typ	Max	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/(N+D))				
f_{INPUT} = 100 kHz		68		dB
f_{INPUT} = 500 kHz	63	68		dB
f_{INPUT} = 1.5 MHz		60		dB
SIGNAL-TO-NOISE RATIO (SNR)				
f_{INPUT} = 100 kHz		70		dB
f_{INPUT} = 500 kHz	66	70		dB
f_{INPUT} = 1.5 MHz		67		dB
TOTAL HARMONIC DISTORTION (THD)				
f_{INPUT} = 100 kHz		–74		dB
f_{INPUT} = 500 kHz		–74	–64	dB
f_{INPUT} = 1.5 MHz		–60		dB
SPURIOUS FREE DYNAMIC RANGE (SFDR)				
f_{INPUT} = 100 kHz		–77		dB
f_{INPUT} = 500 kHz		–77	–65	dB
f_{INPUT} = 1.5 MHz		–61		dB

Specification subject to change without notice.

ANALOG DEVICES

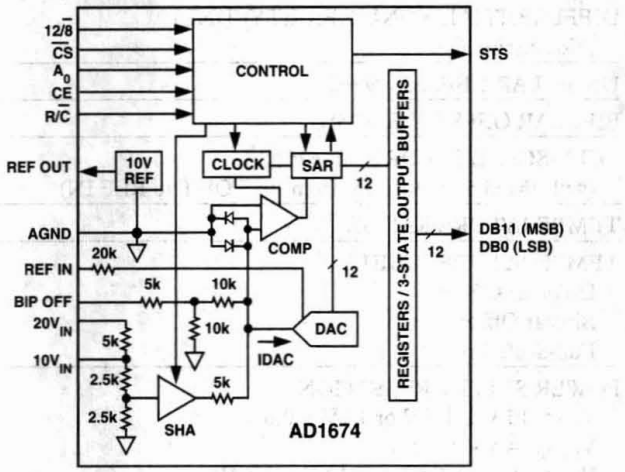
12-Bit 100 kSPS A/D Converter

AD1674*

FEATURES

Complete Monolithic 12-Bit 10 μs Sampling ADC
On-Board Sample-and-Hold Amplifier
Industry Standard Pinout
8- and 16-Bit Microprocessor Interface
AC and DC Specified and Tested
Unipolar and Bipolar Inputs
±5 V, ±10 V, 0 V–10 V, 0 V–20 V Input Ranges
Commercial, Industrial and Military Temperature Range Grades
MIL-STD-883 and SMD Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1674 is a complete, multipurpose, 12-bit analog-to-digital converter, consisting of a user-transparent onboard sample-and-hold amplifier (SHA), 10 volt reference, clock and three-state output buffers for microprocessor interface.

The AD1674 is pin compatible with the industry standard AD574A and AD674A, but includes a sampling function while delivering a faster conversion rate. The on-chip SHA has a wide input bandwidth supporting 12-bit accuracy over the full Nyquist bandwidth of the converter.

The AD1674 is fully specified for ac parameters (such as S/(N+D) ratio, THD, and IMD) and dc parameters (offset, full-scale error, etc.). With both ac and dc specifications, the AD1674 is ideal for use in signal processing and traditional dc measurement applications.

The AD1674 design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic.

Five different temperature grades are available. The AD1674J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from –40°C to +85°C; the AD1674T grade is specified from –55°C to +125°C. The J and K grades are available in both 28-lead plastic DIP and SOIC. The A and B grade devices are available in 28-lead hermetically sealed ceramic DIP and 28-lead SOIC. The T grade is available in 28-lead hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD1674 utilizes the pinout established by the industry standard AD574A and AD674A.
2. Integrated SHA: The AD1674 has an integrated SHA which supports the full Nyquist bandwidth of the converter. The SHA function is transparent to the user; no wait-states are needed for SHA acquisition.
3. DC and AC Specified: In addition to traditional dc specifications, the AD1674 is also fully specified for frequency domain ac parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth. These parameters can be tested and guaranteed as a result of the onboard SHA.

***Protected by U. S. Patent Nos. 4,962,325; 4,250,445; 4,808,908; RE30586.**

ORDERING GUIDE

Model[1]	Temperature Range	INL (T_{MIN} to T_{MAX})	S/(N+D) (T_{MIN} to T_{MAX})	Package Description	Package Option[2]
AD1674JN	0°C to +70°C	±1 LSB	69 dB	Plastic DIP	N-28
AD1674KN	0°C to +70°C	±1/2 LSB	70 dB	Plastic DIP	N-28
AD1674JR	0°C to +70°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674KR	0°C to +70°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AR	–40°C to +85°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674BR	–40°C to +85°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AD	–40°C to +85°C	±1 LSB	69 dB	Ceramic DIP	D-28
AD1674BD	–40°C to +85°C	±1/2 LSB	70 dB	Ceramic DIP	D-28
AD1674TD	–55°C to +125°C	±1 LSB	70 dB	Ceramic DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD1674/883B data sheet. SMD is also available.
[2]N = Plastic DIP; D = Hermetic Ceramic DIP; R = Plastic SOIC. For outline information see Package Information section.

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AD1674–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5% unless otherwise noted)

Parameter	AD1674J Min	AD1674J Typ	AD1674J Max	AD1674K Min	AD1674K Typ	AD1674K Max	Unit
RESOLUTION	12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2	LSB
DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes)	12			12			Bits
UNIPOLAR OFFSET[1] @ +25°C			±3			±2	LSB
BIPOLAR OFFSET[1] @ +25°C			±6			±4	LSB
FULL-SCALE ERROR[1, 2] @ +25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.25	% of FSR
TEMPERATURE RANGE	0		+70	0		+70	°C
TEMPERATURE DRIFT[3]							
Unipolar Offset[2]			±2			±1	LSB
Bipolar Offset[2]			±2			±1	LSB
Full-Scale Error[2]			±6			±3	LSB
POWER SUPPLY REJECTION							
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	–5		+5	–5		+5	Volts
	–10		+10	–10		+10	Volts
Unipolar	0		+10	0		+10	Volts
	0		+20	0		+20	Volts
Input Impedance							
10 Volt Span	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	kΩ
POWER SUPPLIES							
Operating Voltages							
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	–16.5		–11.4	–16.5		–11.4	Volts
Operating Current							
I_{LOGIC}		5	8		5	8	mA
I_{CC}		10	14		10	14	mA
I_{EE}		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4] (External Load Should Not Change During Conversion			2.0			2.0	mA

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from 25°C value to the value at T_{MIN} or T_{MAX}.
[4]Reference should be buffered for ±12 V operation.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ANALOG DEVICES

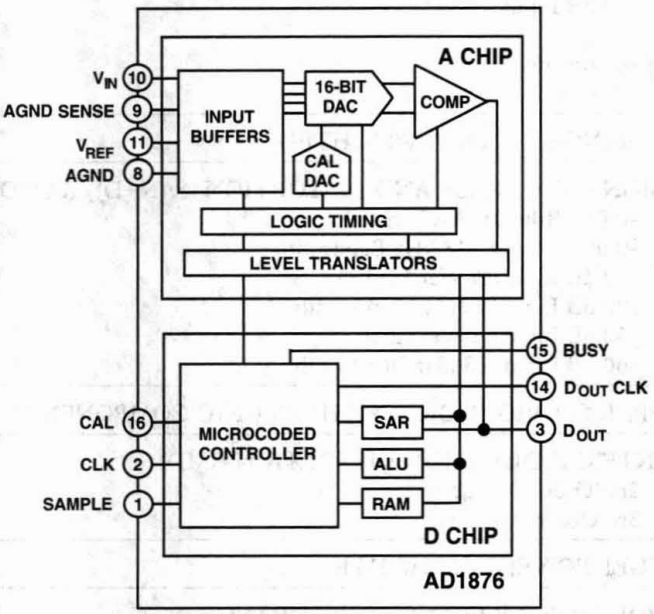
16-Bit 100 kSPS Sampling ADC

AD1876

FEATURES

Autocalibrating
0.002% THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth
On-Chip Sample & Hold Function
2× Oversampling for Audio Applications
16-Pin DIP Package
Serial Twos Complement Output Format
Low Input Capacitance–typ 50 pF
AGND Sense for Improved Noise Immunity

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

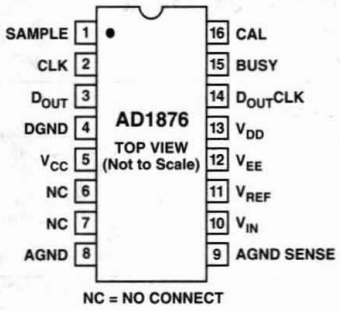
The AD1876 is a 16-bit serial output sampling A/D converter which uses a switched capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The circuitry of the AD1876 is partitioned onto two monolithic chips, a digital control chip fabricated with Analog Devices' DSP CMOS process and an analog ADC chip fabricated with the BiMOS II process. Both chips are contained in a single package.

The serial output interface requires an external clock and sample command signal. The output data rate may be as high as 2.08 MHz, and is controlled by the external clock. The twos complement format of the output data is MSB first and is directly compatible with the NPC SM5805 digital decimation filter used in consumer audio products. The AD1876 is also compatible with a variety of DSP processors.

The AD1876 is packaged in a space saving 16-pin plastic DIP and operates from +5 V and ±12 V supplies; typical power consumption is 235 mW. The digital supply (V_{DD}) is isolated from the linear supplies (V_{EE} and V_{CC}) for reduced digital crosstalk. Separate analog and digital grounds are also provided.

PIN CONFIGURATION



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	THD dB	Package Description	Package Option*
AD1876JN	0°C to +70°C	–95	Plastic 16-Pin DIP	N-16

*N = Narrow Plastic DIP. For outline information see Package Information section.

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AD1876–SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter	AD1876J Min	Typ	Max	Units
TEMPERATURE RANGE	0		70	°C
TOTAL HARMONIC DISTORTION (THD)				
–0.05 dB Input		–95	**–88**	dB
		0.002	**0.004**	%
–20 dB Input		–78		dB
		0.01		%
–60 dB Input		–40		dB
		1.0		%
D-RANGE, –60 dB, A-WEIGHTED		92		dB
SIGNAL-TO-NOISE AND DISTORTION (S/(N+D)) RATIO				
–0.05 dB Input, A-Weighted		92		dB
–0.05 dB Input, 48 kHz Bandwidth	**83**	90		dB
–20 dB Input, A-Weighted		73		dB
–20 dB Input, 48 kHz Bandwidth		70		dB
–60 dB Input, A-Weighted		34		dB
–60 dB Input, 48 kHz Bandwidth		31		dB
PEAK SPURIOUS OR PEAK HARMONIC COMPONENT		–99	**–89**	dB
INTERMODULATION DISTORTION (IMD)				
2nd Order Products		–102		dB
3rd Order Products		–98		dB
FULL POWER BANDWIDTH		1		MHz
VOLTAGE REFERENCE INPUT RANGE (V_{REF})	3	**5**	10.0	V
ANALOG INPUT				
Input Range (V_{IN})			±V_{REF}	V
Input Impedance		*		
Input Capacitance During Sample		50*		pF
Aperture Delay		6		ns
Aperture Jitter		100		ps
POWER SUPPLIES				
Operating Current				
I_{CC}		9	12	mA
I_{EE}		9	12	mA
I_{DD}		3	12	mA
Power Consumption		235	350	mW

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		**2.4**			V
V_{IL}	Low Level Input Voltage		–0.3		**0.8**	V
I_{IH}	High Level Input Current	V_{IH} = V_{DD}	**–10**		**+10**	µA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	**–10**		**+10**	µA
C_{IN}	Input Capacitance				10	pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} – 1 V			V
		I_{OH} = 0.5 mA	**2.4**			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			**0.4**	V

Specifications subject to change without notice.

ANALOG DEVICES

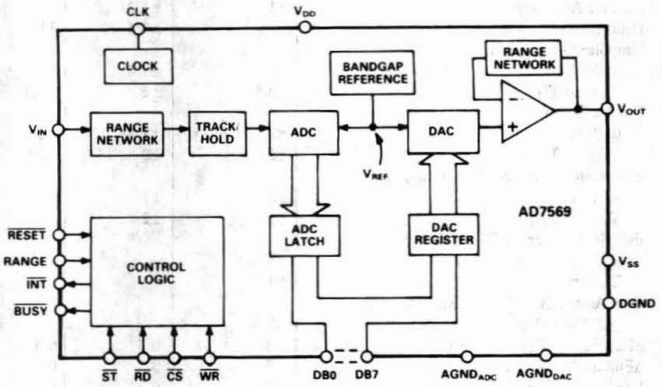
LC²MOS Complete, 8-Bit Analog I/O Systems

AD7569/AD7669

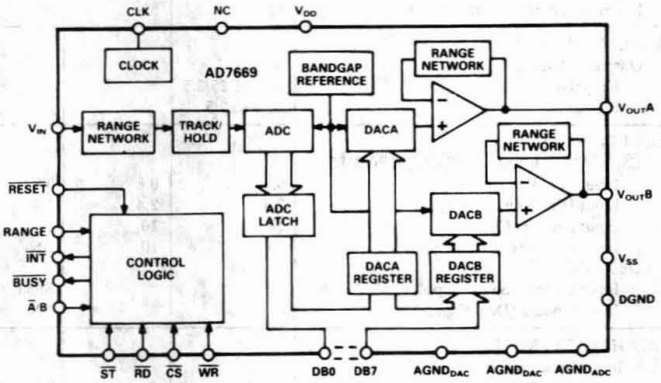
FEATURES

2 μs ADC with Track/Hold
1 μs DAC with Output Amplifier
AD7569, Single DAC Output
AD7669, Dual DAC Output
On-Chip Bandgap Reference
Fast Bus Interface
Single or Dual 5 V Supplies

AD7569 FUNCTIONAL BLOCK DIAGRAM



AD7669 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7569/AD7669 is a complete, 8-bit, analog I/O system on a single monolithic chip. The AD7569 contains a high speed successive approximation ADC with 2 μs conversion time, a track/hold with 200 kHz bandwidth, a DAC and output buffer amplifier with 1 μs setting time. A temperature-compensated 1.25 V bandgap reference provides a precision reference voltage for the ADC and the DAC. The AD7669 is similar but contains two DACs with output buffer amplifiers.

A choice of analog input/output ranges is available. Using a supply voltage of +5 V, input and output ranges of zero to 1.25 V and zero to 2.5 volts may be programmed using the RANGE input pin. Using a ±5 V supply, bipolar ranges of ±1.25 V or ±2.5 V may be programmed.

Digital interfacing is via an 8-bit I/O port and standard microprocessor control lines. Bus interface timing is extremely fast, allowing easy connection to all popular 8-bit microprocessors. A separate start convert line controls the track/hold and ADC to give precise control of the sampling period.

The AD7569/AD7669 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The AD7569 is packaged in a 24-pin, 0.3" wide "skinny" DIP, a 24-terminal SOIC and 28-terminal PLCC and LCCC packages. The AD7669 is available in a 28-pin, 0.6" plastic DIP, 28-terminal SOIC, and 28-terminal PLCC package.

PRODUCT HIGHLIGHTS

1. Complete Analog I/O on a Single Chip.
   The AD7569/AD7669 provides everything necessary to interface a microprocessor to the analog world. No external components or user trims are required, and the overall accuracy of the system is tightly specified, eliminating the need to calculate error budgets from individual component specifications.
2. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications the AD7569/AD7669 is specified for AC parameters, including signal-to-noise ratio, distortion and input bandwidth.
3. Fast Microprocessor Interface.
   The AD7569/AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 75 ns and Write pulse width less than 80 ns.

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AD7569/AD7669–SPECIFICATIONS

DAC SPECIFICATIONS[1] (V_{DD} = +5 V ± 5%; V_{SS}[2] = RANGE = $AGND_{DAC}$ = $AGND_{ADC}$ = DGND = 0 V; R_L = 2 kΩ, C_L = 100 pF to $AGND_{DAC}$ unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7569 J, A Versions[3] AD7669 J Version	AD7569 K, B Versions	AD7569 S Version	AD7569 T Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution[4]	8	8	8	8	Bits	
Total Unadjusted Error[5]	±2	±2	±3	±3	LSB typ	
Relative Accuracy[5]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[5]	±1	±3/4	±1	±3/4	LSB max	Guaranteed Monotonic
Unipolar Offset Error						DAC data is all 0s; V_{SS} = 0 V
@ 25°C	±2	±1.5	±2	±1.5	LSB max	Typical tempco is 10 µV/°C for +1.25 V range
T_{MIN} to T_{MAX}	±2.5	±2	±2.5	±2	LSB max	
Bipolar Zero Offset Error						DAC data is all 0s; V_{SS} = –5 V
@ 25°C	±2	±1 5	±2	±1.5	LSB max	Typical tempco is 20 µV/°C for ±1.25 V range
T_{MIN} to T_{MAX}	±2.5	±2	±2.5	±2	LSB max	
Full-Scale Error[6] (AD7569 Only)						V_{DD} = 5 V
@ 25°C	±2	±1	±2	±1	LSB max	
T_{MIN} to T_{MAX}	±3	±2	±4	±3	LSB max	
Full-Scale Error[6] (AD7669 Only)						V_{DD} = 5 V
@ 25°C	±3				LSB max	
T_{MIN} to T_{MAX}	±4.5				LSB max	
DACA/DACB Full Scale Error Match[6]						
(AD7669 Only)	±2.5				LSB max	V_{DD} = 5 V
ΔFull Scale/$ΔV_{DD}$, T_A = +25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = 2.5 V; $ΔV_{DD}$ = ±5%
ΔFull Scale/$ΔV_{SS}$, T_A = +25°C	0.5	0.5	0.5	0.5	LSB max	V_{OUT} = –2.5 V; $ΔV_{SS}$ = ±5%
Load Regulation at Full Scale	0.2	0.2	0.2	0.2	LSB max	R_L = 2 kΩ to °/C
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio[5] (SNR)	44	46	44	46	dB min	V_{OUT} = 20 kHz full-scale sine wave with $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion[5] (THD)	48	48	48	48	dB max	V_{OUT} = 20 kHz full-scale sine wave with $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion[5] (IMD)	55	55	55	55	dB typ	fa = 18.4 kHz, fb = 14.5 kHz with $f_{SAMPLING}$ = 400 kHz
ANALOG OUTPUT						
Output Voltage Ranges						
Unipolar	0 to +1.25/2.5				Volts	V_{DD} = +5 V, V_{SS} = 0 V
Bipolar	±1.25/±2.5				Volts	V_{DD} = +5 V, V_{SS} = –5 V
LOGIC INPUTS						
$\overline{CS}$, $\overline{X}$/B, $\overline{WR}$, RANGE, $\overline{RESET}$, DB0–DB7						
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Leakage Current	10	10	10	10	µA max	V_{IN} = 0 to V_{DD}
Input Capacitance[7]	10	10	10	10	pF max	
DB0–DB7						
Input Coding (Single Supply)			Binary			
Input Coding (Dual Supply)			2s Complement			
AC CHARACTERISTICS[7]						
Voltage Output Settling Time						Settling time to with in ±1/2 LSB of final value
Positive Full-Scale Change	2	2	2	2	µs max	Typically 1 µs
Negative Full-Scale Change (Single Supply)	4	4	4	4	µs max	Typically 2 µs
Negative Full-Scale Change (Dual Supply)	2	2	2	2	µs max	Typically 1 µs
Digital-to-Analog Glitch Impulse[5]	15	15	15	15	nV secs typ	
Digital Feedthrough[5]	1	1	1	1	nV secs typ	
V_{IN} to V_{OUT} Isolation	60	60	60	60	dB typ	V_{IN} = ±2.5 V, 50 kHz Sine Wave
DAC to DAC Crosstalk[5] (AD7669 0nly)	1				nV secs typ	
DACA to DACB Isolation[5] (AD7669 Only)	–70				dB max	
POWER REQUIREMENTS						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	For Specified Performance
V_{SS} Range (Dual Supplies)	–4.75/–5.25	–4.75/–5.25	–4.75/–5.25	–4.75/–5.25	V min/V max	Specified Performance also applies to V_{SS} = 0 V for unipolar ranges.
I_{DD}						V_{OUT} = V_{IN} = 2.5 V; Logic Inputs = 2.4 V; CLK = 0.8 V
(AD7569)	13	13	13	13	mA max	Output unloaded
(AD7669)	18				mA max	Outputs unloaded
I_{SS} (Dual Supplies)						V_{OUT} = V_{IN} = –2.5 V; Logic Inputs = 2.4 V; CLK = 0.8 V
(AD7569)	4	4	4	4	mA max	Output unloaded
(AD7669)	6				mA max	Outputs unloaded
DAC/ADC MATCHING						
Gain Matching[6]						V_{IN} to V_{OUT} match with V_{IN} = ±2.5 V,
@ 25°C	1	1	1	1	% typ	20 kHz sine wave
T_{MIN} to T_{MAX}	1	1	1	1	% typ	

NOTES

[1]Specifications apply to both DACs in the AD7669. V_{OUT} applies to both V_{OUT}A and V_{OUT}B of the AD7669.

[2]Except where noted, specifications apply for all output ranges including bipolar ranges with dual supply operation.

[3]Temperature ranges as follows: J, K versions; 0°C to +70°C
A, B versions; –25°C to +55°C
S, T versions; –55°C to +125°C

[4]1 LSB = 4.88 mV for 0 V to +1.25 V output range, 9.76 mV for 0 V to +2.5 V and ±1.25 V ranges and 19.5 mV for ±2.5 V range.

[5]See Terminology.

[6]Includes internal voltage reference error and is calculated after offset error ha s been adjusted out. Ideal unipolar full-scale voltage is (FS – 1 LSB); ideal bipolar positive full-scale voltage is (FS/2 – 1 LSB) and ideal bipolar negative full-scale voltage is –FS/2.

[7]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ANALOG DEVICES

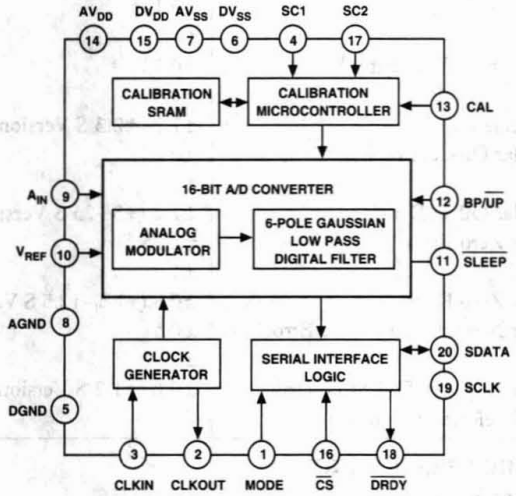
LC²MOS 16-Bit A/D Converter

AD7701

FEATURES
Monolithic 16-Bit ADC
0.0015% Linearity Error
On-Chip Self-Calibration Circuitry
Programmable Low Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 V to +2.5 V or ±2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS
Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7701 is a 16-bit ADC which uses a sigma-delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 16-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by a crystal-controlled on-chip clock oscillator.

The inherent linearity of the ADC is excellent, and end-point accuracy is ensured by self-calibration of zero and full scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a flexible serial port, which has an asynchronous mode compatible with UARTs and two synchronous modes suitable for interfacing to shift registers or the serial ports of industry-standard microcontrollers.

CMOS construction insures low power dissipation, and a power down mode reduces the idle power consumption to only 10 µW.

PRODUCT HIGHLIGHTS

1. The AD7701 offers 16-bit resolution coupled with outstanding 0.0015% accuracy.
2. No missing codes ensures true, usable, 16-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronous/asynchronous interface allows the AD7701 to interface directly to UARTs or to the serial ports of industry-standard microcontrollers.
5. Low operating power consumption and an ultralow power standby mode make the AD7701 ideal for loop-powered remote sensing applications, or battery-powered portable instruments.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	Package Options*
AD7701AN	–40°C to +85°C	0.003	N-20
AD7701BN	–40°C to +85°C	0.0015	N-20
AD7701AR	–40°C to +85°C	0.003	R-20
AD7701BR	–40°C to +85°C	0.0015	R-20
AD7701ARS	–40°C to +85°C	0.003	RS-28
AD7701AQ	–40°C to +85°C	0.003	Q-20
AD7701BQ	–40°C to +85°C	0.0015	Q-20
AD7701SQ	–55°C to +125°C	0.003	Q-20
AD7701TQ	–55°C to +125°C	0.0015	Q-20

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

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AD7701–SPECIFICATIONS

(T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = –5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; Bipolar Mode: MODE = +5 V; A_{IN} Source Resistance = 750 Ω[1] with 1 nF to AGND at A_{IN}, unless otherwise noted.)

Parameter	A, S Versions[2]	B, T Versions[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Integral Nonlinearity				
T_{MIN} to T_{MAX}		±0.0007	% FSR typ	
	±0.003	±0.0015	% FSR max	
Differential Nonlinearity				
T_{MIN} to T_{MAX}	±0.125	±0.125	LSB typ	Guaranteed No Missing Codes
	±0.5	±0.5	LSB max	
Positive Full-Scale Error[3]	±0.13	±0.13	LSB typ	
	±0.5	±0.5	LSB max	
Full-Scale Drift[4]	±1.2 (±2.3 S Version)	±1.2 (±2.3 T Version)	LSB typ	
Unipolar Offset Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Unipolar Offset Drift[4]	±1.6 (+3/–25 S Version)	±1.6 (+3/–25 T Version)	LSB typ	
Bipolar Zero Error[3]	±0.25	±0.25	LSB typ	
	±1	±1	LSB max	
Bipolar Zero Drift[4]	±0.8 (+1.5/–12.5 S Version)	±0.8 (+1.5/–12.5 T Version)	LSB typ	
Bipolar Negative Full-Scale Error[3]	±0.5	±0.5	LSB typ	
	±2	±2	LSB max	
Bipolar Negative Full-Scale Drift[4]	±0.6 (±1.2 S Version)	±0.6 (±1.2 T Version)	LSB typ	
Noise (Referred to Output)	0.1	0.1	LSB rms typ	
DYNAMIC PERFORMANCE				
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\,dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION				Applies to Unipolar and
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V max	Bipolar Ranges. After Cali-
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V max	bration, If $A_{IN} > V_{REF}$, the
Negative Full-Scale Overrange	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	V max	Device Will Output All 1s.
Maximum Offset Calibration Range[5, 6]				If $A_{IN} < 0$ (Unipolar) or
Unipolar Input Range	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	V max	$-V_{REF}$ (Bipolar), the Device
Bipolar Input Range	–0.4 V_{REF} to +0.4 V_{REF}	–0.4 V_{REF} to +0.4 V_{REF}	V max	Will Output All 0s.
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	V min	
	2 V_{REF} + 0.2	2 V_{REF} + 0.2	V max	
ANALOG INPUT				
Unipolar Input Range	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	Volts	
Input Capacitance	10	10	pF typ	
Input Bias Current[1]	1	1	nA typ	
LOGIC INPUTS				
All Inputs Except CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	V min	
CLKIN				
V_{INL}, Input Low Voltage	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	V min	
I_{IN}, Input Current	10	10	µA max	
LOGIC OUTPUTS				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD} – 1	DV_{DD} – 1	V min	I_{SOURCE} = 100 µA
Floating State Leakage Current	±10	±10	µA max	
Floating State Output Capacitance	9	9	pF typ	

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS 20-Bit A/D Converter

AD7703

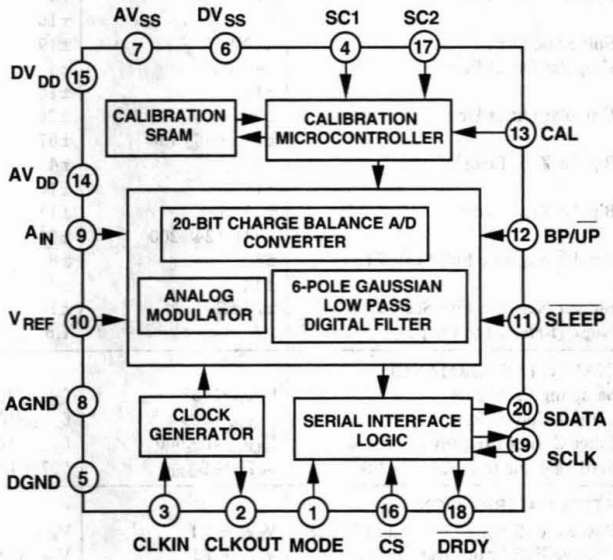
FEATURES

Monolithic 20-Bit ADC
0.0003% Linearity Error
20-Bit No Missed Codes
On-Chip Self-Calibration Circuitry
Programmable Low-Pass Filter
0.1 Hz to 10 Hz Corner Frequency
0 to +2.5 V or +2.5 V Analog Input Range
4 kSPS Output Data Rate
Flexible Serial Interface
Ultralow Power

APPLICATIONS

Industrial Process Control
Weigh Scales
Portable Instrumentation
Remote Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7703 is a 20-bit ADC which uses a sigma delta conversion technique. The analog input is continuously sampled by an analog modulator whose mean output duty cycle is proportional to the input signal. The modulator output is processed by an on-chip digital filter with a six-pole Gaussian response, which updates the output data register with 20-bit binary words at word rates up to 4 kHz. The sampling rate, filter corner frequency and output word rate are set by a master clock input that may be supplied externally, or by an on-chip gate oscillator.

The inherent linearity of the ADC is excellent, and endpoint accuracy is ensured by self-calibration of zero and full scale which may be initiated at any time. The self-calibration scheme can also be extended to null system offset and gain errors in the input channel.

The output data is accessed through a serial port, which has two synchronous modes suitable for interfacing to shift registers or the serial ports of industry standard microcontrollers.

CMOS construction ensures low power dissipation, and a power down mode reduces the idle power consumption to only 10 μW.

PRODUCT HIGHLIGHTS

1. The AD7703 offers 20-bit resolution coupled with outstanding 0.0003% accuracy.
2. No missing codes ensures true, usable, 20-bit dynamic range, removing the need for programmable gain and level-setting circuitry.
3. The effects of temperature drift are eliminated by on-chip self-calibration, which removes zero and gain error. External circuits can also be included in the calibration loop to remove system offsets and gain errors.
4. A flexible synchronization allows the AD7703 to interface directly to the serial ports of industry standard microcontrollers and DSP processors.
5. Low operating power consumption and an ultralow power standby mode make the AD7703 ideal for loop powered remote sensing applications, or battery-powered portable instruments.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	Package Options*
AD7703AN	–40°C to +85°C	0.003	N-20
AD7703BN	–40°C to +85°C	0.0015	N-20
AD7703CN	–40°C to +85°C	0.0012	N-20
AD7703AR	–40°C to +85°C	0.003	R-20
AD7703BR	–40°C to +85°C	0.0015	R-20
AD7703CR	–40°C to +85°C	0.0012	R-20
AD7703AQ	–40°C to +85°C	0.003	Q-20
AD7703BQ	–40°C to +85°C	0.0015	Q-20
AD7703CQ	–40°C to +85°C	0.0012	Q-20
AD7703SQ	–55°C to +125°C	0.003	Q-20

*N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7703—SPECIFICATIONS (T_A = +25°C; AV_{DD} = DV_{DD} = +5 V; AV_{SS} = DV_{SS} = –5 V; V_{REF} = +2.5 V; f_{CLKIN} = 4.096 MHz; BP/$\overline{UP}$ = +5 V; MODE = +5 V; A_{IN} Source Resistance = 1 kΩ with 1 nF to AGND at A_{IN} unless otherwise noted.)

Parameter	A/S Versions[2]	B Version[2]	C Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	20	20	20	Bits	
Integral Nonlinearity, T_{MIN} to T_{MAX}	±0.0015	±0.0007	±0.0003	% FSR typ	
+25°C	±0.003	±0.0015	±0.0008	% FSR max	
T_{MIN} to T_{MAX}	±0.003	±0.0015	±0.0012	% FSR max	
Differential Nonlinearity, T_{MIN} to T_{MAX}	±0.5	±0.5	±0.5	LSB typ	Guaranteed No Missing Codes
Positive Full-Scale Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Full-Scale Drift[4]	±19/±37	±19	±19	LSB typ	
Unipolar Offset Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Unipolar Offset Drift[4]	±26	±26	±26	LSB typ	Temp Range: 0°C to +70°C
	±67 +48/–400	±67	±67	LSB typ	Specified Temp Range
Bipolar Zero Error[3]	±4	±4	±4	LSB typ	
	±16	±16	±16	LSB max	
Bipolar Zero Drift[4]	±13	±13	±13	LSB typ	Temp Range: 0°C to +70°C
	±34 +24/–200	±34	±34	LSB typ	Specified Temp Range
Bipolar Negative Full-Scale Errors[3]	±8	±8	±8	LSB typ	
	±32	±32	±32	LSB max	
Bipolar Negative Full-Scale Drift[4]	±10/±20	±10	±10	LSB typ	
Noise (Referred to Output)	1.6	1.6	1.6	LSB rms typ	
DYNAMIC PERFORMANCE					
Sampling Frequency, f_S	f_{CLKIN}/256	f_{CLKIN}/256	f_{CLKIN}/256	Hz	
Output Update Rate, f_{OUT}	f_{CLKIN}/1024	f_{CLKIN}/1024	f_{CLKIN}/1024	Hz	
Filter Corner Frequency, $f_{-3\,dB}$	f_{CLKIN}/409,600	f_{CLKIN}/409,600	f_{CLKIN}/409,600	Hz	
Settling Time to ±0.0007% FS	507904/f_{CLKIN}	507904/f_{CLKIN}	507904/f_{CLKIN}	sec	For Full-Scale Input Step
SYSTEM CALIBRATION					
Positive Full-Scale Calibration Range	V_{REF} + 0.1	V_{REF} + 0.1	V_{REF} + 0.1	V max	System Calibration Applies to
Positive Full-Scale Overrange	V_{REF} + 0.1	V_{REF} + 0.1	V_{REF} + 0.1	V max	Unipolar and Bipolar Ranges.
Negative Full-Scale Overrange	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	V max	After Calibration, if A_{IN} > V_{REF},
Maximum Offset Calibration Ranges[5, 6]					the Device Will Output All 1s.
Unipolar Input Range	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	–(V_{REF} + 0.1)	V max	If A_{IN} < 0 (Unipolar) or –V_{REF}
Bipolar Input Range	–0.4 V_{REF} to +0.4 V_{REF}	–0.4 V_{REF} to +0.4 V_{REF}	–0.4 V_{REF} to +0.4 V_{REF}	V max	(Bipolar), the Device Will
Input Span[7]	0.8 V_{REF}	0.8 V_{REF}	0.8 V_{REF}	V min	Output all 0s
	2 V_{REF} + 0.2	2 V_{REF} + 0.2	2 V_{REF} + 0.2	V max	
ANALOG INPUT					
Unipolar Input Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Bipolar Input Range	±2.5	±2.5	±2.5	Volts	
Input Capacitance	20	20	20	pF typ	
Input Bias Current[1]	1	1	1	nA typ	
LOGIC INPUTS					
All Inputs except CLKIN					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.0	2.0	2.0	V min	
CLKIN					
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	3.5	3.5	3.5	V min	
I_{IN}, Input Current	10	10	10	µA max	
LOGIC OUTPUTS					
V_{OL}, Output Low Voltage	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	DV_{DD} –1	DV_{DD} –1	DV_{DD} –1	V min	I_{SOURCE} = 100 µA
Floating State Leakage Current	±10	±10	±10	µA max	
Floating State Output Capacitance	9	9	9	pF typ	
POWER REQUIREMENTS					
Power Supply Voltages					
Analog Positive Supply (AV_{DD})	4.5/5.5	4.5/5.5	4.5/5.5	V min/V max	For Specified Performance
Digital Positive Supply (DV_{DD})	4.5/AV_{DD}	4.5/AV_{DD}	4.5/AV_{DD}	V min/V max	
Analog Negative Supply (AV_{SS})	–4.5/–5.5	–4.5/–5.5	–4.5/–5.5	V min/V max	
Digital Negative Supply (DV_{SS})	–4.5/–5.5	–4.5/–5.5	–4.5/–5.5	V min/V max	
Calibration Memory Retention					
Power Supply Voltage	2.0	2.0	2.0	V min	

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS Signal Conditioning ADCs

AD7710/AD7712*

FEATURES

Charge Balancing ADC
- **24 Bits No Missing Codes**
- **±0.0015% Nonlinearity**

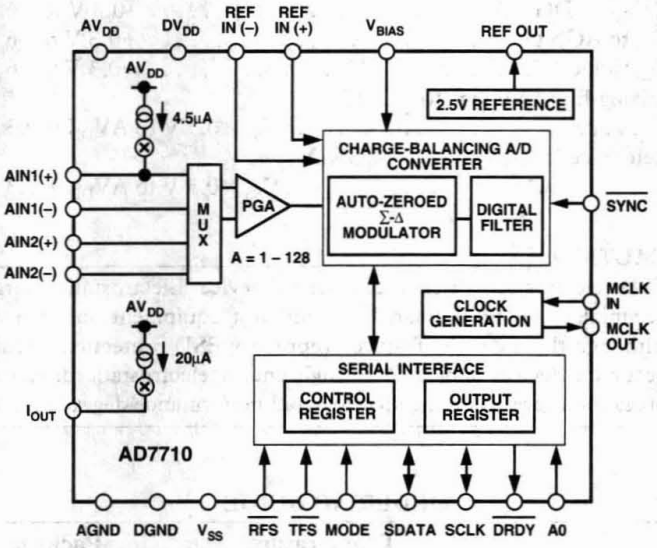
Two-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **Differential Inputs**
- **High-Level Input on AD7712**

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power-Down Mode

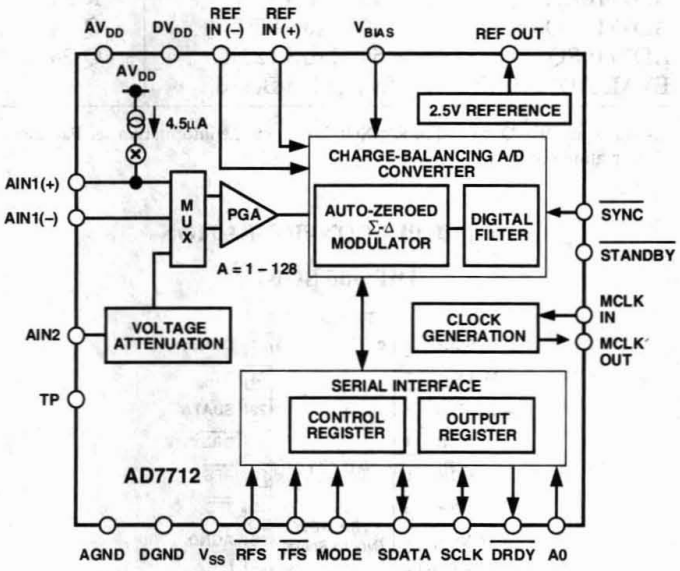
APPLICATIONS

Weigh Scales
Thermocouples
Process Control
Smart Transmitters
Portable Industrial Instruments

AD7710 FUNCTIONAL BLOCK DIAGRAM



AD7712 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7710/AD7712 is a complete analog front end for low frequency measurement applications. The device has two analog input channels and accepts either low level signals directly from a transducer or high level ($\pm 4 \times V_{REF}$ for AD7712 AIN2) signals and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. The part can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the low level analog inputs are more positive than –30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on the low level inputs. The low-level inputs, as well as the reference input, features differential input capability.

The AD7710/AD7712 is ideal for use in smart, microcontroller-based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7710/AD7712 contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures low power dissipation and a power-down mode reduces the standby power consumption to only 100 μW typical (AD7712) and 7 μW typical (AD7710). The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

*Protected by U.S. Patent No. 5,134,401.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

AV_{DD} to DV_{DD} ..... –0.3 V to +12 V
AV_{DD} to V_{SS} ..... –0.3 V to +12 V
AV_{DD} to AGND ..... –0.3 V to +12 V
AV_{DD} to DGND ..... –0.3 V to +12 V
DV_{DD} to AGND ..... –0.3 V to +6 V
DV_{DD} to DGND ..... –0.3 V to +6 V
V_{SS} to AGND ..... +0.3 V to –6 V
V_{SS} to DGND ..... +0.3 V to –6 V
Analog Input Voltage to AGND
..... V_{SS} – 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND
..... V_{SS} – 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND ..... –0.3 V to AV_{DD}
Digital Input Voltage to DGND ..... –0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) ..... –40°C to +85°C
Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates Above +75°C ..... 6 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7710AN	–40°C to +85°C	N-24
AD7710AR	–40°C to +85°C	R-24
AD7710AQ	–40°C to +85°C	Q-24
AD7710SQ	–55°C to +125°C	Q-24
EVAL-AD7710EB	Evaluation Board	

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

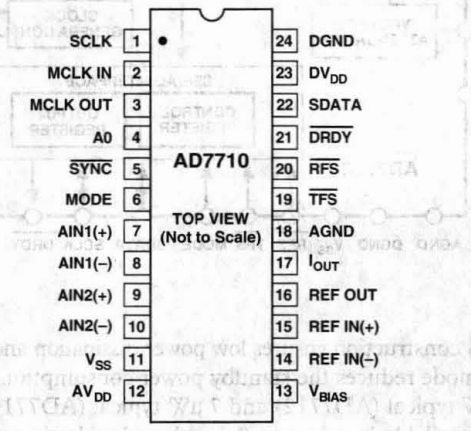
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7712AN	–40°C to +85°C	N-24
AD7712AR	–40°C to +85°C	R-24
AD7712AQ	–40°C to +85°C	Q-24
AD7712SQ	–55°C to +125°C	Q-24
EVAL-AD7712EB	Evaluation Board	

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

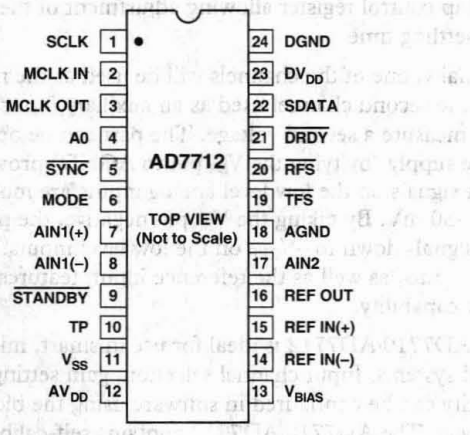
AD7710 PIN CONFIGURATION

DIP and SOIC



AD7712 PIN CONFIGURATION

DIP and SOIC



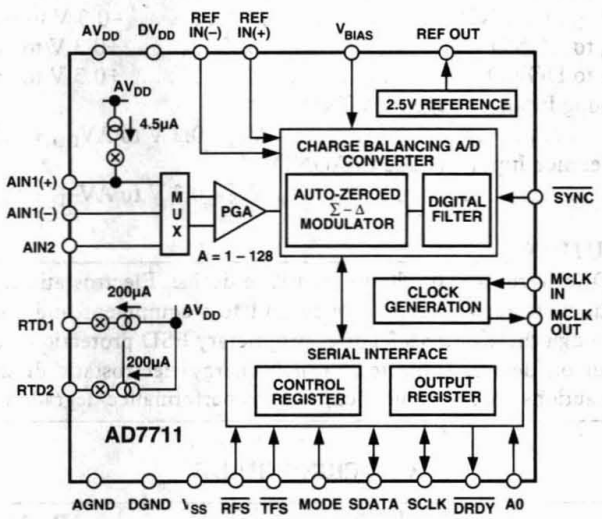
LC²MOS Signal Conditioning ADCs with RTD Excitation Currents

AD7711/AD7713

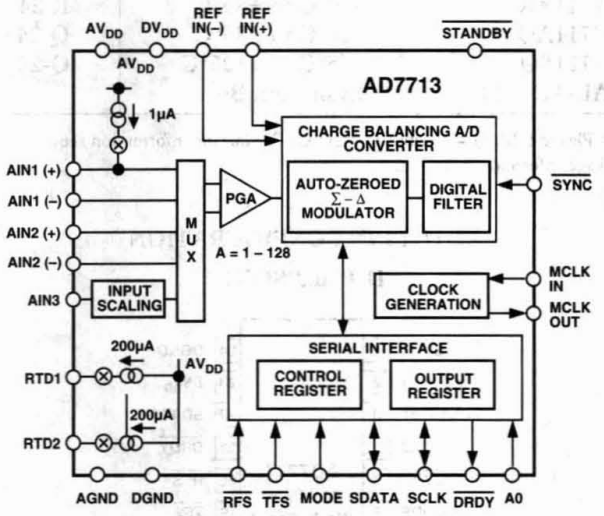
FEATURES

Charge Balancing ADC
24 Bits No Missing Codes
±0.0015% Nonlinearity
Programmable Gain Front End
Gains from 1 to 128
Three Input Channels (AD7713)
Two Input Channels (AD7711)
Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
RTD Excitation Current Sources
Bidirectional Microcontroller Serial Interface
Single Supply Operation
Low Power (AD7711: 25 mW typ; AD7713: 3.5 mW typ)
Power-Down Mode

AD7711 FUNCTIONAL BLOCK DIAGRAM



AD7713 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7711/AD7713 is a complete analog front end for low frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary* programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The AD7711 features one differential analog input and one single-ended analog input. The AD7713 features two differential inputs and one single-ended high level ($4 \times V_{REF}$/Gain) input. Both parts feature a differential reference input and can be operated from a single +5 V supply. The AD7711 can also be operated from dual supplies to allow negative input voltages. The part provides two current sources that can be used to provide excitation in three-wire and four-wire RTD configurations.

The AD7711/AD7713 is ideal for use in smart, microcontroller based systems. Gain settings, signal polarity, input channel selection and RTD current control can be configured in software using the bidirectional serial port. The part contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

*Protected by U.S. Patent No. 5,134,401.

CMOS construction ensures very low power dissipation, and a power-down mode reduces the standby power consumption to only 7 mW typical (AD7711) and 150 µW typical (AD7713). The part is available in a 24-pin, 0.3 inch wide, plastic and hermetic dual-in-line package (DIP) as well as a 24-lead small outline (SOIC) package.

AD7711 ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

AV_{DD} to DV_{DD} ..... –0.3 V to +12 V
AV_{DD} to V_{SS} ..... –0.3 V to +12 V
AV_{DD} to AGND ..... –0.3 V to +12 V
AV_{DD} to DGND ..... –0.3 V to +12 V
DV_{DD} to AGND ..... –0.3 V to +6 V
DV_{DD} to DGND ..... –0.3 V to +6 V
V_{SS} to AGND ..... +0.3 V to –6 V
V_{SS} to DGND ..... +0.3 V to –6 V
Analog Input Voltage to AGND
..... V_{SS} – 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND
..... V_{SS} – 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND ..... –0.3 V to AV_{DD}
Digital Input Voltage to DGND .... –0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Commercial (A Version) .....–40°C to +85°C
Extended (S Version) .....–55°C to +125°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Any Package) to +75°C ..... 450 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7711AN	–40°C to +85°C	N-24
AD7711AR	–40°C to +85°C	R-24
AD7711AQ	–40°C to +85°C	Q-24
AD7711SQ	–55°C to +125°C	Q-24
EVAL-AD7711EB	Evaluation Board	

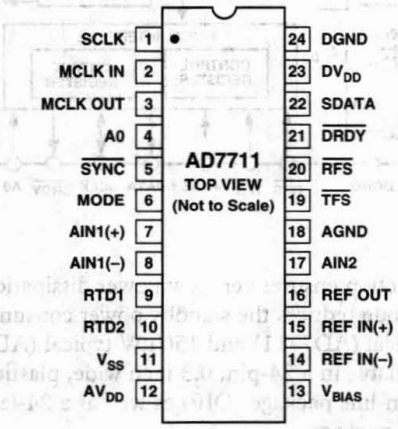
*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

ORDERING GUIDE

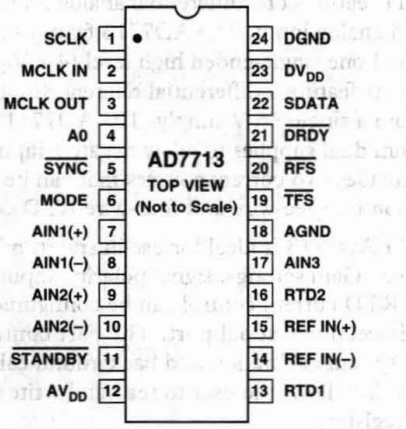
Model	Temperature Range	Package Option*
AD7713AN	–40°C to +85°C	N-24
AD7713AR	–40°C to +85°C	R-24
AD7713AQ	–40°C to +85°C	Q-24
AD7713SQ	–55°C to +125°C	Q-24
EVAL-AD7713EB	Evaluation Board	

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7711 PIN CONFIGURATION
DIP and SOIC



AD7713 PIN CONFIGURATION
DIP and SOIC



LC²MOS Signal Conditioning ADC with RTD Current Source

AD7711A*

FEATURES

Charge Balancing ADC
- **24 Bits No Missing Codes**
- **±0.0015% Nonlinearity**

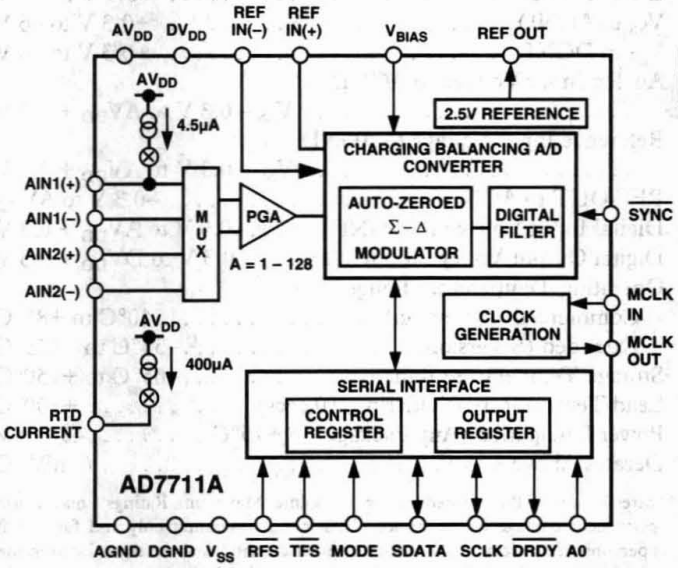
Two-Channel Programmable Gain Front End
- **Gains from 1 to 128**
- **Differential Inputs**

Low-Pass Filter with Programmable Filter Cutoffs
Ability to Read/Write Calibration Coefficients
Bidirectional Microcontroller Serial Interface
Internal/External Reference Option
Single or Dual Supply Operation
Low Power (25 mW typ) with Power-Down Mode (7 mW typ)

APPLICATIONS

RTD Transducers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7711A is a complete analog front end for low-frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features two differential analog inputs and a differential reference input. Normally, one of the channels will be used as the main channel with the second channel used as an auxiliary input to periodically measure a second voltage. It can be operated from a single supply (by tying the V_{SS} pin to AGND) provided that the input signals on the analog inputs are more positive than –30 mV. By taking the V_{SS} pin negative, the part can convert signals down to $-V_{REF}$ on its inputs. The part also provides a 400 µA current source that can be used to provide excitation for RTD transducers. The AD7711A thus performs all signal conditioning and conversion for a single or dual channel system.

The AD7711A is ideal for use in smart, microcontroller based systems. Input channel selection, gain settings and signal polarity can be configured in software using the bidirectional serial port. The AD7711A contains self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

*Protected by U.S. Patent No. 5,134,401.

CMOS construction ensures low power dissipation, and a software programmable power-down mode reduces the standby power consumption to only 7 mW typical. The part is available in a 24-pin, 0.3 inch-wide, hermetic dual-in-line package (cerdip) as well as a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The programmable gain front end allows the AD7711A to accept input signals directly from an RTD transducer, removing a considerable amount of signal conditioning. An on-chip current source provides the excitation current for the RTD.
2. The part features excellent static performance specifications with 24-bit no missing codes, ±0.0015% accuracy and low rms noise (<250 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.
3. The AD7711A is ideal for microcontroller or DSP processor applications with an on-chip control register that allows control over filter cutoff, input gain, channel selection, signal polarity, RTD current control and calibration modes.
4. The AD7711A allows the user to read and to write the on-chip calibration registers. This means that the microcontroller has much greater control over the calibration procedure.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted)

AV_{DD} to DV_{DD}	–0.3 V to +12 V
AV_{DD} to V_{SS}	–0.3 V to +12 V
AV_{DD} to AGND	–0.3 V to +12 V
AV_{DD} to DGND	–0.3 V to +12 V
DV_{DD} to AGND	–0.3 V to +6 V
DV_{DD} to DGND	–0.3 V to +6 V
V_{SS} to AGND	+0.3 V to –6 V
V_{SS} to DGND	+0.3 V to –6 V
Analog Input Voltage to AGND	V_{SS} – 0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND	V_{SS} – 0.3 V to AV_{DD} + 0.3 V
REF OUT to AGND	–0.3 V to AV_{DD}
Digital Input Voltage to DGND	–0.3 V to AV_{DD} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Commercial (A Version)	–40°C to +85°C
Extended (S Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	450 mW
Derates Above +75°C	6 mW/°C

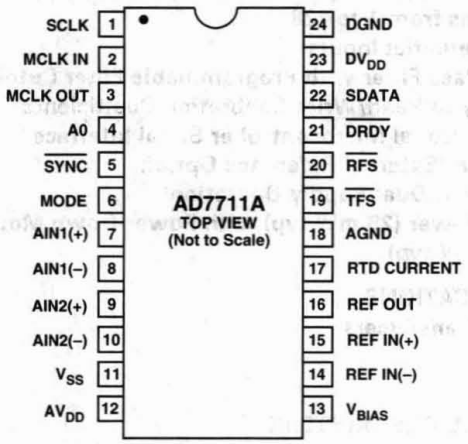
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7711AAR	–40°C to +85°C	R-24
AD7711ASQ	–55°C to +125°C	Q-24

*R = SOIC, Q = Cerdip.

PIN CONFIGURATION
DIP and SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7711A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

3 V/5 V, CMOS, 500 µA Signal Conditioning ADC

AD7714*

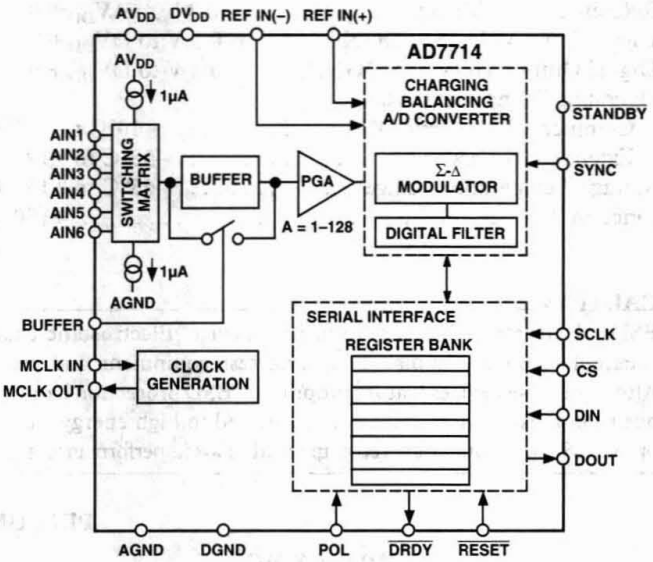
FEATURES

- Charge Balancing ADC
  - 24 Bits No Missing Codes
  - 0.0015% Nonlinearity
- Five-Channel Programmable Gain Front End
  - Gains from 1 to 128
  - Can Be Configured as Three Fully Differential Inputs or Five Pseudo-Differential Inputs
- Three-Wire Serial Interface
- 3 V (AD7714-3) or 5 V (AD7714-5) Operation
- Low Noise (<150 nV rms)
- Low Current (350 µA typ) with Power-Down (5 µA typ)
- Low-Pass Filter with Programmable Filter Cutoffs
- Ability to Read/Write Calibration Coefficients

APPLICATIONS

- Portable Industrial Instruments
- Portable Weigh Scales
- Loop-Powered Systems
- Pressure Transducers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION†

The AD7714 is a complete analog front end for low-frequency measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 24 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and settling time.

The part features three differential analog inputs (which can also be configured as five pseudo-differential analog inputs) as well as a differential reference input. It operates from a single supply (+3 V or +5 V). The AD7714 thus performs all signal conditioning and conversion for a system consisting of up to five channels.

The AD7714 is ideal for use in smart, microcontroller- or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and channel selection can be configured in software using the serial port. The AD7714 provides self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

*Protected by U.S. Patent No. 5,134,401.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 15 µW typ. The part is available in a 24-pin, 0.3 inch-wide, plastic and hermetic dual-in-line package (DIP); a 24 lead small outline (SOIC) package and a 28-lead shrink small outline package (SSOP).

PRODUCT HIGHLIGHTS

1. The AD7714 consumes less than 500 µA ($f_{CLK\ IN}$ = 1 MHz) or 1 mA ($f_{CLK\ IN}$ = 2.5 MHz) in total supply current, making it ideal for use in loop-powered systems.
2. The programmable gain channels allow the AD7714 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
3. The AD7714 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems. The part contains on-chip registers that allow control over filter cutoff, input gain, channel selection, signal polarity and calibration modes.
4. The part features excellent static performance specifications with 24-bit no missing codes, ±0.0015% accuracy and low rms noise (140 nV). End-point errors and the effects of temperature drift are eliminated by on-chip self-calibration, which removes zero-scale and full-scale errors.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND ... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A Version) ..... –40°C to +85°C
  Extended (S Version) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
Cerdip Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 70°C/W
  Lead Temperature (Soldering, 10 sec) ..... +300°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C
Power Dissipation (Any Package) to +75°C ..... 450 mW

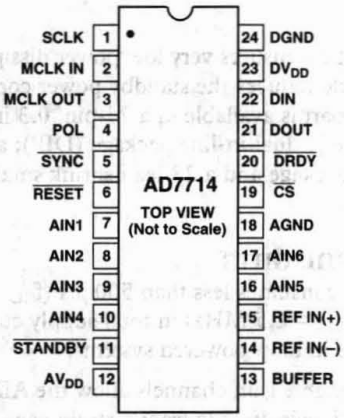
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

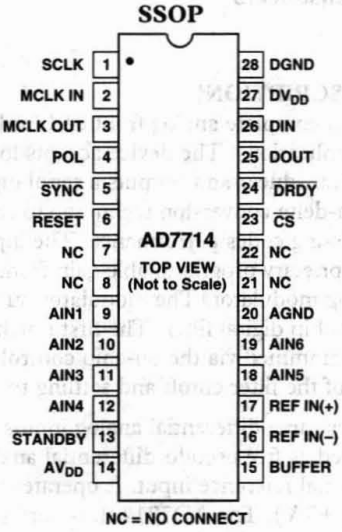
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP and SOIC



SSOP



ORDERING GUIDE

Model	AV_{DD} Supply	Temperature Range	Package Option*
AD7714AN-5	5 V	–40°C to +85°C	N-24
AD7714AR-5	5 V	–40°C to +85°C	R-24
AD7714ARS-5	5 V	–40°C to +85°C	RS-28
AD7714AN-3	3 V	–40°C to +85°C	N-24
AD7714AR-3	3 V	–40°C to +85°C	R-24
AD7714ARS-3	3 V	–40°C to +85°C	RS-28
AD7714SQ-5	5 V	–55°C to +125°C	Q-24
AD7714AChips-5	5 V	–40°C to +85°C	Die
AD7714AChips-3	3 V	–40°C to +85°C	Die
EVAL-AD7714-5EB	5 V	Evaluation Board	
EVAL-AD7714-3EB	3 V	Evaluation Board	

*N = Plastic DIP; R = SOIC; RS = SSOP; Q = Cerdip. For outline information see Package Information section.

3 V/5 V, 450 μA 16-Bit, Sigma Delta ADC

AD7715*

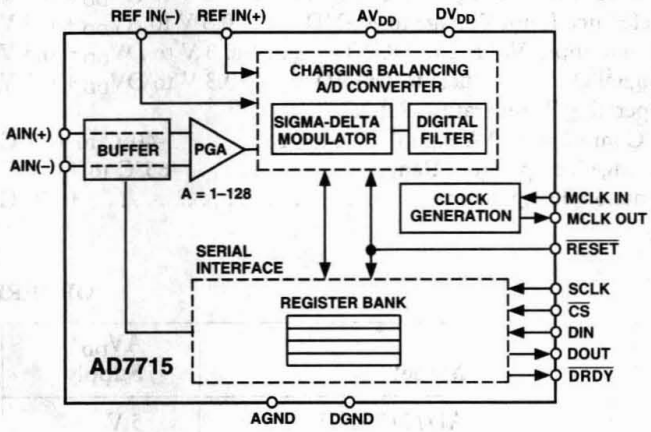
FEATURES

Charge-Balancing ADC
- **16 Bits No Missing Codes**
- **0.0015% Nonlinearity**

Programmable Gain Front End
- **Gains of 1, 2, 32 and 128**
- **Differential Input Capability**

Three-Wire Serial Interface
Ability to Buffer the Analog Input
3 V (AD7715-3) or 5 V (AD7715-5) Operation
Low Supply Current: 450 μA max @ 3 V Supplies
Low-Pass Filter with Programmable Output Update
16-Pin SOIC/DIP

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7715 is a complete analog front end for low frequency measurement applications. The part can accept low level input signals directly from a transducer and outputs a serial digital word. It employs a sigma-delta conversion technique to realize up to 16 bits of no missing codes performance. The input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via the on-chip control register allowing adjustment of the filter cutoff and output update rate.

The AD7715 features a differential analog input as well as a differential reference input. It operates from a single supply (+3 V or +5 V). It can handle unipolar input signal ranges of 0 mV to +20 mV, 0 mV to +80 mV, 0 V to +1.25 V and 0 V to +2.5 V. It can also handle bipolar input signal ranges of ±20 mV, ±80 mV, ±1.25 V and ±2.5 V. These bipolar ranges are referenced to the negative input of the differential analog input. The AD7715 thus performs all signal conditioning and conversion for a single-channel system.

The AD7715 is ideal for use in smart, microcontroller or DSP based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and update rate selection can be configured in software using the input serial port. The part contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 50 μW typ. The part is available in a 16-pin, 0.3 inch-wide, plastic dual-in-line package (DIP) as well as a 16-lead 0.3 inch-wide small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The AD7715 consumes less than 450 μA in total supply current at 3 V supplies and 1 MHz master clock, making it ideal for use in low-power systems. Standby current is less than 10 μA.
2. The programmable gain input allows the AD7715 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
3. The AD7715 is ideal for microcontroller or DSP processor applications with a three-wire serial interface reducing the number of interconnect lines and reducing the number of opto-couplers required in isolated systems. The part contains on-chip registers which allow software control over output update rate, input gain, signal polarity and calibration modes.
4. The part features excellent static performance specifications with 16-bits no missing codes, ±0.0015% accuracy and low rms noise (<550 nV). Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.

*Protected by U.S. Patent No: 5,134,401.

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ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
AV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
DGND to AGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to AGND ... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
  Commercial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 105°C/W
  Lead Temperature, (Soldering, 10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance ..... 75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infared (15 sec) ..... +220°C
Power Dissipation (Any Package) to +75°C ..... 450 mW
ESD Rating ..... >4000 V

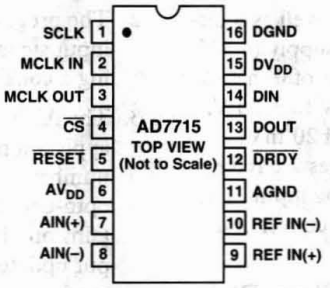
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	AV_{DD} Supply	Temperature Range	Package Option*
AD7715AN-5	5 V	–40°C to +85°C	N-16
AD7715AR-5	5 V	–40°C to +85°C	R-16
AD7715AN-3	3 V	–40°C to +85°C	N-16
AD7715AR-3	3 V	–40°C to +85°C	R-16
AD7715ACHIPS-5	5 V	–40°C to +85°C	Die
AD7715ACHIPS-3	3 V	–40°C to +85°C	Die
EVAL-AD7715-5EB	5 V	Evaluation Board	
EVAL-AD7715-3EB	3 V	Evaluation Board	

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

PIN CONFIGURATION
DIP and SOIC



ANALOG DEVICES

LC²MOS 22-Bit Data Acquisition System

AD7716

FEATURES

22-Bit Sigma-Delta ADC
- **Dynamic Range of 105 dB (146 Hz Input)**
- **±0.003% Integral Nonlinearity**

On-Chip Low-Pass Digital Filter
- **Cutoff Programmable from 584 Hz to 36.5 Hz**
- **Linear Phase Response**

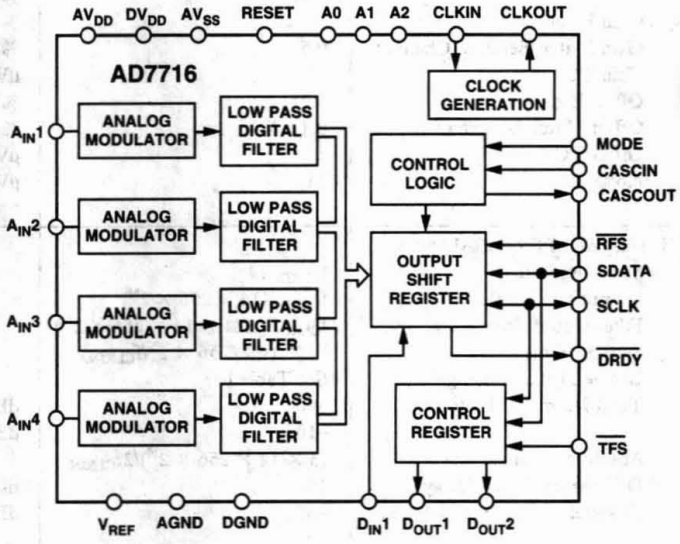
Five Line Serial I/O
Twos Complement Coding
Easy Interface to DSPs and Microcomputers
Software Control of Filter Cutoff
±5 V Supply
Low Power Operation: 50 mW

APPLICATIONS

Biomedical Data Acquisition
- **ECG Machines**
- **EEG Machines**

Process Control
High Accuracy Instrumentation
Seismic Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7716 is a signal processing block for data acquisition systems. It is capable of processing four channels with bandwidths of up to 584 Hz. Resolution is 22 bits and the usable dynamic range varies from 111 dB with an input bandwidth of 36.5 Hz to 99 dB with an input bandwidth of 584 Hz.

The device consists of four separate A/D converter channels that are implemented using sigma-delta technology. Sigma-delta ADCs include on-chip digital filtering and, thus, the system filtering requirements are eased.

Three address pins program the device address. This allows a data acquisition system with up to 32 channels to be set up in a simple fashion. The output word from the device contains 32 bits of data. One bit is determined by the state of the $D_{IN}1$ input and may be used, for example, in an ECG system with an external pacemaker detect circuit to indicate that the output word is invalid because of the presence of a pacemaker pulse. There are 22 bits of data corresponding to the analog input. Two bits contain the channel address and 3 bits are the device address. Thus, each channel in a 32-channel system would have a discrete 5-bit address. The device also has a CASCOUT pin and a CASCIN pin that allow simple networking of multiple devices.

The on-chip control register is programmed using the SCLK, SDATA and $\overline{TFS}$ pins. Three bits of the Control Register set the digital filter cutoff frequency for the device. Selectable frequencies are 584 Hz, 292 Hz, 146 Hz, 73 Hz and 36.5 Hz. A further 2 bits appear as outputs $D_{OUT}1$ and $D_{OUT}2$ and can be used for controlling calibration at the front end. The device is available in a 44-pin PQFP (Plastic Quad Flatpack) and 44-pin PLCC.

ORDERING GUIDE

Model	Temperature Range	Output Noise (Filter: 146 Hz)	Package Option*
AD7716BP	–40°C to +85°C	11 μV rms	P-44A
AD7716BS	–40°C to +85°C	11 μV rms	S-44

*P = PLCC (Plastic Leaded Chip Carrier); S = PQFP (Plastic Quad Flatpack). For outline information see Package Information section.

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AD7716–SPECIFICATIONS[1, 2] (f_{CLKIN} = 8 MHz; MODE Pin Is High (Slave Mode Operation); $AV_{DD} = DV_{DD}$ = +5 V ± 5%; AV_{SS} = –5 V ± 5%; AGND = DGND = 0 V; V_{REF} = 2.5 V; Filter Cutoff = 146 Hz; Noise Measurement Bandwidth = 146 Hz; A_{IN} Source Resistance = 750 Ω[2] with 1 nF to AGND at each A_{IN}. $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	B Version	Units	Test Conditions/Comments
STATIC PERFORMANCE			
Resolution	22	Bits	
Integral Linearity Error	0.003	% FSR typ	Guaranteed No Missed Codes to 21 Bits[3]
	0.006	% FSR max	
Gain Error	1	% FSR max	
Gain Match Between Channels	0.5	% FSR max	
Gain TC	30	µV/°C typ	
Offset Error	0.2	% FSR max	
Offset Match Between Channels	0.1	% FSR max	
Offset TC	4	µV/°C typ	
Noise	11	µV rms max	See Table I for Typical Noise Performance vs. Programmed Cutoff Frequency
DYNAMIC PERFORMANCE			
Sampling Rate	$f_{CLKIN}/14$		570 kHz for f_{CLKIN} = 8 MHz
Output Update Rate	$f_{CLKIN}/(14 \times 256 \times 2^N)$		N Is Decimal Equivalent of FC2, FC1, FC0 in Control Register
Filter Cutoff Frequency	$f_{CLKIN}/(3.81 \times 14 \times 256 \times 2^N)$		
Settling Time	$(3 \times 14 \times 256 \times 2^N/f_{CLKIN})$		
Usable Dynamic Range[4]	See Table I		
Total Harmonic Distortion	–90	dB typ	Input Frequency = 35 Hz
	–100	dB typ	A_{IN} = ±10 mV p-p
Absolute Group Delay[3]	$(3 \times 14 \times 256 \times 2^N)/2f_{CLKIN}$		
Differential Group Delay[3]	10	ns typ	
Channel-to-Channel Isolation	–85	dB typ	Feedthrough from Any One Channel to the Other Three, with 35 Hz Full-Scale Sine Wave Applied to that Channel
ANALOG INPUT			
Input Range	±2.5	Volts	
Input Capacitance	10	pF typ	
Input Bias Current	1	nA typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{IN}, Input Current			
$\overline{SDATA}$, $\overline{RFS}$	+10/-130	µA max	Internal 50 kΩ Pull-Up Resistors
$\overline{TFS}$	+10/-650	µA max	Internal 10 kΩ Pull-Up Resistor
All Other Inputs	±10	µA max	
C_{IN}, Input Capacitance[3]	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	2.4	V min	$\lvert I_{OUT} \rvert \le 40$ µA
V_{OL}, Output Low Voltage	0.4	V max	$\lvert I_{OUT} \rvert \le 1.6$ mA
POWER SUPPLIES			
Reference Input	2.4/2.6	V min/V max	
AV_{DD}	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	V min/V max	
AV_{SS}	–4.75/–5.25	V min/V max	
I_{DD}	7.5	mA max	4.8 mA typ
I_{SS}	2.5	mA max	1.8 mA typ
Power Consumption	50	mW max	35 mW typ
Power Supply Rejection[5]	–70	dB typ	

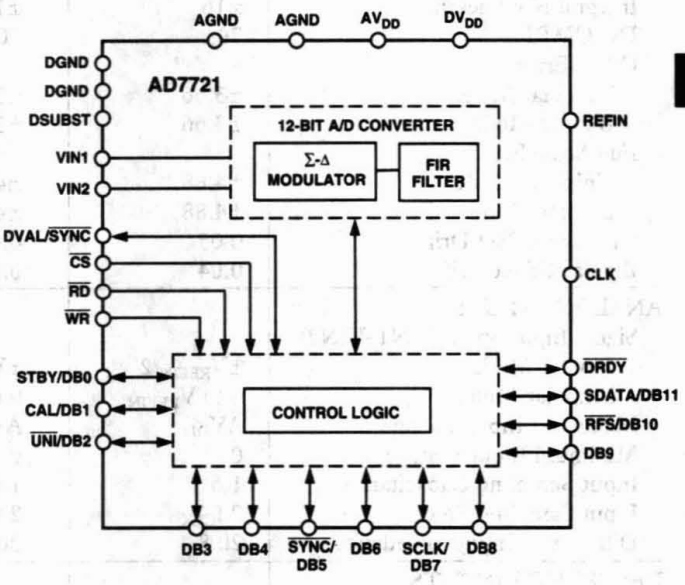
NOTES
[1]Operating temperature ranges as follows: B Version; –40°C to +85°C.
[2]The A_{IN} pins present a very high impedance dynamic load which varies with clock frequency.
[3]Guaranteed by design and characterization. Digital filter has linear phase.
[4]Usable dynamic range is guaranteed by measuring noise and relating this to the full-scale input range.
[5]100 mV p-p, 120 Hz sine wave applied to each supply.
Specifications subject to change without notice.

CMOS 16-Bit, 468.75 kHz, Sigma-Delta ADC

AD7721

FEATURES
16-Bit Sigma-Delta ADC
468.75 kHz Output Word Rate (OWR)
No Missing Codes
Low-Pass Digital Filter
High Speed Serial Interface
Linear Phase
229.2 kHz Input Bandwidth
Power Supplies: AV_{DD}, DV_{DD}: +5 V ± 5%
Standby Mode (70 μW)
Parallel Mode (12-Bit/312.5 kHz OWR)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

GENERAL DESCRIPTION

The AD7721 is a complete low power, 12-/16-bit, sigma-delta ADC. The part operates from a +5 V supply and accepts a differential input of 0 V to 2.5 V or ±1.25 V. The analog input is continuously sampled by an analog modulator at twice the clock frequency eliminating the need for external sample-and-hold circuitry. The modulator output is processed by two finite impulse response (FIR) digital filters in series. The on-chip filtering reduces the external antialias requirements to first order in most cases. Settling time for a step input is 218.4 μs while the group delay for the filter is 109.2 μs when the master clock equals 15 MHz.

The AD7721 can be operated with input bandwidths up to 229.2 kHz. The corresponding output word rate is 468.75 kHz. The part can be operated with lower clock frequencies also. The sample rate, filter corner frequency, settling time, group delay and output word rate will be reduced also, as these are proportional to the external clock frequency. The maximum clock frequencies in parallel mode and serial mode are 10 MHz and 15 MHz respectively.

Use of a single bit DAC in the modulator guarantees excellent linearity and dc accuracy. Endpoint accuracy is ensured by on-chip calibration of offset and gain. This calibration procedure minimizes the part's zero-scale and full-scale errors.

The output data is accessed from the output register through a serial or parallel port. This offers easy, high speed interfacing to modern microcontrollers and digital signal processors. The serial interface operates in internal clocking (master) mode, the AD7721 providing the serial clock.

CMOS construction ensures low power dissipation while a power-down mode reduces the power consumption to only 100 μW.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7721AN	–40°C to +85°C	N-28
AD7721AR	–40°C to +85°C	R-28
AD7721SQ	–55°C to +125°C	Q-28

*N = Plastic DIP; R = 0.3" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

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AD7721–SPECIFICATIONS[1] (AV_{DD} = +5 V ± 5%; DV_{DD} = +5 V ± 5%; AGND = DGND = 0 V, f_{CLK} = 15 MHz, REFIN = +2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A Version	S Version	Units	Test Conditions/Comments
SERIAL MODE ONLY				
STATIC PERFORMANCE				
Resolution	16	16	Bits	
Minimum Resolution for Which No Missing Codes Is Guaranteed	12	12	Bits min	Guaranteed 12 Bits Monotonic
Differential Nonlinearity	±8	±8	LSB typ	
Integral Nonlinearity	±16	±16	LSB max	16-Bit Operation
DC CMRR	70	70	dB min	Bipolar Mode
Offset Error[2]				
Unipolar Mode	±3.66	±3.66	mV max	Typically 0.61 mV
Bipolar Mode	±3.66	±3.66	mV max	Typically 0.61 mV
Full-Scale Error[2, 3]				
Unipolar Mode	±4.88	±4.88	mV max	Typically 0.61 mV
Bipolar Mode	±4.88	±4.88	mV max	Typically 1.22 mV
Unipolar Offset Drift	0.05	0.05	mV/°C typ	
Bipolar Offset Drift	0.04	0.04	mV/°C typ	
ANALOG INPUTS				
Signal Input Span (VIN1–VIN2)				
Bipolar Mode	$\pm V_{REFIN}/2$	$\pm V_{REFIN}/2$	Volts max	$\overline{UNI}$ = V_{IH}
Unipolar Mode	0 to V_{REFIN}	0 to V_{REFIN}	Volts max	$\overline{UNI}$ = V_{IL}
Maximum Input Voltage	AV_{DD}	AV_{DD}	Volts	
Minimum Input Voltage	0	0	Volts	
Input Sampling Capacitance	1.6	1.6	pF typ	
Input Sampling Rate	2 f_{CLK}	2 f_{CLK}	MHz	Guaranteed by Design
Differential Input Impedance	20.8	20.8	kΩ typ	With 15 MHz on CLK Pin
REFERENCE INPUTS				
V_{REFIN}	2.4 to 2.6	2.4 to 2.6	V min/V max	
REFIN Input Current	200	200	µA typ	
DYNAMIC SPECIFICATIONS				
Signal to (Noise + Distortion)	74	74	dB min	Input Bandwidth 0 kHz to 210 kHz
Total Harmonic Distortion	–78	–78	dB max	Input Bandwidth 0 kHz to 229.2 kHz
Frequency Response				
0 kHz–210 kHz	±0.05	±0.05	dB max	
229.2 kHz	–3	–3	dB min	
259.01 kHz to 14.74 MHz	–72	–72	dB min	
CLOCK				
CLK Duty Ratio	45 to 55	45 to 55	% max	For Specified Operation
V_{CLKH}, CLK High Voltage	0.7 × DV_{DD}	0.7 × DV_{DD}	V min	CLK Uses CMOS Logic
V_{CLKL}, CLK Low Voltage	0.3 × DV_{DD}	0.3 × DV_{DD}	V max	
LOGIC INPUTS				
V_{INH}, Input High Voltage	2.0	2.0	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current	10	10	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	4.0	4.0	V min	$\lvert I_{OUT} \rvert \le 200$ µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	$\lvert I_{OUT} \rvert \le 1.6$ mA
POWER SUPPLIES				
AV_{DD}	4.75/5.25	4.75/5.25	V min/V max	
DV_{DD}	4.75/5.25	4.75/5.25	V min/V max	
I_{DD} (Total from AV_{DD}, DV_{DD})	28.5	28.5	mA max	Digital Inputs Equal to 0 V or DV_{DD}
Power Consumption	150	150	mW max	Active Mode
Power Consumption	100	100	µW max	Standby Mode

NOTES

[1]Operating temperature range is as follows: A Version: –40°C to +85°C; S Version: –55°C to +125°C.

[2]Applies after calibration at temperature of interest.

[3]Full-scale error applies to both positive and negative full-scale error. The ADC gain is calibrated w.r.t. the voltage on the REFIN pin.

Specifications subject to change without notice.

ANALOG DEVICES

Transducer ADC

AD7730*

KEY FEATURES
Resolution of 500,000 Counts (Peak-to-Peak)
Offset Drift: <1 ppm/°C
Gain Drift: 2 ppm/°C
Line Frequency Rejection: >150 dB
Buffered Differential Inputs
Programmable Filter Cutoffs
Specified for Drift over Time
Operates with Reference Voltages of 1 V to 5 V

ADDITIONAL FEATURES
Two-Channel Programmable Gain Front End
On-Chip DAC for Offset/TARE Removal
AC or DC Excitation
Single Supply Operation

APPLICATIONS
Weigh Scales
Pressure Measurement

GENERAL DESCRIPTION

The AD7730 is a complete analog front end for weigh-scale and pressure measurement applications. The device accepts low level signals directly from a transducer and outputs a serial digital word. The input signal is applied to a proprietary* programmable gain front end based around an analog modulator. The modulator output is processed by a low-pass programmable digital filter, allowing adjustment of filter cutoff, output rate and settling time.

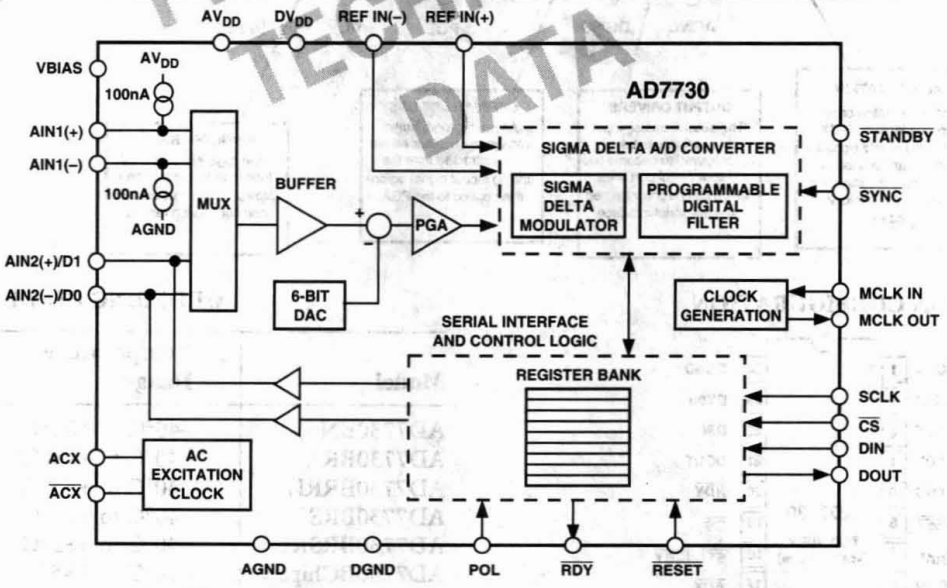
The part features two buffered differential programmable gain analog inputs as well as a differential reference input. The part can operate from a single +5 V supply or from ±2.5 V supplies. It accepts four unipolar analog input ranges: 0 mV to +10 mV, +20 mV, +40 mV and +80 mV and four bipolar ranges ±10 mV, ±20 mV, ±40 mV and ±80 mV. The peak-to-peak resolution achievable directly from the part is 1 in 500,000 counts. An on-chip 6-bit DAC allows the removal of TARE voltages. Clock signals for synchronizing ac excitation of the bridge are also provided.

The serial interface on the part can be configured for three-wire operation and is compatible with microcontrollers and digital signal processors. The AD7730 contains self-calibration and system calibration options and features an offset drift of less than 5 ppm/°C and a gain drift of less than 2 ppm/°C.

The part is available in a 24-pin plastic DIP, a 24-lead SOIC and 24-lead SSOP package.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No: 5,134,401.
Other patents pending.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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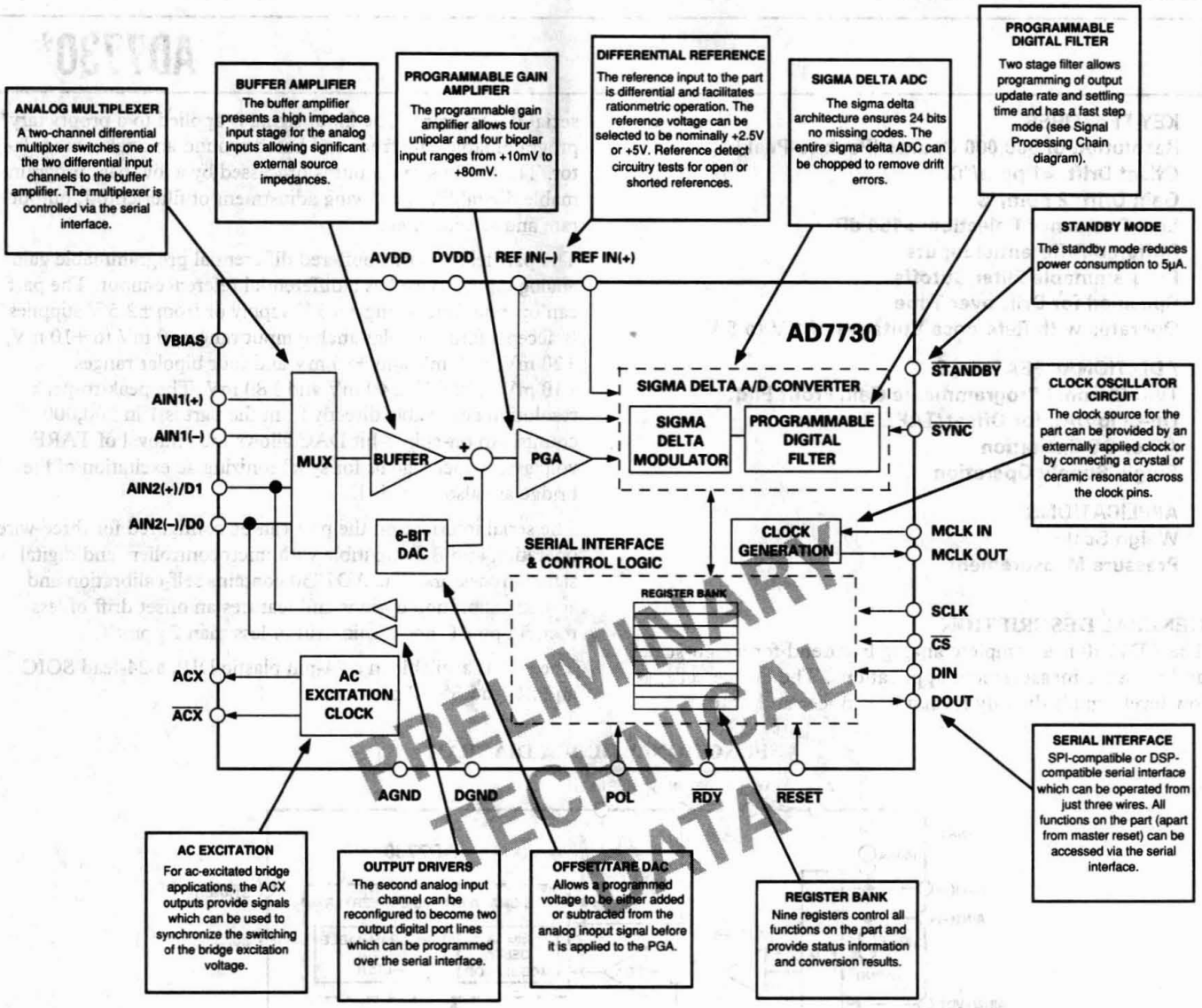
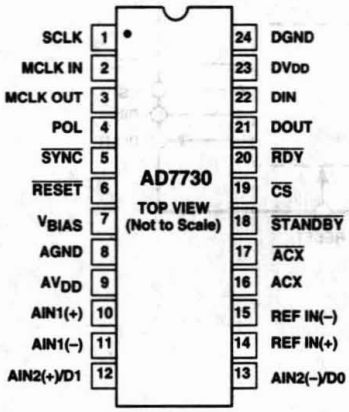
DETAILED FUNCTIONAL BLOCK DIAGRAM


ANALOG MULTIPLEXER
A two-channel differential multiplxer switches one of the two differential input channels to the buffer amplifier. The multiplexer is controlled via the serial interface.
BUFFER AMPLIFIER
The buffer amplifier presents a high impedance input stage for the analog inputs allowing significant external source impedances.
PROGRAMMABLE GAIN AMPLIFIER
The programmable gain amplifier allows four unipolar and four bipolar input ranges from +10mV to +80mV.
DIFFERENTIAL REFERENCE
The reference input to the part is differential and facilitates rationmetric operation. The reference voltage can be selected to be nominally +2.5V or +5V. Reference detect circuitry tests for open or shorted references.
SIGMA DELTA ADC
The sigma delta architecture ensures 24 bits no missing codes. The entire sigma delta ADC can be chopped to remove drift errors.
PROGRAMMABLE DIGITAL FILTER
Two stage filter allows programming of output update rate and settling time and has a fast step mode (see Signal Processing Chain diagram).
STANDBY MODE
The standby mode reduces power consumption to 5µA.
AVDD
DVDD
REF IN(–)
REF IN(+)
AD7730
VBIAS
AIN1(+)
AIN1(–)
AIN2(+)/D1
AIN2(–)/D0
MUX
BUFFER
PGA
SIGMA DELTA A/D CONVERTER
SIGMA DELTA MODULATOR
PROGRAMMABLE DIGITAL FILTER
STANDBY
SYNC
CLOCK OSCILLATOR CIRCUIT
The clock source for the part can be provided by an externally applied clock or by connecting a crystal or ceramic resonator across the clock pins.
6-BIT DAC
SERIAL INTERFACE & CONTROL LOGIC
CLOCK GENERATION
MCLK IN
MCLK OUT
REGISTER BANK
SCLK
CS
DIN
DOUT
ACX
ACX
AC EXCITATION CLOCK
AGND
DGND
POL
RDY
RESET
SERIAL INTERFACE
SPI-compatible or DSP-compatible serial interface which can be operated from just three wires. All functions on the part (apart from master reset) can be accessed via the serial interface.
AC EXCITATION
For ac-excitated bridge applications, the ACX outputs provide signals which can be used to synchronize the switching of the bridge excitation voltage.
OUTPUT DRIVERS
The second analog input channel can be reconfigured to become two output digital port lines which can be programmed over the serial interface.
OFFSET/TARE DAC
Allows a programmed voltage to be either added or subtracted from the analog inoput signal before it is applied to the PGA.
REGISTER BANK
Nine registers control all functions on the part and provide status information and conversion results.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7730BN	–40°C to +85°C	N-24
AD7730BR	–40°C to +85°C	R-24
AD7730BRRL	–40°C to +85°C	Reeled SOIC
AD7730BRS	–40°C to +85°C	RS-24
AD7730BRSRL	–40°C to +85°C	Reeled SSOP
AD7730BChips	–40°C to +85°C	Die

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

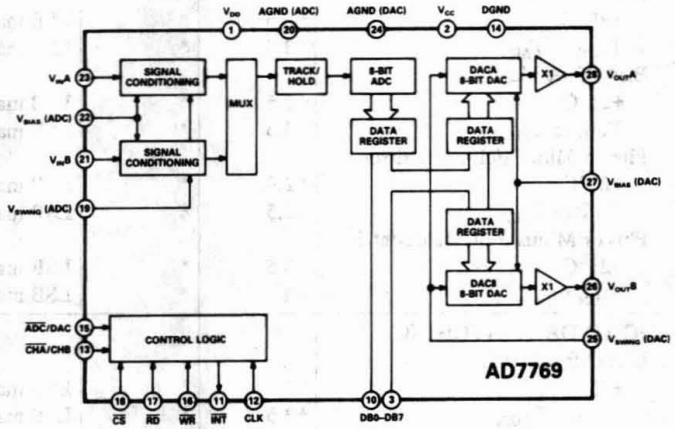
LC²MOS Analog I/O Port

AD7769*

FEATURES
Two-Channel, 8-Bit 2.5 μs ADC
Two 8-Bit, 2.5 μs DACs with Output Amplifiers
Span and Offset of ADC and DAC Independently Adjustable
Low Power

APPLICATIONS
Winchester Disk Servo Controllers
Floppy Disk Microstepping
Closed Loop Servo Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7769 is a complete, two-channel, 8-bit, analog I/O port. It has versatile input and output signal conditioning features that make it ideal for use in head-positioning servos in Winchester disk systems. It is equally suitable for floppy disk microstepping head positioning, other closed loop digital servo systems and general purpose 8-bit data acquisition.

The AD7769 contains a high speed successive approximation ADC, preceded by a two-channel multiplexer and signal conditioning circuits. The input span of the ADC and the offset of the zero point from ground can be independently set by applying ground referenced voltages. The AD7769 also contains two independent, fast settling, 8-bit DACs with output amplifiers. The output span and offset voltage of the DACs can be set independently of those of the ADC. This makes the AD7769 especially useful in disk drives, where only a positive supply rail is available and the ranges of the ADC and DACs must be referenced to some positive voltage less than the supply.

The AD7769 is easily interfaced to a standard 8-bit mpu bus via an 8-bit data port and standard microprocessor control lines.

The AD7769 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic DIP and 28-terminal PLCC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7769JN	0°C to +70°C	N-28
AD7769JP	0°C to +70°C	P-28A
AD7769AN	–40°C to +85°C	N-28
AD7769AP	–40°C to +85°C	P-28A

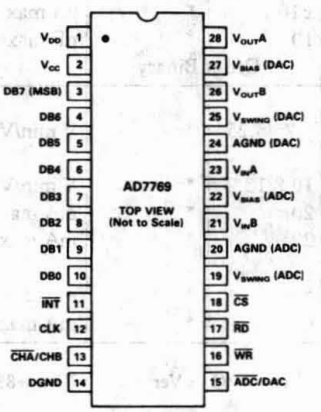
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For package outline information see Package Information section.

PRODUCT HIGHLIGHTS

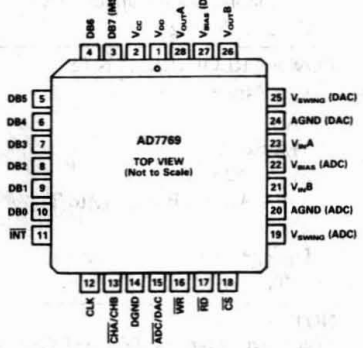
1. Two-Channel, 8-Bit Analog I/O port on a Single Chip.
   The AD7769 contains a two-channel, high speed ADC with input signal conditioning and two, fast settling 8-bit DACs with output amplifiers, on a single chip.
2. Independent Control of Span and Offset.
   The input voltage span of the ADC and the midpoint of the transfer function, the output voltage swing of the two DACs and the half-scale output voltage, can be set independently by applying ground referenced control voltages.
3. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications, the AD7769 is specified with ac parameters including signal-to-noise ratio, distortion and signal bandwidth.
4. Fast Microprocessor Interface.
   The AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 65 ns and a Write pulse width less than 90 ns.

PIN CONFIGURATIONS

DIP



PLCC



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AD7769–SPECIFICATIONS

ADC SPECIFICATIONS (V_{DD} = +12 V ± 10%; V_{CC} = +5 V ± 5%; AGND [ADC] = AGND [DAC] = DGND = 0 V; V_{BIAS} [ADC] = +5 V; V_{SWING} [ADC] = +2.5 V; f_{CLK} = 5 MHz external. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	J Version	A Version	Units	Conditions/Comments
DC ACCURACY				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	No Missing Codes. See Terminology.
Bias Offset Error				See Terminology
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.0	*	LSB max	
Bias Offset Match				Channel A to Channel B
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{MIN} to T_{MAX}	±2.5	*	LSB max	
Plus or Minus Full-Scale Match				Channel A to Channel B
+25°C	±3.5	*	LSB max	
T_{MIN} to T_{MAX}	±4	*	LSB max	
ADC TO DAC MATCHING				Channel A/B to V_{OUT} A/B
Bias Offset Match				V_{BIAS} (DAC) = +5 V, V_{SWING} (DAC) = +2.5 V.
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.5	*	LSB max	
Plus or Minus Full-Scale Match				
+25°C	±3.5	*	LSB max	
T_{MIN} to T_{MAX}	±4.0	*	LSB max	
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	60	*	dB typ	f_a = 99 kHz, f_b = 96.7 kHz with $f_{SAMPLING}$ = 400 kHz
Frequency Response	0.1	*	dB typ	V_{IN} = Full-Scale, dc to 200 kHz Sine Wave
ANALOG INPUTS				
Input Voltage Ranges, $V_{IN}A$, $V_{IN}B$	$V_{BIAS} - V_{SWING}$ or 0		V min	Whichever Is the Higher
	$V_{BIAS} + V_{SWING}$ or 9.8		V max	Whichever Is the Lower
Input Currents, $I_{IN}A$, $I_{IN}B$	±0.4	*	mA max	
ADC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (ADC)	2/6.8	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
V_{SWING} (ADC)	2.0/3.0	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
Input Currents				
V_{BIAS} (ADC) Input	±800	*	µA max	
V_{SWING} (ADC) Input	±1	*	µA max	
LOGIC OUTPUTS				
DB0–DB7, $\overline{INT}$				
V_{OL}, Output Low Voltage	0.4	*	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	*	V min	I_{SOURCE} = 200 µA
DB0–DB7				
Floating State Leakage Current	±10	*	µA max	
Floating State Capacitance[2]	10	*	pF max	
Output Coding	Offset Binary			
POWER REQUIREMENTS				
V_{CC} Range	4.75/5.25	*	V min/V max	For Specified Performance. The Part Will Function with V_{CC} = 5 V ± 10% with Degraded Performance.
V_{DD} Range	10.8/13.2	*	V min/V max	For Specified Performance
I_{DD} @ +25°C	20	*	mA max	For ADC and DAC: V_{BIAS} = 5.0 V; V_{SWING} = 3 0 V; $V_{IN}A$,
$V_{UB}Am$ $V_{IN}B$ = T_{MIN} to T_{MAX}	22	*	mA max	V_{BIAS}; DAC Code = FF (Hex); DACA and DACB Load = 5 kΩ to AGND (DAC). Typically I_{DD} = 14 mA.
I_{CC} @ +25°C	5	*	mA max	Logic Inputs = 2.4 V, CLK Input = 0.8 V. Typically I_{CC} =
T_{MIN} to T_{MAX}	6	*	mA max	1.5 mA.

NOTES
[1] Temperature range as follows: J Version: 0°C to +70°C; A Version: –40°C to +85°C.
[2] Sample tested at +25°C to ensure compliance.
*Specification same as J Version.
Specifications subject to change without notice.

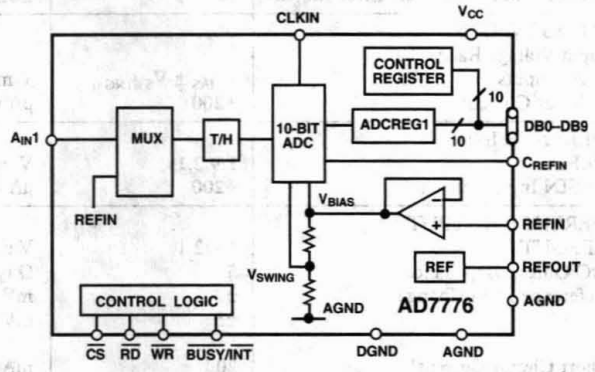
LC²MOS, High Speed 1-, 4- & 8-Channel 10-Bit ADCs

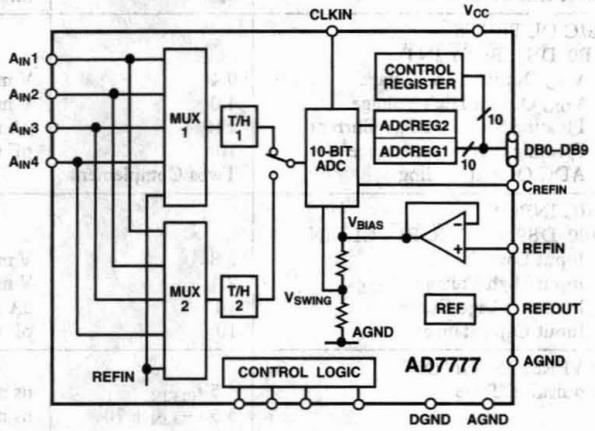
AD7776/AD7777/AD7778

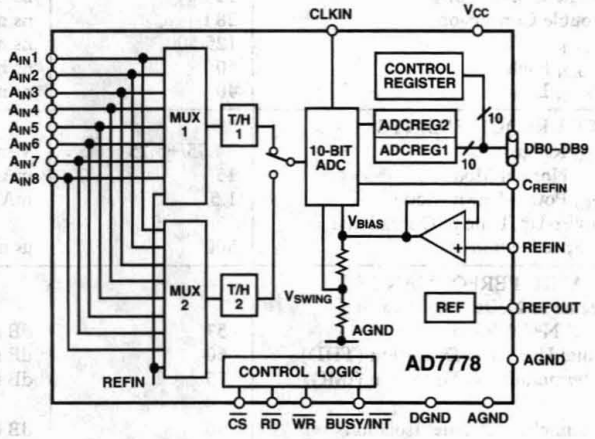
FEATURES
AD7776: Single Channel
AD7777: 4-Channel
AD7778: 8-Channel
Fast 10-Bit ADC: 2.5 μs Worst Case
+5 V Only
Half-Scale Conversion Option
Fast Interface Port
Power-Down Mode

APPLICATIONS
HDD Servos
Instrumentation

FUNCTIONAL BLOCK DIAGRAMS







GENERAL DESCRIPTION

The AD7776, AD7777 and AD7778 are a family of high speed, multichannel, 10-bit ADCs primarily intended for use in R/W head positioning servos found in high density hard disk drives. They have unique input signal conditioning features which make them ideal for use in such single supply applications.

By setting a bit in a control register within both the four-channel version, AD7777, and eight-channel version, AD7778, the input channels can either be independently sampled or any two channels of choice can be simultaneously sampled. For all versions the specified input signal range is of the form $V_{BIAS} \pm V_{SWING}$. However, if the RTN pin is biased at, say, 2 V then the analog input signal range becomes 0 V to +2 V for all input channels. This is dealt with in more detail under the section Changing the Analog Input Voltage Range. The voltage V_{BIAS} is the offset of the ADC's midpoint code from ground and is supplied either by an onboard reference available to the user (REFOUT) or by an external voltage reference applied to REFIN. The full-scale range (FSR) of the ADC is equal to 2 V_{SWING} where V_{SWING} is nominally equal to REFIN/2. Additionally, when placed in the half-scale conversion mode, the value of REFIN is converted. This allows the channel offset(s) to be measured.

Control register loading and ADC register reading, channel select and conversion start are under the control of the μP. The twos complemented coded ADCs are easily interfaced to a standard 16-bit MPU bus via their 10-bit data port and standard microprocessor control lines.

They are fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7776 is available in a 24-pin SOIC package; the AD7777 is available in both 28-pin DIP and 28-pin SOIC packages; the AD7778 is available in a 44-pin PQFP package.

***Protected by U.S. Patent No. 4,990,916.**

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AD7776/AD7777/AD7778–SPECIFICATIONS

(V_{CC} = +5 V ± 5%; AGND = DGND = 0 V; CLKIN = 8 MHz; RTN = 0 V; C_{REFIN} = 10 nF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	Units	Conditions/Comments
DC ACCURACY			
Resolution[2]	10	Bits	
Relative Accuracy	±1	LSB max	See Terminology
Differential Nonlinearity	±1	LSB max	No Missing Codes; See Terminology
Bias Offset Error	±12	LSB max	See Terminology
Bias Offset Error Match	10	LSB max	Between Channels, AD7777/AD7778 Only; See Terminology
Plus or Minus Full-Scale Error	±12	LSB max	See Terminology
Plus or Minus Full-Scale Error Match	10	LSB max	Between Channels, AD7777/AD7778 Only; See Terminology
ANALOG INPUTS			
Input Voltage Range			
All Inputs	V_{BIAS} ± V_{SWING}	V min/V max	
Input Current	+200	µA max	V_{IN} = V_{BIAS} ± V_{SWING}; Any Channel
REFERENCE INPUT			
REFIN	1.9/2.1	V min/V max	For Specified Performance
REFIN Input Current	+200	µA max	
REFERENCE OUTPUT			
REFOUT	1.9/2.1	V min/V max	Nominal REFOUT = 2.0 V
DC Output Impedance	5	Ω typ	
Reference Load Change	±2	mV max	For Reference Load Current Change of 0 to ±500 µA
	±5	mV max	For Reference Load Current Change of 0 to ±1 mA
			Reference Load Should Not Change During Conversion
Short Circuit Current[3]	20	mA max	See Terminology
LOGIC OUTPUTS			
DB0–DB9, BUSY/$\overline{INT}$			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	V min	I_{SOURCE} = 200 µA
Floating State Leakage Current	±10	µA max	
Floating State Capacitance[3]	10	pF max	
ADC Output Coding	Twos Complement		
LOGIC INPUTS			
DB0–DB9, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLKIN			
Input Low Voltage, V_{INL}	0.8	V max	
Input High Voltage, V_{INH}	2.4	V min	
Input Leakage Current	10	µA max	
Input Capacitance[3]	10	pF max	
CONVERSION TIMING			
Acquisition Time	4.5 t_{CLKIN}	ns min	See Terminology
	5.5 t_{CLKIN} + 70	ns max	
Single Conversion	14 t_{CLKIN}	ns max	
Double Conversion	28 t_{CLKIN}	ns max	
t_{CLKIN}	125/500	ns min/ns max	Period of Input Clock CLKIN
t_{CLKIN} High	50	ns min	Minimum High Time for CLKIN
t_{CLKIN} Low	40	ns min	Minimum Low Time for CLKIN
POWER REQUIREMENTS			
V_{CC} Range	+4.75/+5.25	V min/V max	For Specified Performance
I_{CC}, Normal Mode	15	mA max	$\overline{CS}$ = $\overline{RD}$ = +5 V, CR8 = 0
I_{CC}, Power-Down Mode	1.5	mA max	CR8 = 1. All Linear Circuitry OFF
Power-Up Time to Operational Specifications	500	µs max	From Power-Down Mode
DYNAMIC PERFORMANCE			See Terminology
Signal to Noise and Distortion S/(N+D) Ratio	–57	dB min	V_{IN} = 99.88 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz
Total Harmonic Distortion (THD)	–60	dB min	V_{IN} = 99.88 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz
Intermodulation Distortion (IMD)	–75	dB typ	fa = 103.2 kHz, fb = 96.5 kHz with $f_{SAMPLING}$ = 380.95 kHz. Both Signals Are Sine Waves at Half-Scale Amplitude
Channel-to-Channel Isolation	–90	dB typ	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 380.95 kHz

NOTES
[1]Temperature range as follows: A = –40°C to +85°C.
[2]1 LSB = (2 x V_{SWING})/1024 = 1.95 mV for V_{SWING} = 1.0 V.
[3]Guaranteed by design, not production tested.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	No. of Channels	Package Option[1, 2]
AD7776AR[3]	–40°C to +85°C	1	R-24
AD7777AN	–40°C to +85°C	4	N-28
AD7777AR[3]	–40°C to +85°C	4	R-28
AD7778AS[3]	–40°C to +85°C	8	S-44

NOTES
[1]R = SOIC, N = Plastic DIP, S = PQFP.
[2]For outline information see Package Information section.
[3]Analog Devices reserves the right to ship devices branded with a J in place of the A, e.g., AD7776JR instead of AD7776AR. Temperature range remains –40°C to +85°C.

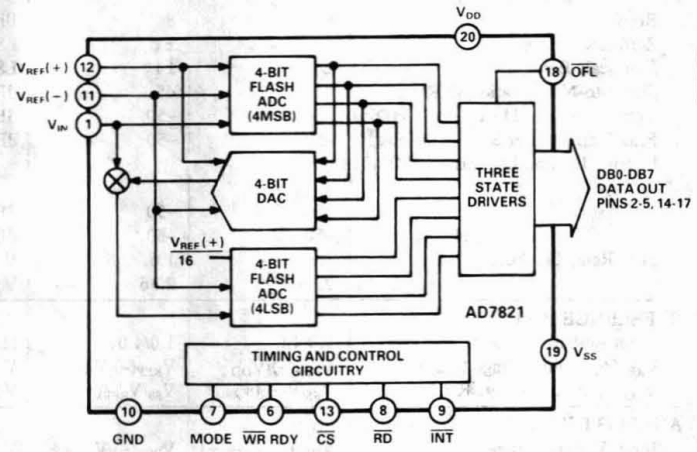
LC²MOS High Speed, µP-Compatible 8-Bit ADC with Track/Hold Function

AD7821

FEATURES

- Fast Conversion Time: 660 ns max
- 100 kHz Track-and-Hold Function
- 1 MHz Sample Rate
- Unipolar and Bipolar Input Ranges
- Ratiometric Reference Inputs
- No External Clock
- Extended Temperature Range Operation
- Skinny 20-Pin DIPs, SOIC and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7821 is a high speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660 ns (vs. 1.36 µs for the AD7820) and 100 kHz signal bandwidth (vs. 6.4 kHz). The sampling instant is better defined and occurs on the falling edge of $\overline{WR}$ or $\overline{RD}$. The provision of a V_{SS} pin (Pin 19) allows the part to operate from ±5 V supplies and to digitize bipolar input signals. Alternatively, for unipolar inputs, the V_{SS} pin can be grounded and the AD7821 will operate from a single +5 V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100 kHz max. It also uses a half-flash conversion technique that eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and latched, three-state data outputs capable of interfacing to high speed data buses. An overflow output ($\overline{OFL}$) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The part features a low power dissipation of 50 mW.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660 ns, with 700 ns for the RD mode.
2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6 V/µs to be converted to 8-bits without an external track-and-hold. This corresponds to a 5 V peak-to-peak, 100 kHz sine wave signal.
3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1 LSB over the full operating temperature range.
4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single supply (+5 V) operation with a unipolar full-scale range of 0 to +5 V, and for dual supply (±5 V) operation with a bipolar input range of ±2.5 V. Typical performance characteristics are given for other input ranges.
5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion and slew rate.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7821KN	–40°C to +85°C	±1 max	N-20
AD7821KP	–40°C to +85°C	±1 max	P-20A
AD7821KR	–40°C to +85°C	±1 max	R-20
AD7821BQ	–40°C to +85°C	±1 max	Q-20
AD7821TQ	–55°C to +125°C	±1 max	Q-20
AD7821TE	–55°C to +125°C	±1 max	E-20A

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.

[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7821–SPECIFICATIONS

V_{DD} = +5 V ± 5%, GND = 0 V. Unipolar Input Range: V_{SS} = GND, $V_{REF}(+)$ = 5 V, $V_{REF}(-)$ = GND. Bipolar Input Range: V_{SS} = –5 V ± 5%, $V_{REF}(+)$ = 2.5 V, $V_{REF}(-)$ = –2.5 V. These test conditions apply unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted. Specifications apply for RD Mode (Pin 7 = 0 V).

Parameter	K Version[1]	B, T Versions	Units	Comments
UNIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Total Unadjusted Error[3]	±1	±1	LSB max	
Minimum Resolution for which No Missing Codes are Guaranteed	8	8	Bits	
BIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Zero Code Error	±1	±1	LSB max	
Full Scale Error	±1	±1	LSB max	
Signal-to-Noise Ratio (SNR)[3]	45	45	dB min	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Total Harmonic Distortion (THD)[3]	–50	–50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Peak Harmonic or Spurious Noise[3]	–50	–50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Intermodulation Distortion (IMD)[3]				fa (84.72 kHz) and fb (94.97 kHz) Full-Scale Sine Waves with $f_{SAMPLING}$ = 500 kHz
	–50	–50	dB max	Second Order Terms
	–50	–50	dB max	Third Order Terms
Slew Rate, Tracking[3]	1.6	1.6	V/μs max	
	2.36	2.36	V/μs typ	
REFERENCE INPUT				
Input Resistance	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)/V_{DD}$	$V_{REF}(-)/V_{DD}$	V min/V max	
$V_{REF}(-)$ Input Voltage Range	$V_{SS}/V_{REF}(+)$	$V_{SS}/V_{REF}(+)$	V min/V max	
ANALOG INPUT				
Input Voltage Range	$V_{REF}(-)/V_{REF}(+)$	$V_{REF}(-)/V_{REF}(+)$	V min/ max	
Input Leakage Current	±3	±3	μA max	$-5\ V \le V_{IN} \le +5\ V$
Input Capacitance	55	55	pF typ	
LOGIC INPUTS				
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				
V_{INH}	2.4	2.4	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	μA max	
I_{INL}	–1	–1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
MODE				
V_{INH}	3.5	3.5	V min	
V_{INL}	1.5	1.5	V max	
I_{INH}	200	200	μA max	50 μA typ
I_{INL}	–1	–1	μA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS				
DB0–DB7, $\overline{OFL}$, $\overline{INT}$				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 360 μA
V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	μA max	Floating State Leakage
Output Capacitance[4] (DB0–DB7)	8	8	pF max	Typically 5 pF
RDY				
V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA
I_{OUT}	±3	±3	μA max	Floating State Leakage
Output Capacitance[4]	8	8	pF max	Typically 5 pF
POWER SUPPLY				
I_{DD}[5]	15	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
I_{SS}	100	100	μA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
Power Dissipation	50	50	mW typ	
Power Supply Sensitivity	±1/4	±1/4	LSB max	±1/16 LSB typ, V_{DD} = 4.75 V to 5.25 V, ($V_{REF}(+)$ = 4.75 V max for Unipolar Mode)

NOTES

[1]Temperature Ranges are as follows: K Version = –40°C to +85°C; B Version = –40°C to +85°C; T Version = –55°C to +125°C.

[2]1 LSB = 19.53 mV for both the unipolar (0 V to +5 V) and bipolar (–2.5 V to +2.5 V) input ranges.

[3]See Terminology.

[4]Sample tested at +25°C to ensure compliance.

[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

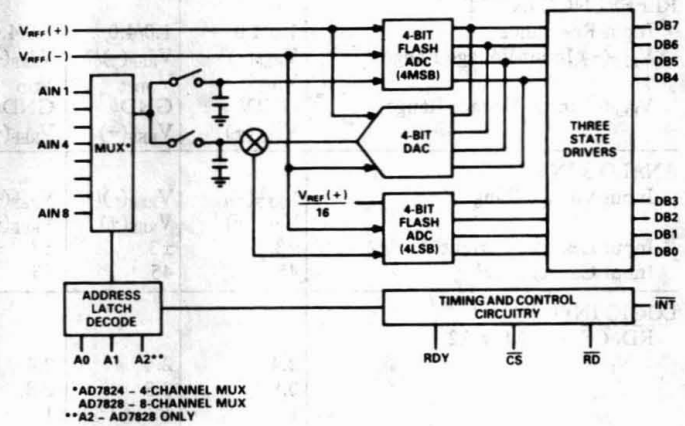
LC²MOS High Speed 4- & 8-Channel 8-Bit ADCs

AD7824/AD7828

FEATURES

4- or 8-Analog Input Channels
Built-In Track/Hold Function
10 kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single +5 V Supply
Low Power: 50 mW
Fast Conversion Rate, 2.5 µs/Channel
Tight Error Specification: 1/2 LSB

FUNCTIONAL BLOCK DIAGRAM



*AD7824 – 4-CHANNEL MUX
AD7828 – 8-CHANNEL MUX
**A2 – AD7828 ONLY

GENERAL DESCRIPTION

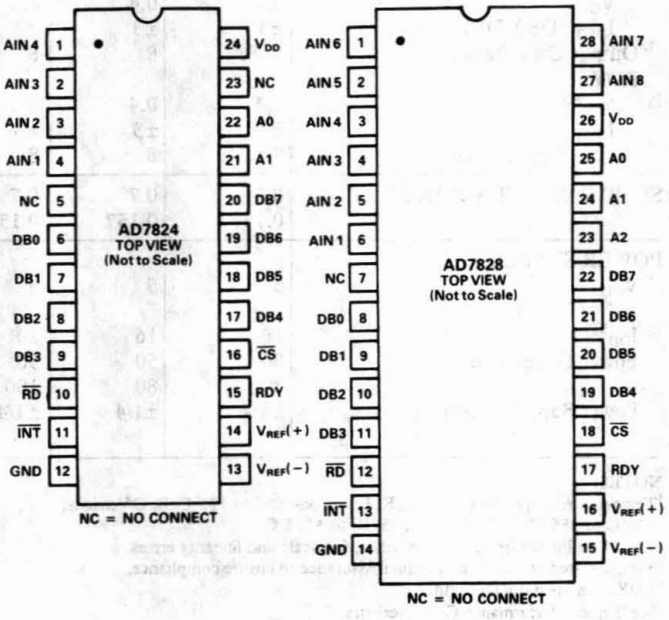
The AD7824 and AD7828 are high-speed, multichannel, 8-bit ADCs with a choice of 4 (AD7824) or 8 (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5 µs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of 10 kHz (157 mV/µs slew rate) on all channels. The AD7824 and AD7828 operate from a single +5 V supply and have an analog input range of 0 V to +5 V, using an external +5 V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select ($\overline{CS}$) and Read ($\overline{RD}$) signals to initiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, Linear-Compatible CMOS process (LC²MOS) and have low power dissipation of 40 mW (typ). The AD7824 is available in a 0.3" wide, 24-pin "skinny" DIP, while the AD7828 is available in a 0.6" wide, 28-pin DIP and in 28-terminal surface mount packages.

PIN CONFIGURATIONS

DIP



PRODUCT HIGHLIGHTS

1. 4- or 8-channel input multiplexer gives cost-effective space-saving multichannel ADC system.
2. Fast conversion rate of 2.5 µs/channel features a per channel sampling frequency of 100 kHz for the AD7824 or 50 kHz for the AD7828.
3. Built-in track-hold function allows handling of 4- or 8-channels up to 10 kHz bandwidth (157 mV/µs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single +5 V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7824/AD7828–SPECIFICATIONS (V_{DD} = +5 V, $V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = GND = 0 V unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted. Specifications apply for Mode 0.)

Parameter	K Version[1]	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which						
No Missing Codes Are Guaranteed	8	8	8	8	Bits	
Channel-to-Channel Mismatch	±1/4	±1/4	±1/4	±1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	$V_{REF}(-)$/ V_{DD}	V min/V max	
$V_{REF}(-)$ Input Voltage Range	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	GND/ $V_{REF}(+)$	V min/V max	
ANALOG INPUT						
Input Voltage Range	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	$V_{REF}(-)$/ $V_{REF}(+)$	V min/V max	
Input Leakage Current	±3	±3	±3	±3	µA max	Analog Input Any Channel
Input Capacitance[3]	45	45	45	45	pF typ	0 V to +5 V
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, A0, A1 & A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	µA max	
I_{INL}	–1	–1	–1	–1	µA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS						
DB0–DB7 & $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360 µA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	±3	±3	µA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5 pF
RDY						
V_{OL}[4]	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6 mA
I_{OUT}	±3	±3	±3	±3	µA max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5 pF
SLEW RATE, TRACKING[3]	0.7	0.7	0.7	0.7	V/µs typ	
	0.157	0.157	0.157	0.157	V/µs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[5]	16	16	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 2.4 V
Power Dissipation	50	50	50	50	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16 LSB typ V_{DD} = 5 V ± 5%

NOTES
[1]Temperature ranges are as follows: K, L Versions; 0°C to +70°C, B, C Versions; –40°C to +85°C, T, U Versions; –55°C to +125°C
[2]Total Unadjusted Error includes offset, full-scale and linearity errors.
[3]Sample tested at +25°C by Product Assurance to ensure compliance.
[4]RDY is an open drain output.
[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Total Unadjusted Error (LSBs)	Package Option[1]
AD7824KN	0°C to +70°C	±1	N-24
AD7824LN	0°C to +70°C	±1/2	N-24
AD7824KR	0°C to +70°C	±1	R-24
AD7824BQ	–40°C to +85°C	±1	Q-24
AD7824CQ	–40°C to +85°C	±1/2	Q-24
AD7824TQ[2]	–55°C to +125°C	±1	Q-24
AD7824UQ[2]	–55°C to +125°C	±1/2	Q-24
AD7828KN	0°C to +70°C	±1	N-28
AD7828LN	0°C to +70°C	±1/2	N-28
AD7828KP	0°C to +70°C	±1	P-28A
AD7828LP	0°C to +70°C	±1/2	P-28A
AD7828BQ	–40°C to +85°C	±1	Q-28
AD7828CQ	–40°C to +85°C	±1/2	Q-28
AD7828BR	–40°C to +85°C	+1	R-28
AD7828BRS	–40°C to +85°C	+1	RS-28
AD7828TQ[2]	–55°C to +125°C	±1	Q-28
AD7828UQ[2]	–55°C to +125°C	±1/2	Q-28
AD7828TE[2]	–55°C to +125°C	±1	E-28A
AD7828UE[2]	–55°C to +125°C	±1/2	E-28A

NOTES
[1]For outline information see Package Information section.
[2]Available to /883B processing only. Contact our local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5692-88764.

ANALOG DEVICES

14-Bit Sampling A/D Converter

AD7851*

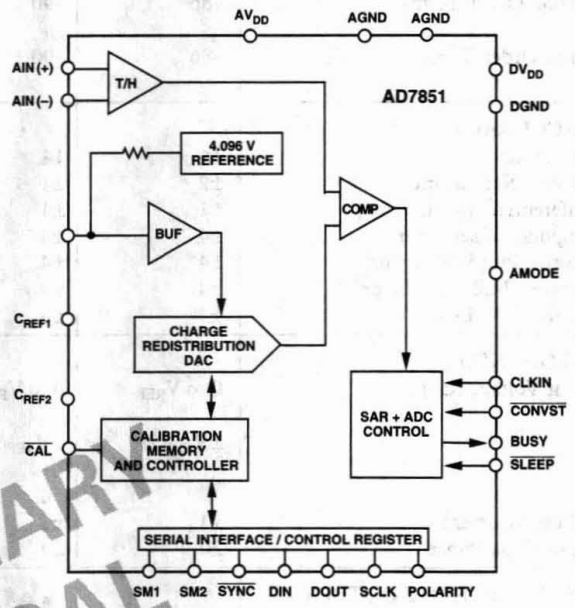
FEATURES

Single 5 V Supply
272 kSPS Throughtput Rate
Pseudo-Diff. Input with Two Input Ranges (AD7851)
System and Self-Calibration with Autocalibration on Power-Up
Read/Write Capability of Calibration Data
Low Power: 60 mW typ
Power-Down Mode: 5 μW typ Power Consumption
Flexible Serial Interface:
8051/SPI/QSPI/μP Compatible
24-Pin DIP, SOIC and SSOP Packages

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7851 is a high speed, 14-bit ADC that operates from a single 5 V power supply. The ADC powers up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and has a number of power-down options for low power applications.

The AD7851 is capable of 272 kHz throughput rate. The input track-and-hold acquires a signal in 0.33 μs and features a pseudo-differential sampling scheme. The AD7851 has the added advantage of two input voltage ranges (0 to V_{REF}, and $-V_{REF}/2$ to $+V_{REF}/2$ centered about $V_{REF}/2$). The input signal range is to V_{DD}, and the part is capable of converting full-power signals to 140 kHz.

CMOS construction ensures low power dissipation (60 mW typ) with power-down mode (5 μW typ). The part is available in 24-pin, 0.3" wide dual-in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.

PRELIMINARY TECHNICAL DATA

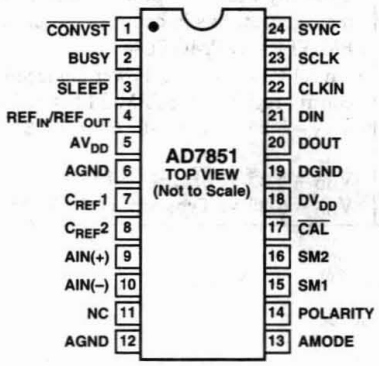
PRODUCT HIGHLIGHTS

1. Single 5 V supply.
2. Operates with reference voltages from 4 V to V_{DD}.
3. Analog input ranges from 0 V to V_{DD}.
4. Self-calibration and System calibration including power-down mode.
5. Versatile serial I/O port.

***Patent pending.**

See Page 35 for data sheet index.

PINOUT FOR DIP, SOIC AND SSOP



ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Package Option[2]
AD7851AN	±2	N-24
AD7851BN	±1	N-24
AD7851AR	±2	R-24
AD7851BR	±1	R-24
AD7851ARS	±2	RS-24
EVAL-AD7851CB[3]		
EVAL-CONTROL BOARD[4]		

NOTES
[1]Linearity error refers to the integral linearity error.
[2]N = Plastic DIP; R = SOIC; RS = SSOP. For outline information see Package Information section.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designators.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD7851–SPECIFICATIONS[1, 2] (AV_{DD} = DV_{DD} = +5.0 V ± 5%, f_{CLKIN} = 6 MHz; f_{SAMPLE} = 272 kHz ; REF_{IN}/REF_{OUT} = 4.096 V; $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A[1]	B[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise+Distortion Ratio[3] (SNR)	80	80	dB min	Typically SNR is 83 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 272 kHz
Total Harmonic Distortion (THD)	–86	–90	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 272 kHz
Peak Harmonic or Spurious Noise	–87	–90	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 272 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	–86	–90	dB typ	fa = 9.983 kHz, fb =10.05 kHz, f_{SAMPLE} = 272 kHz
Third Order Terms	–86	–90	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 272 kHz
DC ACCURACY				
Resolution	14	14	Bits	
Integral Nonlinearity	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed No Missing Codes to 14 Bits
Unipolar Offset Error	±4	±4	LSB max	
Positive Full Scale Error	±4	±4	LSB max	
Negative Full Scale Error	±4	±4	LSB max	
Bipolar Zero Error	±4	±4	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) can be biased up but AIN(+) cannot go below AIN(–).
	$\pm V_{REF}/2$	$\pm V_{REF}/2$	Volts	i.e., AIN(+) – AIN(–) = $-V_{REF}/2$ to $+V_{REF}/2$, AIN(–) should be biased up and AIN(+) can go below AIN(–) but cannot go below 0 V.
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	$4/V_{DD}$	$4/V_{DD}$	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	Resistor Connected to Internal Reference Node
REF_{OUT} Output Voltage	4.096	4.096	V nom	
REF_{OUT} Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
CONVERSION RATE				
Conversion Time	3.33	3.33	µs max	20 CLKIN Cycles
Track/Hold Acquisition Time	0.33	0.33	µs max	
POWER REQUIREMENTS				
AV_{DD}, DV_{DD}	+4.75/+5.25	+4.75/+5.25	V min/max	
I_{DD}				
Normal Mode[5]	15	15	mA max	AV_{DD} = DV_{DD} = 4.75 V to 5.25 V. Typically 12 mA
Sleep Mode[6]				
With External Clock On	10	10	µA typ	Full Power-Down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	400	400	µA typ	Partial power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
With External Clock Off	5	5	µA max	Typically 1 µA. Full power down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 0.
	200	200	µA typ	Partial Power-Down. Power management bits in control register set as PMGT1 = 1, PMGT0 = 1.
Normal Mode Power Dissipation	78.75	78.75	mW max	V_{DD} = 5.25 V: Typically 60 mW; $\overline{SLEEP}$ = V_{DD}
Sleep Mode Power Dissipation				
With External Clock On	52.5	52.5	µW typ	V_{DD} = 5.25 V; $\overline{SLEEP}$ = 0 V
With External Clock Off	26.25	26.25	µW max	V_{DD} = 5.25 V: Typically 5.25 µW; $\overline{SLEEP}$ = 0 V

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

3 V to 5 V Single Supply, 200 kSPS 12-Bit Sampling ADCs

AD7853/AD7853L*

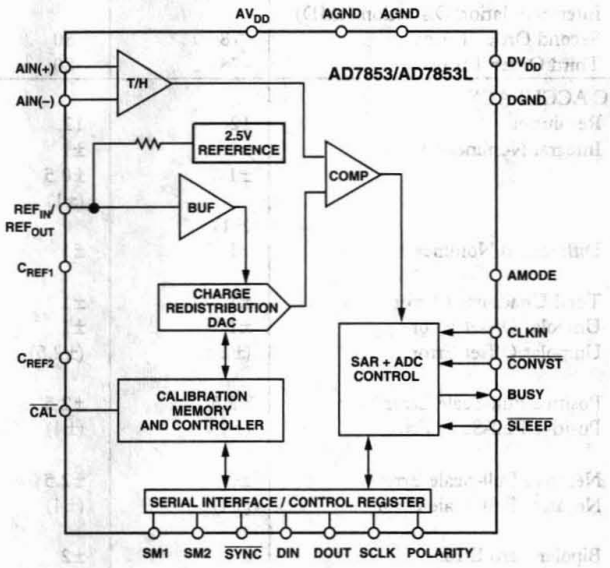
FEATURES

Specified for V_{DD} of 3 V to 5.5 V
Read-Only Operation
AD7853–200 kSPS; AD7853L–100 kSPS
System and Self-Calibration with Autocalibration on Power-Up
Low Power:
AD7853: 15 mW (V_{DD} = 3 V)
AD7853L: 5.5 mW (V_{DD} = 3 V)
Automatic Power Down After Conversion (25 μW)
Flexible Serial Interface:
8051/SPI/QSPI/μP Compatible
24-Pin DIP, SOIC and SSOP Packages

APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Pen Computers
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7853/AD7853L are high speed, low power, 12-bit ADCs that operate from a single 3 V or 5 V power supply, the AD7853 being optimized for speed and the AD7853L for low power. The ADC powers up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system-calibration options to ensure accurate operation over time and temperature and have a number of power-down options for low power applications. The part powers up with a set of default conditions and can operate as a read only ADC.

The AD7853 is capable of 200 kHz throughput rate while the AD7853L is capable of 100 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7853/AD7853L voltage range is 0 to V_{REF} with both straight binary and 2s complement output coding. Input signal range is to the supply, and the part is capable of converting full power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6 μW in power-down mode. The part is available in 24-pin, 0.3 inch wide dual-in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.

PRODUCT HIGHLIGHTS

1. Specified for 3 V and 5 V supplies.
2. Automatic calibration on power-up.
3. Flexible power management options including automatic power-down after conversion.
4. Operates with reference voltages from 1.2 V to V_{DD}.
5. Analog input ranges from 0 V to V_{DD}.
6. Self and system calibration.
7. Versatile serial I/O port (SPI/QSPI/8051/μP).
8. Lower power version AD7853L.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Power Dissipation (mW)	Package Option[2]
AD7853AN	±1	20	N-24
AD7853BN	±1/2	20	N-24
AD7853LAN[3]	±1	6.85	N-24
AD7853LBN[3]	±1	6.85	N-24
AD7853AR	±1	20	R-24
AD7853BR	±1/2	20	R-24
AD7853LAR[3]	±1	6.85	R-24
AD7853LBR[3]	±1	6.85	R-24
AD7853LARS[3]	±1	6.85	RS-24
EVAL-AD7853CB[4]			
EVAL-CONTROL BOARD[5]			

NOTES
[1]Linearity error refers to the integral linearity error.
[2]N = Plastic DIP; R = SOIC; RS = SSOP. For outline information see Package Information section.
[3]L signifies the low power version.
[4]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[5]This board is a complete unit allowing a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designators.

*Patent pending.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7853/AD7853L–SPECIFICATIONS[1, 2]

(AV_{DD} = DV_{DD} = +3.0 V to +5.5 V, REF_{IN}/REF_{OUT} = 2.5 V External Reference, f_{CLKIN} = 4 MHz (1.8 MHz B Grade (0°C to +70°C), 1 MHz A and B Grades (–40°C to +85°C) for L Version); f_{SAMPLE} = 200 kHz (AD7853) 100 kHz (AD7853L); $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) Specifications in () apply to the AD7853L.

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[3] (SNR)	70	71	dB min	Typically SNR is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)
Total Harmonic Distortion (THD)	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)
Peak Harmonic or Spurious Noise	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)
Intermodulation Distortion (IMD)				
Second Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)
Third Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1	LSB max	2.5 V External Reference V_{DD} = 3 V, V_{DD} = 5 V (B Grade Only)
	±1	±0.5	LSB max	5 V External Reference V_{DD} = 5 V
		(±1)	LSB max	(L Version, 5 V External Reference, V_{DD} = 5 V)
	(±1)		LSB max	(L Version)
Differential Nonlinearity	±1	±1	LSB max	Guaranteed No Missed Codes to 12 Bits. 2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V
Total Unadjusted Error	±1	±1	LSB typ	
Unipolar Offset Error	±1	±1	LSB max	2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V
Unipolar Offset Error	(±2.5)	(±2.5)	LSB max	(L Versions, 2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V)
Positive Full-Scale Error	±2.5	±2.5	LSB max	2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V
Positive Full-Scale Error	(±4)	(±4)	LSB max	(L Versions, 2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V)
Negative Full-Scale Error	±2.5	±2.5	LSB max	2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V
Negative Full-Scale Error	(±4)	(±4)	LSB max	(L Versions, 2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V)
Bipolar Zero Error	±2	±2	LSB max	2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V
Bipolar Zero Error	(±2.5)	(±2.5)	LSB max	(L Versions, 2.5 V External Reference V_{DD} = 3 V, 5 V External Reference V_{DD} = 5 V)
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) can be biased up but AIN(+) cannot go below AIN(-)
	$\pm V_{REF}/2$	$\pm V_{REF}/2$	Volts	i.e., AIN(+) – AIN(–) = $-V_{REF}/2$ to $+V_{REF}/2$, AIN(–) should be biased to $+V_{REF}/2$ and AIN(+) can go below AIN(–) but cannot go below 0 V
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	$2.3/V_{DD}$	$2.3/V_{DD}$	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	
REF_{OUT} Output Voltage	2.3/2.7	2.3/2.7	V min/max	
REF_{OUT} Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}				
	2.4	2.4	V min	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	2.1	2.1	V min	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Input Low Voltage, V_{INL}				
	0.8	0.8	V max	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	0.6	0.6	V max	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Input Current, I_{IN}	±10	±10	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}				I_{SOURCE} = 200 µA
	4	4	V min	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	2.4	2.4	V min	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			Unipolar Input Range
	2s Complement			Bipolar Input Range
CONVERSION RATE				
Conversion Time	4.6 (18)	4.6 (18)	µs max	(L Versions Only, –40°C to +85°C, 1 MHz CLKIN)
		(10)	µs max	(L Versions Only, 0°C to +70°C, 1.8 MHz CLKIN)
Track/Hold Acquisition Time	0.4 (1)	0.4 (1)	µs min	(L Versions Only)

Specifications subject to change without notice.

3 V to 5 V Single Supply, 200 kSPS 12-Bit Sampling ADCs

AD7854/AD7854L*

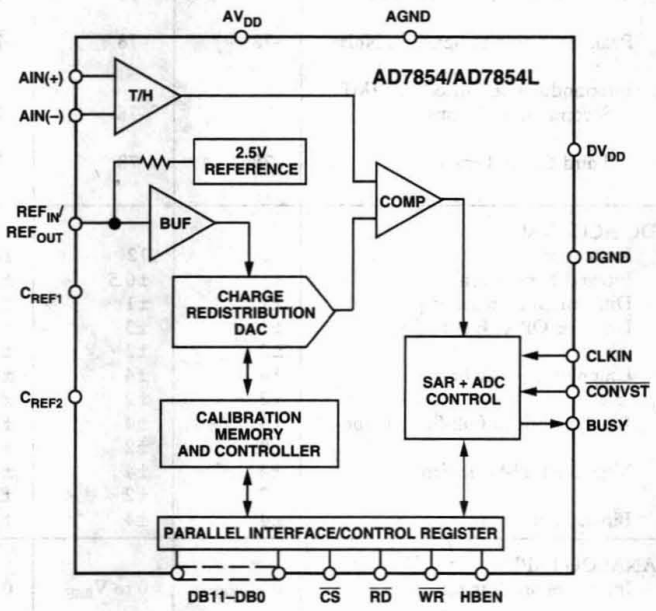
FEATURES

Specified for V_{DD} of 3 V to 5.5 V
Read-Only Operation
AD7854–200 kSPS; AD7854L–100 kSPS
System and Self-Calibration
Low Power
Normal Operation
AD7854: 15 mW (V_{DD} = 3 V)
AD7854L: 5.5 mW (V_{DD} = 3 V)
Automatic Power-Down After Conversion (25 μW)
AD7854: 1.3 mW 10 kSPS
AD7854L: 650 μW 10 kSPS
Flexible Parallel Interface
12-Bit Parallel/8-Bit Parallel (AD7854)
28-Pin DIP, SOIC and SSOP Packages (AD7854)

APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Pen Computers
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7854/AD7854L is a high speed, low power, 12-bit ADC that operates from a single 3 V or 5 V power supply, the AD7854 being optimized for speed and the AD7854L for low power. The ADC powers up with a set of default conditions at which time it can be operated as a read-only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and has a number of power-down options for low power applications.

The AD7854 is capable of 200 kHz throughput rate while the AD7854L is capable of 100 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7854 and AD7854L input voltage range is 0 to V_{REF} (unipolar) and $-V_{REF}/2$ to $+V_{REF}/2$, centered at $V_{REF}/2$ (bipolar). The coding is straight binary in unipolar mode and twos complement in bipolar mode. Input signal range is to the supply and the part is capable of converting full-power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6 μW in power-down mode. The part is available in 28-pin, 0.6 inch wide dual-in-line package (DIP), 28-lead small outline (SOIC) and 28-lead small shrink outline (SSOP) packages.

***Patent pending.**

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)	Power Dissipation (mW)	Package Option*
AD7854AQ	–40°C to +85°C	1	15	Q-28
AD7854SQ	–55°C to +125°C	1	15	Q-28
AD7854AR	–40°C to +85°C	1	15	R-28
AD7854BR	–40°C to +85°C	1/2	15	R-28
AD7854ARS	–40°C to +85°C	1	15	RS-28
AD7854LAQ	–40°C to +85°C	1	5.5	Q-28
AD7854LAR	–40°C to +85°C	1	5.5	R-28
AD7854LARS	–40°C to +85°C	1	5.5	RS-28
EVAL-AD7854CB				
EVAL-CONTROL BOARD				

*For outline information see Package Information section.

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AD7854/AD7854L–SPECIFICATIONS

(AV_{DD} = DV_{DD} = +3.0 V to +5.5 V, REF_{IN}/REF_{OUT} = 2.5 V External Reference, f_{CLKIN} = 4 MHz (for L Version: 1.8 MHz (0°C to +70°C) and 1 MHz (–40°C to +85°C)); f_{SAMPLE} = 200 kHz (AD7854), 100 kHz (AD7854L); $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) Specifications in () apply to the AD7854L.

Parameter	A Version[1]	B Version[1]	S Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Signal to Noise + Distortion Ratio (SNR)	70	71	70	dB min	Typically SNR is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Total Harmonic Distortion (THD)	–78	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Peak Harmonic or Spurious Noise	–78	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Intermodulation Distortion (IMD)					
Second Order Terms	–78	–78	–78	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Third Order Terms	–78	–78	–78	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
DC ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity	±1	±0.5	±1	LSB max	5 V Reference V_{DD} = 5 V
Differential Nonlinearity	±1	±1	±1	LSB max	Guaranteed No Missed Codes to 12 Bits
Unipolar Offset Error	±3	±3	±4	LSB max	
	±2	±2	±2	LSB typ	
Unipolar Gain Error	±4	±4	±4	LSB max	
	±2	±2	±2	LSB typ	
Bipolar Positive Full-Scale Error	±4	±4	±5	LSB max	
	±2	±2	±2	LSB typ	
Negative Full-Scale Error	±4	±4	±5	LSB max	
	±2	±2	±2	LSB typ	
Bipolar Zero Error	±4	±4	±5	LSB max	
ANALOG INPUT					
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) can be biased up but AIN(+) cannot go below AIN(–).
	$\pm V_{REF}/2$	$\pm V_{REF}/2$	$\pm V_{REF}/2$	Volts	i.e., AIN(+) – AIN(–) = $-V_{REF}/2$ to $+V_{REF}/2$, AIN(–) should be biased to $+V_{REF}/2$ and AIN(+) can go below AIN(–) but cannot go below 0 V.
Leakage Current	±1	±1	±1	µA max	
Input Capacitance	20	20	20	pF typ	
REFERENCE INPUT/OUTPUT					
REF_{IN} Input Voltage Range	2.3/V_{DD}	2.3/V_{DD}	2.3/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	150	150	150	kΩ typ	
REF_{OUT} Output Voltage	2.3/2.75	2.3/2.7	2.3/2.7	V min/max	
REF_{OUT} Tempco	20	20	20	ppm/°C typ	
LOGIC INPUTS					
Input High Voltage, V_{INH}	3	3	3	V min	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	2.1	2.1	2.1	V min	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Input Low Voltage, V_{INL}	0.4	0.4	0.4	V max	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	0.6	0.6	0.6	V max	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Input Current, I_{IN}	±10	±10	±10	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}					I_{SOURCE} = 200 µA
	4	4	4	V min	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	2.4	2.4	2.4	V min	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance	10	10	10	pF max	
Output Coding	Straight (Natural) Binary				Unipolar Input Range
	Twos Complement				Bipolar Input Range
CONVERSION RATE					t_{CLKIN} × 18
Conversion Time	4.6 (10)	4.6 (9)	4.6 (9)	µs max	(L Versions Only, 0°C to +70°C, 1.8 MHz CLKIN)
Track/Hold Acquisition Time	0.5 (1)	0.5 (1)	0.5 (1)	µs min	(L Versions Only, –40°C to +85°C, 1 MHz CLKIN)
POWER REQUIREMENTS					
See AD7859/AD7859L data sheet Power Requirements Specifications					

Specifications subject to change without notice.

3 V to 5 V Single Supply, 200 kSPS 8-Channel, 12-Bit Sampling ADCs

AD7858/AD7858L*

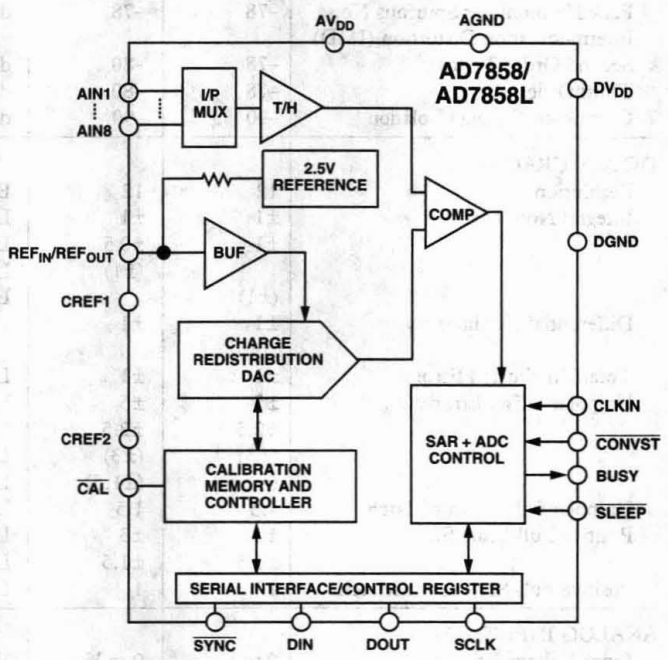
FEATURES

- Specified for V_{DD} of 3 V to 5.5 V
- AD7858—200 kSPS; AD7858L—100 kSPS
- System and Self-Calibration with Autocalibration on Power-Up
- Eight Single-Ended or Four Pseudo-Differential Inputs
- Low Power
  - AD7858: 15 mW (V_{DD} = 3 V)
  - AD7858L: 5.5 mW (V_{DD} = 3 V)
- Automatic Power Down After Conversion (25 μW)
- Flexible Serial Interface:
  - 8051/SPI/QSPI/μP Compatible
- 24-Pin DIP, SOIC and SSOP Packages

APPLICATIONS

- Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
- Pen Computers
- Instrumentation and Control Systems
- High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7858/AD7858L are high speed, low power, 12-bit ADCs that operate from a single 3 V or 5 V power supply, the AD7858 being optimized for speed and the AD7858L for low power. The ADC powers up with a set of default conditions at which time it can be operated as a read only ADC. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and have a number of power-down options for low power applications. The part powers up with a set of default conditions and can operate as a read only ADC.

The AD7858 is capable of 200 kHz throughput rate while the AD7858L is capable of 100 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7858/AD7858L voltage range is 0 to V_{REF} with both straight binary and 2s complement output coding. Input signal range is to the supply and the part is capable of converting full power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6 μW in power-down mode. The part is available in 24-pin, 0.3 inch-wide dual-in-line package (DIP), 24-lead small outline (SOIC) and 24-lead small shrink outline (SSOP) packages.

PRODUCT HIGHLIGHTS

1. Specified for 3 V and 5 V supplies.
2. Automatic calibration on power-up.
3. Flexible power management options including automatic powerdown after conversion.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Power Dissipation (mW)	Package Option[2]
AD7858AN	±1	20	N-24
AD7858BN	±1/2	20	N-24
AD7858LAN[3]	±1	6.85	N-24
AD7858LBN[3]	±1	6.85	N-24
AD7858AR	±1	20	R-24
AD7858BR	±1/2	20	R-24
AD7858LAR[3]	±1	6.85	R-24
AD7858LBR[3]	±1	6.85	R-24
AD7858LARS[3]	±1	6.85	RS-24
EVAL-AD7858CB[4]			
EVAL-CONTROL BOARD[5]			

NOTES
[1]Linearity error here refers to integral linearity error.
[2]N = Plastic DIP; R = SOIC; RS = SSOP. For outline information see Package Information section.
[3]L signifies the low power version.
[4]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[5]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

*Patent pending.

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AD7858/AD7858L–SPECIFICATIONS[1, 2]

(AV_{DD} = DV_{DD} = +3.0 V to +5.5 V, REF_{IN}/REF_{OUT} = 2.5 V External Reference unless otherwise noted, f_{CLKIN} = 4 MHz (1.8 MHz B Grade (0°C to +70°C), 1 MHz A and B Grades (–40°C to +85°C) for L Version); f_{SAMPLE} = 200 kHz (AD7858), 100 kHz (AD7858L); $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) Specifications in ( ) apply to the AD7858L.

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[3] (SNR)	70	71	dB min	Typically SNR is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)
Total Harmonic Distortion (THD)	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)
Peak Harmonic or Spurious Noise	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (100 kHz)
Intermodulation Distortion (IMD)				
Second Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)
Third Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (100 kHz)
Channel-to-Channel Isolation	–90	–90	dB typ	V_{IN} = 25 kHz
DC ACCURACY				Any Channel
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1	LSB max	2.5 V External Reference V_{DD} = 3 V, V_{DD} = 5 V (B Grade Only)
	±1	±0.5	LSB max	5 V External Reference V_{DD} = 5 V
		(±1)	LSB max	(L Version, 5 V External Reference, V_{DD} = 5 V)
	(±1)		LSB max	(L Version)
Differential Nonlinearity	±1	±1	LSB max	Guaranteed No Missed Codes to 12 Bits. 2.5 V External Reference V_{DD} = 3 V, 5 V External Reference, V_{DD} = 5 V
Total Unadjusted Error	±1	±1	LSB typ	
Unipolar Offset Error	±5	±5	LSB max	Typically ±2 LSBs
	±2.5	±2.5	LSB max	5 V External Reference, V_{DD} = 5 V
	(±3)	(±3)	LSB max	(L Version)
	(±1.5)	(±1.5)	LSB max	(L Version, 5 V External Reference, V_{DD} = 5 V)
Unipolar Offset Error Match	1.5	1.5	LSB max	
Positive Full-Scale Error	±3	±3	LSB max	
	±1.5	±1.5	LSB max	5 V External Reference, V_{DD} = 5 V
Positive Full-Scale Error Match	1	1	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) can be biased up but AIN(+) cannot go below AIN(–)
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	2.3/V_{DD}	2.3/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	
REF_{OUT} Output Voltage	2.3/2.7	2.3/2.7	V min/max	
REF_{OUT} Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	2.1	2.1	V min	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Input Low Voltage, V_{INL}	0.8	0.8	V max	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	0.6	0.6	V max	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Input Current, I_{IN}	±10	±10	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}				I_{SOURCE} = 200 µA
	4	4	V min	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V
	2.4	2.4	V min	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8 mA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	4.6 (18)	4.6	µs max	(L Versions Only, –40°C to +85°C, 1 MHz CLKIN)
		(10)	µs max	(L Versions Only, 0°C to +70°C, 1.8 MHz CLKIN)
Track/Hold Acquisition Time	0.4 (1)	0.4 (1)	µs min	(L Versions Only)

Specifications subject to change without notice.

3 V to 5 V Single Supply, 200 kSPS 8-Channel, 12-Bit Sampling ADCs

AD7859/AD7859L*

FEATURES

Specified for V_{DD} of 3 V to 5.5 V
AD7859–200 kSPS; AD7859L–100 kSPS
System and Self-Calibration
Low Power
Normal Operation
AD7859: 15 mW (V_{DD} = 3 V)
AD7859L: 5.5 mW (V_{DD} = 3 V)
Using Automatic Power-Down After Conversion (25 μW)
AD7859: 1.3 mW (V_{DD} = 3 V 10 kSPS)
AD7859L: 650 μW (V_{DD} = 3 V 10 kSPS)
Flexible Parallel Interface:
16-Bit Parallel/8-Bit Parallel
44-Pin PQFP and PLCC Packages

APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Pen Computers
Instrumentation and Control Systems
High Speed Modems

GENERAL DESCRIPTION

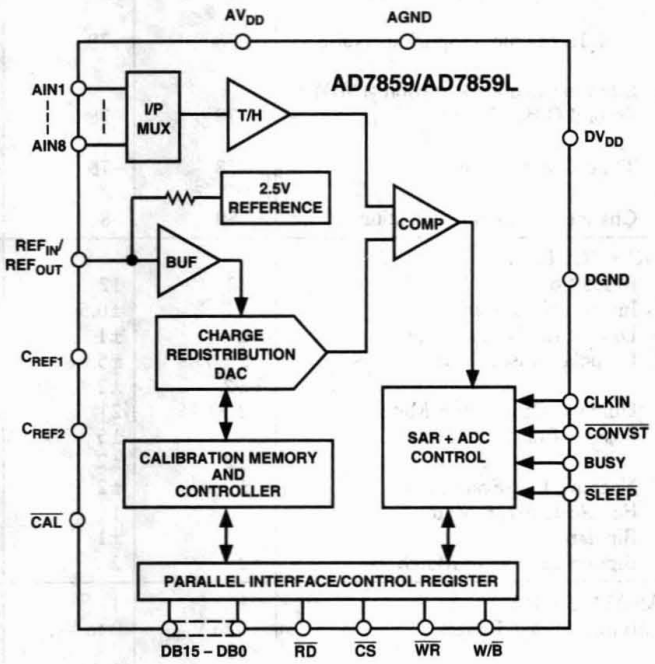
The AD7859/AD7859L are high speed, low power, 8-channel, 12-bit ADCs which operate from a single 3 V or 5 V power supply, the AD7859 being optimized for speed and the AD7859L for low power. The ADC contains self-calibration and system calibration options to ensure accurate operation over time and temperature and have a number of power-down options for low power applications.

The AD7859 is capable of 200 kHz throughput rate while the AD7859L is capable of 100 kHz throughput rate. The input track-and-hold acquires a signal in 500 ns and features a pseudo-differential sampling scheme. The AD7859 and AD7859L input voltage range is 0 to V_{REF} (unipolar) and $-V_{REF}/2$ to $+V_{REF}/2$ about $V_{REF}/2$ (bipolar) with both straight binary and 2s complement output coding respectively. Input signal range is to the supply and the part is capable of converting full-power signals to 100 kHz.

CMOS construction ensures low power dissipation of typically 5.4 mW for normal operation and 3.6 μW in power-down mode. The part is available in 44-pin, plastic quad flatpack package (PQFP) and plastic lead chip carrier (PLCC).

*Patent pending.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Operation with either 3 V or 5 V power supplies.
2. Flexible power management options including automatic power-down after conversion.
3. By using the power management options a superior power performance at slower throughput rates can be achieved.
   AD7859: 1 mW typ @ 10 kSPS
   AD7859L: 1 mW typ @ 20 kSPS
4. Operates with reference voltages from 1.2 V to the supply.
5. Analog input ranges from 0 V to V_{DD}.
6. Self and system calibration.
7. Versatile parallel I/O port.
8. Lower power version AD7859L.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Power Dissipation (mW)	Package Option[2]
AD7859AP	±1	15	P-44A
AD7859AS	±1	15	S-44
AD7859BS	±1/2	15	S-44
AD7859LAS	±1	5.5	S-44
EVAL-AD7859CB EVAL-CONTROL BOARD			

[2]For outline information see Package Information section.

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AD7859/AD7859L–SPECIFICATIONS

(AV_{DD} = DV_{DD} = +3.0 V to +5.5 V, REF_{IN}/REF_{OUT} = 2.5 V External Reference, f_{CLKIN} = 4 MHz (for L Version: 1.8 MHz (0°C to +70°C) and 1 MHz (–40°C to +85°C)); f_{SAMPLE} = 200 kHz (AD7859) 100 kHz (AD7859L); $\overline{SLEEP}$ = Logic High; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) Specifications in () apply to the AD7859L.

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio (SNR)	70	71	dB min	Typically SNR is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (for L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Total Harmonic Distortion (THD)	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (for L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Peak Harmonic or Spurious Noise	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz (for L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Intermodulation Distortion (IMD)				
Second Order Terms	–78	–78	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (for L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Third Order Terms	–78	–78	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz (for L Version: f_{SAMPLE} = 100 kHz @ f_{CLKIN} = 2 MHz)
Channel-to-Channel Isolation	–80	–80	dB typ	V_{IN} = 25 kHz
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±0.5	LSB max	5 V Reference V_{DD} = 5 V
Differential Nonlinearity	±1	±1	LSB max	Guaranteed No Missed Codes to 12 Bits
Unipolar Offset Error	±5	±5	LSB max	
	±2	±2	LSB typ	
Unipolar Offset Error Match	2(3)	2	LSB max	
Positive Full-Scale Error	±5	±5	LSB max	
	±2	±2	LSB typ	
Negative Full-Scale Error	±2	±2	LSB typ	
Full-Scale Error Match	1	1	LSB max	
Bipolar Zero Error	±1	±1	LSB typ	
Bipolar Zero Error Match	2	2	LSB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	i.e., AIN(+) – AIN(–) = 0 to V_{REF}, AIN(–) Can Be Biased Up But AIN(+) Cannot Go Below AIN(–)
	$\pm V_{REF}/2$	$\pm V_{REF}/2$	Volts	i.e., AIN(+) – AIN(–) = $-V_{REF}/2$ to $+V_{REF}/2$, AIN(–) Should Be Biased to $+V_{REF}/2$ and AIN(+) Can Go Below AIN(–) But Cannot Go Below 0 V
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	$2.3/V_{DD}$	$2.3/V_{DD}$	V min/max	Functional from 1.2 V
Input Impedance	150	150	kΩ typ	
REF_{OUT} Output Voltage	2.3/2.75	2.3/2.7	V min/max	
REF_{OUT} Tempco	20	20	ppm/°C typ	
CONVERSION RATE				$t_{CLKIN} \times 18$
Conversion Time	4.5 (10)	4.5	µs max	(L Versions Only, 0°C to +70°C, 1.8 MHz CLKIN)
Track/Hold Acquisition Time	0.5 (1)	0.5	µs min	(L Versions Only, –40°C to +85°C, 1 MHz CLKIN)
POWER REQUIREMENTS				
AV_{DD}, DV_{DD}	+3.0/+5.5	+3.0/+5.5	V min/max	
I_{DD}				
Normal Mode	5.5 (1.95)	5.5	mA max	AV_{DD} = DV_{DD} = 4.5 V to 5.5 V. Typically 4.5 mA
	5.5 (1.95)	5.5	mA max	AV_{DD} = DV_{DD} = 3.0 V to 3.6 V. Typically 4.0 mA
Sleep Mode				
With External Clock On	10	10	µA typ	Full Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 0.
	400	400	µA typ	Partial Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 1.
With External Clock Off	5	5	µA max	Typically 1 µA. Full Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 0.
	200	200	µA typ	Partial Power-Down. Power Management Bits in Control Register Set as PMGT1 = 1, PMGT0 = 1.
LOGIC OUTPUT/INPUTS				
See AD7854/AD7854L data sheet Logic Output/Input Specifications.				

Specifications subject to change without notice.

11-Bit Resolution Simultaneous Sampling A/D Converter

AD7861

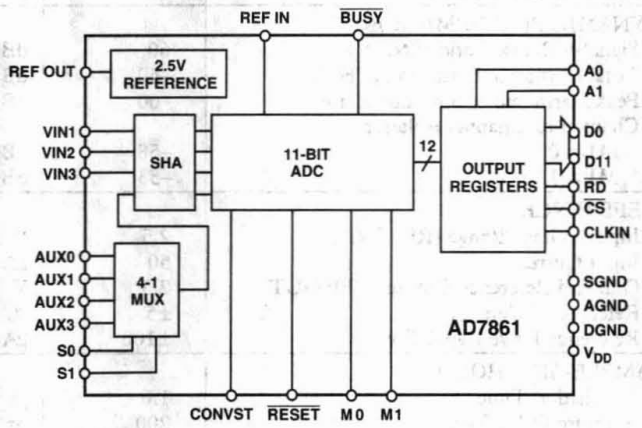
FEATURES

11-Bit Resolution Analog-to-Digital Converter
7 Single-Ended Analog Inputs
4 Input Channels Simultaneously Sampled
Expansion with 4 Multiplexed Inputs
Internal 2.5 V Reference
3.2 µs Conversion Time per Channel
User Definable Channel Sequencing
Single Supply +5 V Operation
Double Buffered Register Outputs
6.25 MHz to 12.5 MHz Operating Clock Range

APPLICATIONS

Motor Control
3-Phase Power Measurement
Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7861 is a multichannel simultaneous sampling A/D Converter (ADC) configured for the acquisition of voltage inputs in a motor control solution or three-phase power system.

The AD7861 combined with Analog Devices' 16-bit fixed-point digital signal processor (DSP) provides a low cost 16-bit fixed-point microcontroller solution.

The input stage has been designed to accommodate the types of signals frequently found in motor drives. The VIN1, VIN2, and VIN3 channels are simultaneously sampled inputs suitable for stator current acquisition. The AUX0–AUX3 channels are multiplexed and are suitable for slower moving inputs such as temperature and bus voltage of the diode rectifier output in a motor control application.

PRODUCT HIGHLIGHTS

Simultaneous Sampling of Four Inputs

Four channel sample and hold amplifier (SHA) allows out of phase input signals to be sampled simultaneously, preserving the relative phase information. Sample-and-hold acquisition time is 1.6 µs and conversion time per channel is 3.2 µs (using a 12.5 MHz system clock).

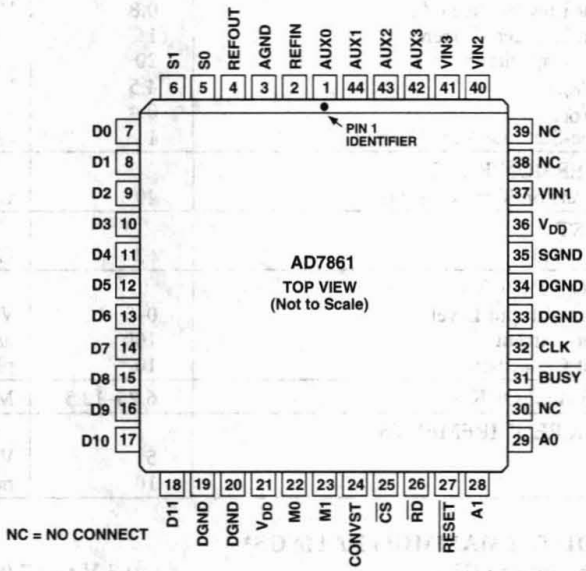
Flexible Analog Channel Sequencing

AD7861 supports acquisition of 2, 3 or 4 channels per group. Converted channel results are stored in registers and the data can be read in any order. The sampling and conversion time for two channels is 8 µs, three channels is 11.2 µs, and four channels is 14.4 µs (using a 12.5 MHz system clock).

Single 5 V dc Operation

Low power, digital process.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7861AP	–40°C to +85°C	P-44A

*For outline information see Package Information section.

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AD7861–SPECIFICATIONS (V_{DD} = 5 V ± 5%; T_A = –40°C to +85°C; REFIN = 2.5 V; Ext CLK @ 12.5 MHz, unless otherwise noted)

Parameter	AD7861AP	Units	Conditions/Comments
DC ACCURACY			
Resolution	11	Bits	Twos Complement Data Format
Relative Accuracy	±2	LSB max	Integral Nonlinearity
Differential Nonlinearity	±2.5	LSB max	No Missing Codes Guaranteed
Bias Offset Error	±9	LSB max	Any Channel
Bias Offset Error Match	4	LSB max	Between Channels
Full-Scale Error	±13	LSB max	Any Channel
Full-Scale Error Match	4	LSB max	Between Channels
DYNAMIC PERFORMANCE			
Signal-to-Noise Ratio (SNR)	60	dB min	f_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 75 kHz
Total Harmonic Distortion (THD)	–60	dB max	f_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 75 kHz
Peak Harmonic or Spurious Noise	–60	dB max	f_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 75 kHz
Channel-to-Channel Isolation			
M1 = 0	–58	dB max	1 kHz Sine Wave Applied to Unselected Channels
M1 = 1	–53	dB max	1 kHz Sine Wave Applied to Unselected Channels
REFERENCE			
Input Voltage Range (REF IN)	2.5	V	
Input Current	50	µA max	
Onboard Reference Output (REF OUT)	2.5	V	
Reference Tolerance	±5	%	
Reference Drive Capability	±100	µA max	
SAMPLE-AND-HOLD			
Acquisition Time	1.6	µs	20 CLK Cycles @ 12.5 MHz
Aperture Delay Time	200	ns max	
Aperture Delay Time Match	20	ns max	
Droop Rate	5	mV/ms max	
LOGIC			
Input High Voltage (V_{IH})	2	V min	
Input Low Voltage (V_{IL})	0.8	V max	
Input Leakage Current	1	µA max	
Input Capacitance	20	pF typ	
(V_{OH})	4.5	V min	I_{SOURCE} Current = 20 µA, V_{DD} = 5 V
(V_{OL})	0.4	V max	I_{SINK} Current = 400 µA, V_{DD} = 5 V
Three-State Leakage Current	1	µA max	
CONVERSION RATE			
Conversion Time/Channel	40	CLK Cycles	
CONVST			
Pulse Width	2	CLK Cycles min	
ANALOG INPUTS			
Nominal Input Level	0–5	V	VIN1, VIN2, VIN3, AUX0–AUX3
Input Current	100	µA	
Input Capacitance	10	pF	
SYSTEM CLOCK	6.25–12.5	MHz	
POWER REQUIREMENTS			
V_{DD}	5	V dc	
I_{DD}	10	mA max	

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) ..... –0.3 V to +7.0 V
Digital Input Voltage ..... –0.3 V to V_{DD}
Analog Input Voltage ..... –0.3 V to V_{DD}
Analog Reference Input Voltage ..... –0.3 V to V_{DD}
Digital Output Voltage Swing ..... –0.3 V to V_{DD}
Analog Reference Output Swing ..... –0.3 V to V_{DD}
Operating Temperature ..... –40°C to +85°C
Lead Temperature (Soldering, 10 sec) ..... +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7861 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ANALOG DEVICES

LC²MOS Complete, 12-Bit Analog I/O System

AD7868

FEATURES

Complete 12-Bit I/O System, Comprising:
- **12-Bit ADC with Track/Hold Amplifier**
  - **83 kHz Throughput Rate**
  - **72 dB SNR**
- **12-Bit DAC with Output Amplifier**
  - **3 μs Settling Time**
  - **72 dB SNR**
- **On-Chip Voltage Reference**

Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3" Wide DIP

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

GENERAL DESCRIPTION

The AD7868 is a complete 12-bit I/O system containing a DAC and an ADC. The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 3 μs to 12 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines. Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7868 operates from ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

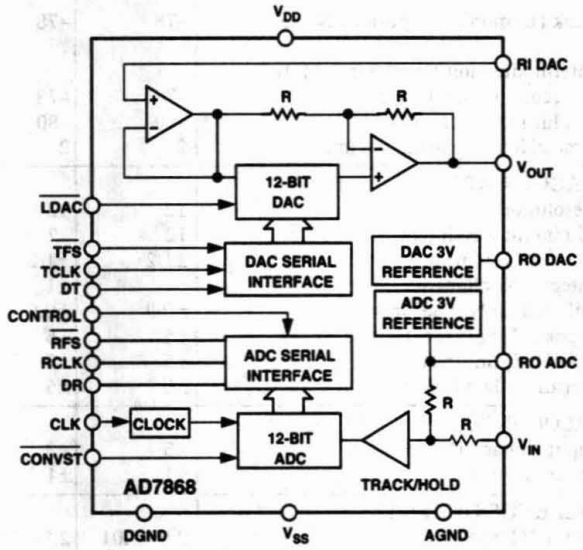
The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

ORDERING GUIDE

Model	Temperature Range	SNR	Relative Accuracy (LSB)	Package Option*
AD7868AN	–40°C to +85°C	70 dB	±1/2 typ	N-24
AD7868AQ	–40°C to +85°C	70 dB	±1/2 typ	Q-24
AD7868BN	–40°C to +85°C	72 dB	±1 max	N-24
AD7868BQ	–40°C to +85°C	72 dB	±1 max	Q-24
AD7868AR	–40°C to +85°C	70 dB	±1/2 typ	R-28
AD7868BR	–40°C to +85°C	72 dB	±1 max	R-28

NOTES
*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline IC).
For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM

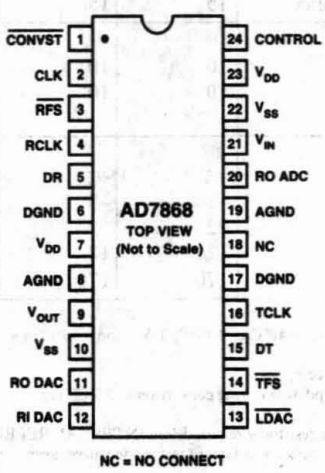


PRODUCT HIGHLIGHTS

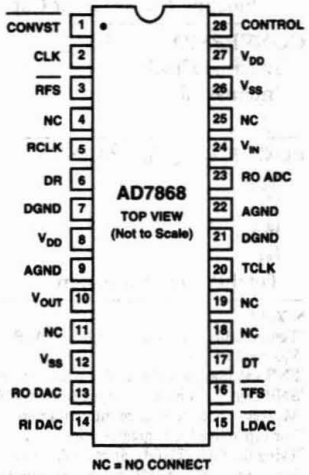
1. Complete 12-Bit I/O System.
   The AD7868 contains a 12-bit ADC with a track-and-hold amplifier and a 12-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7868 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7868 is available in a 24-pin DIP and a 28-pin SOIC package.

PIN CONFIGURATIONS

DIP



SOIC



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AD7868–SPECIFICATIONS

ADC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.0 MHz external. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCES					
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	70	72	70	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	70	71	70	dB min	Typically 71.5 dB for 0 < V_{IN} < 41.5 kHz
Total Harmonic Distortion (THD)	–78	–78	–76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically –84 dB for 0 < V_{IN} < 41.5 kHz
Peak Harmonic or Spurious Noise	–78	–78	–76	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz Typically –84 dB for 0 < V_{IN} < 41.5 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	–78	–78	–76	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	–80	–78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	µs max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution	12	12	12	Bits	No Missing Codes Guaranteed
Integral Nonlinearity	±1/2	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	
Bipolar Zero Error	±5	±5	±5	LSB max	
Positive Gain Error[5]	±5	±5	±5	LSB max	
Negative Gain Error[5]	±5	±5	±5	LSB max	
ANALOG INPUTS					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±1	±1	±1	mA max	
REFERENCE OUTPUT[6]					
RO ADC @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
RO ADC TC	±25	±25	±25	ppm/°C typ	
RO ADC TC		±40	±50	ppm/°C max	
Reference Load Sensitivity (ΔRO DAC vs. ΔI)	–1.5	–1.5	–1.5	mV max	Reference Load Current Change (0–500 µA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS ($\overline{CONVST}$, CLK, CONTROL)					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL Input Only)	±10	±10	±10	µA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	10	pF max	
LOGIC OUTPUTS					
DR, $\overline{RFS}$ Outputs					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, $\overline{RFS}$, RCLK Outputs					
Floating-State Leakage Current	±10	±10	±10	µA max	
Floating-State Output Capacitance[8]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	µs max	
Internal Clock	10	10	10	µs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	22	22	25	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	13	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	190	mW max	Typically 130 mW

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; T Version: –55°C to +125°C.
[2]V_{IN} = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.
[5]Measured with respect to internal reference.
[6]For capacitive loads greater than 50 pF a series resistor is required (see INTERNAL REFERENCE section).
[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.
[8]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

LC²MOS
Complete, 14-Bit Analog I/O System

AD7869

FEATURES

Complete 14-Bit I/O System, Comprising:
- **14-Bit ADC with Track/Hold Amplifier**
  - **83 kHz Throughput Rate**
- **14-Bit DAC with Output Amplifier**
  - **3.5 µs Settling Time**
- **On-Chip Voltage Reference**

Operates from ±5 V Supplies
Low Power – 130 mW typ
Small 0.3" Wide DIP

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

GENERAL DESCRIPTION

The AD7869 is a complete 14-bit I/O system containing a DAC and an ADC. The ADC is a successive approximation type with a track-and-hold amplifier having a combined throughput rate of 83 kHz. The DAC has an output buffer amplifier with a settling time of 4 µs to 14 bits. Temperature compensated 3 V buried Zener references provide precision references for the DAC and ADC.

Interfacing to both the DAC and ADC is serial, minimizing pin count and giving a small 24-pin package size. Standard control signals allow serial interfacing to most DSP machines.

Asynchronous ADC conversion control and DAC updating is made possible with the $\overline{\text{CONVST}}$ and $\overline{\text{LDAC}}$ logic inputs.

The AD7869 operates from ±5 V power supplies, the analog input/output range of the ADC/DAC is ±3 V. The part is fully specified for dynamic parameters such as signal-to-noise ratio and harmonic distortion as well as traditional dc specifications.

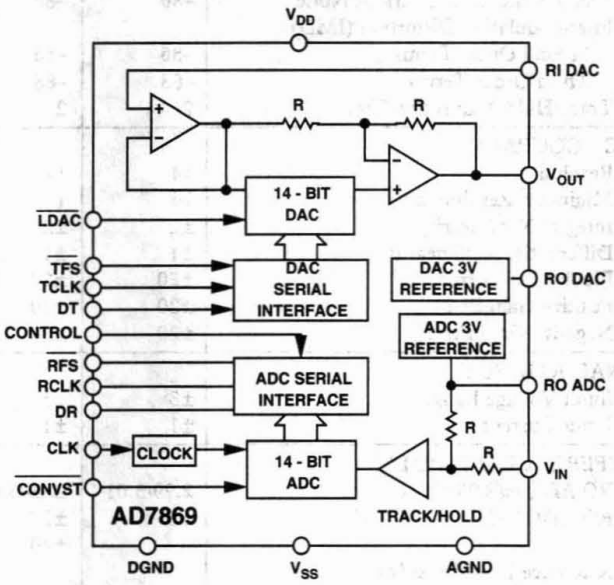
The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic SOIC package.

ORDERING GUIDE

Model	Temperature Range	Signal-to-Noise Ratio (SNR)	Relative Accuracy (LSB)	Package Option*
AD7869JN	0°C to +70°C	78 dB	±2 max	N-24
AD7869JR	0°C to +70°C	78 dB	±2 max	R-28
AD7869AQ	–40°C to +85°C	77 dB	±2 max	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline IC).
For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. Complete 14-Bit I/O System.
   The AD7869 contains a 14-bit ADC with a track-and-hold amplifier and a 14-bit DAC with output amplifier. Also included are separate on-chip voltage references for the DAC and the ADC.
2. Dynamic Specifications for DSP Users.
   In addition to traditional dc specifications, the AD7869 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Small Package.
   The AD7869 is available in a 24-pin DIP and a 28-pin SOIC package.

PIN CONFIGURATIONS

DIP

SOIC

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AD7869–SPECIFICATIONS

ADC SECTION (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.0 MHz external. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J Version[1]	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3, 4] (SNR) @ +25°C	78	78	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
T_{MIN} to T_{MAX}	78	77	dB min	
Total Harmonic Distortion (THD)	–86	–86	dB typ	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Peak Harmonic or Spurious Noise	–86	–86	dB typ	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 83 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	–86	–86	dB typ	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–88	–88	dB typ	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	µs max	
DC ACCURACY				
Resolution	14	14	Bits	
Minimum Resolution	14	14	Bits	No Missing Codes Guaranteed
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	
Bipolar Zero Error	±20	±20	LSB max	
Positive Gain Error[5]	±20	±20	LSB max	
Negative Gain Error[5]	±20	±20	LSB max	
ANALOG INPUT				
Input Voltage Range	±3	±3	Volts	
Input Current	±1	±1	mA max	
REFERENCE OUTPUT[6]				
RO ADC @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
RO ADC TC	±25	±25	ppm/°C typ	
		±40	±ppm/°C max	
Reference Load Sensitivity (ΔRO ADC vs. ΔI)	–1.5	–1.5	mV max	Reference Load Current Change (0–500 µA), Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS ($\overline{CONVST}$, CLK, CONTROL)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current[7] (CONTROL & CLK)	±10	±10	µA max	V_{IN} = V_{SS} to DGND
Input Capacitance, C_{IN}[8]	10	10	pF max	
LOGIC OUTPUTS				
DR, $\overline{RFS}$ Outputs				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA, Pull-Up Resistor = 4.7 kΩ
RCLK Output				
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA, Pull-Up Resistor = 2 kΩ
DR, $\overline{RFS}$, RCLK Outputs				
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[8]	15	15	pF max	
CONVERSION TIME				
External Clock	10	10	µs max	
Internal Clock	10	10	µs max	The Internal Clock Has a Nominal Value of 2.0 MHz
POWER REQUIREMENTS				For Both DAC and ADC
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	V nom	±5% for Specified Performance
I_{DD}	22	22	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	12	12	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	170	170	mW max	Typically 130 mW

NOTES

[1]Temperature ranges are as follows: J Version: 0°C to +70°C; A Version: –40°C to +85°C.

[2]V_{IN} = ±3 V

[3]SNR calculation includes distortion and noise components.

[4]SNR degradation due to asynchronous DAC updating during conversion is 0.1 dB typ.

[5]Measured with respect to internal reference.

[6]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).

[7]Tying the CONTROL input to V_{DD} places the device in a factory test mode where normal operation is not exhibited.

[8]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS Complete, 12-Bit, 100 kHz, Sampling ADCs

AD7870/AD7875/AD7876

FEATURES

Complete Monolithic 12-Bit ADC with:
- **2 µs Track/Hold Amplifier**
- **8 µs A/D Converter**
- **On-Chip Reference**
- **Laser-Trimmed Clock**
- **Parallel, Byte and Serial Digital Interface**

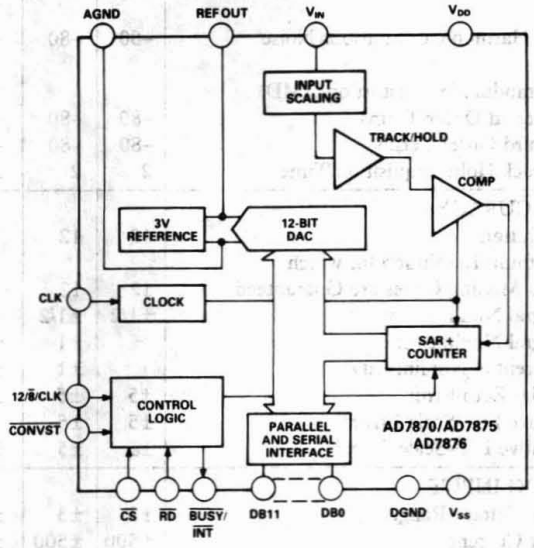
72 dB SNR at 10 kHz Input Frequency (AD7870, AD7875)

57 ns Data Access Time

Low Power: –60 mW typ

Variety of Input Ranges:
- **±3 V for AD7870**
- **0 V to +5 V for AD7875**
- **±10 V for AD7876**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7870/AD7875/AD7876 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8 µs successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may he overridden by an external clock if required.

The parts offer a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes, or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

All parts operate from ±5 V power supplies. The AD7870 and AD7876 accept input signal ranges of ±3 V and ±10 V, respectively, while the AD7875 accepts a unipolar 0 to +5 V input range. The parts can convert full power signals up to 50 kHz.

The AD7870/AD7875/AD7876 feature dc accuracy specifications such as linearity, full-scale and offset error. In addition, the AD7870 and AD7875 are fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

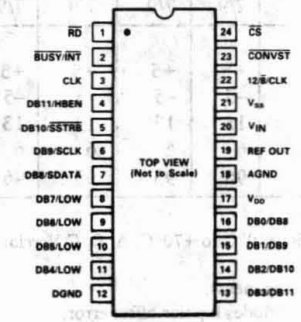
The parts are available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP). The AD7870 and AD7875 are available in a 28-pin plastic leaded chip carrier (PLCC), while the AD7876 is available and in a 24-pin small outline (SOIC) package.

PRODUCT HIGHLIGHTS

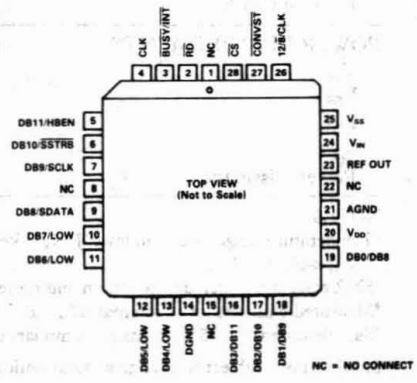
1. Complete 12-Bit ADC on a Chip.
   The AD7870/AD7875/AD7876 provides all the functions necessary for analog-to-digital conversion and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic Specifications for DSP Users.
   The AD7870 and AD7875 are fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion.
3. Fast Microprocessor Interface.
   Data access times of 57 ns make the parts compatible with modern 8- and 16-bit microprocessors and digital signal processors. Key digital timing parameters are tested and guaranteed over the full operating temperature range.

PIN CONNECTIONS

DIP



PLCC



AD7870/AD7875/AD7876–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external, unless otherwise stated. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7870 J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)							
@ +25°C	70	70	72	69	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}	70	70	71	69	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	–80	–80	–80	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically –86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	–80	–80	–80	–78	–78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically –86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)							
Second Order Terms	–80	–80	–80	–78	–78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	–80	–80	–78	–78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	2	2	µs max	
DC ACCURACY							
Resolution	12	12	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2		±1	LSB max	
Differential Nonlinearity		±1	±1		±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	±5	LSB max	
Positive Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
Negative Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
ANALOG INPUT							
Input Voltage Range	±3	±3	±3	±3	±3	Volts	
Input Current	±500	±500	±500	±500	±500	µA max	
REFERENCE OUTPUT							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	±1	±1	mV max	Reference Load Current Change (0 µA–500 µA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	10	pF max	
LOGIC OUTPUTS							
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0							
Floating-State Leakage Current	±10	±10	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	15	15	pF max	
CONVERSION TIME							
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	8	8	µs max	
Internal Clock	7/9	7/9	7/9	7/9	7/9	µs min/µs max	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	13	13	mA max	Typically 8 mA
I_{SS}	6	6	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	95	95	mW max	Typically 60 mW

NOTES

[1]Temperature ranges are as follows: J, K, L Versions; 0°C to +70°C: A, B, C Versions; –25°C to +85°C: S, T Versions; –55°C to +125°C.

[2]V_{IN} (pk-pk) = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to internal reference and includes bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS Complete 14-Bit Sampling ADCs

AD7871/AD7872

FEATURES

Complete Monolithic 14-Bit ADC
2s Complement Coding
Parallel, Byte and Serial Digital Interface
80 dB SNR at 10 kHz Input Frequency
57 ns Data Access Time
Low Power—50 mW typ
83 kSPS Throughput Rate
16-Lead SOIC (AD7872)

APPLICATIONS

Digital Signal Processing
High Speed Modems
Speech Recognition and Synthesis
Spectrum Analysis
DSP Servo Control

GENERAL DESCRIPTION

The AD7871 and AD7872 are fast, complete, 14-bit analog-to-digital converters. They consist of a track/hold amplifier, successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained, laser trimmed internal clock, so no external clock timing components are required. The on-chip clock may be overridden to synchronize ADC operation to the digital system for minimum noise.

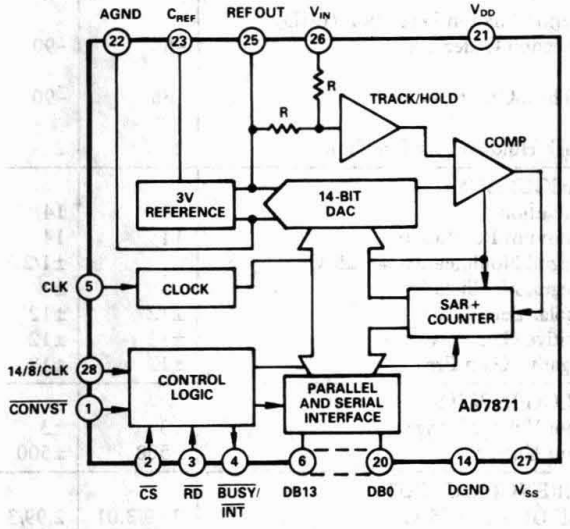
The AD7871 offers a choice of three data output formats: a single, parallel, 14-bit word; two 8-bit bytes or a 14-bit serial data stream. The AD7872 is a serial output device only. The two parts are capable of interfacing to all modern microprocessors and digital signal processors.

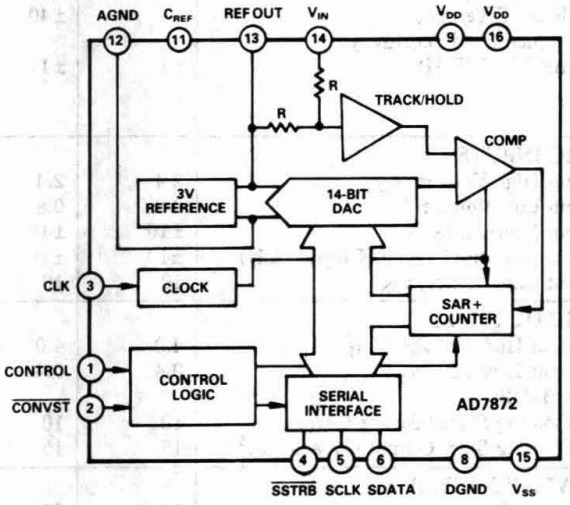
The AD7871 and AD7872 operate from ±5 V power supplies, accept bipolar input signals of ±3 V and can convert full power signals up to 41.5 kHz.

In addition to the traditional dc accuracy specifications, the AD7871 and AD7872 are also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Both devices are fabricated in Analog Devices' LC²MOS mixed technology process. The AD7871 is available in 28-pin plastic DIP, hermetic DIP and PLCC packages. The AD7872 is available in 16-pin plastic and hermetic DIP packages or 16-lead SOIC.

FUNCTIONAL BLOCK DIAGRAM





ORDERING GUIDE

Model[1, 2]	Temperature Range	SNR	Relative Accuracy (LSB)	Package Option[3]
AD7871JN	0°C to +70°C	80 dBs min		N-28
AD7871KN	0°C to +70°C	80 dBs min	±1 max	N-28
AD7871JP	0°C to +70°C	80 dBs min		P-28A
AD7871KP	0°C to +70°C	80 dBs min	±1 max	P-28A
AD7871AQ	–40°C to +85°C	80 dBs min		Q-28
AD7871BQ	–40°C to +85°C	80 dBs min	±1 max	Q-28
AD7871TQ[4]	–55°C to +125°C	79 dBs min	±1 max	Q-28

NOTES
[1]To order MIL-STD-883; Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for military data sheet.
[3]For outline information see Package Information section.
[4]Available to /883B processing only.

ORDERING GUIDE

Model[1]	Temperature Range	SNR	Relative Accuracy (LSB)	Package Option[2]
AD7872AN	–40°C to +85°C	80 dBs min		N-16
AD7872JN	0°C to +70°C	80 dBs min		N-16
AD7872KN	0°C to +70°C	80 dBs min	±1 max	N-16
AD7872BR	–40°C to +85°C	78 dBs min	±1 max	R-16
AD7872JR	0°C to +70°C	80 dBs min		R-16
AD7872KR	0°C to +70°C	80 dBs min	±1 max	R-16
AD7872AQ	–40°C to +85°C	80 dBs min		Q-16
AD7872BQ	–40°C to +85°C	80 dBs min	±1 max	Q-16
AD7872TQ[3]	–55°C to +125°C	79 dBs min	±1 max	Q-16

NOTES
[1]To order MIL-STD-883; Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]For outline information see Package Information section.
[3]Available to /883B processing only.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7871/AD7872–SPECIFICATIONS

(V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2 MHz external, f_{SAMPLE} = 83 kHz unless otherwise noted.)
All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Parameter	J, A Versions[1]	K, B Versions[1]	T Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal-to-Noise Ratio[3] (SNR) @ +25°C	80	80	79	dB min	V_{IN} = 10 kHz Sine Wave
T_{MIN} to T_{MAX}	80	80	79	dB min	SNR is Typically 82 dB for <V_{IN}<41.5 kHz;
Total Harmonic Distortion (THD)	–86	–90		dB max	V_{IN} = 10 kHz Sine Wave;
			–85	dB typ	
Peak Harmonic or Spurious Noise	–86	–90		dB max	V_{IN} = 10 kHz
			–85	dB typ	
Intermodulation Distortion (IMD)					
Second Order Terms	–86	–90		dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
			–85	dB typ	
Third Order Terms	–86	–90		dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
			–85	dB typ	
Track/Hold Acquisition Time	2	2	2	µs max	
DC ACCURACY					
Resolution	14	14	14	Bits	
Minimum Resolution	14	14	14	Bits	No Missing Codes Guaranteed
Integral Nonlinearity @ +25°C		±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1	LSB max	
Bipolar Zero Error	±12	±12	±12	LSB max	
Positive Gain Error[5]	±12	±12	±12	LSB max	
Negative Gain Error[5]	±12	±12	±12	LSB max	
ANALOG INPUTS					
Input Voltage Range	±3	±3	±3	Volts	
Input Current	±500	±500	±500	µA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99/3.01	2.99/3.01	2.99/3.01	V min/V max	
T_{MIN} to T_{MAX}	2.98/3.02	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco		±40	±40	ppm/°C max	Typically 35 ppm
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	mV max	Reference Load Current Change (0–500 µA); Reference Load Should Not Be Changed During Conversion
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (14/8/CLK Input Only)	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB13–DB0					
Floating-State Leakage Current	10	10	10	µA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock	10	10	10	µs max	
Internal Clock	10.5	10.5	10.5	µs max	The Internal Clock Has a Nominal Value of 2 MHz
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	mA max	Typically 6 mA
I_{SS}	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	mW max	Typically 50 mW

NOTES
[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; A, B Versions: –40°C to +85°C; T Version: –55°C to +125°C.
[2]V_{IN} = ±3 V
[3]SNR calculation includes distortion and noise components.
[4]Measured with respect to internal reference.
[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

LC²MOS 4-Channel, 12-Bit Simultaneous Sampling Data Acquisition System

AD7874

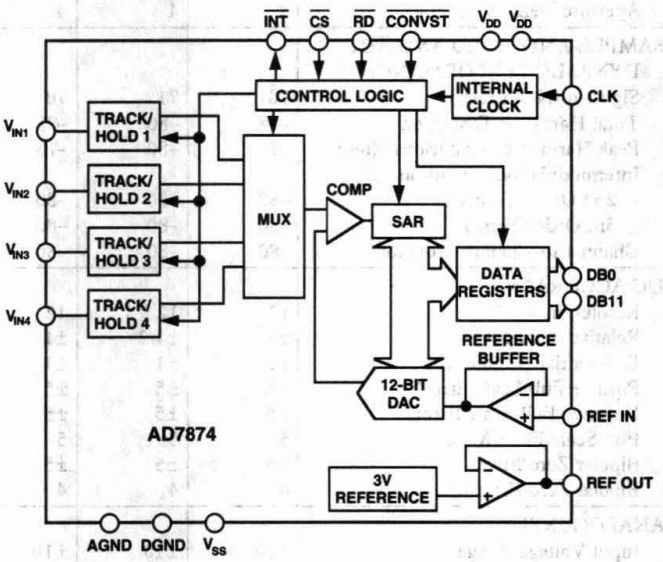
FEATURES

Four On-Chip Track/Hold Amplifiers
Simultaneous Sampling of 4 Channels
Fast 12-Bit ADC with 8 μs Conversion Time/Channel
29 kHz Sample Rate for All Four Channels
On-Chip Reference
±10 V Input Range
±5 V Supplies

APPLICATIONS

Sonar
Motor Controllers
Adaptive Filters
Digital Signal Processing

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7874 is a four-channel simultaneous sampling, 12-bit data acquisition system. The part contains a high speed 12-bit ADC, on-chip reference, on-chip clock and four track/hold amplifiers. This latter feature allows the four input channels to be sampled simultaneously, thus preserving the relative phase information of the four input channels, which is not possible if all four channels share a single track/hold amplifier. This makes the AD7874 ideal for applications such as phased-array sonar and ac motor controllers where the relative phase information is important.

The aperture delay of the four track/hold amplifiers is small and specified with minimum and maximum limits. This allows several AD7874s to sample multiple input channels simultaneously without incurring phase errors between signals connected to several devices. A reference output/reference input facility also allows several AD7874s to be driven from the same reference source.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7874 is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The AD7874 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. The part is available in a 28-pin, 0.6" wide, plastic or hermetic dual-in-line package (DIP), in a 28-terminal leadless ceramic chip carrier (LCCC) and in a 28-pin SOIC.

PRODUCT HIGHLIGHTS

1. Simultaneous Sampling of Four Input Channels.
   Four input channels, each with its own track/hold amplifier, allow simultaneous sampling of input signals. Track/hold acquisition time is 2 μs, and the conversion time per channel is 8 μs, allowing 29 kHz sample rate for all four channels.
2. Tight Aperture Delay Matching.
   The aperture delay for each channel is small and the aperture delay matching between the four channels is less than 4 ns. Additionally, the aperture delay specification has upper and lower limits allowing multiple AD7874s to sample more than four channels.
3. Fast Microprocessor Interface.
   The high speed digital interface of the AD7874 allows direct connection to all modern 16-bit microprocessors and digital signal processors.

ORDERING GUIDE

Model[1]	Temperature Range	SNR (dBs)	Relative Accuracy (LSB)	Package Option[2]
AD7874AN	–40°C to +85°C	70 min	±1 max	N-28
AD7874BN	–40°C to +85°C	72 min	±1/2 max	N-28
AD7874AR	–40°C to +85°C	70 min	±1 max	R-28
AD7874BR	–40°C to +85°C	72 min	±1/2 max	R-28
AD7874AQ	–40°C to +85°C	70 min	±1 max	Q-28
AD7874BQ	–40°C to +85°C	72 min	±1/2 max	Q-28
AD7874SQ[3]	–55°C to +125°C	70 min	±1 max	Q-28
AD7874SE[3]	–55°C to +125°C	70 min	±1 max	E-28A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leaded Ceramic Chip Carrier; N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[3]Available to /883B processing only.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7874–SPECIFICATIONS

(V_{DD} = +5 V, V_{SS} = –5 V, AGND = DGND = 0 V, REF IN = +3 V, f_{CLK} = 2.5 MHz external. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version	B Version	S Version	Units	Test Conditions/Comments
SAMPLE-AND-HOLD					
Acquisition Time[2] to 0.01%	2	2	2	µs max	
Droop Rate[2, 3]	1	1	2	mV/ms max	
–3 dB Small Signal Bandwidth[3]	500	500	500	kHz typ	V_{IN} = 500 mV p-p
Aperture Delay[2]	0	0	0	ns min	
	40	40	40	ns max	
Aperture Jitter[2, 3]	200	200	200	ps typ	
Aperture Delay Matching[2]	4	4	4	ns max	
SAMPLE-AND-HOLD AND ADC DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio	70	71	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Total Harmonic Distortion	–78	–80	–78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Peak Harmonic or Spurious Noise	–78	–80	–78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 29 kHz
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 29 kHz
2nd Order Terms	–80	–80	–80	dB max	
3rd Order Terms	–80	–80	–80	dB max	
Channel-to-Channel Isolation[2]	–80	–80	–80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	No Missing Codes Guaranteed
Positive Full-Scale Error[4]	±5	±5	±5	LSB max	Any Channel
Negative Full-Scale Error[4]	±5	±5	±5	LSB max	Any Channel
Full-Scale Error Match	5	5	5	LSB max	Between Channels
Bipolar Zero Error	±5	±5	±5	LSB max	Any Channel
Bipolar Zero Error Match	4	4	4	LSB max	Between Channels
ANALOG INPUTS					
Input Voltage Range	±10	±10	±10	Volts	
Input Current	±600	±600	±600	µA max	
REFERENCE OUTPUTS					
REF OUT	3	3	3	V nom	
REF OUT Error @ +25°C	±0.33	±0.33	±0.33	% max	
T_{MIN} to T_{MAX}	±1	±1	±1	% max	
REF OUT Temperature Coefficient	±35	±35	±35	ppm/°C typ	
Reference Load Change	±1	±1	±2	mV max	Reference Load Current Change (0–500 µA) Reference Load Should Not Be Changed During Conversion
REFERENCE INPUT					
Input Voltage Range	2.85/3.15	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	±1	±1	±1	µA max	
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	V_{DD} = 5 V ± 5%; I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	V_{DD} = 5 V ± 5%; I_{SINK} = 1.6 mA
DB0–DB11					
Floating-State Leakage Current	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Floating-State Output Capacitance	10	10	10	pF max	
Output Coding	2s COMPLEMENT				
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	18	18	18	mA max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 12 mA
I_{SS}	12	12	12	mA max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 8 mA
Power Dissipation	150	150	150	mW max	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = +5 V; Typically 100 mW

NOTES

[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.

[2]See Terminology.

[3]Sample tested @ +25°C to ensure compliance.

[4]Measured with respect to the REF IN voltage and includes bipolar offset error.

[5]For capacitive loads greater than 50 pF a series resistor is required.

Specifications subject to change without notice.

LC²MOS Single +5 V Supply, Low Power, 12-Bit Sampling ADC

AD7880

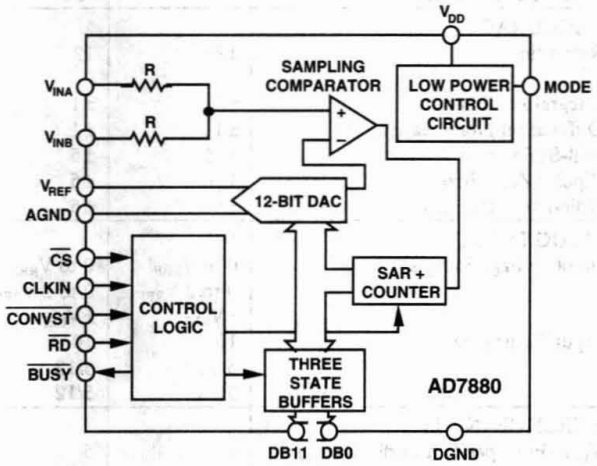
FEATURES

- 12-Bit Monolithic A/D Converter
- 66 kHz Throughput Rate
  - 12 μs Conversion Time
  - 3 μs On-Chip Track/Hold Amplifier
- Low Power
  - Power Save Mode: 2 mW typ
  - Normal Operation: 25 mW typ
- 70 dB SNR
- Fast Data Access Time: 57 ns
- Small 24-Lead SOIC and 0.3" DIP Packages

APPLICATIONS

- Battery Powered Portable Systems
- Digital Signal Processing
- Speech Recognition and Synthesis
- High Speed Modems
- Control and Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7880 is a high speed, low power, 12-bit A/D converter which operates from a single +5 V supply. It consists of a 3 μs track/hold amplifier, a 12 μs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

An internal resistor network allows the part to accept both unipolar and bipolar input signals while operating from a single +5 V supply. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7880 features a total throughput time of 15 μs and can convert full power signals up to 33 kHz with a sampling frequency of 66 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7880 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7880 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time.
   12 μs conversion time and 3 μs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.
2. Low Power Consumption.
   2 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.
3. Multiple Input Ranges.
   The part features three user-determined input ranges, 0 V to +5 V, 0 V to 10 V and ±5 V. These unipolar and bipolar ranges are achieved with a 5 V only power supply.

ORDERING GUIDE

Model	Temperature Range	Full-Scale Error (LSBs)	Bipolar Zero Error (LSBs)	Package Option*
AD7880BN	–40°C to +85°C	±15	±10	N-24
AD7880BQ	–40°C to +85°C	±15	±10	Q-24
AD7880CN	–40°C to +85°C	±5	±5	N-24
AD7880CQ	–40°C to +85°C	±5	±5	Q-24
AD7880BR	–40°C to +85°C	±15	±10	R-24
AD7880CR	–40°C to +85°C	±5	±5	R-24

*N = Plastic DIP; Q = Cerdip; R = SOIC (Small Outline Integrated Circuit).
For outline information see Package Information section.

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AD7880–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{REF} = V_{DD}, AGND = DGND = 0 V, f_{CLKIN} = 2.5 MHz, MODE = V_{DD} unless otherwise noted. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Versions[1]	C Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio[3] (SNR)	70	70	dB min	Typically SNR Is 72 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Total Harmonic Distortion (THD)	–80	–80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 66 kHz
Peak Harmonic or Spurious Noise	–80	–80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 66 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	–80	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
Third Order Terms	–80	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 66 kHz
DC ACCURACY				
Resolution	12	12	Bits	All DC ACCURACY Specifications Apply for the Three Analog Input Ranges
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±15	±5	LSB max	
Bipolar Zero Error	±10	±5	LSB max	
Unipolar Offset Error	±5	±5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	See Figure 5
	0 to 2 V_{REF}	0 to 2 V_{REF}	Volts	See Figure 6
	±V_{REF}	±V_{REF}	Volts	See Figure 7
Input Resistance	10	10	MΩ min	0 to V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: 0 to 2 V_{REF} Range
	5/12	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT				
V_{REF} (For Specified Performance)	5	5	V	±5%: Normally V_{REF} = V_{DD} (See Reference Input Section)
I_{REF}	1.5	1.5	mA max	
Nominal Reference Range	2.5/V_{DD}	2.5/V_{DD}	V min/max	See Figure 3 for Degradation in Performance Down to 2.5 V
LOGIC INPUTS				
$\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$, CLKIN				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
MODE INPUT				
Input High Voltage, V_{INH}	4	4	V min	
Input Low Voltage, V_{INL}	1	1	V max	
Input Current, I_{IN}	±125	±125	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0				
Floating-State Leakage Current	±10	±10	μA max	
Floating-State Output Capacitance[4]	10	10	pF max	
CONVERSION				
Conversion Time	12	12	μs max	f_{CLKIN} = 2.5 MHz
Track/Hold Acquisition Time	3	3	μs max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}				
Normal Power Mode @ +25°C	7.5	7.5	mA max	Typically 4 mA; MODE = V_{DD}
T_{MIN} to T_{MAX}	10	10	mA max	Typically 5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	750	750	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
T_{MIN} to T_{MAX}	1	1	mA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V
Power Dissipation				
Normal Power Mode @ +25°C	37.5	37.5	mW max	V_{DD} = 5 V: Typically 20 mW; MODE = V_{DD}
T_{MIN} to T_{MAX}	50	50	mW max	V_{DD} = 5 V: Typically 25 mW; MODE = V_{DD}
Power Save Mode @ +25°C	3.75	3.75	mW max	V_{DD} = 5 V: Typically 2 mW; MODE = 0 V
T_{MIN} to T_{MAX}	5	5	mW max	V_{DD} = 5 V: Typically 2.5 mW; MODE = 0 V

NOTES
[1]Temperature ranges are as follows: B/C Versions, –40°C to +85°C.
[2]V_{IN} = 0 to V_{REF}
[3]SNR calculation includes distortion and noise components.
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS 16-Bit, 2.5 µs, Sampling ADC

AD7882

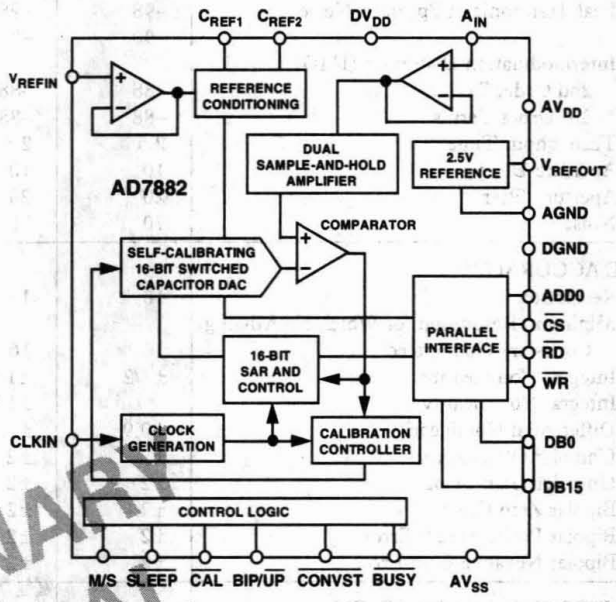
FEATURES

- 2.5 µs Throughput Time
- 16-Bit Sampling ADC
- Self-Calibration
- High Speed Parallel Interface
- 92 dB Signal-to-Noise Ratio
- Low Power: 200 mW typ
  - 1 mW in Power-Down Mode
- Unipolar and Bipolar Input Signal Ranges
- On-Chip 2.5 V Reference
- Operates from ±5 V Supplies

APPLICATIONS

- Data Acquisition Systems
- Digital Signal Processing
- Spectrum Analysis
- DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7882 is a fast, 16-bit self-calibrating A/D converter. It consists of a sample-and-hold amplifier, a self-calibrating 16-bit ADC, a 2.5 V reference and versatile interface logic. An on-chip controller manages the self-calibrating algorithm that reduces linearity, offset and gain errors to ±0.0015%. System offset and gain errors, caused by external conditioning circuitry, can also be included in the calibration procedure. Throughput time is minimized at 2.5 µs by the use of a dual sample-and-hold amplifier. The ADC also has a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time; alternatively, an external clock may be used.

Another feature of the AD7882 is a power-down mode that reduces power dissipation from its normal operating value of 200 mW to 1 mW.

The AD7882 operates from ±5 V supplies. Analog input ranges can be unipolar, 0 V to 2.5 V, or bipolar, ±2.5 V. The analog input bandwidth is 200 kHz.

In addition to traditional dc accuracy specifications such as linearity, the AD7882 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio (SNR).

The AD7882 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power, high speed CMOS logic. The part is available in a 44-pin plastic quad flatpack (PQFP) and 40-pin cerdip.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. Fast 2.5 µs Throughput Time
   A fast 2.5 µs throughput time makes the AD7882 suitable for a wide range of data acquisition applications.
2. Self-Calibration Achieves High Accuracy
   A self-calibrating algorithm minimizes linearity, offset and gain errors. The calibration procedure can also include external offset and gain errors.

ORDERING GUIDE

Model	Temperature Range	Integral Nonlinearity (LSB)	Package Option*
AD7882SQ	–55°C to +125°C	±0.5 typ	Q-40
AD7882TQ	–55°C to +125°C	±1 max	Q-40
AD7882AS	–40°C to +85°C	±0.5 typ	S-44
AD7882BS	–40°C to +85°C	±1 max	S-44
AD7882SX	–55°C to +125°C	±0.5 typ	X-44
AD7882TX	–55°C to +125°C	±1 max	X-44

*Q = Cerdip; S = PQFP; X = Cerquad. For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD7882–SPECIFICATIONS (AV_{DD} = 5 V ± 5%, DV_{DD} = 5 V ± 5%, AV_{SS} = –5 V ± 5%, V_{REFIN} = 2.5 V, AGND = DGND = 0 V, f_{CLKIN} = 10 MHz, f_{SAMPLE} = 400 kHz. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A, S Versions[1]	B, T Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				
Signal to (Noise + Distortion Ratio)	90	90	dB min	A_{IN} = 10 kHz, Typical SNR = 92 dB
	85	85	dB min	A_{IN} = 100 kHz, Typical SNR = 87 dB
THD	–95	–95	dB max	A_{IN} = 10 kHz, Typical THD = –100 dB
	–88	–88	dB max	A_{IN} = 100 kHz, Typical THD = –90 dB
Peak Harmonic or Spurious Noise	–98	–98	dB max	A_{IN} = 10 kHz, Typical Peak Harmonic = –100 dB
	–90	–90	dB max	A_{IN} = 100 kHz, Typical Peak Harmonic = –92 dB
Intermodulation Distortion (IMD)				
2nd Order Terms	–88	–88	dB max	f_A = 98 kHz, f_B = 100 kHz
3rd Order Terms	–88	–88	dB max	
Throughput Time	2.5	2.5	µs max	
Aperture Delay	10	10	ns typ	
Aperture Jitter	20	20	ps typ	
Noise	70	70	µV rms typ	
DC ACCURACY[2]				
Resolution	16	16	Bits	
Minimum Resolution for Which No Missing Codes are Guaranteed	16	16	Bits	
Integral Nonlinearity	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1.0	LSB max	
Differential Nonlinearity	±0.9	±0.5	LSB max	
Unipolar Offset Error	±2	±2	LSB max	
Unipolar Gain Error	±2	±2	LSB max	
Bipolar Zero Error	±2	±2	LSB max	
Bipolar Positive Gain Error	±2	±2	LSB max	
Bipolar Negative Gain Error	±2	±2	LSB max	
POWER SUPPLY REJECTION				
AV_{DD} Only	84	84	dB typ	
AV_{SS} Only	84	84	dB typ	
ANALOG I/P				
Input Current	±1	±1	µA max	Input Range = 0 V to +2.5 V or ±2.5 V
Input Capacitance[3]	20	20	pF max	
REFERENCE OUTPUT				
V_{REFOUT} @ +25°C	2.5	2.5	Volts Nominal	±1%
V_{REFOUT} Tempco	20	20	ppm/°C typ	
REFERENCE INPUT				
V_{REFIN} Range	2.5	2.5	Volts	±2%
V_{REFIN} Current	±1	±1	µA max	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	Volts min	
Input Low Voltage, V_{INL}	0.8	0.8	Volts max	
Input Current	±10	±10	µA max	
Input Capacitance[3]	10	10	pF max	
$\overline{SLEEP}$ INPUT				
Input High Voltage, V_{INH}	V_{DD} – 0.2	V_{DD} – 0.2	Volts min	
Input Low Voltage, V_{INL}	0.2	0.2	Volts max	
CLKIN INPUT				
Negative Trigger Level	–2	–2	Volts min	This is the Trigger Level for Choosing Internal Clock Operation of the Device

PRELIMINARY TECHNICAL DATA

NOTES

[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S, T Versions: –55°C to +125°C.

[2]Specifications apply after calibration.

[3]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

LC²MOS 12-Bit, 3.3 V Sampling ADC

AD7883

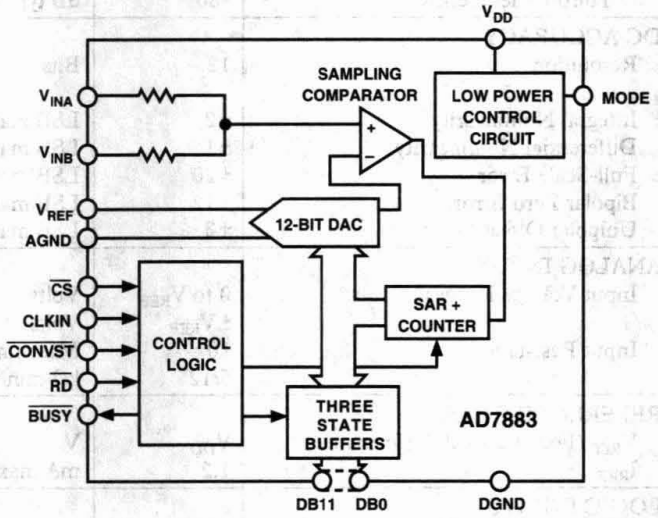
FEATURES

Battery-Compatible Supply Voltage: Guaranteed Specs for V_{DD} of 3 V to 3.6 V
12-Bit Monolithic A/D Converter
50 kHz Throughput Rate
15 µs Conversion Time
5 µs On-Chip Track/Hold Amplifier
Low Power
Power Save Mode: 1 mW typ
Normal Operation: 8 mW typ
70 dB SNR
Small 24-Lead SOIC and 0.3" DIP Packages

APPLICATIONS

Battery Powered Portable Systems
Laptop Computers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7883 is a high speed, low power, 12-bit A/D converter which operates from a single +3 V to +3.6 V supply. It consists of a 5 µs track/hold amplifier, a 15 µs successive-approximation ADC, versatile interface logic and a multiple-input-range circuit. The part also includes a power save feature.

Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7883 features a total throughput time of 20 µs and can convert full power signals up to 25 kHz with a sampling frequency of 50 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7883 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7883 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP) as well as a small 24-lead SOIC package.

PRODUCT HIGHLIGHTS

1. 3 V Operation
   The AD7883 is guaranteed and tested with a supply voltage of 3 V to 3.6 V. This makes it ideal for battery-powered applications where 12-bit A/D conversion is required.
2. Fast Conversion Time
   15 µs conversion time and 5 µs acquisition time allow for large input signal bandwidth. This performance is ideally suited for applications in areas such as telecommunications, audio, sonar and radar signal processing.
3. Low Power Consumption
   1 mW power consumption in the power-down mode makes the part ideally suited for portable, hand held, battery powered applications.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7883BN	–40°C to +85°C	N-24
AD7883BR	–40°C to +85°C	R-24

*N = Plastic DIP; R = SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

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AD7883—SPECIFICATIONS (V_{DD} = +3 V to +3.6 V, V_{REF} = V_{DD}, AGND = DGND = 0 V, f_{CLKIN} = 2 MHz, MODE = Logic High. All specifications T_{MIN} to T_{MAX} unless othewise noted.)

Parameter	B Versions[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]			
Signal-to-Noise Ratio[3] (SNR)	69	dB min	Typically SNR Is 71 dB V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 50 kHz
Total Harmonic Distortion (THD)	–80	dB typ	V_{IN} = 1 kHz Sine Wave, f_{SAMPLE} = 50 kHz
Peak Harmonic or Spurious Noise	–80	dB typ	V_{IN} = 1 kHz, f_{SAMPLE} = 50 kHz
Intermodulation Distortion (IMD)			
Second Order Terms	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	dB typ	fa = 0.983 kHz, fb = 1.05 kHz, f_{SAMPLE} = 50 kHz
DC ACCURACY			
Resolution	12	Bits	All DC ACCURACY Specifications Apply for the Two Analog Input Ranges
Integral Nonlinearity	±2	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±20	LSB max	
Bipolar Zero Error	±12	LSB max	
Unipolar Offset Error	±3	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	Volts	See Figure 4
	±V_{REF}	Volts	See Figure 5
Input Resistance	10	MΩ min	0 to V_{REF} Range
	5/12	kΩ min/max	8 kΩ typical: ±V_{REF} Range
REFERENCE INPUT			
V_{REF} (For Specified Performance)	V_{DD}	V	
I_{REF}	1.2	mA max	
LOGIC INPUTS			
$\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$, CLKIN			
Input High Voltage, V_{INH}	2.1	V min	
Input Low Voltage, V_{INL}	0.6	V max	
Input Current, I_{IN}	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
MODE INPUT			
Input High Voltage, V_{INH}	V_{DD} – 0.2	V	
Input Low Voltage, V_{INL}	0.2	V	
Input Current, I_{IN}	±100	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	pF max	
LOGIC OUTPUTS			
DB11–DB0, $\overline{BUSY}$			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
DB11–DB0			
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance[4]	10	pF max	
CONVERSION			
Conversion Time	15	μs max	f_{CLKIN} = 2 MHz
Track/Hold Acquisition Time	5	μs max	
POWER REQUIREMENTS			
V_{DD}	+3.3	V nom	+3 V to +3.6 V for Specified Performance
I_{DD}			
Normal Power Mode @ +25°C	3	mA max	Typically 2 mA; MODE = V_{DD}
T_{MIN} to T_{MAX}	4	mA max	Typically 2.5 mA; MODE = V_{DD}
Power Save Mode @ +25°C	400	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V; Typically 250 μA
T_{MIN} to T_{MAX}	800	μA max	Logic Inputs @ 0 V or V_{DD}; MODE = 0 V; Typically 300 μA
Power Dissipation			
Normal Power Mode @ +25°C	11	mW max	V_{DD} = 3.6 V: Typically 8 mW; MODE = V_{DD}
T_{MIN} to T_{MAX}	15	mW max	V_{DD} = 3.6 V: Typically 9 mW; MODE = V_{DD}
Power Save Mode @ +25°C	1.5	mW max	V_{DD} = 3.6 V: Typically 1 mW; MODE = 0 V
T_{MIN} to T_{MAX}	3	mW max	V_{DD} = 3.6 V: Typically 1 mW; MODE = 0 V

NOTES
[1]Temperature range is as follows: B Versions, –40°C to +85°C.
[2]V_{IN} = 0 to V_{REF}.
[3]SNR calculation includes distortion and noise components.
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS 16-Bit, High Speed Sampling ADCs

AD7884/AD7885

FEATURES
Monolithic Construction
Fast Conversion: 5.3 µs
High Throughput: 166 kSPS
Low Power: 250 mW

APPLICATIONS
Automatic Test Equipment
Medical Instrumentation
Industrial Control
Data Acquisition Systems
Robotics

GENERAL DESCRIPTION

The AD7884/AD7885 is a 16-bit monolithic analog-to-digital converter with internal sample-and-hold and a conversion time of 5.3 µs. The maximum throughput rate is 166 kSPS. It uses a two pass flash architecture to achieve this speed. Two input ranges are available: ±5 V and ±3 V. Conversion is initiated by the $\overline{\text{CONVST}}$ signal. The result can be read into a microprocessor using the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs on the device. The AD7884 has a 16-bit parallel reading structure while the AD7885 has a byte reading structure. The conversion result is in 2s complement code.

The AD7884/AD7885 has its own internal oscillator which controls conversion. It runs from ±5 V supplies and needs a V_{REF+} of +3 V.

The AD7884 is available in a 40-pin plastic DIP package and in a 44-pin PLCC package.

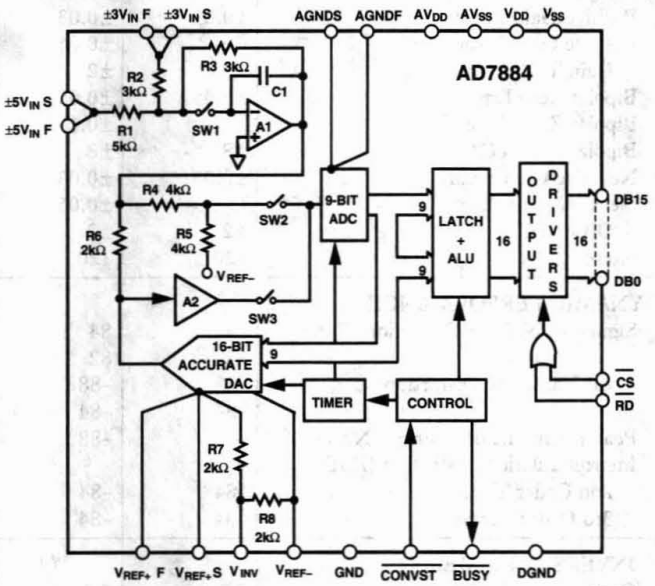
The AD7885 is available in a 28-pin plastic DIP package and the AD7885A is available in a 44-pin PLCC package.

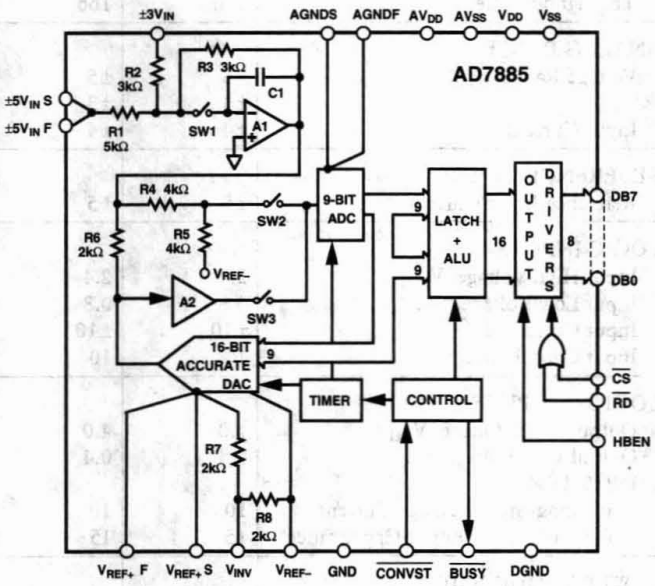
ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error (% FSR)	SNR (dB)	Package Option[2]
AD7884AN	–40°C to +85°C		84	N-40A
AD7884BN	–40°C to +85°C	±0.0075	84	N-40A
AD7884AP	–40°C to +85°C		84	P-44A
AD7884BP	–40°C to +85°C	±0.0075	84	P-44A
AD7885AN	–40°C to +85°C		84	N-28A
AD7885BN	–40°C to +85°C	±0.0075	84	N-28A
AD7885AAP	–40°C to +85°C		84	P-44A
AD7885ABP	–40°C to +85°C	±0.0075	84	P-44A

NOTES
[1]Analog Devices reserves the right to ship cerdip (Q) packages in lieu of plastic DIP (N) packages.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAMS





AD7884/AD7885/AD7885A–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, V_{REF}+S = +3 V; AGND = DGND = GND = 0 V; f_{SAMPLE} = 166 kHz. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1, 2, 3]	B Versions[1, 2, 3]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	16	16	Bits	
Minimum Resolution for Which				
No Missing Codes Are Guaranteed	16	16	Bits	
Integral Nonlinearity		±0.0075	% FSR max	Typically 0.003% FSR
Positive Gain Error	±0.03	±0.03	% FSR typ	AD7885AN/BN: 0.1% typ
Positive Gain Error		±0.05	% FSR max	AD7885BN: 0.2% max
Gain TC[4]	±2	±2	ppm FSR/°C typ	
Bipolar Zero Error	±0.05	±0.05	% FSR typ	
Bipolar Zero Error		±0.15	% FSR max	
Bipolar Zero TC[4]	±8	±8	ppm FSR/°C typ	
Negative Gain Error	±0.03	±0.03	% FSR typ	AD7885AN/BN: 0.1% typ
Negative Gain Error		±0.05	% FSR max	AD7885BN: 0.2% max
Offset TC[4]	±2	±2	ppm FSR/°C typ	
Noise	120	120	µV rms typ	78 µV rms typical in ±3 V Input Range
DYNAMIC PERFORMANCE				
Signal to (Noise + Distortion) Ratio	84	84	dB min	Input Signal: ±5 V, 1 kHz Sine Wave, Typically 86 dB
	82	82	dB typ	Input Signal: ±5 V, 12 kHz Sine Wave
Total Harmonic Distortion	–88	–88	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
	–84	–84	dB typ	Input Signal: ±5 V, 12 kHz Sine Wave
Peak Harmonic or Spurious Noise	–88	–88	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
Intermodulation Distortion (IMD)				
2nd Order Terms	–84	–84	dB typ	f_A = 11.5 kHz, f_B = 12 kHz, f_{SAMPLE} = 166 kHz
3rd Order Terms	–84	–84	dB typ	f_A = 11.5 kHz, f_B = 12 kHz, f_{SAMPLE} = 166 kHz
CONVERSION TIME				
Conversion Time	5.3	5.3	µs max	
Acquisition Time	2.5	2.5	µs max	
Throughput Rate	166	166	kSPS max	There is an overlap between conversion and acquisition.
ANALOG INPUT				
Voltage Range	±5	±5	Volts	
	±3	±3	Volts	
Input Current	±4	±4	mA max	
REFERENCE INPUT				
Reference Input Current	±5	±5	mA max	V_{REF} + S = +3 V
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	Input Level = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB15–DB0				
Floating-State Leakage Current	10	10	µA max	
Floating-State Output Capacitance[4]	15	15	pF max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	V nom	±5% for Specified Performance
I_{DD}	35	35	mA max	Typically 25 mA
I_{SS}	30	30	mA max	Typically 25 mA
Power Supply Rejection Ratio				
$\Delta Gain/\Delta V_{DD}$	86	86	dB typ	
$\Delta Gain/\Delta V_{SS}$	86	86	dB typ	
Power Dissipation	325	325	mW max	Typically 250 mW

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C.
[2]V_{IN} = ±5 V.
[3]The AD7885AAP has the same specs as the AD7884AP. The AD7885ABP has the same specs as the AD7884BP.
[4]Sample tested to ensure compliance.
Specifications subject to change without notice.

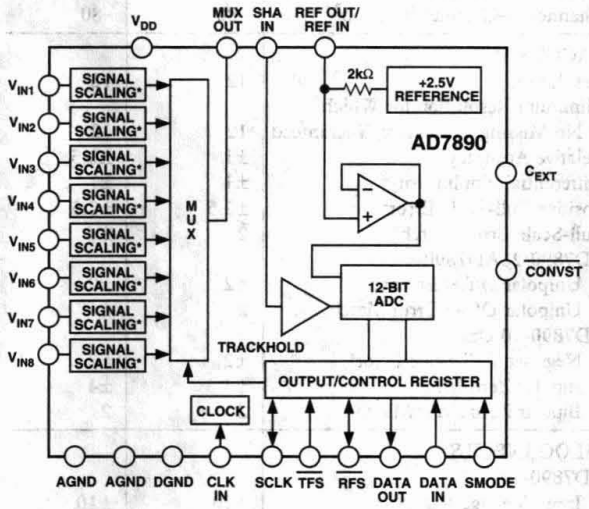
LC²MOS 8-Channel, 12-Bit, Serial, Data Acquisition System

AD7890

FEATURES

Fast 12-Bit ADC with 5.9 μs Conversion Time
Eight Single-Ended Analog Input Channels
Selection of Input Ranges:
±10 V for AD7890-10
0 V to +4.096 V for AD7890-4
0 V to +2.5 V for AD7890-2
Allows Seperate Access to Multiplexer and ADC
On-Chip Track/Hold Amplifier
On-Chip Reference
High Speed, Flexible, Serial Interface
Single Supply, Low Power Operation (50 mW max)
Power Down Mode (75 μW typ)

FUNCTIONAL BLOCK DIAGRAM



*NO SCALING ON AD7890-2

GENERAL DESCRIPTION

The AD7890 is an eight-channel 12-bit data acquisition system. The part contains an input multiplexer, an on-chip track/hold amplifier, a high-speed 12-bit ADC, a +2.5 V reference and a high speed, serial interface. The part operates from a single +5 V supply and accepts an analog input range of ±10 V (AD7890-10), 0 to +4.096 V (AD7890-4) and 0 to +2.5 V (AD7890-2).

The multiplexer on the part is independently accessible. This allows the user to insert an antialiasing filter or signal conditioning, if required, between the multiplexer and the ADC. This means that one antialiasing filter can be used for all eight channels. Connection of an external capacitor allows the user to adjust the time given to the multiplexer settling to include any external delays in the filter or signal conditioning circuitry.

Output data from the AD7890 is provided via a high speed bidirectional serial interface port. The part contains an on-chip control register, allowing control of channel selection, conversion start and power-down via the serial port. Versatile, high speed logic ensures easy interfacing to serial ports on microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7890 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

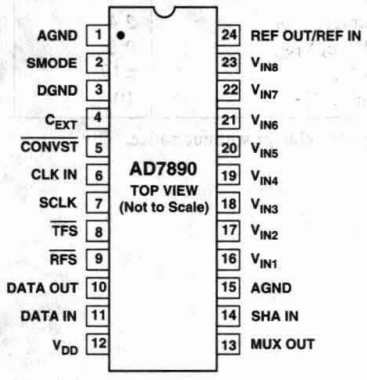
Power dissipation in normal mode is low at 30 mW typ and the part can be placed in a standby (power-down) mode if it is not required to perform conversions. The AD7890 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3" wide, plastic or hermetic dual-in-line package or in a 24-pin small outline package (SOIC).

ORDERING GUIDE

Model	Temperature Range	Linearity Error	Package Option*
AD7890AN-2	–40°C to +85°C	±1 LSB	N-24
AD7890BN-2	–40°C to +85°C	±1/2 LSB	N-24
AD7890AR-2	–40°C to +85°C	±1 LSB	R-24
AD7890BR-2	–40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-2	–55°C to +125°C	±1 LSB	Q-24
AD7890AN-4	–40°C to +85°C	±1 LSB	N-24
AD7890BN-4	–40°C to +85°C	±1/2 LSB	N-24
AD7890AR-4	–40°C to +85°C	±1 LSB	R-24
AD7890BR-4	–40°C to +85°C	±1/2 LSB	R-24
AD7890SQ-4	–55°C to +125°C	±1 LSB	Q-24
AD7890AN-10	–40°C to +85°C	±1 LSB	N-24
AD7890BN-10	–40°C to +85°C	±1/2 LSB	N-24
AD7890AR-10	–40°C to +85°C	±1 LSB	R-24
AD7890BR-10	–40°C to +85C	±1/2 LSB	R-24
AD7890SQ-10	–55°C to +125°C	±1 LSB	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD7890 PINOUT



To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7890–SPECIFICATIONS (V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V, $f_{CLK\ IN}$ = 2.5 MHz external, MUX OUT connect to SHA IN. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					Using External $\overline{\text{CONVST}}$. Any Channel
Signal to (Noise + Distortion) Ratio[2]	70	70	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Total Harmonic Distortion (THD)[2]	–78	–78	–78	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Peak Harmonic or Spurious Noise[2]	–79	–79	–79	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz[3]
Intermodulation Distortion					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 100 kHz[3]
2nd Order Terms	–80	–80	–80	dB typ	
3rd Order Terms	–80	–80	–80	dB typ	
Channel-to-Channel Isolation[2]	–80	–80	–80	dB max	f_{IN} = 1 kHz Sine Wave
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[2]	±1	±0.5	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±2.5	±2.5	±2.5	LSB max	
Full-Scale Error Match[4]	2	2	2	LSB max	
AD7890-2, AD7890-4					
Unipolar Offset Error[2]	±2	±2	±2	LSB max	
Unipolar Offset Error Match	2	2	2	LSB max	
AD7890-10 Only					
Negative Full-Scale Error[2]	±2	±2	±2	LSB max	
Bipolar Zero Error[2]	±4	±4	±4	LSB max	
Bipolar Zero Error Match	2	2	2	LSB max	
ANALOG INPUTS					
AD7890-10					
Input Voltage Range	±10	±10	±10	Volts	
Input Resistance	20	20	20	kΩ min	
AD7890-4					
Input Voltage Range	0 to +4.096	0 to +4.096	0 to +4.096	Volts	
Input Resistance	11	11	11	kΩ min	
AD7890-2					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	50	50	200	nA max	
MUX OUT OUTPUT					
Output Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Output Resistance					
(AD7890-10, AD7890-4)	3/5	3/5	3/5	kΩ min/kΩ max	
(AD7890-2)	2	2	2	kΩ max	Assuming V_{IN} Is Driven from Low Impedance
SHA IN INPUT					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	±50	±50	±50	nA max	
REFERENCE OUTPUT/INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[5]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	2	2	2	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	

Specifications subject to change without notice.

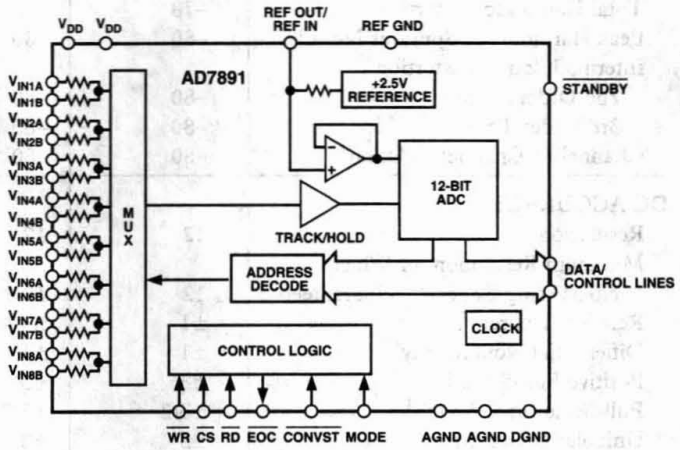
LC²MOS 8-Channel, 12-Bit High Speed Data Acquisition System

AD7891

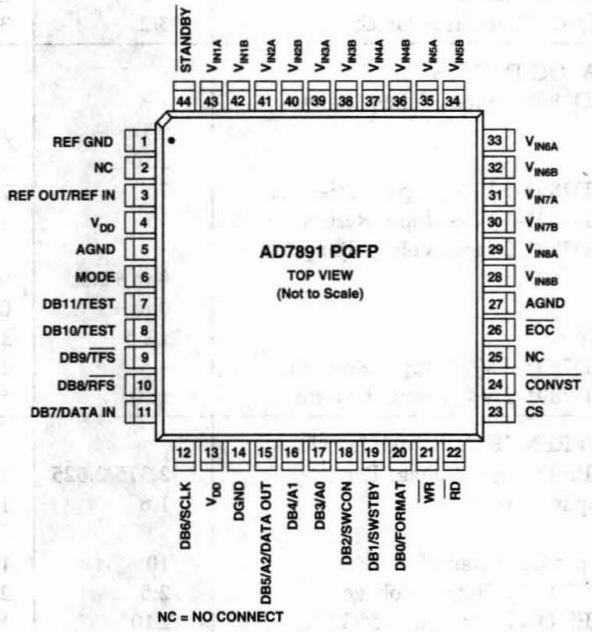
FEATURES
- Fast 12-Bit ADC with 1.6 µs Conversion Time
- Eight Single-Ended Analog Input Channels
- Overvoltage Protection on Each Channel
- Selection of Input Ranges:
  - ±5 V, ±10 V for AD7891-1
  - 0 to +2.5 V, 0 to +5 V, ±2.5 V for AD7891-2
- Parallel and Serial Interface
- On-Chip Track/Hold Amplifier
- On-Chip Reference
- Single Supply, Low Power Operation (85 mW max)
- Power-Down Mode (75 µW typ)

APPLICATIONS
- Data Acquisition Systems
- Motor Control
- Mobile Communication Base Stations
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PQFP Pinout



GENERAL DESCRIPTION

The AD7891 is an eight-channel 12-bit data acquisition system with a choice of either parallel or serial interface structure. The part contains an input multiplexer, an on-chip track/hold amplifier, a high speed 12-bit ADC, a +2.5 V reference and a high speed interface. The part operates from a single +5 V supply and accepts a variety of analog input ranges across two models, the AD7891-1 (±5 V and ±10 V) and the AD7891-2 (0 V to +2.5 V, 0 V to +5 V and ±2.5 V).

The AD7891 provides the option of either a parallel interface or serial interface structure determined by the MODE pin. The part has standard control inputs and fast data access times for both the serial and parallel interfaces which ensures easy interfacing to modern microprocessors, microcontrollers and digital signal processors.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

Power dissipation in normal mode is 90 mW typical while in the standby mode this is reduced to 75 µW typ. The part is available in a 44-pin plastic quad flat-pack (PQFP) and a 44-lead plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. The AD7891 is a complete monolithic 12-bit data acquisition system combining an eight-channel multiplexer, 12-bit ADC, +2.5 V reference and track/hold amplifier on a single chip.
2. The AD7891-2 features a conversion time of 1.6 µs and an acquisition time of 0.4 µs. This allows a sample rate of 500 kSPS when sampling one channel and 62.5 kSPS when channel hopping. These sample rates can be achieved using either a software or hardware convert start. The AD7891-1 has an acquisition time of 0.6 µs when using a hardware convert start and an acquisition time of 0.7 µs when using a software convert start. These acquisition times allow sample rates of 454.5 kSPS and 435 kSPS respectively for hardware and software convert start.
3. Each channel on the AD7891 has overvoltage protection. This means that an overvoltage on an unselected channel does not affect the conversion on a selected channel. The AD7891-1 can withstand overvoltages of ±17 V.

AD7891–SPECIFICATIONS (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	B Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]				Sample Rate = 454.5 kSPS[3] (AD7891-1), 500 kSPS[3] (AD7891-2). Any Channel
Signal to (Noise+Distortion) Ratio[4]				
@ +25°C	70	70	dB min	
T_{MIN} to T_{MAX}	70	70	dB min	
Total Harmonic Distortion[4]	–78	–78	dB max	
Peak Harmonic or Spurious Noise[4]	–80	–80	dB max	
Intermodulation Distortion[4]				fa = 9 kHz, fb = 9.5 kHz
2nd Order Terms	–80	–80	dB typ	
3rd Order Terms	–80	–80	dB typ	
Channel-to-Channel Isolation[4]	–80	–80	dB max	
DC ACCURACY				Any Channel
Resolution	12	12	Bits	
Minimum Resolution for Which				
No Missing Codes are Guaranteed	12	12	Bits	
Relative Accuracy[4]	±1	±3/4	LSB max	
Differential Nonlinearity[4]	±1	±1	LSB max	
Positive Full-Scale Error[4]	±3	±3	LSB max	
Full-Scale Error Match[4]	±3/2	±3/2	LSB max	
Unipolar Offset Error	±3	±3	LSB max	Input Ranges of 0 V to +2.5 V, 0 V to +5 V
Unipolar Offset Error Match	1	1	LSB max	Input Ranges of 0 V to +2.5 V, 0 V to +5 V
Negative Full-Scale Error[4]	±3	±3	LSB max	Input Ranges of ±2.5 V, ±5 V, ±10 V
Bipolar Zero Error	±4	±4	LSB max	Input Ranges of ±2.5 V, ±5 V, ±10 V
Bipolar Zero Error Match	3/2	3/2	LSB max	Input Ranges of ±2.5 V, ±5 V, ±10 V
ANALOG INPUTS				
AD7891-1 Input Voltage Range				
	±5	±5	Volts	Input Applied to Both V_{INXA} and V_{INXB}
	±10	±10	Volts	Input Applied to V_{INXA}, V_{INXB} = AGND
AD7891-1 V_{INXA} Input Resistance	7.5	7.5	kΩ min	Input Range of ±5 V
AD7891-1 V_{INXA} Input Resistance	15	15	kΩ min	Input Range of ±10 V
AD7891-2 Input Voltage Range				
	0 to +2.5	0 to +2.5	Volts	Input Applied to Both V_{INXA} and V_{INXB}
	0 to +5	0 to +5	Volts	Input Applied to V_{INXA}, V_{INXB} = AGND
	±2.5	±2.5	Volts	Input Applied to V_{INXA}, V_{INXB} = REF IN[5]
AD7891-2 V_{INXA} Input Resistance	1.5	1.5	kΩ min	Input Ranges of ±2.5 V and 0 to +5 V
AD7891-2 V_{INXA} Input Current	±50	±50	nA max	Input Range of 0 V to +2.5 V
REFERENCE INPUT/OUTPUT				
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[6]	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	mV max	
REF OUT Temperature Coefficient	25	25	ppm/°C typ	
REF OUT Output Impedance	5	5	kΩ nom	See REF IN Input Impedance
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{INH}	±10	±10	μA max	
Input Capacitance,[6] C_{IN}	10	10	pF max	

Specifications subject to change without notice.

LC²MOS Single Supply, 12-Bit 600 kSPS ADC

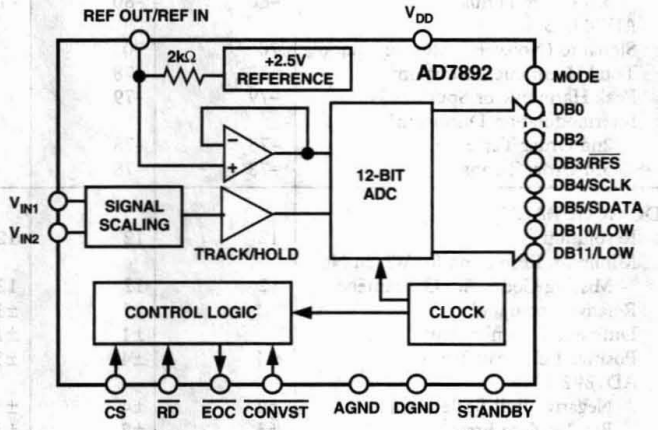
AD7892

FEATURES

Fast 12-Bit ADC with 1.47 µs Conversion Time
600 kSPS Throughput Rate (AD7892-3)
500 kSPS Throughput Rate (AD7892-1, AD7892-2)
Single Supply Operation
On-Chip Track/Hold Amplifier
Selection of Input Ranges:
- **±10 V or ±5 V for AD7892-1**
- **0 V to +2.5 V for AD7892-2**
- **±2.5 V for AD7892-3**

High Speed Serial and Parallel Interface
Low Power, 60 mW typ
Overvoltage Protection on Analog Inputs (AD7892-1 and AD7892-3)

FUNCTIONAL BLOCK DIAGRAM



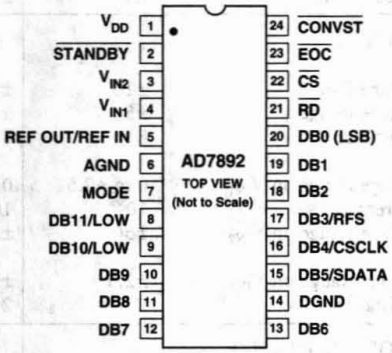
GENERAL DESCRIPTION

The AD7892 is a high speed, low power, 12-bit A/D converter that operates from a single +5 V supply. The part contains a 1.47 µs successive approximation ADC, an on-chip track/hold amplifier, an internal +2.5 V reference and on-chip versatile interface structures that allow both serial and parallel connection to a microprocessor. The part accepts an analog input range of ±10 V or ±5 V (AD7892-1), 0 V to +2.5 V (AD7892-2) and ±2.5 V (AD7892-3). Overvoltage protection on the analog inputs for the AD7892-1 and AD7892-3 allows the input voltage to go to ±17 V or ±7 V respectively without damaging the ports.

The AD7892 offers a choice of two data output formats: a single, parallel, 12-bit word or serial data. Fast bus access times and standard control inputs ensure easy parallel interface to microprocessors and digital signal processors. A high speed serial interface allows direct connection to the serial ports of microcontrollers and digital signal processors.

PIN CONFIGURATION

DIP and SOIC



ORDERING GUIDE

Model	Input Range	Sample Rate	Relative Accuracy	Temperature Range	Package Option[1]
AD7892AN-1	±5 V or ±10 V	500 kSPS		–40°C to +85°C	N-24
AD7892BN-1	±5 V or ±10 V	500 kSPS	±1 LSB	–40°C to +85°C	N-24
AD7892AR-1	±5 V or ±10 V	500 kSPS		–40°C to +85°C	R-24
AD7892BR-1	±5 V or ±10 V	500 kSPS	±1 LSB	–40°C to +85°C	R-24
AD7892SQ-1	±5 V or ±10 V	500 kSPS	±1 LSB	–55°C to +125°C	Q-24
AD7892AN-2	0 V to +2.5 V	500 kSPS		–40°C to +85°C	N-24
AD7892BN-2	0 V to +2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	N-24
AD7892AR-2	0 V to +2.5 V	500 kSPS		–40°C to +85°C	R-24
AD7892BR-2	0 V to +2.5 V	500 kSPS	±1 LSB	–40°C to +85°C	R-24
AD7892AN-3	±2.5 V	600 kSPS		–40°C to +85°C	N-24
AD7892BN-3	±2.5 V	600 kSPS	±1 LSB	–40°C to +85°C	N-24
AD7892AR-3	±2.5 V	600 kSPS		–40°C to +85°C	R-24
AD7892BR-3	±2.5 V	600 kSPS	±1 LSB	–40°C to +85°C	R-24
EVAL-AD7892-2CB[2] – Evaluation Board					
EVAL-AD7892-3CB[2] – Evaluation Board					
EVAL-CONTROL BOARD[3] – Controller Board					

NOTES
[1]N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.
[2]These boards can be used as stand-alone evaluation boards or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices' evaluation boards ending in the CB designators.

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AD7892–SPECIFICATIONS (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
AD7892-1, AD7892-2					f_{IN} = 100 kHz. f_{SAMPLE} = 500 kSPS
Signal to (Noise + Distortion) Ratio[3]	70	70	70	dB min	
Total Harmonic Distortion[3]	–80	–80	–78	dB max	
Peak Harmonic or Spurious Noise[3]	–81	–81	–79	dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–80	–80	–78	dB max	
3rd Order Terms	–80	–80	–78	dB max	
AD7892-3					f_{IN} = 100 kHz. f_{SAMPLE} = 600 kSPS
Signal to (Noise + Distortion) Ratio[3]	70	70		dB min	
Total Harmonic Distortion[3]	–78	–78		dB max	
Peak Harmonic or Spurious Noise[3]	–79	–79		dB max	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–78	–78		dB max	
3rd Order Terms	–78	–78		dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]		±1	±1	LSB max	
Differential Nonlinearity[3]		±1	±1	LSB max	
Positive Full-Scale Error[3]	±4	±4	±5	LSB max	
AD7892-1					
Negative Full-Scale Error[3]	±4	±4	±5	LSB max	
Bipolar Zero Error[3]	±3	±2	±3	LSB max	
AD7892-3					
Negative Full-Scale Error[3]	±4	±4		LSB max	
Bipolar Zero Error[3]	±4	±3		LSB max	
AD7892-2 Only					
Unipolar Offset Error[3]	±4	±3	±4	LSB max	
ANALOG INPUT					
AD7892-1					
Input Voltage Range	±10	±10	±10	Volts	Input Applied to V_{IN1} with V_{IN2} Grounded
Input Voltage Range	±5	±5	±5	Volts	Input Applied to V_{IN1} and V_{IN2}
Input Resistance	8	8	8	kΩ min	Input Applied to V_{IN1} with V_{IN2} Grounded
AD7892-2					
Input Voltage Range on V_{IN1}	0 to +2.5	0 to +2.5	0 to +2.5	Volts	Input Applied to V_{IN1}
Input Current	10	10	50	nA max	
Input Voltage Range on V_{IN2}	±50	±50	±50	mV max	
AD7892-3					
Input Voltage Range on V_{IN1}	±2.5	±2.5		Volts	Input Applied to V_{IN1}
Input Resistance	2	2		kΩ min	
REFERENCE OUTPUT/INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Impedance	1.6	1.6	1.6	kΩ min	Resistor Connected to Internal Reference Node
Input Capacitance[4]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
T_{MIN} to T_{MAX}	±20	±20	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	5.5	5.5	5.5	kΩ nom	
CONVERSION RATE					
Conversion Time	1.47	1.47		µs max	AD7892-3
Track/Hold Acquisition Time[3]	0.2	0.2		µs max	AD7892-3
Conversion Time	1.6	1.6	1.68	µs max	AD7892-1 and AD7892-2
Track/Hold Acquisition Time[3]	0.4	0.4	0.32	µs max	AD7892-1 and AD7892-2
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}[5]					
Normal Operation	18	18	19	mA max	
Standby Mode[6]					
AD7892-1, AD7892-2	250	250	15	µA typ	
AD7892-3	40	40		µA max	
Power Dissipation[5]					
Normal Operation	90	90	95	mW max	V_{DD} = +5 V. Typically 60 mW
Standby Mode[6]					
AD7892-1, AD7892-2	1.25	1.25	0.075	mW typ	
AD7892-3	200	200		µW max	V_{DD} = +5 V. Typically 50 mW

Specifications subject to change without notice.

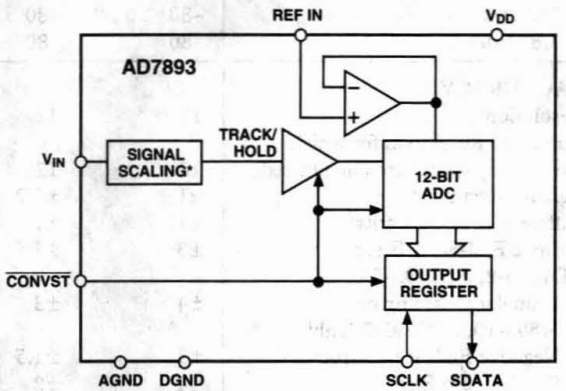
LC²MOS 12-Bit, Serial 6 µs ADC in 8-Pin Package

AD7893

FEATURES

Fast 12 Bit ADC with 6 µs Conversion Time
8-Pin Mini-DIP and SOIC
Single Supply Operation
High Speed, Easy-to-Use, Serial Interface
On-Chip Track/Hold Amplifier
Selection of Input Ranges
±10 V for AD7893-10
±2.5 V for AD7893-3
0 V to +2.5 V for AD7893-2
0 V to +5 V for AD7893-5
Low Power: 25 mW typ

FUNCTIONAL BLOCK DIAGRAM



*AD7893-5, AD7893-10, AD7893-3

GENERAL DESCRIPTION

The AD7893 is a fast, 12-bit ADC which operates from a single +5 V supply and is housed in a small 8-pin mini-DIP and 8-pin SOIC. The part contains a 6 µs successive approximation A/D converter, an on-chip track/hold amplifier, an on-chip clock and a high speed serial interface.

Output data from the AD7893 is provided via a high speed, serial interface port. This two-wire serial interface has a serial clock input and a serial data output with the external serial clock accessing the serial data from the part.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7893 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part accepts an analog input range of ±10 V (AD7893-10), ±2.5 V (AD7893-3), 0 V to +5 V (AD7893-5) or 0 V to +2.5 V (AD7893-2) and operates from a single +5 V supply consuming only 25 mW typical.

The AD7893 is fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a small, 8-pin, 0.3" wide, plastic or hermetic dual-in-line package (mini-DIP) and in an 8-pin, small outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Fast, 12-Bit ADC in 8-Pin Package
   The AD7893 contains a 6 µs ADC, a track/hold amplifier, control logic and a high speed serial interface, all in an 8-pin package. This offers considerable space saving over alternative solutions.
2. Low Power, Single Supply Operation
   The AD7893 operates from a single +5 V supply and consumes only 25 mW. This low power, single supply operation makes it ideal for battery-powered or portable applications.
3. High Speed Serial Interface
   The part provides high speed serial data and serial clock lines allowing for an easy, two-wire serial interface arrangement.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)	SNR (dB)	Package Option*
AD7893AN-2	–40°C to +85°C	±1 LSB	70 dB	N-8
AD7893BN-2	–40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7893AR-2	–40°C to +85°C	±1 LSB	70 dB	SO-8
AD7893BR-2	–40°C to +85°C	±1/2 LSB	72 dB	SO-8
AD7893SQ-2	–55°C to +125°C	±1 LSB	70 dB	Q-8
AD7893AN-5	–40°C to +85°C	±1 LSB	70 dB	N-8
AD7893BN-5	–40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7893AR-5	–40°C to +85°C	±1 LSB	70 dB	SO-8
AD7893BR-5	–40°C to +85°C	±1/2 LSB	72 dB	SO-8
AD7893SQ-5	–55°C to +125°C	±1 LSB	70 dB	Q-8
AD7893AN-10	–40°C to +85°C	±1 LSB	70 dB	N-8
AD7893BN-10	–40°C to +85°C	±1/2 LSB	72 dB	N-8
AD7893AR-10	–40°C to +85°C	±1 LSB	70 dB	SO-8
AD7893BR-10	–40°C to +85°C	±1/2 LSB	72 dB	SO-8
AD7893SQ-10	–55°C to +125°C	±1 LSB	70 dB	Q-8
AD7893AN-3†	–40°C to +85°C	±1 LSB	70 dB	N-8
AD7893AR-3†	–40°C to +85°C	±1 LSB	70 dB	SO-8

*N = Plastic DIP, Q = Cerdip, SO = SOIC. For outline information see Package Information section. †Contact factory for availability.

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AD7893–SPECIFICATIONS (V_{DD} = +5 V, AGND = DGND = 0 V, REF IN = +2.5 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Signal to (Noise + Distortion) Ratio[2]					
@ +25°C	70	70	70	dB min	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 117 kHz
Total Harmonic Distortion (THD)[2]	–80	–80	–80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 117 kHz
Peak Harmonic or Spurious Noise[2]	–80	–80	–80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 117 kHz
Intermodulation Distortion (IMD)[2]					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 117 kHz
2nd Order Terms	–80	–80	–80	dB max	
3rd Order Terms	–80	–80	–80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which					
No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	
Positive Full-Scale Error[2]	±3	±1.5	±3	LSB max	
AD7893-2, AD7893-5					
Unipolar Offset Error	±4	±3	±4	LSB max	
AD7893-10, AD7893-3 Only					
Negative Full-Scale Error[2]	±3	±1.5	±3	LSB max	
Bipolar Zero Error	±4	±2	±4	LSB max	
ANALOG INPUT					
AD7893-10					
Input Voltage Range	±10	±10	±10	Volts	
Input Resistance	16	16	16	kΩ min	
AD7893-3					
Input Voltage Range	±2.5	±2.5	±2.5	Volts	
Input Current	500	500	500	µA max	
AD7893-5					
Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	
Input Resistance	9	9	9	kΩ min	
AD7893-2					
Input Voltage Range	0 to +2.5	0 to +2.5	0 to +2.5	Volts	
Input Current	500	500	500	nA max	
REFERENCE INPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
Input Current	2	2	10	µA max	
Input Capacitance[3]	10	10	10	pF max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
Output Coding					
AD7893-10, AD7893-3	2s Complement				
AD7893-2, AD7893-5	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	6	6	6	µs max	
Track/Hold Acquisition Time[2]	1.5	1.5	1.5	µs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}	9	9	9	mA max	
Power Dissipation	45	45	45	mW max	Typically 25 mW

NOTES

[1]Temperature Ranges are as follows: A, B Versions: –40°C to +85°C, S Version: –55°C to +125°C.

[2]See Terminology.

[3]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

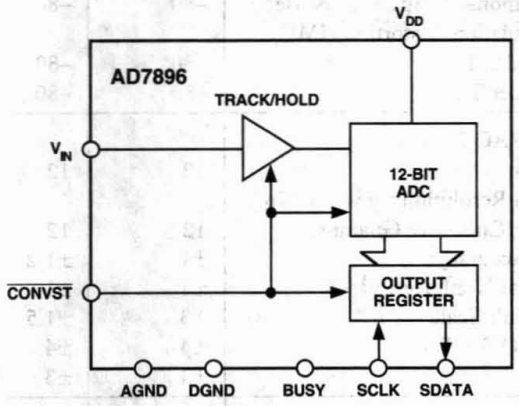
2.7 V to 5.5 V, 12-Bit, 8 µs ADC in 8-Pin SO/DIP

AD7896*

FEATURES

100 kHz Throughput Rate
Fast 12-Bit Sampling ADC with 8 µs Conversion Time
8-Pin Mini-DIP and SOIC
Single +2.7 V to +5.5 V Supply Operation
High Speed, Easy-to-Use, Serial Interface
On-Chip Track/Hold Amplifier
Analog Input Range is 0 V to Supply
High Input Impedance
Low Power: 9 mW typ

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7896 is a fast, 12-bit ADC which operates from a single +2.7 V to 5.5 V supply and is housed in a small 8-pin mini-DIP and 8-pin SOIC. The part contains an 8 µs successive approximation A/D converter, an on-chip track/hold amplifier, an on-chip clock and a high speed serial interface.

Output data from the AD7896 is provided via a high speed, serial interface port. This two-wire serial interface has a serial clock input and a serial data output with the external serial clock accessing the serial data from the part.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7896 is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The part accepts an analog input range of 0 V to V_{DD} and operates from a single +2.7 V to +5.5 V supply consuming only 9 mW typical. The V_{DD} input is also used as the reference for the part so that no external reference is required.

The AD7896 features a high sampling rate mode and, for low power applications, a proprietary automatic power down mode where the part automatically goes into power down once conversion is complete and "wakes up" before the next conversion cycle.

The part is available in a small, 8-pin, 0.3" wide, plastic or hermetic dual-in-line package (mini-DIP) and in an 8-pin, small outline IC (SOIC).

PRODUCT HIGHLIGHTS

1. Complete, 12-bit ADC in 8-Pin Package
   The AD7896 contains an 8 µs ADC, a track/hold amplifier, control logic and a high speed serial interface, all in an 8-pin DIP. The V_{DD} input is used as the reference for the part so no external reference is needed. This offers considerable space saving over alternative solutions.
2. Low Power, Single Supply Operation
   The AD7896 operates from a single +2.7 V to 5.5 V supply and consumes only 9 mW typical. The automatic power down mode, where the part goes into power down once conversion is complete and "wakes up" before the next conversion cycle, makes the AD7896 ideal for battery powered or portable applications.
3. High Speed Serial Interface
   The part provides high speed serial data and serial clock lines allowing for an easy, two-wire serial interface arrangement.

***Patent pending.**

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)	SNR (dB)	Package Option*
AD7896AN	–40°C to +85°C	±1 LSB	70 dB	N-8
AD7896BN	–40°C to +85°C	±1/2 LSB	70 dB	N-8
AD7896AR	–40°C to +85°C	±1 LSB	70 dB	SO-8
AD7896BR	–40°C to +85°C	±1/2 LSB	70 dB	SO-8
AD7896SQ	–55°C to +125°C	±1 LSB	70 dB	Q-8

*N = Plastic DIP; Q = Cerdip; SO = SOIC. For outline information see Package Information section.

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AD7896–SPECIFICATIONS (V_{DD} = +2.7 V to +5.5 V, AGND = DGND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	A Versions[1]	B Versions	S Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE [2]					
Signal to (Noise + Distortion) Ratio[3]					
@ +25°C	70	70	70	dB min	f_{IN} =10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}		70		dB min	
Total Harmonic Distortion (THD)[3]	–80	–80	–80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
Peak Harmonic or Spurious Noise[3]	–80	–80	–80	dB max	f_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
Intermodulation Distortion (IMD)[3]					fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 100 kHz
2nd Order Terms	–80	–80	–80	dB max	
3rd Order Terms	–80	–80	–80	dB max	
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	LSB max	
Positive Full-Scale Error[3]	±3	±1.5	±3	LSB max	
Unipolar Offset Error	±4	±4	±4	LSB max	V_{DD} = 5 V ± 10%
	±4	±3	±4	LSB max	V_{DD} = 2.7 V to 3.6 V
ANALOG INPUT					
Input Voltage Range	0 to +V_{DD}	0 to +V_{DD}	0 to +V_{DD}	Volts	
Input Current	±2	±2	±5	μA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.0	2.0	2.0	V min	V_{DD} = 2.7 V to 3.6 V
	2.4	2.4	2.4		V_{DD} = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.4	2.4	2.4	V min	I_{SOURCE} = 2 mA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 2 mA
Output Coding	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time:					
Mode 1 Operation	8	8	8.5	μs max	
Mode 2 Operation[5]	14	14	14.5	μs max	
Track/Hold Acquisition Time[3]	1.5	1.5	1.5	μs max	
POWER REQUIREMENTS					
V_{DD}	+2.7/+5.5	+2.7/+5.5	+2.7/+5.5	V min/max	
I_{DD}	4	4	4	mA max	Digital Input @ DGND, V_{DD} = 2.7 V to 3.6 V
	5	5	5	mA max	Digital Inputs @ DGND, V_{DD} = 5 V ± 10%
Power Dissipation	10.8	10.8	10.8	mW max	V_{DD} = 2.7 V, Typically 9 mW
Power-Down Mode					Digital Inputs @ DGND
I_{DD} @ +25°C	5	5	5	μA max	V_{DD} = 2.7 V to 3.6 V
T_{MIN} to T_{MAX}	15	15	75	μA max	V_{DD} = 2.7 V to 3.6 V
I_{DD} @ +25°C	50	50	50	μA max	V_{DD} = 5 V ± 10%
T_{MIN} to T_{MAX}	150	150	500	μA max	V_{DD} = 5 V ± 10%
Power Dissipation @ +25°C	13.5	13.5	13.5	μW max	V_{DD} = 2.7 V

NOTES

[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.

[2]Applies to Mode 1 operation. See section on operating modes.

[3]See Terminology.

[4]Sample tested @ +25°C to ensure compliance.

[5]This 14 μs includes the "wake-up" time from standby. This "wake-up" time is timed from the rising edge of $\overline{\text{CONVST}}$, whereas conversion is timed from the falling edge of $\overline{\text{CONVST}}$, for narrow $\overline{\text{CONVST}}$ pulse width the conversion time is effectively the "wake-up" time plus conversion time hence 14 μs. This can be seen from Figure 3. Note that if the $\overline{\text{CONVST}}$ pulse width is greater than 6 μs then the effective conversion time will increase beyond 14 μs.

Specifications subject to change without notice.

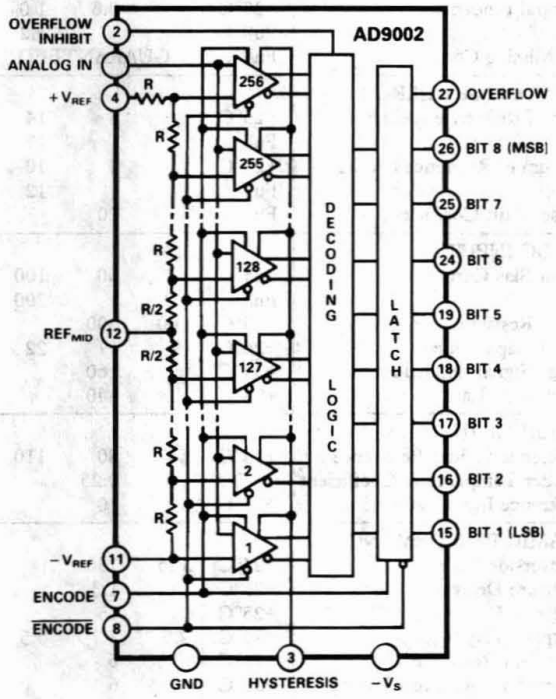
High Speed 8-Bit Monolithic A/D Converter

AD9002

FEATURES
150 MSPS Encode Rate
Low Input Capacitance: 17 pF
Low Power: 750 mW
–5.2 V Single Supply
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Systems
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9002 is an 8-bit, high speed, analog-to-digital converter. The AD9002 is fabricated in an advanced bipolar process which allows operation at sampling rates in excess of 150 megasamples/second. Functionally, the AD9002 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the ECL compatible output latches.

An exceptionally wide large signal analog input bandwidth of 160 MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9002 allows very accurate acquisition of high speed pulse inputs, without an external track-and-hold. The comparator output decoding scheme minimizes false codes which is critical to high speed linearity.

The AD9002 provides an external hysteresis control pin which can be used to optimize comparator sensitivity to further improve performance. Additionally, the AD9002's low power dissipation of 750 mW makes it usable over the full extended temperature range. The AD9002 also incorporates an overflow bit to indicate overrange inputs. This overflow output can be disabled with the overflow inhibit pin.

The AD9002 is available in two grades, one with 0.5 LSB linearity and one with 0.75 LSB linearity. Both versions are offered in an industrial grade, –25°C to +85°C, packaged in a 28-pin DIP and a 28-pin JLCC. The military temperature range devices, –55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

ORDERING GUIDE

Device	Linearity	Temperature Range	Package Option*
AD9002AD	0.75 LSB	–25°C to +85°C	D-28
AD9002BD	0.50 LSB	–25°C to +85°C	D-28
AD9002AJ	0.75 LSB	–25°C to +85°C	J-28
AD9002BJ	0.50 LSB	–25°C to +85°C	J-28
AD9002SD	0.75 LSB	–55°C to +125°C	D-28
AD9002SE	0.75 LSB	–55°C to +125°C	E-28A
AD9002TD	0.50 LSB	–55°C to +125°C	D-28
AD9002TE	0.50 LSB	–55°C to +125°C	E-28A

*For outline information see Package Information section.

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AD9002–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($-V_S = -5.2$ V; Differential Reference Voltage = 2.0 V; unless otherwise noted)

Parameter	Temp	AD9002AD/AJ Min	AD9002AD/AJ Typ	AD9002AD/AJ Max	AD9002BD/BJ Min	AD9002BD/BJ Typ	AD9002BD/BJ Max	AD9002SD/SE Min	AD9002SD/SE Typ	AD9002SD/SE Max	AD9002TD/TE Min	AD9002TD/TE Typ	AD9002TD/TE Max	Units
RESOLUTION		8			8			8			8			Bits
DC ACCURACY														
Differential Linearity	+25°C		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR														
Top of Reference Ladder	+25°C		8	14		8	14		8	14		8	14	mV
	Full			17			17			17			17	mV
Bottom of Reference Ladder	+25°C		4	10		4	10		4	10		4	10	mV
	Full			12			12			12			12	mV
Offset Drift Coefficient	Full		20			20			20			20		µV/°C
ANALOG INPUT														
Input Bias Current	+25°C		60	100		60	100		60	100		60	100	µA
	Full			200			200			200			200	µA
Input Resistance	+25°C	100	200		100	200		100	200		100	200		kΩ
Input Capacitance	+25°C		17	22		17	22		17	22		17	22	pF
Large Signal Bandwidth	+25°C		160			160			160			160		MHz
Input Slew Rate	+25°C		440			440			440			440		V/µs
REFERENCE INPUT														
Reference Ladder Resistance	+25°C	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient			0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C		10			10			10			10		MHz
DYNAMIC PERFORMANCE														
Conversion Rate	+25°C	125	150		125	150		125	150		125	150		MSPS
Aperture Delay	+25°C		1.3			1.3			1.3			1.3		ns
Aperture Uncertainty (Jitter)	+25°C		15			15			15			15		ps
Output Delay (t_{PD})	+25°C	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	2.5	3.7	5.5	ns
Transient Response	+25°C		6			6			6			6		ns
Overvoltage Recovery Time	+25°C		6			6			6			6		ns
Output Rise Time	+25°C			3.0			3.0			3.0			3.0	ns
Output Fall Time	+25°C			2.5			2.5			2.5			2.5	ns
Output Time Skew	+25°C		0.6			0.6			0.6			0.6		ns
ENCODE INPUT														
Logic "1" Voltage	Full	–1.1			–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full			–1.5			–1.5			–1.5			–1.5	V
Logic "1" Current	Full			150			150			150			150	µA
Logic "0" Current	Full			120			120			120			120	µA
Input Capacitance	+25°C		3			3			3			3		pF
Encode Pulse Width (Low)	+25°C	1.5			1.5			1.5			1.5			ns
Encode Pulse Width (High)	+25°C	1.5			1.5			1.5			1.5			ns
OVERFLOW INHIBIT INPUT														
0 V Iutput Current	Full		144	300		144	300		144	300		144	300	µA
AC LINEARITY														
Effective Bits	+25°C		7.6			7.6			7.6			7.6		Bits
In-Band Harmonics														
dc to 1.23 MHz	+25°C	48	55		48	55		48	55		48	55		dB
dc to 9.3 MHz	+25°C		50			50			50			50		dB
dc to 19.3 MHz	+25°C		44			44			44			44		dB
Signal-to-Noise Ratio	+25°C	46	47.6		46	47.6		46	47.6		46	47.6		dB
Two Tone Intermod Rejection	+25°C		60			60			60			60		dB
DIGITAL OUTPUT														
Logic "1" Voltage	Full	–1.1			–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full			–1.5			–1.5			–1.5			–1.5	V
POWER SUPPLY														
Supply Current (–5.2 V)	+25°C		145	175		145	175		145	175		145	175	mA
	Full			200			200			200			200	mA
Nominal Power Dissipation	+25°C		750			750			750			750		mW
Reference Ladder Dissipation	+25°C		50			50			50			50		mW
Power Supply Rejection Ratio	+25°C		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	mV/V

Specifications subject to change without notice.

ANALOG DEVICES

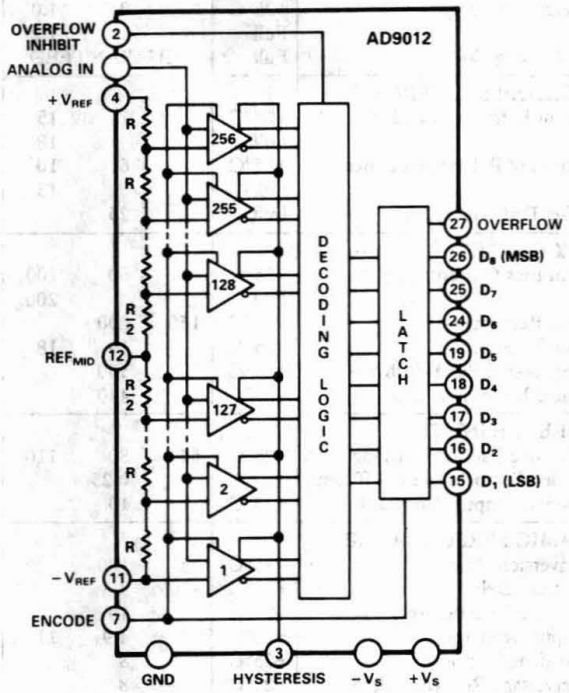
High Speed 8-Bit TTL A/D Converter

AD9012

FEATURES
100 MSPS Encode Rate
Very Low Input Capacitance – 16 pF
Low Power – 1 W
TTL Compatible Outputs
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Radar Guidance
Digital Oscilloscopes/ATE Equipment
Laser/Radar Warning Receivers
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Communication/Signal Intelligence

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9012 is an 8-bit, ultrahigh speed, analog-to-digital converter. The AD9012 is fabricated in an advanced bipolar process, which allows operation at sampling rates up to 100 megasamples/second. Functionally, the AD9012 is comprised of 256 parallel comparator stages whose outputs are decoded to drive the TTL compatible output latches.

The exceptionally wide large signal analog input bandwidth of 160 MHz is due to an innovative comparator design and very close attention to device layout considerations. The wide input bandwidth of the AD9012 allows very accurate acquisition of high speed pulse inputs without an external track-and-hold. The comparator output decoding scheme minimizes false codes, which is critical to high speed linearity.

The AD9012 is available in two grades, one with 0.5 LSB linearity and one with 0.75 LSB linearity. Both versions are offered in an industrial grade, –25°C to +85°C, packaged in a 28-pin DIP and a 28-pin JLCC. The military temperature range devices, –55°C to +125°C, are available in ceramic DIP and LCC packages and are compliant to MIL-STD-883 Class B.

The AD9012 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9012/883B data sheet for detailed specifications.

ORDERING GUIDE

Device	Linearity	Temperature Range	Package Option*
AD9012AQ	0.75 LSB	–25°C to +85°C	Q-28
AD9012BQ	0.50 LSB	–25°C to +85°C	Q-28
AD9012AJ	0.75 LSB	–25°C to +85°C	J-28
AD9012BJ	0.50 LSB	–25°C to +85°C	J-28
AD9012SQ	0.75 LSB	–55°C to +125°C	Q-28
AD9012SE	0.75 LSB	–55°C to +125°C	E-28A
AD9012TQ	0.50 LSB	–55°C to +125°C	Q-28
AD9012TE	0.50 LSB	–55°C to +125°C	E-28A

*E = Leadless Ceramic Chip Carrier; J = Ceramic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

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AD9012–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S = +5.0$ V; $-V_S = -5.2$ V; Differential Reference Voltage = 2.0 V; unless otherwise noted)

Parameter	Temp	AD9012AQ/AJ Min	AD9012AQ/AJ Typ	AD9012AQ/AJ Max	AD9012BQ/BJ Min	AD9012BQ/BJ Typ	AD9012BQ/BJ Max	AD9012SQ/SE Min	AD9012SQ/SE Typ	AD9012SQ/SE Max	AD9012TQ/TE Min	AD9012TQ/TE Typ	AD9012TQ/TE Max	Units
RESOLUTION		8			8			8			8			Bits
DC ACCURACY														
Differential Linearity	+25°C		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full			1.0			0.75			1.0			0.75	LSB
Integral Linearity	+25°C		0.6	1.0		0.4	0.5		0.6	1.0		0.4	0.5	LSB
	Full			1.2			1.2			1.2			1.2	LSB
No Missing Codes	Full	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
INITIAL OFFSET ERROR														
Top of Reference Ladder	+25°C		7	15		7	15		7	15		7	15	mV
	Full			18			18			18			18	mV
Bottom of Reference Ladder	+25°C		6	10		6	10		6	10		6	10	mV
	Full			13			13			13			13	mV
Offset Drift Coefficient	Full		25			25			25			25		µV/°C
ANALOG INPUT														
Input Bias Current	+25°C		60	100		60	100		60	100		60	100	µA
	Full			200			200			200			200	µA
Input Resistance	+25°C	150	200		150	200		150	200		150	200		kΩ
Input Capacitance	+25°C		16	18		16	18		16	18		16	18	pF
Large Signal Bandwidth	+25°C		160			160			160			160		MHz
Analog Input Slew Rate	+25°C		440			440			440			440		V/µs
REFERENCE INPUT														
Reference Ladder Resistance	+25°C	64	80	110	64	80	110	64	80	110	64	80	110	Ω
Ladder Temperature Coefficient			0.25			0.25			0.25			0.25		Ω/°C
Reference Input Bandwidth	+25°C		10			10			10			10		MHz
DYNAMIC PERFORMANCE														
Conversion Rate	+25°C	75	100		75	100		75	100		75	100		MSPS
Aperture Delay	+25°C		3.8			3.8			3.8			3.8		ns
Aperture Uncertainty (Jitter)	+25°C		15			15			15			15		ps
Output Delay (t_{PD})	+25°C	4	4.9	11	4	4.9	11	4	4.9	11	4	4.9	11	ns
Transient Response	+25°C		8			8			8			8		ns
Overvoltage Recovery Time	+25°C		8			8			8			8		ns
Output Rise Time	+25°C		6.6	8.0		6.6	8.0		6.6	8.0		6.6	8.0	ns
Output Fall Time	+25°C		3.3	4.3		3.3	4.3		3.3	4.3		3.3	4.3	ns
Output Time Skew	+25°C		3.0			3.0			3.0			3.0		ns
ENCODE INPUT														
Logic "1" Voltage	Full	2.0			2.0			2.0			2.0			V
Logic "0" Voltage	Full			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full			250			250			250			250	µA
Logic "0" Current	Full			400			400			400			400	µA
Input Capacitance	+25°C		2.5			2.5			2.5			2.5		pF
Encode Pulse Width (Low)	+25°C	2.5			2.5			2.5			2.5			ns
Encode Pulse Width (High)	+25°C	2.5			2.5			2.5			2.5			ns
OVERFLOW INHIBIT INPUT														
0 V Iutput Current	Full		200	250		200	250		200	250		200	250	µA
AC LINEARITY														
Effective Bits	+25°C		7.5			7.5			7.5			7.5		Bits
In-Band Harmonics														
dc to 1.23 MHz	+25°C	48	55		48	55		48	55		48	55		dBc
dc to 9.3 MHz	+25°C		50			50			50			50		dBc
dc to 19.3 MHz	+25°C		44			44			44			44		dBc
Signal-to-Noise Ratio	+25°C	46	47.6		46	47.6		46	47.6		46	47.6		dBc
Noise Power Ratio	+25°C		37			37			37			37		dBc
DIGITAL OUTPUT														
Logic "1" Voltage	Full	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full			0.4			0.4			0.4			0.4	V
POWER SUPPLY														
Positive Supply Current (+5.0 V)	+25°C		33	45		33	45		33	45		33	45	mA
	Full			48			48			48			48	mA
Supply Current (–5.2 V)	+25°C		152	179		152	179		152	179		152	179	mA
	Full			191			191			191			191	mA
Nominal Power Dissipation	+25°C		955			955			955			955		mW
Reference Ladder Dissipation	+25°C		44			44			44			44		mW
Power Supply Rejection Ratio	+25°C		0.85	2.5		0.85	2.5		0.8	2.5		0.8	2.5	mV/V

Specifications subject to change without notice.

ANALOG DEVICES

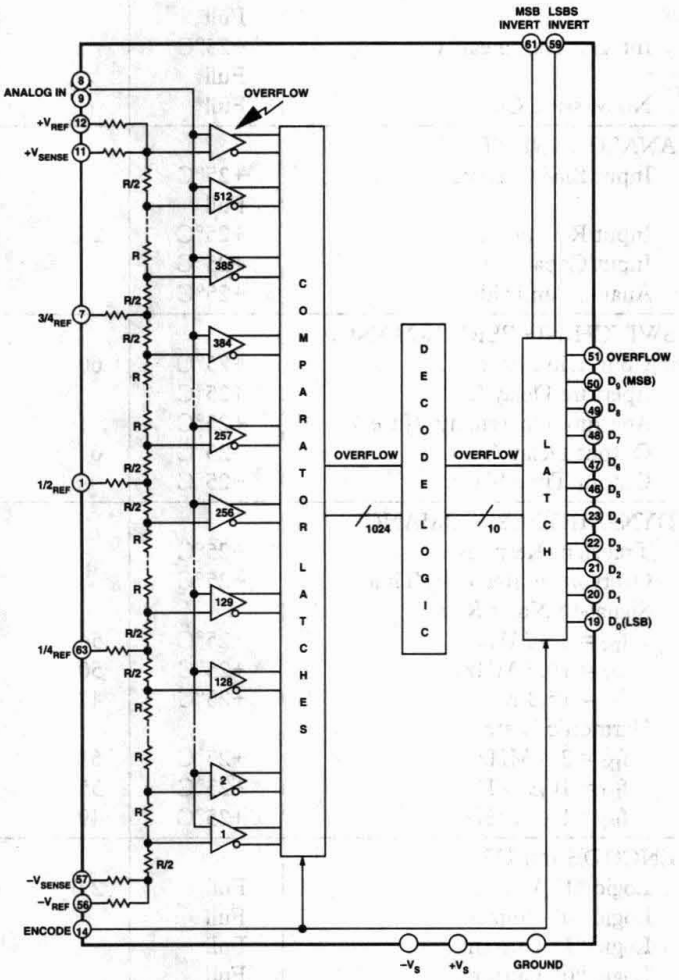
10-Bit 60 MSPS A/D Converter

AD9020

FEATURES
Monolithic 10-Bit/60 MSPS Converter
TTL Outputs
Bipolar (±1.75 V) Analog Input
56 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9020 A/D converter is a 10-bit monolithic converter capable of word rates of 60 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Encode and outputs are TTL-compatible, making the AD9020 an ideal candidate for use in low power systems. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0°C to +70°C and –55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9020 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9020/883B data sheet for detailed specifications.

ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9020JZ	0°C to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020JE	0°C to +70°C	68-Pin Ceramic LCC	E-68A
AD9020KZ	0°C to +70°C	68-Pin Leaded Ceramic	Z-68
AD9020KE	0°C to +70°C	68-Pin Ceramic LCC	E-68A
AD9020SZ/883	–55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020SE/883	–55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020TZ/883	–55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9020TE/883	–55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9020/PCB	0°C to +70°C	Evaluation Board	

*For outline information see Package Information section.

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AD9020–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = ±5 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 40 MSPS unless otherwise noted)

Parameter (Conditions)	Temp	AD9020JE/JZ Min	AD9020JE/JZ Typ	AD9020JE/JZ Max	AD9020KE/KZ Min	AD9020KE/KZ Typ	AD9020KE/KZ Max	Units
RESOLUTION		10			10			Bits
DC ACCURACY								
Differential Nonlinearity	+25°C		1.0	1.25		0.75	1.0	LSB
	Full			1.5			1.25	LSB
Integral Nonlinearity	+25°C		1.25	2.0		1.0	1.5	LSB
	Full			2.5			2.0	LSB
No Missing Codes	Full					Guaranteed		
ANALOG INPUT								
Input Bias Current	+25°C		0.4	1.0		0.4	1.0	mA
	Full			2.0			2.0	mA
Input Resistance	+25°C	2.0	7.0		2.0	7.0		kΩ
Input Capacitance	+25°C		45			45		pF
Analog Bandwidth	+25°C		175			175		MHz
SWITCHING PERFORMANCE								
Conversion Rate	+25°C	60			60			MSPS
Aperture Delay (t_A)	+25°C		1			1		ns
Aperture Uncertainty (Jitter)	+25°C		5			5		ps, rms
Output Delay (t_{OD})	+25°C	6	10	13	6	10	13	ns
Output Time Skew	+25°C		3	5		3	5	ns
DYNAMIC PERFORMANCE								
Transient Response	+25°C		10			10		ns
Overvoltage Recovery Time	+25°C		10			10		ns
Signal-to-Noise Ratio								
f_{IN} = 2.3 MHz	+25°C	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	50	53		50	53		dB
f_{IN} = 15.3 MHz	+25°C	47	50		47	50		dB
Harmonic Distortion								
f_{IN} = 2.3 MHz	+25°C	61	67		61	67		dBc
f_{IN} = 10.3 MHz	+25°C	55	59		55	59		dBc
f_{IN} = 15.3 MHz	+25°C	49	53		49	53		dBc
ENCODE INPUT								
Logic "1" Voltage	Full	2.0			2.0			V
Logic "0" Voltage	Full			0.8			0.8	V
Logic "1" Current	Full			20			20	µA
Logic "0" Current	Full			800			800	µA
Input Capacitance	+25°C		5			5		pF
Pulse Width (High)	+25°C	6			6			ns
Pulse Width (Low)	+25°C	6			6			ns
DIGITAL OUTPUTS								
Logic "1" Voltage (I_{OH} = 2 mA)	Full	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 6 mA)	Full			0.4				V
POWER SUPPLY								
$+V_S$ Supply Current	+25°C		440	530		440	530	mA
	Full			542			542	mA
$-V_S$ Supply Current	+25°C		140	170		140	170	mA
	Full			177			177	mA
Power Dissipation	+25°C		2.8	3.3		2.8	3.3	W
	Full			3.4			3.4	W
Power Supply Rejection Ratio (PSRR)	Full		6	10		6	10	mV/V

Specifications subject to change without notice.

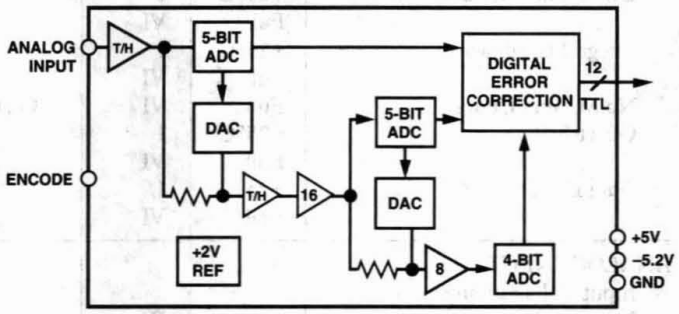
12-Bit 20 MSPS Monolithic A/D Converter

AD9022

FEATURES
Monolithic
12-Bit 20 MSPS A/D Converter
Low Power Dissipation: 1.4 Watts
On-Chip T/H and Reference
High Spurious-Free Dynamic Range
TTL Logic

APPLICATIONS
Radar Receivers
Digital Communications
Digital Instrumentation
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9022 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution. It is a companion unit to the AD9023; the primary difference between the two is that all logic for the AD9022 is TTL compatible, while the AD9023 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

Operating from +5 V and –5.2 V supplies, the AD9022 provides excellent dynamic performance. Sampling at 20 MSPS with A_{IN} = 1 MHz, the spurious-free dynamic range (SFDR) is typically 76 dB; with A_{IN} = 9.6 MHz, SFDR is 74 dB. SNR is typically 65 dB.

The on-board T/H has a 110 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many under-sampling signal processing applications, such as in direct IF-to-digital conversion.

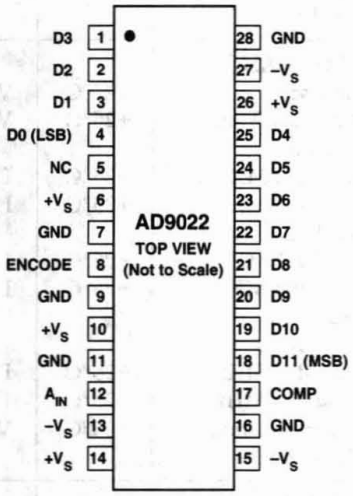
To maintain dynamic performance at higher IFs, monolithic RF track-and-holds (such as the AD9100 and AD9101 Samplifier™) can be used with the AD9022 to process signals up to and beyond 70 MHz.

With DNL typically less than 0.5 LSB and 20 ns transient response settling time, the AD9022 provides excellent results when low-frequency analog inputs must be oversampled (such as CCD digitization). The full scale analog input is ±1 V with a 300 Ω input impedance. The analog input can be driven directly from the signal source, or can be buffered by the AD96xx series of low noise, low distortion buffer amplifiers.

All timing is internal to the AD9022; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9022 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in 28-pin ceramic DIPs and gullwing surface mount packages. The AD9022 is specified to operate over the industrial (–25°C to +85°C) and military (–55°C to +125°C) temperature ranges.

PIN DESIGNATIONS



NC = NO CONNECT
COMPENSATION (PIN 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.01μF

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9022AQ/BQ	–25°C to +85°C	28-Pin Ceramic DIP	Q-28
AD9022AZ/BZ	–25°C to +85°C	28-Pin Ceramic Leaded Chip Carrier	Z-28
AD9022SQ	–55°C to +125°C	28-Pin Ceramic DIP	Q-28
AD9022SZ	–55°C to +125°C	28-Pin Ceramic Leaded Chip Carrier	Z-28

*For outline information see Package Information section.

Samplifier is a trademark of Analog Devices, Inc.

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AD9022–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; Encode = 20 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9022AQ/AZ Min	AD9022AQ/AZ Typ	AD9022AQ/AZ Max	AD9022BQ/BZ Min	AD9022BQ/BZ Typ	AD9022BQ/BZ Max	AD9022SQ/SZ Min	AD9022SQ/SZ Typ	AD9022SQ/SZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75	LSB
	Full	VI			1.0			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I		1.3	2.5		1.3	2.0		1.3	2.5	LSB
	Full	VI		1.6	3.0		1.6	3.0		1.6	3.0	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	25		5	25		5	25	mV
	Full	VI		15	35		15	35		15	35	mV
Gain Error	+25°C	I		0.5	2.5		0.5	2.5		0.5	2.5	% FS
	Full	VI		0.6	3.5		0.6	3.5		0.6	3.5	% FS
ANALOG INPUT												
Input Voltage Range				±1.024			±1.024			±1.024		V
Input Resistance	Full	IV	240	300	360	240	300	360	240	300	360	Ω
Input Capacitance	+25°C	V		5			5			5		pF
Analog Bandwidth	+25°C	V		110			110			110		MHz
SWITCHING PERFORMANCE[1]												
Minimum Conversion Rate	+25°C	IV			4			4			4	MSPS
Maximum Conversion Rate	Full	VI	20			20			20			MSPS
Aperture Delay (t_A)	+25°C	IV	0.55	0.71	0.85	0.55	0.71	0.85	0.55	0.71	0.85	ns
Aperture Uncertainty (Jitter)	+25°C	V		6			6			6		ps, rms
Output Delay (t_{OD})	Full	VI	15		27.5	15		27.5	15		27.5	ns
ENCODE INPUT												
Logic Compatibility				TTL			TTL			TTL		
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		20			20			20		ns
Overvoltage Recovery Time	+25°C	V		20			20			20		ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	65	73		70	75		65	73		dBc
@ 9.6 MHz	+25°C	I	63	72		69	74		63	72		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	64		64	66		62	64		dB
@ 9.6 MHz	+25°C	I	61	63		63	65		61	63		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	63	66		65	67		63	66		dB
@ 9.6 MHz	+25°C	I	62	65		64	66		62	65		dB
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		74			74			74		dBc
DIGITAL OUTPUTS[1]												
Logic Compatibility				TTL			TTL			TTL		
Output Coding				Offset Binary			Offset Binary			Offset Binary		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		100	120		100	120		100	120	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		180	220		180	220		180	220	mA
Power Dissipation	Full	VI		1.4	1.9		1.4	1.9		1.4	1.9	W

Specifications subject to change without notice.

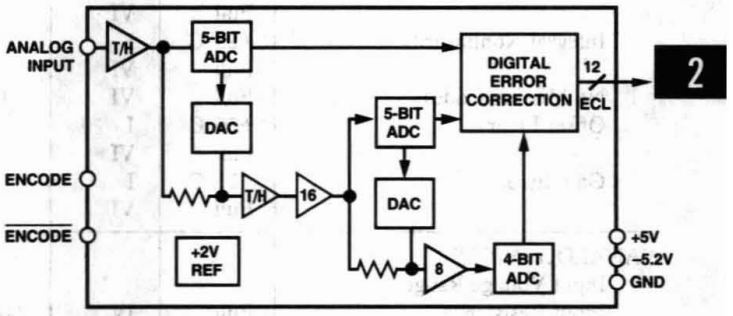
12-Bit 20 MSPS Monolithic A/D Converter

AD9023

FEATURES
Monolithic
12-Bit 20 MSPS A/D Converter
Low Power Dissipation: 1.5 Watts
On-Chip T/H and Reference
High Spurious-Free Dynamic Range
ECL Logic

APPLICATIONS
Radar Receivers
Digital Communications
Digital Instrumentation
Electro-Optic
Medical Imaging
Digital Filters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9023 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on chip to provide a complete conversion solution. It is a companion unit to the AD9022; the primary difference between the two is that all logic for the AD9022 is TTL compatible, while the AD9023 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

Operating from +5 V and –5.2 V supplies, the AD9023 provides excellent dynamic performance. Sampling at 20 MSPS with A_{IN} = 1 MHz, the spurious-free dynamic range (SFDR) is typically 74 dB; with A_{IN} = 9.6 MHz, SFDR is 72 dB. SNR is typically 65 dB.

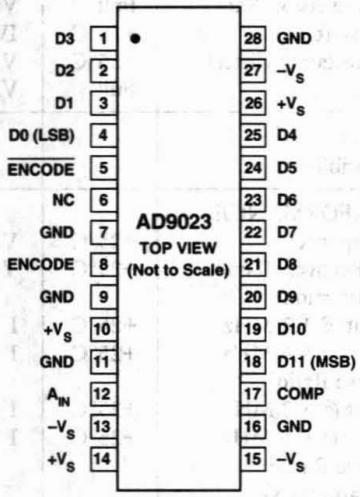
The on-board T/H has a 110 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many undersampling signal processing applications, such as in direct IF-to-digital conversion.

With DNL typically less than 0.5 LSB and 20 ns transient response settling time, the AD9023 provides excellent results when low frequency analog inputs must be over-sampled (such as CCD digitization). The full-scale analog input is ±1 V with a 300 Ω input impedance. The analog input can be driven directly from the signal source, or can be buffered by the AD96xx series of low noise, low distortion buffer amplifiers.

All timing is internal to the AD9023; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9023 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in 28-pin ceramic DIPs and gullwing surface mount packages. The AD9023 is specified to operate over the industrial (–25°C to +85°C) and extended (–55°C to +125°C) temperature ranges.

PIN DESIGNATIONS



NC = NO CONNECT
COMPENSATION (PIN 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.1μF

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9023AQ/BQ	–25°C to +85°C	28-Pin Ceramic DIP	Q-28
AD9023AZ/BZ	–25°C to +85°C	28-Pin Ceramic Leaded Chip Carrier	Z-28
AD9023SQ	–55°C to +125°C	28-Pin Ceramic DIP	Q-28
AD9023SZ	–55°C to +125°C	28-Pin Ceramic Leaded Chip Carrier	Z-28

*For outline information see Package Information section.

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AD9023–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; Encode = 20 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9023AQ/AZ Min	AD9023AQ/AZ Typ	AD9023AQ/AZ Max	AD9023BQ/BZ Min	AD9023BQ/BZ Typ	AD9023BQ/BZ Max	AD9023SQ/SZ Min	AD9023SQ/SZ Typ	AD9023SQ/SZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75	LSB
	Full	VI			1.0			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I		1.2	2.5		1.2	2.0		1.2	2.5	LSB
	Full	VI		1.6	3.0		1.6	3.0		1.6	3.0	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	25		5	25		5	25	mV
	Full	VI		15	35		15	35		15	35	mV
Gain Error	+25°C	I		0.5	2.5		0.5	2.5		0.5	2.5	% FS
	Full	VI		0.6	3.5		0.6	3.5		0.6	3.5	% FS
ANALOG INPUT												
Input Voltage Range				±1.024			±1.024			±1.024		V
Input Resistance	Full	IV	240	300	360	240	300	360	240	300	360	Ω
Input Capacitance	+25°C	V		6			6			6		pF
Analog Bandwidth	+25°C	V		110			110			110		MHz
SWITCHING PERFORMANCE[1]												
Minimum Conversion Rate	+25°C	IV			4			4			4	MSPS
Maximum Conversion Rate	Full	VI	20			20			20			MSPS
Aperture Delay (t_A)	+25°C	IV	0.50	0.78	1.05	0.50	0.78	1.05	0.50	0.78	1.05	ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5			5		ps, rms
Output Delay (t_{OD})	Full	VI	8.5		19.5	8.5		19.5	8.5		19.5	ns
ENCODE INPUT												
Logic Compatibility				ECL			ECL			ECL		
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		20			20			20		ns
Overvoltage Recovery Time	+25°C	V		20			20			20		ns
Harmonic Distortion[2]												
Analog Input @ 1.2 MHz	+25°C	I	65	72		70	74		65	72		dBc
@ 9.6 MHz	+25°C	I	63	69		69	71		63	69		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	63		64	65		62	63		dB
@ 9.6 MHz	+25°C	I	61	62		63	64		61	62		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	63	64		65	66		63	64		dB
@ 9.6 MHz	+25°C	I	62	63		64	65		62	63		dB
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		74			74			74		dBc
DIGITAL OUTPUTS[1]												
Logic Compatibility				ECL			ECL			ECL		
Output Coding				Offset Binary			Offset Binary			Offset Binary		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		100	120		100	120		100	120	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		195	240		195	240		195	240	mA
Power Dissipation	Full	VI		1.5	2.0		1.5	2.0		1.5	2.0	W

Specifications subject to change without notice.

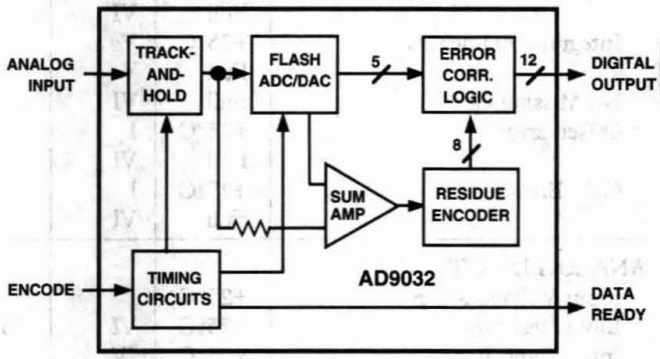
12-Bit 25 MSPS A/D Converter

AD9032

FEATURES
25.6 MSPS Conversion Speeds
On-Board T/H, References, Timing
Low Power: 3.8 W
Single 40-Pin Package
74 dB Spurious-Free Dynamic Range to 12 MHz A_{IN}
Bipolar Input: ±1.024 V

APPLICATIONS
Radar
Signal Intelligence
Digital Spectrum Analyzers
Medical Imaging
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



2

GENERAL DESCRIPTION

The AD9032 is the world's fastest 12-bit analog-to-digital converter (ADC) that includes on-board T/H, voltage references, and timing circuits. The AD9032 uses a subranging converter architecture to achieve sample rates from dc to 25.6 MSPS. Packaged in a single 40-pin hybrid, the AD9032 is pin-compatible with the AD9034, which operates at word rates up to 20 MSPS.

This ECL-compatible ADC requires only +5 V and –5.2 V supplies, an analog input, and a stable ECL clock to obtain the best dynamic performance available in a 12-bit ADC. This kind of performance is achieved with advanced bipolar circuits, custom designed and manufactured by Analog Devices. The latest in monolithic track-and-hold technology ensures accurate sampling of high frequency analog inputs.

Dynamic performance has been optimized to achieve SNR of 64 dB and a spurious-free dynamic range (SFDR) of 74 dB for analog bandwidths up to 12 MHz. All units are tested for dynamic performance at a sample rate of 25.6 MSPS.

The AD9032 is available in either a 40-pin ceramic DIP or leaded flatpack. The two versions operate over an industrial (–25°C to +85°C) or military (–55°C to +125°C) temperature range.

EVALUATION BOARD

An evaluation board which is available for the AD9032 (part number AD9034/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specified printed circuit board. The evaluation board was originally designed and used for evaluating the AD9034 A/D converter, but is equally useful for the pin-compatible AD9032.

The board includes a reconstruction DAC, analog input amplifier, and digital output interface. Physically, it is 7.25 inches × 6 inches in size and uses the layout and applications information contained in the AD9034 data sheet.

Generous space is provided near the analog input and digital outputs of the evaluation board to support additional signal processing components the user may wish to add. These two prototyping areas include through holes with 100-mil centers to support a variety of component additions.

For additional operating details, a schematic of the evaluation board, and complete layout information, consult the data sheet on the AD9034 A/D converter.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD9032AD	–25°C to +85°C	40-Pin Ceramic DIP	DH-40A
AD9032AZ[2]	–25°C to +85°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9032BD	–25°C to +85°C	40-Pin Ceramic DIP	DH-40A
AD9032BZ[2]	–25°C to +85°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9032TD	–55°C to +125°C	40-Pin Ceramic DIP	DH-40A
AD9032TZ[2]	–55°C to +125°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9034/PWB	Printed Circuit Board (Only) of Evaluation Circuit		
AD9034/PCB	Complete Evaluation Board, Assembled and Tested (Order AD9032 DIP Separately)		

NOTES
[1]For outline information see Package Information section.
[2]Ceramic leaded chip carrier packages are tested and shipped with unformed leads. Consult the factory for availability.

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AD9032–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; Encode = 25.6 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	AD9032AD/AZ Typ	AD9032AD/AZ Max	AD9032BD/BZ Min	AD9032BD/BZ Typ	AD9032BD/BZ Max	AD9032TD/TZ Min	AD9032TD/TZ Typ	AD9032TD/TZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.65	1.25		0.5	1.0		0.5	1.0	LSB
	Full	VI			1.75			1.5			1.5	LSB
Integral Nonlinearity	+25°C	V		1.0			1.0			1.0		LSB
	Full	V		2.0			2.0			2.0		LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	15		5	15		5	15	mV
	Full	VI			25			25			30	mV
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.5			±2.5			±2.5	% FS
ANALOG INPUT												
Input Voltage Range	+25°C	I		±1.024			±1.024			±1.024		V
Input Resistance	+25°C	VI	95	100	105	95	100	105	95	100	105	Ω
Input Capacitance	+25°C	IV		7	10		7	10		7	10	pF
Analog Bandwidth	+25°C	IV	150	220		150	220		150	220		MHz
SWITCHING PERFORMANCE												
Conversion Rate	Full	VI	dc		25.6	dc		25.6	dc		25.6	MSPS
Aperture Delay (t_A)	Full	IV	1	3	5	1	3	5	1	3	5	ns
Aperture Uncertainty (jitter)	Full	IV		4	8		4	8		4	8	ps, rms
Output Delay (t_{OD})	Full	IV	9	13	17	9	13	17	9	13	17	ns
Data Ready Delay (t_{DR})	Full	IV	3.5	7.5	10.5	3.5	7.5	10.5	3.5	7.5	10.5	ns
Output Time Skew	Full	IV		1	2		1	2		1	2	ns
ENCODE INPUT												
Logic "1" Voltage	Full	IV	–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	IV			–1.5			–1.5			–1.5	V
Logic "1" Current	Full	VI		150	300		150	300		150	300	µA
Logic "0" Current	Full	VI		150	300		150	300		150	300	µA
Input Capacitance	+25°C	V		10			10			10		pF
Pulse Width (High)	+25°C	IV	10			10			10			ns
Pulse Width (Low)	+25°C	IV	10			10			10			ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	IV		12	27		12	27		12	27	ns
Overvoltage Recovery Time	+25°C	IV		25	37		25	37		25	37	ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	70	80		75	82		75	82		dBc
@ 1.2 MHz	Full	VI	67			70			70			dBc
@ 4.3 MHz	+25°C	V		76			77			77		dBc
@ 9.6 MHz	+25°C	I	68	75		72	76		72	76		dBc
@ 9.6 MHz	Full	VI	64			68			64			dBc
@ 12.1 MHz	+25°C	V		72			74			74		dBc
Signal-to-Noise Ratio												
Analog Input @ 1.2 MHz	+25°C	I	63	66		64	67		64	67		dB
@ 1.2 MHz	Full	VI	61			63			61			dB
@ 4.3 MHz	+25°C	V		64			65			65		dB
@ 9.6 MHz	+25°C	I	62	64		62	64		62	64		dB
@ 9.6 MHz	Full	VI	60			61			58			dB
@ 12.1 MHz	+25°C	V		64			64			64		dB
Two-Tone Intermodulation												
Distortion Rejection	+25°C	V		66			68			68		dBc

Specifications subject to change without notice.

ANALOG DEVICES

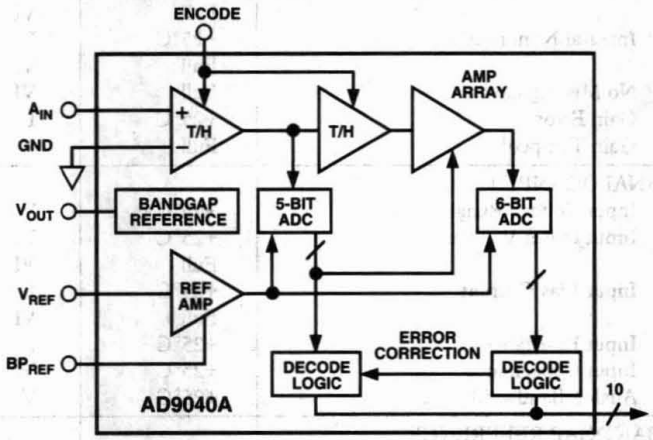
10-Bit, 40 MSPS A/D Converter

AD9040A

FEATURES
Low Power: 940 mW
53 dB SNR @ 10 MHz A_{IN}
On-Chip T/H, Reference
CMOS-Compatible
2 V p-p Analog Input
Fully Characterized Dynamic Performance

APPLICATIONS
Ultrasound Medical Imaging
Digital Oscilloscopes
Professional Video
Digital Communications
Advanced Television (MUSE Decoders)
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9040A is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with on-board track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only an encode signal to achieve 40 MSPS sample rates with 10-bit resolution.

Digital inputs and outputs are CMOS compatible; the analog input requires a signal of 2 V p-p amplitude. The two-step architecture used in the AD9040A is optimized to provide the best dynamic performance available while maintaining low power requirements of only 940 mW typically; maximum dissipation is 1.1 watt at 40 MSPS.

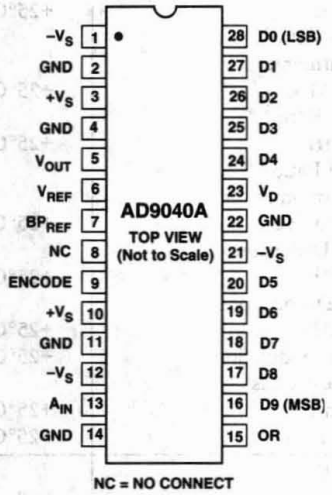
The signal-to-noise ratio (SNR), including harmonics, is 53 dB, or 8.5 ENOB, when sampling an analog input of 10.3 MHz at 40 MSPS. Competitive devices perform at less than 7.5 ENOB and require external references and larger input signals.

The AD9040A A/D converter is available as either a 28-pin plastic DIP or a 28-pin SOIC. The two models operate over a commercial temperature range of 0°C to +70°C. Contact the factory regarding availability of ceramic military temperature range devices.

PRODUCT HIGHLIGHTS

1. CMOS compatible logic for direct interface to ASICs.
2. On-board T/H provides excellent high frequency performance on analog inputs, critical for communications and medical imaging applications.
3. High input impedance and 2 volt p-p input range reduce need for external amplifiers.
4. Easy to use; no cumbersome external voltage references required, allowing denser packing of ADCs for multichannel applications.
5. Available in 28-lead plastic DIP and SOIC packages.
6. Evaluation board includes AD9040AJR, reconstruction DAC, and latches. Space is available near the analog input and digital outputs of the converter for additional circuits. Order as part number AD9040A/PCB (schematic shown in data sheet).

PIN DESIGNATIONS



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9040AJN	0°C to +70°C	28-Pin Plastic DIP	N-28
AD9040AJR	0°C to +70°C	28-Pin SOIC Package	R-28
AD9040A/PWB	Printed Circuit Board (Only) of Evaluation Circuit		
AD9040A/PCB	Complete Evaluation Board, Assembled and Tested, Including AD9040AJR		

*For outline information see Package Information section.

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AD9040A–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S = V_D = +5$ V; $-V_S = -5$ V; internal reference: ENCODE = 40.5 MSPS unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9040AJN/JR Min	Typ	Max	Units
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		1.0	2.0	LSB
	Full	VI			2.5	LSB
Integral Nonlinearity	+25°C	I		1.0	2.0	LSB
	Full	VI			2.5	LSB
No Missing Codes	Full	VI		Guaranteed		
Gain Error	+25°C	I		±0.5	±1.5	% FS
Gain Tempco[1]	Full	V		±70		ppm/°C
ANALOG INPUT						
Input Voltage Range	+25°C	V		2		V p-p
Input Offset Voltage	+25°C	I		±2	±25	mV
	Full	VI			±30	mV
Input Bias Current	+25°C	I		7	15	µA
	Full	VI			25	µA
Input Resistance	+25°C	I	200	350		kΩ
Input Capacitance	+25°C	V		5		pF
Analog Bandwidth	+25°C	V		48		MHz
BANDGAP REFERENCE						
Output Voltage	Full	VI	2.4		2.6	V
Temperature Coefficient[1]	Full	V		±40		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	+25°C	I	40			MSPS
Minimum Conversion Rate	+25°C	IV		2	10	MSPS
Aperture Delay (t_A)	+25°C	V		1.9		ns
Aperture Uncertainty (Jitter)	+25°C	V		7		ps, rms
Output Propagation Delay (t_{PD})[2]	Full	IV	6		14	ns
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V		25		ns
Overvoltage Recovery Time	+25°C	V		40		ns
Signal-to-Noise Ratio[3] f_{IN} = 10.3 MHz	+25°C	I	50	53		dB
Signal-to-Noise Ratio[3] (Without Harmonics) f_{IN} = 10.3 MHz	+25°C	I	51	54		dB
Signal-to-Noise Ratio[3, 4] f_{IN} = 10.3 MHz	+25°C	I	51	55		dB
Signal-to-Noise Ratio[3, 4] (Without Harmonics) f_{IN} = 10.3 MHz	+25°C	I	53	56		dB
2nd Harmonic Distortion f_{IN} = 10.3 MHz	+25°C	I	56	65		dBc
3rd Harmonic Distortion f_{IN} = 10.3 MHz	+25°C	I	58	70		dBc
Two-Tone Intermodulation Distortion Rejections	+25°C	V		62		dBc
Differential Phase	+25°C	III		0.15	0.5	Degrees
Differential Gain	+25°C	III		0.25	1.0	%
ENCODE INPUT						
Logic "1" Voltage	Full	VI	4.0			V
Logic "0" Voltage	Full	VI			1.0	V
DIGITAL OUTPUTS						
Output Coding				Offset Binary		
POWER SUPPLY						
V_D Supply Current	Full	VI		13	20	mA
$+V_S$ Supply Current	Full	VI		89	105	mA
$-V_S$ Supply Current	Full	VI		87	100	mA
Power Dissipation	Full	VI		0.94	1.1	W

Specifications subject to change without notice.

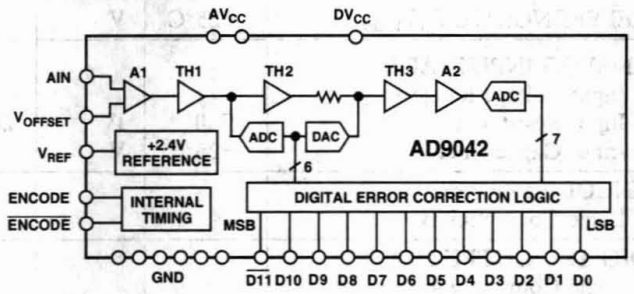
12-Bit, 41 MSPS Monolithic A/D Converter

AD9042

FEATURES
- 41 MSPS Minimum Sample Rate
- 80 dB Spurious-Free Dynamic Range
- 595 mW Power Dissipation
- Single +5 V Supply
- On-Chip T/H and Reference
- Twos Complement Output Format
- CMOS-Compatible Output Levels

APPLICATIONS
- Cellular/PCS Base Stations
- GPS Anti-Jamming Receivers
- Communications Receivers
- Spectrum Analyzers
- Electro-Optics
- Medical Imaging
- ATE

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9042 is a high speed, high performance, low power, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference are included on chip to provide a complete conversion solution. The AD9042 runs off of a single +5 V supply and provides CMOS-compatible digital outputs at 41 MSPS.

Designed specifically to address the needs of wideband, multichannel receivers, the AD9042 maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 20 MHz. Noise performance is also exceptional; typical signal-to-noise ratio is 68 dB.

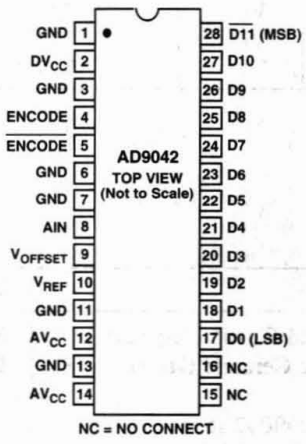
The AD9042 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative multipass architecture. Units are packaged in a 28-pin DIP; this custom cofired ceramic package forms a multilayer substrate to which internal bypass capacitors and the 9042 die are attached and a 44-pin TQFP low profile surface mount package. The AD9042 industrial grade is specified from –40°C to +85°C. However, the AD9042 was designed to perform over the full military temperature range (–55°C to +125°C); consult factory for military grade product options.

PRODUCT HIGHLIGHTS

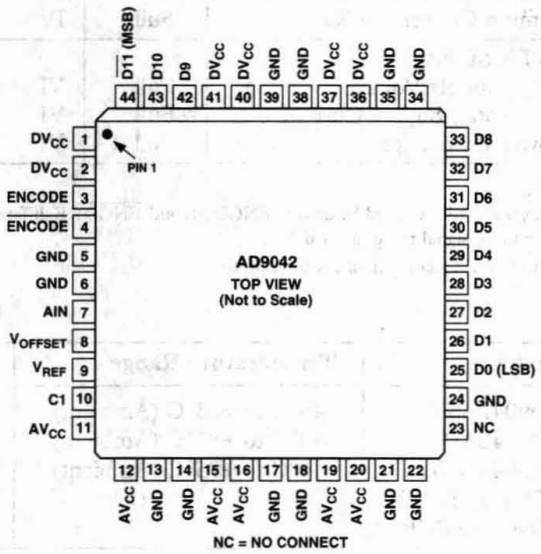
1. Guaranteed sample rate is 41 MSPS.
2. Dynamic performance specified over entire Nyquist band; spurious signals typ. 80 dBc for –1 dBFS input signals.
3. Low power dissipation: 595 mW off a single +5 V supply.
4. Reference and track-and-hold included on chip.
5. Packaged in 28-pin ceramic DIP and 44-pin TQFP.

PIN DESIGNATIONS

AD9042AD



AD9042AST



AD9042–SPECIFICATIONS (AV_{CC} = DV_{CC} = +5 V; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = –40°C, T_{MAX} = +85°C)[1]

Parameter	Temp	Test Level	AD9042AST Min	AD9042AST Typ	AD9042AST Max	Test Level	AD9042AD Min	AD9042AD Typ	AD9042AD Max	Units
RESOLUTION				12				12		Bits
DC ACCURACY										
No Missing Codes	Full	VI		Guaranteed		VI		Guaranteed		
Offset Error	Full	VI	–10	±3	+10	VI	–10	±3	+10	mV
Gain Error	Full	VI	–6.5	0	+6.5	VI	–6.5	0	+6.5	% FS
REFERENCE OUT (V_{REF})	+25°C	V		2.4				2.4		V
ANALOG INPUT (AIN)										
Input Voltage Range				V_{REF} ±0.500				V_{REF} ±0.500		V
Input Resistance	Full	IV	200	250	300		200	250	300	Ω
Input Capacitance	+25°C	V		5.5		V		7		pF
ENCODE INPUT										
Logic Compatibility				TTL/CMOS				TTL/CMOS		
DIGITAL OUTPUTS										
Logic Compatibility				CMOS				CMOS		
SNR[2]										
Analog Input 1.2 MHz	+25°C	V		68		I	65	68		dB
@ –1 dBFS	Full	V		67.5		V		67.5		dB
9.6 MHz	+25°C	V		67.5		I	64.5	67.5		dB
	Full	V		67		V		67		dB
19.5 MHz	+25°C	I	64	67		I	64	67		dB
	Full	V		66.5		V		66.5		dB
SINAD[2]										
Analog Input 1.2 MHz	+25°C	V		67.5		I	64	67.5		dB
@ –1 dBFS	Full	V		67		V		67		dB
9.6 MHz	+25°C	V		67.5		I	64	67.5		dB
	Full	V		67		V		67		dB
19.5 MHz	+25°C	I	64	67		I	64	67		dB
	Full	V		66.5		V		66.5		dB
Worst Spur[2]										
Analog Input 1.2 MHz	+25°C	V		80		I	74	80		dBc
@ –1 dBFS	Full	V		78		V		78		dBc
9.6 MHz	+25°C	V		80		I	74	80		dBc
	Full	V		78		V		78		dBc
19.5 MHz	+25°C	I	73	80		I	73	80		dBc
	Full	V		78		V		78		dBc
Maximum Conversion Rate	Full	VI	41			I	41			MSPS
Minimum Conversion Rate	Full	IV			5	V			5	MSPS
POWER SUPPLY										
AV_{CC} Supply Voltage	Full	VI		5.0		VI		5.0		V
I_{CC} (Total) Supply Current	Full	VI		119	147	VI		119	147	mA
Power Dissipation	Full	VI		595	735	VI		595	735	mW

NOTES

[1]All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.

[2]Analog input signal power at –1 dBFS.

Specification subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9042AST	–40°C to +85°C (Ambient)	44-Pin TQFP (Thin Quad Plastic Flatpack)	ST-44
AD9042AD	–40°C to +85°C (Ambient)	28-Pin 600 Mil Hermetic Ceramic DIP (DH-28)	DH-28
AD9042CHIPS	–40°C to +85°C (Ambient)	Unpackaged Die	
AD9042ST/PCB		Evaluation Board with AD9042AST	
AD9042D/PCB		Evaluation Board with AD9042AD	

*For outline information see Package Information section.

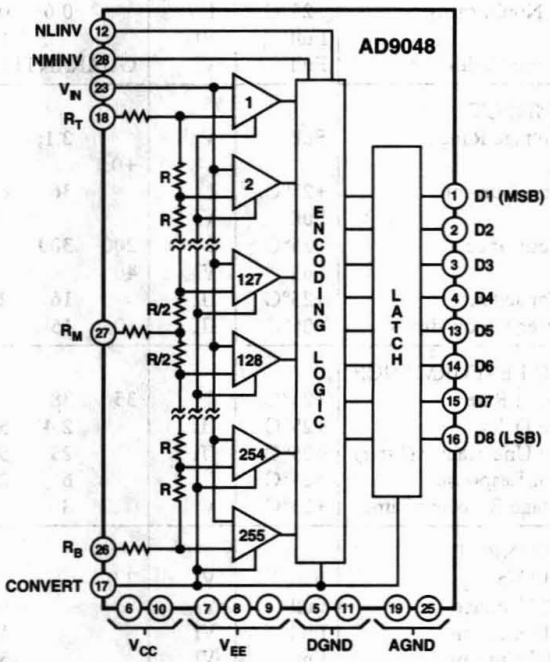
Monolithic 8-Bit Video A/D Converter

AD9048

FEATURES
35 MSPS Encode Rate
16 pF Input Capacitance
550 mW Power Dissipation
Industry-Standard Pinouts
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Professional Video Systems
Special Effects Generators
Electro-Optics
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9048 is an 8-bit, 35 MSPS flash converter, made on a high speed bipolar process, which is an alternate source for the TDC1048 unit but offers enhancements over its predecessor. Lower power dissipation makes the AD9048 attractive for a variety of system designs.

Because of its wide bandwidth, it is an ideal choice for real-time conversion of video signals. Input bandwidth is flat with no missing codes.

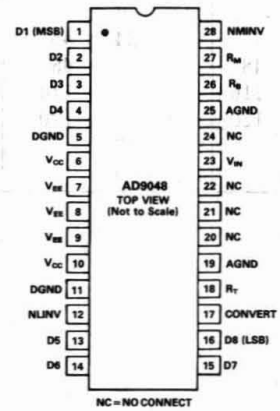
Clocked latching comparators, encoding logic and output buffer registers operating at minimum rates of 35 MSPS preclude a need for a sample-and-hold (S/H) or track-and-hold (T/H) in most system designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices operating over two ambient temperature ranges and with two grades of linearity are available. Linearities of either 0.5 LSB or 0.75 LSB can be ordered for a commercial range of 0°C to +70°C, or extended case temperatures of –55°C to +125°C. Commercial versions are packaged in 28-pin DIPs; extended temperature versions are available in ceramic DIP and ceramic LCC packages. Both commercial units and MIL-STD-883 units are standard products.

The AD9048 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9048/883B data sheet for detailed specifications.

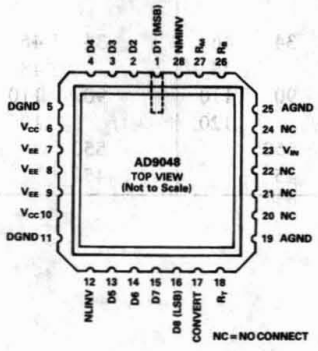
PIN DESIGNATIONS

DIP (Q Package)



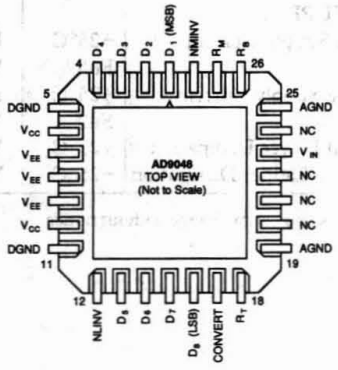
NC = NO CONNECT

LCC (E Package)



NC = NO CONNECT

J-Leaded Ceramic (J Package)



NC = NO CONNECT

AD9048–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V; V_{EE} = –5.2 V; Differential Reference Voltage = 2.0 V, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9048JJ/JQ Min	Typ	Max	AD9048KJ/KQ Min	Typ	Max	AD9048SE/SQ Min	Typ	Max	AD9048TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.4	0.75		0.3	0.5		0.4	0.75		0.3	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
Integral Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75		0.4	0.5	LSB
	Full	VI			1.0			0.75			1.0			0.75	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED			GUARANTEED			GUARANTEED			
ANALOG INPUT															
Input Voltage Range	Full	V	+0.1	2.1;		+0.1	2.1;		+0.1	2.1;		+0.1	2.1;	V	
Input Bias Current	+25°C	I		36	60		36	60		36	60		36	60	µA
	Full	VI			100			100			100			100	µA
Input Resistance	+25°C	I	200	300		200	300		200	300		200	300		kΩ
	Full	VI	40			40			40			40			kΩ
Input Capacitance	+25°C	III		16	20		16	20		16	20		16	20	pF
Full Power Bandwidth	+25°C	III	10	15		10	15		10	15		10	15		MHz
DYNAMIC PERFORMANCE															
Conversion Rate	+25°C	I	35	38		35	38		35	38		35	38		MHz
Aperture Delay	+25°C	III		2.4	5		2.4	5		2.4	5		2.4	5	ns
Aperture Uncertainty (Jitter)	+25°C	III		25	50		25	50		25	50		25	50	ps
Transient Response	+25°C	I		6	20		6	20		6	20		6	20	ns
Overvoltage Recovery Time	+25°C	V		8			8			8			8		ns
CONVERT INPUT															
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8			0.8	V
Logic "1" Current	Full	VI			15			15			15			15	µA
Logic "0" Current	Full	VI			500			500			500			500	µA
Input Capacitance	+25°C	III		4	6		4	6		4	6		4	6	pF
AC LINEARITY															
In-Band Harmonics															
dc to 2.438 MHz	+25°C	I	47	50		49	55		47	50		49	55		dBc
dc to 9.35 MHz	+25°C	V		48			48			48			48		dBc
Signal-to-Noise Ratio (SNR)															
1.248 MHz Input Frequency	+25°C	I	43.5	44		45	46		43.5	44		45	46		dB
2.438 MHz Input Frequency	+25°C	I	43	44		44	46		43	44		44	46		dB
1.248 MHz Input Frequency	+25°C	I	52.5	53		54	55		52.5	53		54	55		dB
2.438 MHz Input Frequency	+25°C	I	52	53		53	55		52	53		53	55		dB
DIGITAL OUTPUTS															
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.5			0.5			0.5			0.5	V
Short Circuit Current	Full	VI			30			30			30			30	mA
POWER SUPPLY															
Positive Supply Current	+25°C	I		34	46		34	46		34	46		34	46	mA
	Full	VI			48			48			48			48	mA
Negative Supply Current	+25°C	I		90	110		90	110		90	110		90	110	mA
	Full	VI			120			120			120			120	mA
Nominal Power Dissipation	+25°C	V		550			550			550			550		mW
Reference Ladder Dissipation	+25°C	V		45			45			45			45		mW

Specifications subject to change without notice.

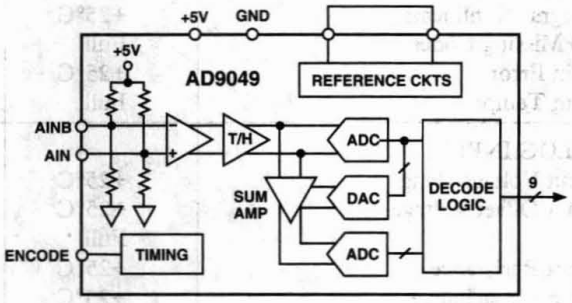
9-Bit, 30 MSPS ADC

AD9049

FEATURES
Low Power: 300 mW
On-Chip T/H, Reference
Single +5 V Power Supply Operation
Selectable 5 V or 3 V Logic I/O
Wide Dynamic Performance

APPLICATIONS
Digital Communications
Professional Video
Medical Imaging
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



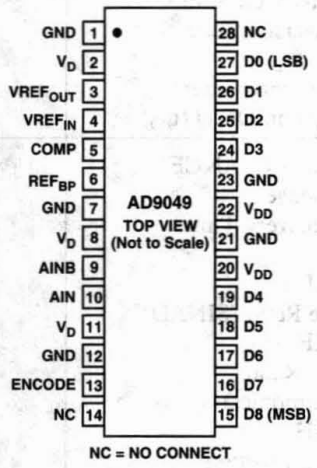
PRODUCT DESCRIPTION

The AD9049 is a complete 9-bit monolithic sampling analog-to-digital converter (ADC) with an onboard track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only +5 V and an encode clock to achieve 30 MSPS sample rates with 9-bit resolution.

The encode clock is TTL compatible and the digital outputs are CMOS; both can operate with 5 V/3 V logic, selected by the user. The two-step architecture used in the AD9049 is optimized to provide the best dynamic performance available while maintaining low power consumption.

A 2.5 V reference is included onboard, or the user can provide an external reference voltage for gain control or matching of multiple devices. Fabricated on an advanced BiCMOS process, the AD9049 is packaged in space saving surface mount packages (SOIC, SSOP) and is specified over the industrial (–40°C to +85°C) temperature range.

PIN CONNECTIONS



NC = NO CONNECT

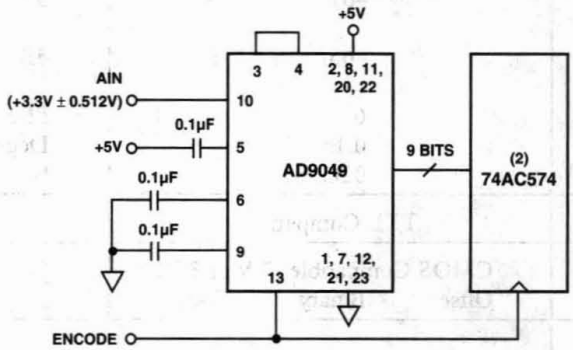


Figure 1. Typical Connections

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9049BR	–40°C to +85°C	R-28
AD9049BRS	–40°C to +85°C	RS-28

*R = Small Outline (SO); RS = Shrink Small Outline (SSOP). For outline information see Package Information section.

AD9049–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_D, V_{DD} = +5 V; internal reference; ENCODE = 30 MSPS unless otherwise noted)

Parameter	Temp	Test Level	AD9049BR/BRS Min	Typ	Max	Units
RESOLUTION				9		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.5	1.0	LSB
Integral Nonlinearity	+25°C	I		0.5	1.0	LSB
No Missing Codes	Full	IV		GUARANTEED		
Gain Error	+25°C	I		±1.0	±7.5	% FS
Gain Tempco	Full	V		±100		ppm/°C
ANALOG INPUT						
Input Voltage Range	+25°C	V		1.024		V p-p
Input Offset Voltage	+25°C	I	–10	+7	+25	mV
	Full	IV	–32		+51	mV
Input Resistance	+25°C	I	3.5	5.0	6.5	kΩ
Input Capacitance	+25°C	V		5		pF
Analog Bandwidth	+25°C	V		100		MHz
BANDGAP REFERENCE						
Output Voltage	+25°C	I	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±50		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	+25°C	I	30			MSPS
Minimum Conversion Rate	+25°C	IV		1.5	3	MSPS
Aperture Delay (t_A)	+25°C	V		2.7		ns
Aperture Uncertainty (Jitter)	+25°C	V		5		ps, rms
Output Propagation Delay (t_{PD})	Full	IV	5		15	ns
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V		10		ns
Overvoltage Recovery Time	+25°C	V		10		ns
ENOBS						
f_{IN} = 10.3 MHz	+25°C	I	8.01	8.51		ENOBs
Signal-to-Noise Ratio (SINAD)						
f_{IN} = 10.3 MHz	+25°C	I	50	53		dB
Signal-to-Noise Ratio (Without Harmonics)						
f_{IN} = 10.3 MHz	+25°C	I	51	53.3		dB
2nd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I		–67	–60	dBc
3rd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I		–66	–60	dBc
Two-Tone Intermodulation Distortion (IMD)	+25°C	V		65		dBc
Differential Phase	+25°C	V		0.15		Degrees
Differential Gain	+25°C	V		0.35		%
ENCODE INPUT				TTL Compatible		
DIGITAL OUTPUTS				CMOS Compatible (5 V or 3 V)		
Output Coding				Offset Binary	Code	
POWER SUPPLY						
V_D, V_{DD} Supply Current	Full	IV	40	60	80	mA
Power Dissipation	Full	IV		300	400	mW

Specifications subject to change without notice.

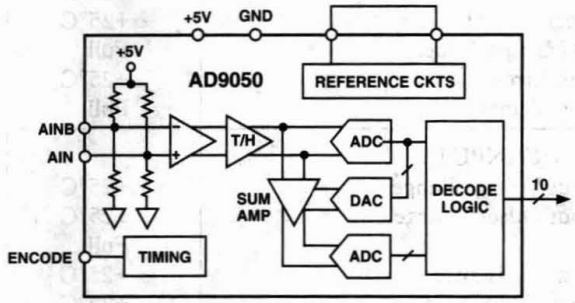
10-Bit, 40 MSPS ADC

AD9050

FEATURES
Low Power: 315 mW
On-Chip T/H, Reference
Single +5 V Power Supply Operation
Selectable 5 V or 3 V Logic I/O
SNR: 53 dB Minimum at 10 MHz

APPLICATIONS
Medical Imaging
Instrumentation
Digital Communications
Professional Video

FUNCTIONAL BLOCK DIAGRAM



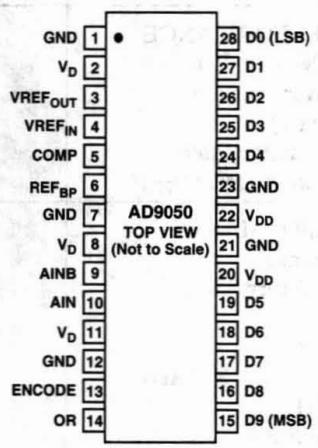
PRODUCT DESCRIPTION

The AD9050 is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with an onboard track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only +5 V and an encode clock to achieve 40 MSPS sample rates with 10-bit resolution.

The encode clock is TTL compatible and the digital outputs are CMOS; both can operate with 5 V/3 V logic, selected by the user. The two-step architecture used in the AD9050 is optimized to provide the best dynamic performance available while maintaining low power consumption.

A 2.5 V reference is included onboard, or the user can provide an external reference voltage for gain control or matching of multiple devices. Fabricated on an advanced BiCMOS process, the AD9050 is packaged in space saving surface mount packages (SOIC, SSOP) and is specified over the industrial (–40°C to +85°C) temperature range.

PIN CONNECTIONS



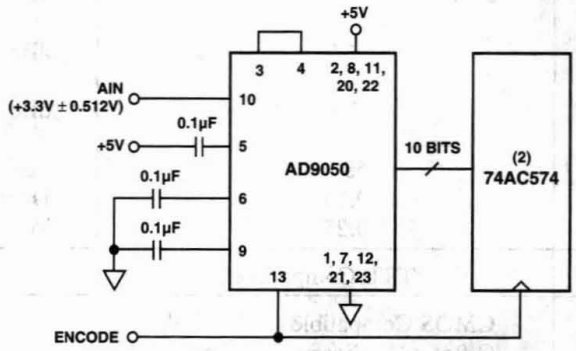


Figure 1. Typical Connections

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9050BR	–40°C to +85°C	R-28
AD9050BRS	–40°C to +85°C	RS-28

*R = Small Outline (SO); RS = Shrink Small Outline (SSOP). For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD9050–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_D, V_{DD} = +5 V; internal reference; ENCODE = 40 MSPS unless otherwise noted)

Parameter	Temp	Test Level	AD9050BR/BRS Min	Typ	Max	Units
RESOLUTION				10		Bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		0.75	1.75	LSB
Integral Nonlinearity	+25°C	I		1.0	1.75	LSB
No Missing Codes	Full	IV		GUARANTEED		
Gain Error	+25°C	I		±1.0	7.5	% FS
Gain Tempco	Full	V		±100		ppm/°C
ANALOG INPUT						
Input Voltage Range	+25°C	V		1.024		V p-p
Input Offset Voltage	+25°C	I	–10	+7	+25	mV
	Full	IV	–32		+51	mV
Input Resistance	+25°C	I	3.5	5.0	6.5	kΩ
Input Capacitance	+25°C	V		5		pF
Analog Bandwidth	+25°C	V		100		MHz
BANDGAP REFERENCE						
Output Voltage	+25°C	I	2.4	2.5	2.6	V
Temperature Coefficient	Full	V		±50		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	+25°C	I	40			MSPS
Minimum Conversion Rate	+25°C	IV		1.5	3	MSPS
Aperture Delay (t_A)	+25°C	V		2.7		ns
Aperture Uncertainty (Jitter)	+25°C	V		5		ps, rms
Output Propagation Delay (t_{PD})	Full	IV	5		15	ns
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V		10		ns
Overvoltage Recovery Time	+25°C	V		10		ns
ENOBS						
f_{IN} = 10.3 MHz	+25°C	I	8.51	8.85		ENOBs
Signal-to-Noise Ratio (SINAD)						
f_{IN} = 10.3 MHz	+25°C	I	53	55		dB
Signal-to-Noise Ratio (Without Harmonics)						
f_{IN} = 10.3 MHz	+25°C	I	53.5	55.5		dB
2nd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I		–67	–60	dBc
3rd Harmonic Distortion						
f_{IN} = 10.3 MHz	+25°C	I		–70	–63	dBc
Two-Tone Intermodulation Distortion (IMD)	+25°C	V		65		dBc
Differential Phase	+25°C	V		0.15		Degrees
Differential Gain	+25°C	V		0.25		%
ENCODE INPUT				TTL Compatible		
DIGITAL OUTPUTS				CMOS Compatible (5 V or 3 V)		
Output Coding				Offset Binary	Code	
POWER SUPPLY						
V_D, V_{DD} Supply Current	Full	IV	40	63	80	mA
Power Dissipation	Full	IV		315	400	mW

Specifications subject to change without notice.

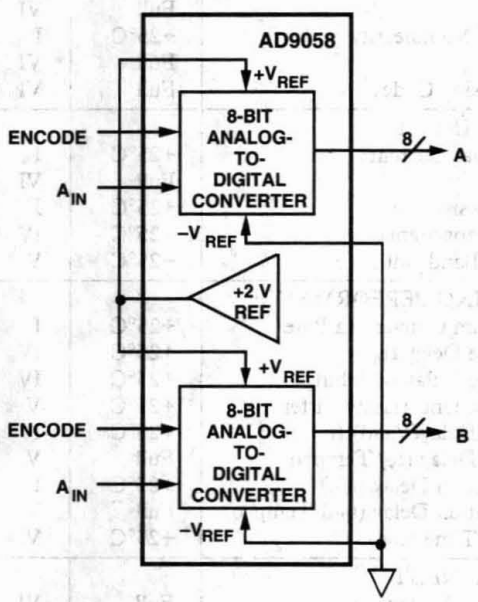
Dual 8-Bit 50 MSPS A/D Converter

AD9058

FEATURES
Two Matched ADCs on Single Chip
50 MSPS Conversion Speed
On-Board Voltage Reference
Low Power (<1 W)
Low Input Capacitance (10 pF)
±5 V Power Supplies
Flexible Input Range

APPLICATIONS
Quadrature Demodulation for Communications
Digital Oscilloscopes
Electronic Warfare
Radar

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9058 combines two independent high performance 8-bit analog-to-digital converters (ADCs) on a single monolithic IC. Combined with an optional on-board voltage reference, the AD9058 provides a cost effective alternative for systems requiring two or more ADCs.

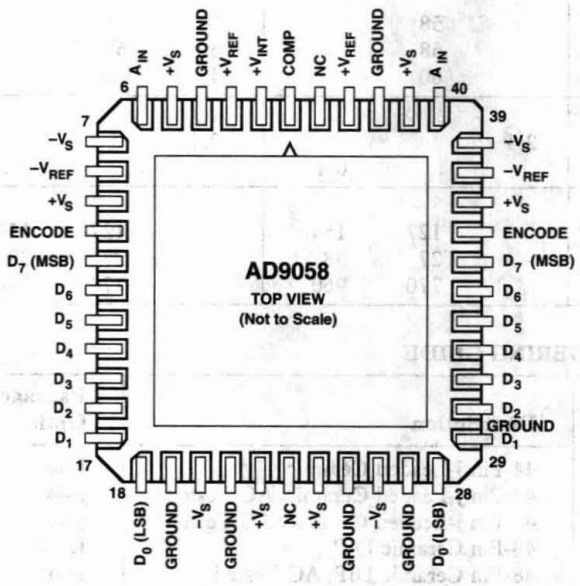
Dynamic performance (SNR, ENOB) is optimized to provide up to 50 MSPS conversion rates. The unique architecture results in low input capacitance while maintaining high performance and low power (<0.5 watt/channel). Digital inputs and outputs are TTL compatible.

Performance has been optimized for an analog input of 2 V p-p (±1 V; 0 to +2 V). Using the on-board +2 V voltage reference, the AD9058 can be set up for unipolar positive operation (0 to +2 V). This internal voltage reference can drive both ADCs.

Commercial (0°C to +70°C) and military (–55°C to +125°C) temperature range parts are available. Parts are supplied in hermetic 48-pin DIP and 44-pin "J" lead packages.

PIN CONFIGURATIONS

J-Lead Package



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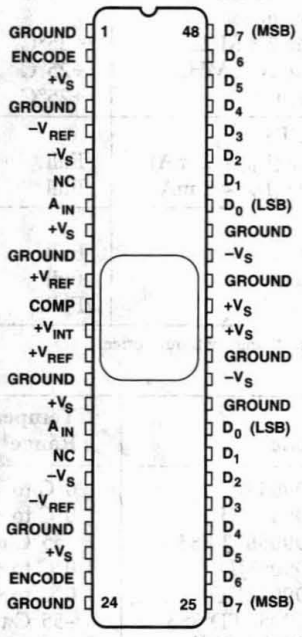
DIP



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AD9058–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $V_{REF} = +2$ V (internal); ENCODE = 40 MSPS; $A_{IN} = 0$ V to +2 V; $-V_{REF}$ = GROUND, unless otherwise noted.)[2] All specifications apply to either of the two ADCs.

Parameter (Conditions)	Temp	Test Level	AD9058JD/JJ Min	AD9058JD/JJ Typ	AD9058JD/JJ Max	AD9058KD/KJ Min	AD9058KD/KJ Typ	AD9058KD/KJ Max	Units
RESOLUTION			8			8			Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.25	0.65		0.25	0.5	LSB
	Full	VI			0.8			0.7	LSB
Integral Nonlinearity	+25°C	I		0.5	1.3		0.5	1.0	LSB
	Full	VI			1.4			1.25	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Bias Current	+25°C	I		75	170		75	170	μA
	Full	VI			340			340	μA
Input Resistance	+25°C	I	12	28		12	28		kΩ
Input Capacitance	+25°C	IV		10	15		10	15	pF
Analog Bandwidth	+25°C	V		175			175		MHz
SWITCHING PERFORMANCE									
Maximum Conversion Rate	+25°C	I		50		50	60		MSPS
Aperture Delay (t_A)	+25°C	IV	0.1	0.8	1.5	0.1	0.8	1.5	ns
Aperture Delay Matching	+25°C	IV		0.2	0.5		0.2	0.5	ns
Aperture Uncertainty (Jitter)	+25°C	V		10			10		ps, rms
Output Delay(Valid) (t_V)	+25°C	I		8		5	8		ns
Output Delay (t_V) Tempco	Full	V		16			16		ps/°C
Propagation Delay (t_{PD})	+25°C	I		12			12	19	ns
Propagation Delay (t_{PD}) Tempco	Full	V		–16			–16		ps/°C
Output Time Skew	+25°C	V		1			1		ns
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2			2			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		2			2		ns
Overvoltage Recovery Time	+25°C	V		2			2		ns
Signal-to-Noise Ratio									
Analog Input @ 2.3 MHz	+25°C	I		48		45	48		dB
@ 10.3 MHz	+25°C	I		46		44	46		dB
2nd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		48	58		dBc
@ 10.3 MHz	+25°C	I		58		48	58		dBc
3rd Harmonic Distortion									
Analog Input @ 2.3 MHz	+25°C	I		58		50	58		dBc
@ 10.3 MHz	+25°C	I		58		50	58		dBc
Crosstalk Rejection	+25°C	IV		60		48	60		dBc
DIGITAL OUTPUTS									
Logic "1" Voltage (I_{OH} = 2 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (I_{OL} = 2 mA)	Full	VI			0.4			0.4	V
POWER SUPPLY									
$+V_S$ Supply Current	Full	VI		127	154		127	154	mA
$-V_S$ Supply Current	Full	VI		27	38		27	38	mA
Power Dissipation	Full	VI		770	960		770	960	W

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD9058JJ	0°C to +70°C	44-Pin J-Leaded Ceramic	J-44
AD9058KJ	0°C to +70°C	44-Pin J-Leaded Ceramic, AC Tested	J-44
AD9058TJ/883	–55°C to +125°C	44-Pin J-Leaded Ceramic, AC Tested	J-44
AD9058JD	0°C to +70°C	48-Pin Ceramic DIP	D-48
AD9058KD	0°C to +70°C	48-Pin Ceramic DIP, AC Tested	D-48
AD9058TD/883	–55°C to +125°C	48-Pin Ceramic DIP, AC Tested	D-48
AD9058/PCB	0°C to +70°C	AD9058 Evaluation Board (J-Lead)	

*For outline information see Package Information section.

ANALOG DEVICES

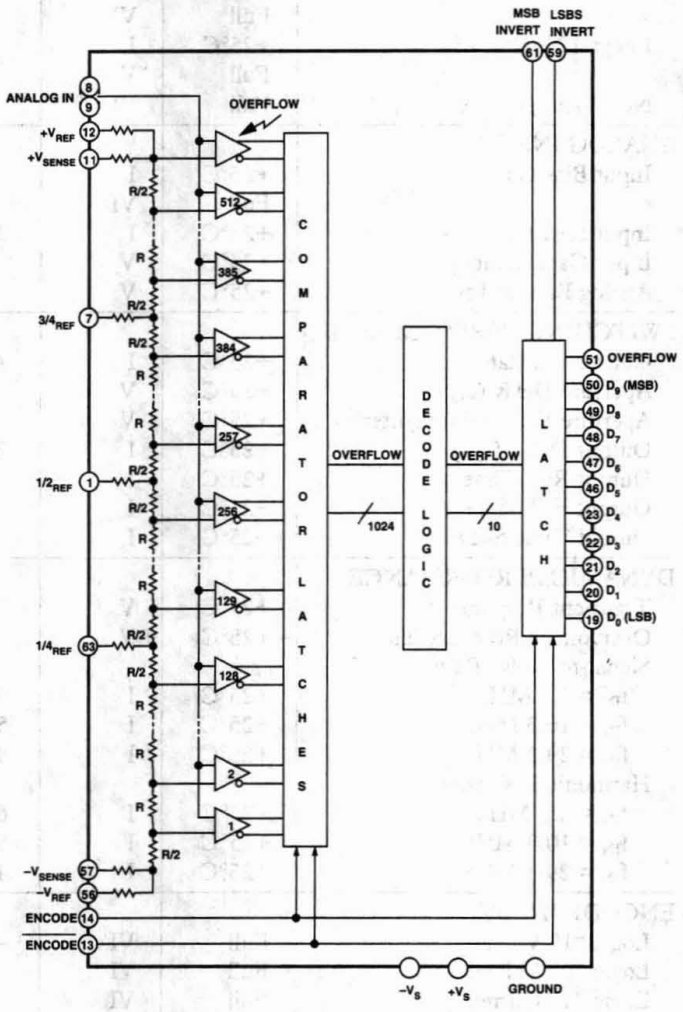
10-Bit 75 MSPS A/D Converter

AD9060

FEATURES
Monolithic 10-Bit/75 MSPS Converter
ECL Outputs
Bipolar (±1.75 V) Analog Input
57 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9060 A/D converter is a 10-bit monolithic converter capable of word rates of 75 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Inputs and outputs are ECL-compatible, which makes the AD9060 the recommended choice for systems with conversion rates >30 MSPS, to minimize system noise. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to insure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter-point taps on the resistor ladder help optimize the integral linearity of the unit.

Either 68-pin ceramic leaded (gull wing) packages or ceramic LCCs are available and are specifically designed for low thermal impedances. Two performance grades for temperatures of both 0°C to +70°C and –55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at +25°C. MIL-STD-883 units are available.

The AD9060 A/D converter is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9060/883B data sheet for detailed specifications.

ORDERING GUIDE

Device	Temperature Range	Package Options[1]
AD9060JZ	0°C to +70°C	Z-68
AD9060JE	0°C to +70°C	E-68A
AD9060KZ	0°C to +70°C	Z-68
AD9060KE	0°C to +70°C	E-68A
AD9060SZ[2]	–55°C to +125°C	Z-68
AD9060SE[2]	–55°C to +125°C	E-68A
AD9060TZ[2]	–55°C to +125°C	Z-68
AD9060TE[2]	–55°C to +125°C	E-68A
AD9060/PCB	0°C to +70°C	Evaluation Board

NOTES
[1]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

AD9060–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 60 MSPS unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9060JE/JZ Min	AD9060JE/JZ Typ	AD9060JE/JZ Max	AD9060KE/KZ Min	AD9060KE/KZ Typ	AD9060KE/KZ Max	Units
RESOLUTION			10			10			Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	+25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current	+25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	+25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance	+25°C	V		45			45		pF
Analog Bandwidth	+25°C	V		175			175		MHz
SWITCHING PERFORMANCE									
Conversion Rate	+25°C	I	75			75			MSPS
Aperture Delay (t_A)	+25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Delay (t_{OD})	+25°C	I	2	4	9	2	4	9	ns
Output Rise Time	+25°C	I		1	3		1	3	ns
Output Fall Time	+25°C	I		1	3		1	3	ns
Output Time Skew	+25°C	I		1.5	3		1.5	3	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
Signal-to-Noise Ratio									
f_{IN} = 2.3 MHz	+25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	+25°C	I	51	54		51	54		dB
f_{IN} = 29.3 MHz	+25°C	I	44	47		44	47		dB
Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	I	61	65		61	65		dBc
f_{IN} = 10.3 MHz	+25°C	I	55	58		55	58		dBc
f_{IN} = 29.3 MHz	+25°C	I	47	50		47	50		dBc
ENCODE INPUT									
Logic "1" Voltage	Full	VI	–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5	V
Logic "1" Current	Full	VI		150	300		150	300	µA
Logic "0" Current	Full	VI		150	300		150	300	µA
Input Capacitance	+25°C	V		5			5		pF
Pulse Width (High)	+25°C	I	6			6			ns
Pulse Width (Low)	+25°C	I	6			6			ns
POWER SUPPLY									
$+V_S$ Supply Current	+25°C	VI		420	500		420	500	mA
	Full	VI			500			500	mA
$-V_S$ Supply Current	+25°C	VI		150	180		150	180	mA
	Full	VI			190			190	mA
Power Dissipation	+25°C	VI		2.8	3.3		2.8	3.3	W
	Full	VI			3.5			3.5	W
Power Supply Rejection Ratio (PSRR)	Full	VI		6	10		6	10	mV/V

Specifications subject to change without notice.

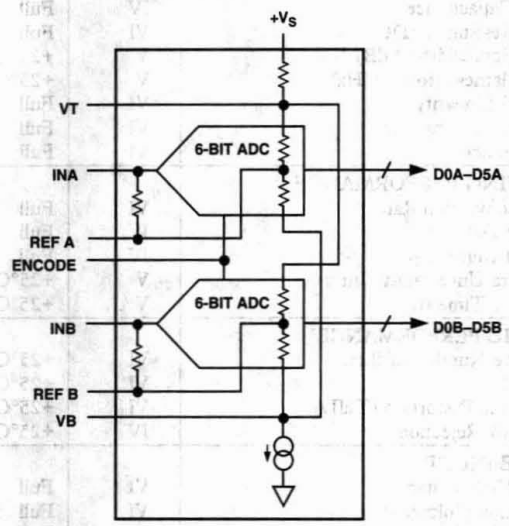
Dual 6-Bit, 60 MSPS Monolithic A/D Converter

AD9066

FEATURES
Two Matched ADCs on Single Chip
CMOS Compatible I/O
Low Power (400 mW) Dissipation
Single +5 V Supply
On-Chip Voltage Reference
Self-Biased for AC Coupled Inputs
28-Pin SOIC Package

APPLICATIONS
Direct Broadcast Satellite (DBS) Receivers
QAM Demodulators
Wireless LANs
VSAT Receivers

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

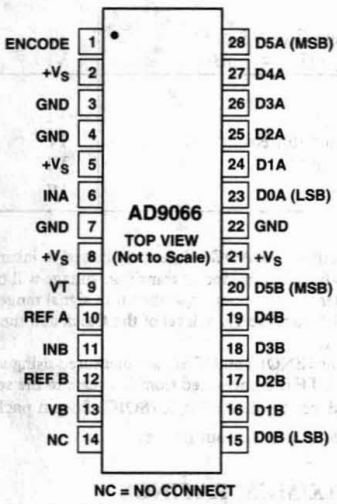
The AD9066 is a dual 6-bit ADC that has been optimized for low cost in-phase and quadrature (I&Q) demodulators. Primary applications include digital direct broadcast satellite applications where broadband quadrature phase shift keying (QPSK) modulation is used. In these receivers the recovered signal is separated into I&Q vector components and digitized.

To reduce total system cost and power dissipation, the AD9066 provides an internal voltage reference and operates from a single +5 volt power supply. Digital outputs are CMOS compatible and rated to 60 MSPS conversion rates. The digital input (ENCODE) utilizes a CMOS input stage with a TTL compatible (1.4 V) threshold.

The AD9066 is housed in a 28-pin SOIC package and available in two temperature grades. The AD9066JR is rated for operation over the 0°C to +70°C commercial temperature range. The AD9066AR is rated for the –40°C to +85°C industrial temperature range.

The internal voltage reference insures that the analog input is biased to midscale with low offset when driven from an ac coupled source. In dc coupled applications, the midscale voltage reference can be used to control external biasing amplifiers to minimize offsets due to variations in temperature or supply voltage.

PIN CONFIGURATION



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9066AR	–40°C to +85°C	R-28
AD9066JR	0°C to +70°C	R-28
AD9066/PCB	0°C to +70°C	Evaluation Board

*R = "SO" Small Outline Package. For outline information see Package Information section.

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AD9066–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V, AIN = 15.5 MHz, Encode Rate = 60 MSPS, $T_C = T_A$)

Parameter	Test Level	Temp	AD9066JR Min	AD9066JR Typ	AD9066JR Max	AD9066AR Min	AD9066AR Typ	AD9066AR Max	Units
ANALOG INPUT									
Full-Scale Input Range	VI	Full	475	500	525	450	500	530	mV
Gain Matching (FS Range)	IV	Full			16			16	mV
DC Input (Midscale)[1]	V	+25°C		$+V_S - 1.1$			$+V_S - 1.1$		V
Input Offset[1]	VI	Full	–1.0		+1.0	–1.0		+1.0	LSBs
Input Capacitance	IV	Full		10	15		10	15	pF
Input Resistance (DC)	VI	Full	25	40	50	22	40	52	kΩ
Input Bandwidth (3 dB)	V	+25°C		100			100		MHz
Gain Flatness (to 15 MHz)	V	+25°C		0.25			0.25		dB
Integral Linearity	VI	Full	–1.0		+1.0	–1.0		+1.0	LSBs
Differential Linearity	VI	Full	–0.5		+0.5	–0.5		+0.5	LSBs
Monotonicity	VI	Full		Guaranteed			Guaranteed		
SWITCHING PERFORMANCE									
Max Conversion Rate	VI	Full	60			60			MSPS
Output Delay (t_V)[2]	IV	Full	4			4			ns
Output Delay (t_{PD})[2]	IV	Full			11			12	ns
Aperture Uncertainty (Jitter)	V	+25°C		10			10		ps rms
Aperture Time (t_A)	V	+25°C		1.0			1.0		ns
DYNAMIC PERFORMANCE[3]									
Effective Number of Bits	VI	+25°C	5.3	5.7		5.3	5.7		Bits
SINAD	VI	+25°C	34	36		34	36		dB
Harmonic Distortion (THD)	VI	+25°C	40	50		40	50		dB
Crosstalk Rejection	IV	+25°C	40	50		40	50		dBc
ENCODE INPUT									
Logic High Voltage	VI	Full	2.0			2.0			V
Logic Low Voltage	VI	Full			0.8			0.8	V
Input High Current	VI	Full			500			500	μA
Input Low Current	VI	Full			500			500	μA
Pulse Width High	IV	Full	7.0			7.0			ns
Pulse Width Low	IV	Full	7.0			7.0			ns
DIGITAL OUTPUTS									
Output Coding		Full		Offset Binary			Offset Binary		
Logic High Voltage (I_{OH} = 1 mA)	VI	Full	3.8			3.8			V
Logic Low Voltage (I_{OL} = 1 mA)	VI	Full			0.4			0.4	V
POWER SUPPLY									
$+V_S$ Supply Voltage	VI	Full	4.75		5.25	4.75		5.25	V
Power Supply Rejection Ratio[1]	IV	Full		110	130		110	130	mV/V
$+V_S$ Supply Current	VI	Full		80	120		80	120	mA
Power Dissipation[4]	VI	Full		400	600		400	600	mW

NOTES

[1]For ac coupled applications, the ADC is internally biased to insure that the midpoint transition of the ADC is within the limits specified with no signal applied. For dc coupled applications, the dc value of the midpoint transition voltage will track the supply voltage within the limits shown for dc input (midscale) plus the dc offset. Power Supply Rejection Ratio (PSRR) refers to the variation of the input signal range (gain) to supply voltage.

[2]t_V and t_{PD} are measured from the 1.4 V level of the Clock and the 50% level between V_{OH} and V_{OL}. The ac load on all the digital outputs during test is 10 pF (max), the dc load will not exceed ±40 μA.

[3]Effective number of bits (ENOB) and THD are measured using a FFT with a pure sine wave analog input @ 15.5 MHz, 1 dB below full scale. ENOB is calculated by ENOB = (SNR – 1.76 dB)/6.02; THD is measured from full scale to the sum of the second through seventh harmonic of the input.

[4]Typical thermal impedance for the "R" style (SOIC) 28-pin package is: θ_{JC} = 4°C/W, θ_{CA} = 41°C/W, θ_{JA} = 45°C/W.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Pin	Min	Max	Units
ENCODE	–0.5	$+V_S$	V
$+V_S$		7.0	V
INA, INB	–0.5	$+V_S$	V
VT	2.5	$+V_S$	V
REF A, REF B	–0.5	$+V_S$	V
VB	0.0	$+V_S$	V
D0–D5 Current OUT		20	mA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9066 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

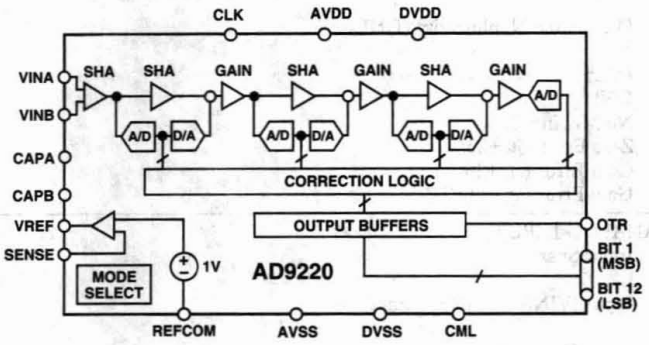
Complete 12-Bit, 10 MSPS Monolithic A/D Converter

AD9220

FEATURES

Monolithic 12-Bit 10 MSPS A/D Converter
Low Power Dissipation: 250 mW
Single +5 V Supply
No Missing Codes Guaranteed
Differential Nonlinearity Error: 0.3 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 70 dB @ 1 MHz
Spurious-Free Dynamic Range: –88 dB @ 1 MHz
Out-of-Range Indicator
Straight Binary Output Data
28-Pin SOIC

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9220 is a monolithic, single supply, 12-bit, 10 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9220 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 10 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9220 combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of previous hybrid and monolithic implementations at a fraction of the power consumption.

The input of the AD9220 has been designed to ease the development of both imaging and communications systems. With a truly differential input structure, the user can select a variety of input ranges and offsets.

The sample-and-hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. The dynamic performance is excellent.

The AD9220's wideband input combined with the power and cost savings over previously available monolithics and hybrids will enable new design applications in communications, imaging and medical applications.

The AD9220 has an onboard, programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9220 is fabricated on a very cost effective CMOS process. High speed, precision analog circuits are now combined with high density logic circuits.

The AD9220 offers a complete single-chip sampling 12-bit, 10 MSPS analog-to-digital conversion function in a 28-pin SOIC package.

Low Power—The AD9220 at 250 mW consumes a fraction of the power of presently available hybrids and existing monolithic solutions.

On-Board Sample-and-Hold (SHA)—The versatile SHA input can be configured for either single ended or differential inputs.

OUT OF RANGE (OTR)—The OTR output bit indicates when the input signal is beyond the AD9220's input range.

Single Supply—The AD9220 uses a single +5 V power supply simplifying system power supply design.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9220AR	–40°C to +85°C	28-Pin 300 Mil SOIC	R-28
AD9220-EB	Evaluation Board		

*For outline information see Package Information section.

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AD9220–SPECIFICATIONS

DC SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +5 V, f_{SAMPLE} = 10 MSPS, VREF = 2.5 V, VINB = 2.5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9220	Units
RESOLUTION	12	Bits min
MAX CONVERSION RATE	10	MHz min
ACCURACY		
Integral Nonlinearity (INL)	±0.5	LSB typ
	±1	LSB max
Differential Nonlinearity (DNL)	±0.30	LSB typ
	±0.75	LSB max
INL[1]	±0.7	LSB typ
DNL[1]	±0.35	LSB typ
No Missing Codes	12	Bits Guaranteed
Zero Error (@ +25°C)	±0.3	% FSR max
Gain Error (@ +25°C)[2]	±1.5	% FSR max
Gain Error (@ +25°C)[3]	±0.75	% FSR max
ANALOG INPUT		
Input Span	2	V p-p min
	5	V p-p max
Input (VINA or VINB) Range	0	V min
	AV_{DD}	V max
Input Capacitance	16	pF typ
INPUT REFERRED NOISE		
VREF = 1 V	0.33	LSBs rms typ
VREF = 2.5 V	0.13	LSBs rms typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1 V Mode)	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	mV max
Output Voltage (2.5 V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	mV max
Load Regulation[4]	1.5	mV
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER CONSUMPTION	250	mW typ
	310	mW max

NOTES

[1]V_{REF} = 1 V.

[2]Including internal voltage reference.

[3]Excluding internal voltage reference.

[4]Load Regulation w/1 mA load current (in addition to that required by the AD9220).

Specifications subject to change without notice.

AC SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +5 V, f_{SAMPLE} = 10 MSPS, VREF = 1 V, VINB = 2.5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9220	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)		
f_{INPUT} = 1 MHz	68.5	dB min
	70	dB typ
f_{INPUT} = 4.99 MHz	65	dB min
	67	dB typ
SIGNAL-TO-NOISE RATIO (SNR)		
f_{INPUT} = 1 MHz	69	dB min
	70.2	dB typ
f_{INPUT} = 4.99 MHz	67.5	dB min
	68.8	dB typ
TOTAL HARMONIC DISTORTION (THD)		
f_{INPUT} = 1 MHz	–83.7	dB typ
	–76	dB max
f_{INPUT} = 4.99 MHz	–72	dB typ
	–68	dB max
SPURIOUS FREE DYNAMIC RANGE		
f_{INPUT} = 1 MHz	–88	dB typ
	–77.5	dB max
f_{INPUT} = 4.99 MHz	–75	dB typ
	–69	dB max
Full Power Bandwidth	50	MHz typ
Small Signal Bandwidth	50	MHz typ
Aperture Delay	1	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step (0.01%)	30	ns typ

Specifications subject to change without notice.

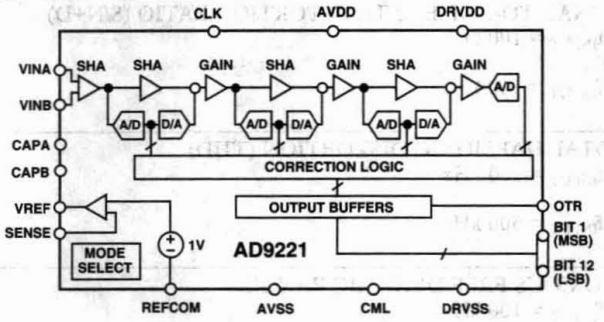
Complete 12-Bit, 1 MSPS Monolithic A/D Converter

AD9221

FEATURES

Monolithic 12-Bit 1 MSPS A/D Converter
Low Power Dissipation: 60 mW
Single +5 V Supply
No Missing Codes Guaranteed
Differential Nonlinearity Error: 0.3 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 70 dB
Spurious-Free Dynamic Range: –88 dB
Out of Range Indicator
Straight Binary Output Data
28-Pin SOIC

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9221 is a monolithic, single supply 12-bit, 1 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9221 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 1 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9221 combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of hybrid and monolithic implementations at a fraction of the power consumption.

The input of the AD9221 has been designed to ease the development of both imaging and communications systems. With a truly differential input structure, the user can select a variety of input ranges and offsets. The dynamic performance is excellent.

The sample-and-hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate.

The AD9221's wideband input combined with the power and cost savings over previously available monolithics and hybrids will enable new design applications in communications, imaging and medical applications.

The AD9221 has an onboard, programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9221 is fabricated on a very cost effective CMOS process. High speed, precision analog circuits are now combined with high density logic circuits.

The AD9221 offers a complete single-chip sampling 12-bit, 1 MSPS analog-to-digital conversion function in a 28-pin SOIC package.

Low Power—The AD9221 at 60 mW consumes a fraction of the power of presently available hybrids and existing monolithic solutions.

Onboard Sample-and-Hold (SHA)—The versatile SHA input can be configured for either single ended or differential inputs.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9221's input range.

Single Supply—The AD9221 uses a single +5 V power supply simplifying system power supply design.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9221AR	–40°C to +85°C	28-Pin 300 mil SOIC	R-28
AD9221-EB		Evaluation Board	

*For outline information see Package Information section.

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AD9221–SPECIFICATIONS

AC SPECIFICATIONS (AV_{DD} = +5 V, DRV_{DD} = +5 V, f_{SAMPLE} = 1 MSPS, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	AD9221	Units
SIGNAL-TO-NOISE RATIO		
f_{INPUT} = 100 kHz	70	dB typ
	69	dB min
f_{INPUT} = 500 kHz	70	dB typ
	69	dB min
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)		
f_{INPUT} = 100 kHz	69	dB min
	70	dB typ
f_{INPUT} = 500 kHz	69	dB min
	70	dB typ
TOTAL HARMONIC DISTORTION (THD)		
f_{INPUT} = 100 kHz	–83.4	dB typ
	–77	dB max
f_{INPUT} = 500 kHz	–83.4	dB typ
	–77.5	dB max
SPURIOUS FREE DYNAMIC RANGE		
f_{INPUT} = 100 kHz	–86	dB typ
	–79	dB min
f_{INPUT} = 500 kHz	–86	dB typ
	–79	dB min
Full Power Bandwidth	10	MHz typ
Small Signal Bandwidth	10	MHz typ
Aperture Delay	5	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step	300	ns typ
Overvoltage Recovery Time	400	ns typ

Specifications subject to change without notice.

DC SPECIFICATIONS (AV_{DD} = +5 V, DRV_{DD} = +5 V, f_{SAMPLE} = 1 MSPS, V_{REF} = 2.5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9221	Units
RESOLUTION	12	Bits min
MAX CONVERSION RATE	1.25	MHz min
ACCURACY		
Integral Nonlinearity (INL)	±0.4	LSB typ
	±1	LSB max
Differential Nonlinearity (DNL)	±0.3	LSB typ
	±1	LSB max
INL	±0.6	LSB typ
DNL	±0.3	LSB typ
No Missing Codes	12	Bits Guaranteed
ANALOG INPUT		
Input Span	2	V p-p min
	5	V p-p max
Input (V_{INA} or V_{INB}) Range	0	V min
	AV_{DD}	V max
Input Capacitance	16	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1 V Mode)	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	mV max
Output Voltage (2.5 V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	mV max
Load Regulation	1.5	mA min
(External Load Should Not Change During Conversion)		
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER CONSUMPTION	56.5	mW typ
	65	mW max

Specifications subject to change without notice.

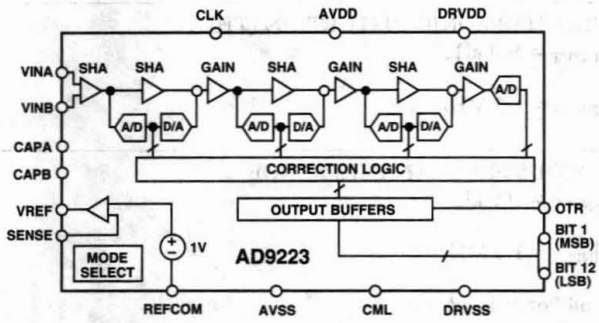
Complete 12-Bit, 3 MSPS Monolithic A/D Converter

AD9223

FEATURES

- Monolithic 12-Bit, 3 MSPS A/D Converter
- Low Power Dissipation: 100 mW
- Single +5 V Supply
- No Missing Codes Guaranteed
- Differential Nonlinearity Error: 0.3 LSB
- Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
- Signal-to-Noise and Distortion Ratio: 70 dB
- Spurious-Free Dynamic Range: –88 dB
- Out of Range Indicator
- Straight Binary Output Data
- 28-Pin SOIC

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9223 is a monolithic, single supply 12-bit, 3 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9223 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 3 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9223 combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of hybrid and monolithic implementations at a fraction of the power consumption.

The input of the AD9223 has been designed to ease the development of both imaging and communications systems. With a truly differential input structure, the user can select a variety of input ranges and offsets. The dynamic performance is excellent.

The sample-and-hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate.

The AD9223's wideband input combined with the power and cost savings over previously available monolithics and hybrids will enable new design applications in communications, imaging and medical applications.

The AD9223 has an onboard, programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9223 is fabricated on a very cost effective CMOS process. High speed, precision analog circuits are now combined with high density logic circuits.

The AD9223 offers a complete single-chip sampling 12-bit, 3 MSPS analog-to-digital conversion function in a 28-pin SOIC package.

Low Power—The AD9223 at 100 mW consumes a fraction of the power of presently available hybrids and existing monolithic solutions.

Onboard Sample-and-Hold (SHA)—The versatile SHA input can be configured for either single ended or differential inputs.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9223's input range.

Single Supply—The AD9223 uses a single +5 V power supply simplifying system power supply design.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9223AR	–40°C to +85°C	28-Pin 300 mil SOIC	R-28
AD9223-EB		Evaluation Board	

*For outline information see Package Information section.

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AD9223–SPECIFICATIONS

AC SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +5 V, f_{SAMPLE} = 3 MSPS, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	AD9223	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)		
f_{INPUT} = 500 kHz	68.5	dB min
	70	dB typ
f_{INPUT} = 1.5 MHz	69.4	dB min
	68	dB typ
TOTAL HARMONIC DISTORTION (THD)		
f_{INPUT} = 500 kHz	–83.4	dB typ
	–76	dB max
f_{INPUT} = 1.5 MHz	–82.9	dB typ
	–75	dB max
SPURIOUS FREE DYNAMIC RANGE		
f_{INPUT} = 500 kHz	87.5	dB typ
	77.5	dB max
f_{INPUT} = 1.5 MHz	85.7	dB typ
	76	dB max
Full Power Bandwidth	40	MHz typ
Small Signal Bandwidth	40	MHz typ
Aperture Delay	1	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step	43	ns typ
Overvoltage Recovery Time	100	ns typ

DC SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +5 V, f_{SAMPLE} = 3 MSPS, V_{REF} = 2.5 V, VINB = 2.5 V dc, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9223	Units
RESOLUTION	12	Bits min
MAX CONVERSION RATE	3	MHz min
ACCURACY		
Integral Nonlinearity (INL)	±0.5	LSB typ
	±1.25	LSB max
Differential Nonlinearity (DNL)	±0.3	LSB typ
	±1	LSB max
INL	±0.6	LSB typ
DNL	±0.3	LSB typ
No Missing Codes	12	Bits Guaranteed
Zero Error (@ +25°C)	±0.03	% FSR max
Gain Error (@ +25°C)	±1.5	% FSR max
Gain Error (@ +25°C)	±0.75	% FSR max
ANALOG INPUT		
Input Span	2	V p-p min
	5	V p-p max
Input (V_{INA} or V_{INB}) Range	0	V min
	AV_{DD}	V max
Input Capacitance	16	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1 V Mode)	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	mV max
Output Voltage (2.5 V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	mV max
Load Regulation	2.0	mV max
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER CONSUMPTION	100	mW typ
	130	mW max

Specifications subject to change without notice.

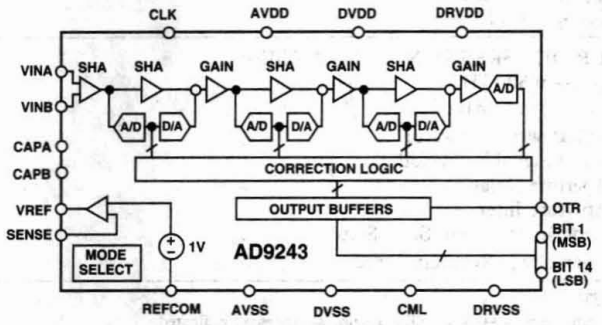
Complete 14-Bit, 3 MSPS Monolithic A/D Converter

AD9243

FEATURES

Monolithic 14-Bit, 3 MSPS A/D Converter
Low Power Dissipation: 100 mW
Single +5 V Supply
No Missing Codes Guaranteed
Differential Nonlinearity Error: ±0.6 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 78 dB F_{IN} = 500 kHz
Spurious-Free Dynamic Range: 86 dB F_{IN} = 500 kHz
Out of Range Indicator
Straight Binary Output Data
44-Pin PQFP
–40°C to 86°C Operating Temperature Range

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9243 is a monolithic, single supply 14-bit, 3 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9243 uses a multistage differential pipelined architecture with output error correction logic to provide 14-bit accuracy at 3 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The AD9243 combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of hybrid and monolithic implementations at a fraction of the power consumption.

The input of the AD9243 has been designed to ease the development of both imaging and communications systems. With a truly differential input structure, the user can select a variety of input ranges and offsets. The dynamic performance is excellent.

The sample-and-hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate.

The AD9243's wideband input combined with the power and cost savings over previously available monolithics and hybrids will enable new design applications in communications, imaging and medical applications.

The AD9243 has an onboard, programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9243 is fabricated on a very cost effective CMOS process. High speed, precision analog circuits are now combined with high density logic circuits.

The AD9243 offers a complete single-chip sampling 14-bit, 3 MSPS analog-to-digital conversion function in a 44-pin PQFP package.

Low Power—The AD9243 at 100 mW consumes a fraction of the power of presently available hybrids and existing monolithic solutions.

Onboard Sample-and-Hold (SHA)—The versatile SHA inputs can be configured for either single ended or differential inputs.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9243's input range.

Single Supply—The AD9243 uses a single +5 V power supply simplifying system power supply design.

Excellent ac Performance and Low Noise—The AD9243 provides better than 12.5 ENOB performance and has an input referred noise of 0.36 LSB rms.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD9243–SPECIFICATIONS

AC SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, f_{SAMPLE} = 3 MSPS, V_{IN} = 5 V p-p Differential, V_{CM} = 2.5 V, V_{REF} = 2.5 V, VINB = 2.5 V dc unless otherwise noted)[1]

Parameters	AD9243	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)		
f_{INPUT} = 500 kHz	78	dB typ
f_{INPUT} = 1.5 MHz	72	dB typ
TOTAL HARMONIC DISTORTION (THD)		
f_{INPUT} = 500 kHz	–84	dB typ
f_{INPUT} = 1.5 MHz	–72	dB typ
SPURIOUS FREE DYNAMIC RANGE		
f_{INPUT} = 500 kHz	86	dB typ
f_{INPUT} = 1.5 MHz	74	dB typ
Full Power Bandwidth	40	MHz typ
Small Signal Bandwidth	40	MHz typ
Aperture Delay	1	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step	100	ns typ
Overvoltage Recovery Time[1]	100	ns typ

NOTES
[1]F_{IN} amplitude = –0.5 dB full scale unless otherwise indicated.

Specifications subject to change without notice.

DC SPECIFICATIONS (AV_{DD} = +5 V, DV_{DD} = +5 V, DRV_{DD} = +5 V, f_{SAMPLE} = 3 MSPS, V_{REF} = 2.5 V, VINB = 2.5 V dc unless otherwise noted)

Parameter	AD9243	Units
RESOLUTION	14	Bits min
MAX CONVERSION RATE	3	MHz min
ACCURACY		
Integral Nonlinearity (INL)	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.6	LSB typ
No Missing Codes	14	Bits Guaranteed
Zero Error (@ 25°C)	±0.3	% FSR max
Gain Error (@ 25°C)[1]	±1.5	% FSR max
Gain Error (@ 25°C)[2]	±0.75	% FSR max
POWER SUPPLY REJECTION		
AV_{DD}, DV_{DD} (+5 V ± 0.25 V)	±0.06	% FSR max
ANALOG INPUT		
Input Span	2	V p-p min
	5	V p-p max
Input (V_{INA} or V_{INB}) Range	0	V min
	AV_{DD}	V max
Input Capacitance	16	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1 V Mode)	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	mV max
Output Voltage (2.5 V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	mV max
Output Current (Available for External Loads) (External Load Should Not Change During Conversion)	1.5	mA min
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER DISSIPATION	100	mW typ
INPUT REFERRED NOISE (TYP)		
V_{REF} = 1	1	LSB rms typ
V_{REF} = 2.5	0.36	LSB rms typ

NOTES
[1]Includes internal voltage reference error.
[2]Excludes internal voltage reference error.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

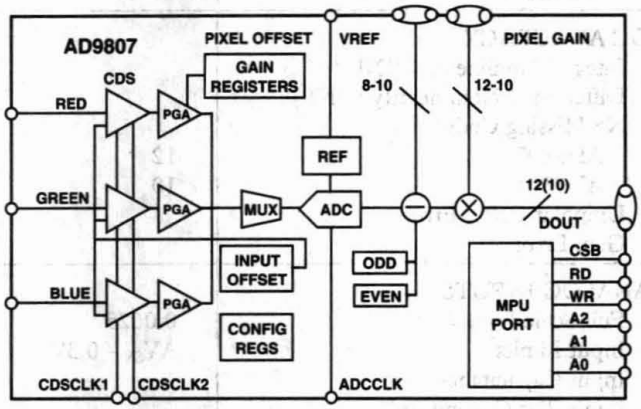
Complete 12-Bit 6 MSPS CCD Signal Processor

AD9807

FEATURES

12-Bit 6 MSPS A/D Converter
Integrated Triple Correlated Double Sampler
3-Channel, 2 MSPS Color Mode
1×–4× Analog Programmable Gain Amplifier
Pin Compatible 10-Bit Version
Pixel-Rate Digital Gain Adjustment
Pixel-Rate Digital Offset Adjustment
Internal Voltage Reference
No Missing Codes Guaranteed
Microprocessor-Compatible Control Interface
+3.3 V/+5 V Digital I/O Compatibility
Low Power CMOS: 500 mW
64-Pin PQFP Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

PRODUCTION DESCRIPTION

The AD9807 is a complete CCD imaging decoder and signal processor on a single monolithic integrated circuit. The input of the AD9807 allows direct ac coupling of the charge-coupled device (CCD) output(s). The AD9807 includes all the circuitry to perform three-channel correlated double sampling (CDS) and programmable gain adjustment of the CCD output; a 12-bit analog-to-digital converter (ADC) quantizes the analog signal. After digitization, the onboard digital signal processor (DSP) circuitry allows pixel rate offset and gain correction. The DSP also corrects odd/even CCD register imbalance errors. A parallel control bus provides a simple interface to 8-bit microcontrollers. The AD9807 comes in a space saving 64-pin plastic quad flatpack (PQFP) and is specified over the commercial (0°C–70°C) temperature range. By disabling the CDS, the AD9807 is also suitable for non-CCD applications or applications that do not require CDS.

PRODUCT HIGHLIGHTS

The AD9807 offers a complete, single-chip, CCD imaging front end in a 64-pin plastic quad flatpack (PQFP).

1. On-Chip PGA
   The AD9807 includes a 3-Channel analog programmable gain amplifier; it is programmable from 1× to 4× in 16 increments.
2. On-Chip CDS
   An integrated 3-channel correlated double sampler allows easy ac coupling directly from the CCD sensor outputs. Additionally the CDS reduces 1/f noise and reset feedthrough.
3. On-Chip Voltage Reference
   The AD9807 includes a 2 V bandgap reference which allows the input range of the AD9807 to be configured for input spans up to 4 V.
4. 12-Bit 6 MSPS A/D Converter
   A highly linear 12-bit A/D converter sequentially digitizes the red, green, and blue CDS outputs ensuring no missing code performance. The user may also configure the AD9807 for single channel operation.
5. Digital Gain & Offset Correction
   Pixel rate digital gain and offset correction blocks allow precise, repeatable correction of imaging system error sources.
6. Digital I/O Compatibility
   The AD9807 offers +3.3 V/+5 V logic level compatibility.
7. Pin-Compatible 10-Bit Version
   The AD9807 is also offered in a pin-compatible 10-bit version, the AD9805, to allow upgradeability and simplifying design issues across different scanner models.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD9807–SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, f_{ADCCLK} = 6 MSPS, $f_{CDSCLK1}$ = 2 MSPS, $f_{CDSCLK2}$ = 2 MSPS unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION				
AD9807	12			Bits
AD9805	10			Bits
CONVERSION RATE				
3-Channel Mode With CDS		6		MSPS
1-Channel Mode With CDS		6		MSPS
DC ACCURACY				
Integral Nonlinearity (INL)[1]		1		LSBs
Differential Nonlinearity (DNL)[1]		1/2	1	LSBs
No Missing Codes				
AD9807	12			LSBs
AD9805	10			LSBs
Unipolar Offset Error		TBD		% FSR
Gain Error		TBD		% FSR
ANALOG INPUTS				
Full Scale Input Span	0.0625		4	V p-p
Input Limits[2]	AV_{SS} – 0.3V		AV_{DD} + 0.3	V
Input Capacitance		TBD		pF
Input Bias Current		0.01		mA
Transient Response		TBD		ns
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	V
DV_{DD}	+4.75		+5.25	V
Operating Current				
AV_{DD}		TBD		mA
DV_{DD}		TBD		mA
POWER CONSUMPTION		500		mW
TEMPERATURE RANGE				
Operating	0		+70	°C

PRELIMINARY TECHNICAL DATA

NOTES
[1]Measured with 4 V p-p input range; AD9807 - 0.01%; AD9805 - 0.1% @ 1 MHz ADC CLK.
[2]Input signals exceeding these limits are subject to excessive overvoltage recovery times.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dual, 12-Bit, 41 MSPS MCM A/D Converter with Front End Analog Signal Conditioning

AD10242

FEATURES

Two Matched ADCs with Input Signal Conditioning
Selectable Bipolar Input Voltage Range (±0.5 V, ±1.0, ±2.0)
Full MIL-STD-883B Compliant
80 dB Spurious-Free Dynamic Range
Trimmed Channel-Channel Matching

APPLICATIONS

Radar Processing
Communications Receivers
FLIR Processing
Secure Communications
Any I/Q Signal Processing Application

PRODUCT DESCRIPTION

The AD10242 is a complete dual signal chain solution including onboard amplifiers, references, ADCs, and output buffering providing unsurpassed total system performance. Each channel is laser trimmed for gain and offset matching and provides channel-to-channel crosstalk performance better than 80 dB. The AD10242 utilizes two each of the AD9631, OP279, and the AD9042 in a custom MCM to gain space, performance, and cost advantages over solutions previously available.

The AD10242 operates with ±5.0 V for the analog signal conditioning with a separate +5.0 V supply for the analog-to-digital conversion. Each channel is completely independent allowing operation with independent encode or analog inputs. The AD10242 also offers the user a choice of analog input signal ranges to minimize additional signal conditioning required for multiple functions within a single system. The heart of the AD10242 is the AD9042 which is designed specifically for applications requiring wide dynamic range.

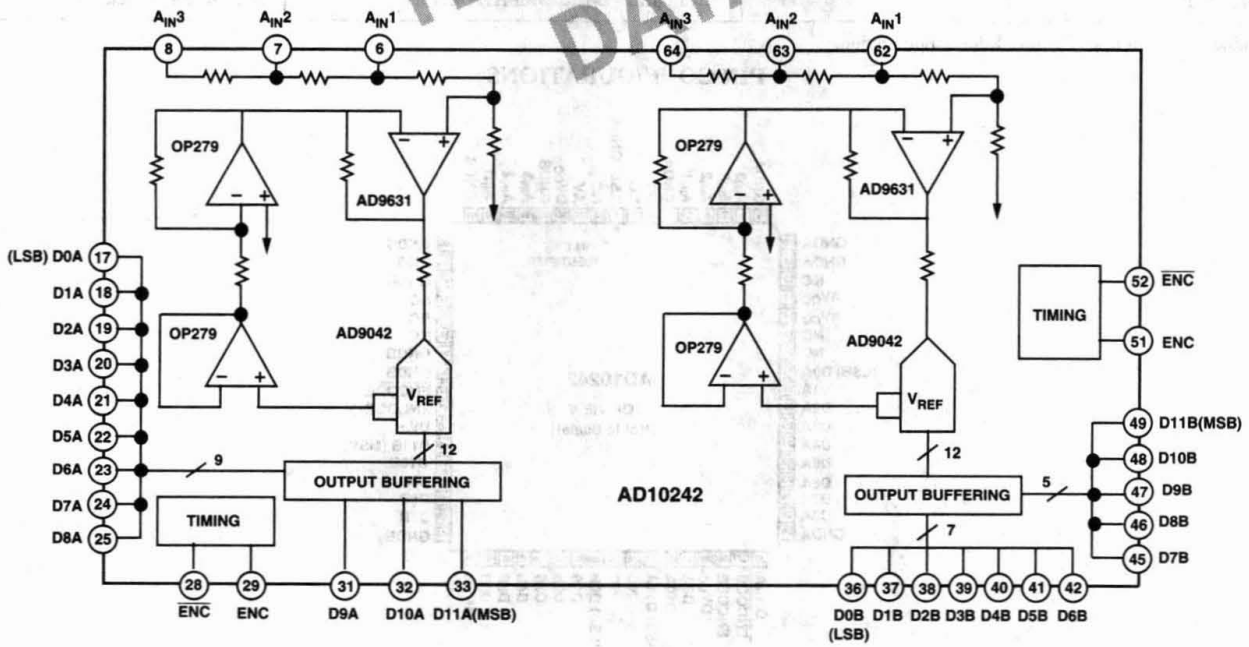
The AD10242 is manufactured by Analog Devices on our MIL-1772 MCM line and is completely qualified to MIL-STD-883B. Units are packaged in a custom cofired ceramic 68-lead gull wing package and specified for operation from –55°C to +125°C. Contact the factory for additional custom options including those which allow the user to ac couple the ADC directly, bypassing the front end amplifier section. Also see the AD9042 data sheet for additional details on ADC performance.

PRODUCT HIGHLIGHTS

1. Guaranteed sample rate of 41 MSPS.
2. Dynamic performance specified over entire Nyquist band; spurious signals @ 80 dBc for –1 dBFS input signals.
3. Low power dissipation: <2 W off ±5.0 V supplies.
4. User defined input amplitude.
5. Packaged in 68-lead ceramic leaded chip carrier.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



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AD10242–SPECIFICATIONS

Electrical Characteristics (AV_{CC} = +5 V; AV_{EE} = –5.0 V; DV_{CC} = +5 V; applies to each ADC unless otherwise noted)

Parameter	Temp	Test Level	Mil Subgroup	AD10242BZ/TZ Min	Typ	Max	Units
DC ACCURACY							
No Missing Codes	Full	VI	1, 2, 3		Guaranteed		
Offset Error	+25°C	I	1	–0.25	±0.05	+0.25	% FS
	Full	VI	2, 3	–2.2	±1.0	+2.2	% FS
Offset Error Channel Match	Full	V			±0.1		% FS
Gain Error	+25°C	I	1	–1.0	±0.5	+1.0	% FS
	Full	VI	2, 3	–1.5	±0.8	+1.5	% FS
Gain Error Channel Match	Full	V			±0.1		% FS
ANALOG INPUT (A_{IN})							
Input Voltage Range							
$A_{IN}1$	Full	I			±0.5		V
$A_{IN}2$	Full	I			±1.0		V
$A_{IN}3$	Full	I			±2.0		V
SNR							
Analog Input @ 1.2 MHz	+25°C	I	4	63	66		dB
	Full	II	5, 6	62	65		dB
@ 9.6 MHz	+25°C	I	4	63	65		dB
	Full	II	5, 6	62	64		dB
@ 19.5 MHz	+25°C	I	4	60	62		dB
	Full	II	5, 6	59	61		dB
Spurious-Free Dynamic Range							
Analog Input @ 1.2MHz	+25°C	I	4	76	80		dBFS
	Full	II	5, 6	75	79		dBFS
@ 9.6 MHz	+25°C	I	4	65	70		dBFS
	Full	II	5, 6	64	69		dBFS
@ 19.5 MHz	+25°C	V			61		dBFS
	Full	IV			61		dBFS

Specifications subject to change without notice.

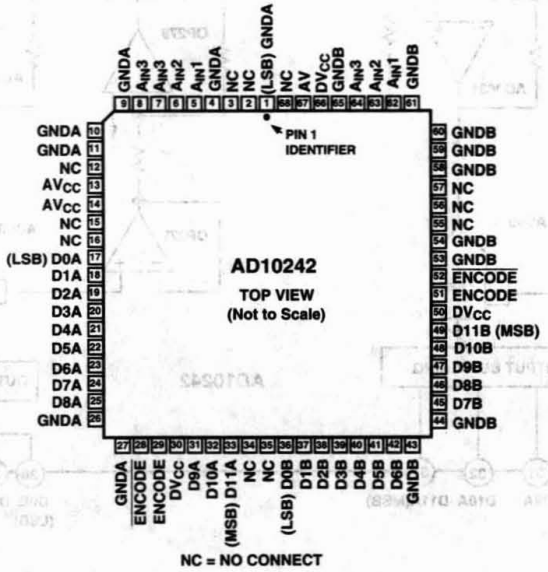
PRELIMINARY TECHNICAL DATA

ORDERING GUIDE*

Model	Temperature Range	Package Description	Notes
AD10242BZ	–40°C to +85°C (Case)	68-Pin Ceramic Leaded Chip Carrier	Part # after Product Release
AD10242TZ/883B	–55°C to +125°C (Case)	68-Pin Ceramic Leaded Chip Carrier	Part # after Product Release
AD10242/PCB	+25°C	Evaluation Board with AD10242BZ	Available after release.

*For outline information see Package Information section.

PIN CONFIGURATIONS



NC = NO CONNECT

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Analog Computation Circuits
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Analog Computation Circuits–Selection Guides

Analog Multipliers

Model	Transfer Function	Small Signal BW MHz	Slew Rate V/μs	Total Nonlinearity Error @ +25°C % FS	X Input % FS	Y Input % FS	Power Supplies Volts	Page No.	Comments	Fax-code
AD534	$V_{OUT} = (X_1 - X_2)(Y_1 - Y_2)/10 - (Z_1 + Z_2)$	1	20	±0.25–1	0.12–0.3	0.1	±15 @ 6 mA	3–5	High Accuracy	1146
AD633	$V_{OUT} = (X_1 - X_2)(Y_1 - Y_2)/10 + Z$	1	20	±2	1	0.4	±15 @ 6 mA	3–13	Low Cost	1204
AD734	$V_{OUT} = (X_1 - X_2)(Y_1 - Y_2)/(U_1 - U_2) - (Z_1 - Z_2)$	8		±0.4–1	NS	NS	±15 @ 12 mA	3–23	Wide Bandwidth	1274
AD538	$V_{OUT} = (V_Y)\left(\frac{V_Z}{V_X}\right)^m$	0.4	1.4	±1			±15 @ 7 mA	*	m = 1/5 to 5	1149
AD539	$V_{OUT1} = -(V_X)(V_{Y1})$ $V_{OUT2} = (V_X)(V_{Y2})$	50		±2.5			±15 @ 10.2/22.2 mA	*	Dual Signal Channels	1150
AD834	$V_{OUT} = \left[\frac{(V_X)(V_Y)}{V^2}\right][4\text{ mA}]$	500		±2			±5 @ 14/35 mA	3–29	Differential Current Output	1414
AD835	$V_{OUT} = (V_X)(V_Y) + V_Z$	200		±5	0.7	0.5	±5 @ 14/35 mA	3–31	Single Ended Voltage Output	1415
MLT04	$V_{OUT} = (V_X)(V_Y)/2.5$ V	8	30	±5	1	1	±5 @ ±240 mA	3–33	Quad	1652
AD639	See Data Sheet for Specs							*	Trig Function Generator	1207

Log Amplifiers

Model	V_{SS} Volts	I_{SS} mA	–3 dB BW MHz	AC Linearity dB	DC Linearity dB	Gain dB	# Pins	Page No.	Comments	Fax-code
AD640	±5	15, –60	145	0.5–2	0.6–1.2	50	20	3–19	Laser Trimmed	1208
AD640	±5	15, –60	145	1–3	0.6–1.2	> 70 dB	NA	3–19	Cascading 2 AD640s	
AD641	±5	15, –60	250	2	NS	44	20	3–21		1908
AD606	+5	20	50	1.5	NS	80	16	3–9	With Limiters + RSSI	1196

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

True RMS Converters

Model	Total Error @ +25°C mV ± % of Reading	Error vs. Crest Factor CF = 3 % Reading	Error vs. Crest Factor CF = 7 % Reading	±3 dB Bandwidth kHz 100 mV	Input Level V rms	dB Output	Power Supplies Volts	Page No.	Comments	Fax-code
AD536A	±2/5 ± 0.2/0.5	0.1	1	450	7 V	Yes	±15 @ 2 mA	3–7	Specs are with Internal Trim	1147
AD636	±0.2/0.5 ± 0.5/1.0	0.2	0.5	900	200 mV	Yes	±5 @ 1 mA	3–15	Specs are with Internal Trim	1205
AD637	±0.5/1.0 ± 0.2/0.5	0.1	1	1000	7 V	Yes	±15 @ 3 mA	3–17	With Shutdown I_Q = 450 µA	1206
AD736	±0.3/5 ± 0.3/0.5	0.7	2.5	37	200 mV	No	±5 @ 0.2 mA	3–25		1276
AD737	±0.2/0.4 ± 0.3/0.5	0.7	2.5	90	200 mV	No	±5 @ 0.16 mA	3–27	With Shutdown I_Q = 4 µA	1277

Balanced Modulator Demodulator

Model	Unity Gain BW MHz	Gain	Gain Error	Output Slew Rate V/µs	CH Separation @ 10 kHz	# Pins	Power Supplies Volts	Page No.	Comments	Fax-code
AD630	2	±1, ±2	0.05%	45	100 dB	20	±15 @ 5 mA	3–11	Recover a Signal from 100 dB Noise	1202

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

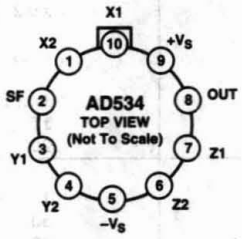
AD534

FEATURES

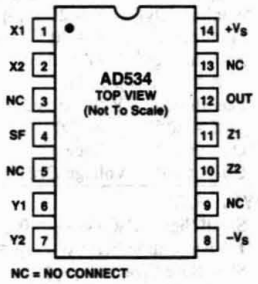
Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1 - X_2)(Y_1 - Y_2)/10\ V] + Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90 μV rms, 10 Hz–10 kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

PIN CONFIGURATIONS

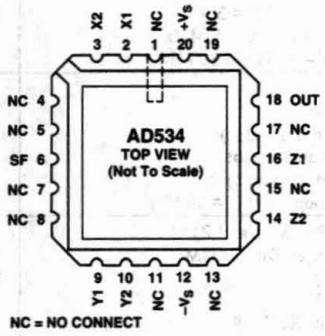
TO-100 (H-10A) Package



TO-116 (D-14) Package



LCC (E-20A) Package



PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability preserve accuracy even under adverse conditions of use. It offers fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00 V; by means of an external resistor, this can be reduced to values as low as 3 V.

PROVIDES GAIN WITH LOW NOISE

The AD534 is a general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. This feature is enhanced by the inherent low noise of the AD534: 90 μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD534JD	0°C to +70°C	Side Brazed DIP	D-14
AD534KD	0°C to +70°C	Side Brazed DIP	D-14
AD534LD	0°C to +70°C	Side Brazed DIP	D-14
AD534JH	0°C to +70°C	Header	H-10A
AD534KH	0°C to +70°C	Header	H-10A
AD534LH	0°C to +70°C	Header	H-10A
AD534JCHIP	0°C to +70°C	Chip	
AD534KCHIP	0°C to +70°C	Chip	
AD534SD	–55°C to +125°C	Side Brazed DIP	D-14
AD534SD/883B	–55°C to +125°C	Side Brazed DIP	D-14
AD534TD	–55°C to +125°C	Side Brazed DIP	D-14
AD534TD/883B	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13902BCA	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13901BCA	–55°C to +125°C	Side Brazed DIP	D-14

Model	Temperature Range	Package Description	Package Option*
AD534SE	–55°C to +125°C	LCC	E-20A
AD534SE/883B	–55°C to +125°C	LCC	E-20A
AD534TE	–55°C to +125°C	LCC	E-20A
AD534TE/883B	–55°C to +125°C	LCC	E-20A
AD534SH	–55°C to +125°C	Header	H-10A
AD534SH/883B	–55°C to +125°C	Header	H-10A
AD534TH	–55°C to +125°C	Header	H-10A
AD534TH/883B	–55°C to +125°C	Header	H-10A
JM38510/13902BIA	–55°C to +125°C	Header	H-10A
JM38510/13901BIA	–55°C to +125°C	Header	H-10A
AD534SCHIP	–55°C to +125°C	Chip	
AD534TCHIP	–55°C to +125°C	Chip	

*For outline information see Package Information section.

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AD534—SPECIFICATIONS (@ T_A = + 25°C, $\pm V_S$ = 15 V, R ≥ 2 kΩ)

Model	AD534J			AD534K			AD534L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$		
Total Error[1] (–10 V ≤ X, Y ≤ +10 V)			±1.0			±0.5			±0.25	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs. Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000 V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15 V ± 1 V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)		±0.4			±0.2	±0.3		±0.10	±0.12	%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)		±0.2			±0.1	±0.1		±0.005	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20 V p-p 50 Hz)		±0.3			±0.15	±0.3		±0.05	±0.12	%
Feedthrough[3], Y (X Nulled, Y = 20 V p-p 50 Hz)		±0.01			±0.01	±0.1		±0.003	±0.1	%
Output Offset Voltage		±5	±30		±2	±15		±2	±10	mV
Output Offset Voltage Drift		200			100			100		µV/°C
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000 pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 p-p)		20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20 V)		2			2			2		µs
NOISE										
Noise Spectral-Density SF = 10 V		0.8			0.8			0.8		µV/√Hz
SF = 3 V[4]		0.4			0.4			0.4		µV/√Hz
Wideband Noise f = 10 Hz to 5 MHz		1			1			1		mV/rms
f = 10 Hz to 10 kHz		90			90			90		µV/rms
OUTPUT										
Output Voltage Swing	±11			±11			±11			V
Output Impedance (f ≤ 1 kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50 Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	±20		±2	±10		±2	±10	mV
Offset Voltage Drift X, Y		100			50			50		µV/°C
Offset Voltage Z		±5	±30		±2	±15		±2	±10	mV
Offset Voltage Drift Z		200			100			100		µV/°C
CMRR	60	80		70	90		70	90		dB
Bias Current		0.8	2.0		0.8	2.0		0.8	2.0	µA
Offset Current		0.1			0.1			0.05	0.2	µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10 V, –10 V ≤ Z ≤ +10 V)		±0.75			±0.35			±0.2		%
(X = 1 V, –1 V ≤ Z ≤ +1 V)		±2.0			±1.0			±0.8		%
(0.1 V ≤ X ≤ 10 V, –10 V ≤ Z ≤ 10 V)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$		
Total Error (–10 V ≤ X ≤ 10 V)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$		
Total Error[1] (1 V ≤ Z ≤ 10 V)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±8		±18	±8		±18	±8		±18	V
Supply Current										
Quiescent		4	6		4	6		4	6	mA

NOTES

[1]Figures given are percent of full scale, ±10 V (i.e., 0.01% = 1 mV).

[2]May be reduced down to 3 V using external resistor between $-V_S$ and SF.

[3]Irreducible component due to nonlinearity: excludes effect of offsets.

[4]Using external resistor adjusted to give SF = 3 V.

[5]See Functional Block Diagram for definition of sections.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ANALOG DEVICES

Integrated Circuit, True RMS-to-DC Converter

AD536A

FEATURES

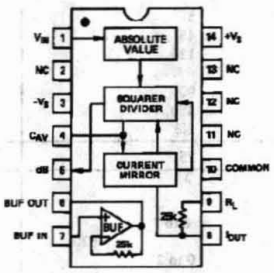
True RMS-to-DC Conversion
Laser-Trimmed to High Accuracy
- **0.2% max Error (AD536AK)**
- **0.5% max Error (AD536AJ)**

Wide Response Capability:
- **Computes RMS of AC and DC Signals**
- **450 kHz Bandwidth: V rms > 100 mV**
- **2 MHz Bandwidth: V rms > 1 V**
- **Signal Crest Factor of 7 for 1% Error**

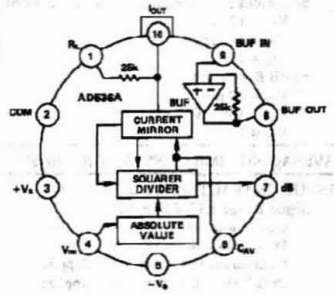
dB Output with 60 dB Range
Low Power: 1.2 mA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit
–55°C to +125°C Operation (AD536AS)

PIN CONFIGURATIONS AND FUNCTIONAL BLOCK DIAGRAMS

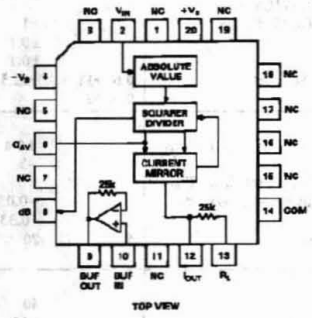
TO-116 (D-14) and Q-14 Package



TO-100 (H-10A) Package



LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300 kHz with 3 dB error for signal levels above 100 mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0 dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 7 V rms. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0°C to +70°C) applications, and one grade (S) rated for the –55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2 mV ±0.2% of reading, and the AD536AJ and AD536AS have maximum errors of ±5 mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can. The AD536AS is also available in a 20-pin hermetically sealed ceramic leadless chip carrier.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD536AJD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AKD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AJH	0°C to +70°C	Header	H-10A
AD536AKH	0°C to +70°C	Header	H-10A
AD536AJQ	0°C to +70°C	Cerdip	Q-14
AD536AKQ	0°C to +70°C	Cerdip	Q-14
AD536ASD	–55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASD/883B	–55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASE	–55°C to +125°C	LCC	E-20A
AD536ASE/883B	–55°C to +125°C	LCC	E-20A
AD536ASH	–55°C to +125°C	Header	H-10A
AD536ASH/883B	–55°C to +125°C	Header	H-10A

NOTES
[1]"S" grade chips are available tested at +25°C and +125°C. "J" grade chips are also available.
[2]For outline information see Package Information section.

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AD536A–SPECIFICATIONS (@ +25°C, and ±15 V dc unless otherwise noted)

Model	AD536AJ Min	AD536AJ Typ	AD536AJ Max	AD536AK Min	AD536AK Typ	AD536AK Max	AD536AS Min	AD536AS Typ	AD536AS Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			**±5 ±0.5**			**±2 ±0.2**			**±5 ±0.5**	mV ± % of Reading
vs. Temperature, T_{MIN} to +70°C			±0.1 ±0.01			±0.05 ±0.005			**±0.1 ±0.005**	mV ± % of Reading/°C
+70°C to +125°C									**±0.3 ±0.005**	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		–0.1			–0.1			–0.1		% of Reading
Crest Factor = 7		–1.0			–1.0			–1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% Additional Error (0.09 dB)										
V_{IN} = 10 mV		5			5			5		kHz
V_{IN} = 100 mV		45			45			45		kHz
V_{IN} = 1 V		120			120			120		kHz
±3 dB Bandwidth										
V_{IN} = 10 mV		90			90			90		kHz
V_{IN} = 100 mV		450			450			450		kHz
V_{IN} = 1 V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ±5 V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ±5 V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive										
Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	±2		±0.5	±1			**±2**	mV
vs. Temperature		±0.1			±0.1				**±0.2**	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15 V Supplies	**0 to +11**	+12.5		**0 to +11**	+12.5		**0 to +11**	+12.5		V
±5 V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 13)										
Error, V_{IN} 7 mV to 7 V rms, 0 dB = 1 V rms		±0.4	**±0.6**		±0.2	**±0.3**		±0.5	**±0.6**	dB
Scale Factor		–3			–3			–3		mV/dB
Scale Factor TC (Uncompensated, see Figure 1 for Temperature Compensation)		–0.033			–0.033			–0.033		dB/°C
		+0.33			+0.33			+0.33		% of Reading/°C
I_{REF} for 0 dB = 1 V rms	5	20	**80**	5	20	**80**	5	20	**80**	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ –2.5 V)			$-V_S$ to ($+V_S$ –2.5 V)			$-V_S$ to ($+V_S$ –2.5 V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to ($+V_S$ –2.5 V)			$-V_S$ to ($+V_S$ –2.5 V)			$-V_S$ to ($+V_S$ –2.5 V)			V
Input Offset Voltage, R_S = 25 k		±0.5	**±4**		±0.5	**±4**		±0.5	**±4**	mV
Input Bias Current		20	**60**		20	**60**		20	**60**	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5 mA, –130 μA)			(+5 mA, –130 μA)			(+5 mA, –130 μA)			
Short Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5 V to 36 V, T_{MIN} to T_{MAX}		1.2	**2**		1.2	**2**		1.2	**2**	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	–55		+125	°C
NUMBER OF TRANSISTORS		65			65			65		

NOTES

[1]Accuracy is specified for 0 V to 7 V rms, dc or 1 kHz sine wave input with the AD536A connected as in the figure referenced.

[2]Error vs. crest factor is specified as an additional error for 1 V rms rectangular pulse input, pulse width = 200μs.

[3]Input voltages are expressed in volts rms, and error is percent of reading.

[4]With 2k external pull-down resistor.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output

AD606

FEATURES

Logarithmic Amplifier Performance
- –75 dBm to +5 dBm Dynamic Range
- ≤1.5 nV/√Hz Input Noise
- Usable to >50 MHz
- 37.5 mV/dB Voltage Output
- On-Chip Low-Pass Output Filter

Limiter Performance
- ±1 dB Output Flatness over 80 dB Range
- ±3° Phase Stability at 10.7 MHz over 80 dB Range
- Adjustable Output Amplitude

Low Power
- +5 V Single Supply Operation
- 65 mW Typical Power Consumption
- CMOS Compatible Power-Down to 325 μW typ
- <5 μs Enable/Disable Time

APPLICATIONS

- Ultrasound and Sonar Processing
- Phase-Stable Limiting Amplifier to 100 MHz
- Received Signal Strength Indicator (RSSI)
- Wide Range Signal and Power Measurement

PRODUCT DESCRIPTION

The AD606 is a complete, monolithic logarithmic amplifier using a 9-stage "successive-detection" technique. It provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation low-pass filter and provides a loadable output voltage of +0.1 V dc to +4 V dc. The logarithmic scaling is such that the output is +0.5 V for a sinusoidal input of –75 dBm and +3.5 V at an input of +5 dBm; over this range the logarithmic linearity is typically within ±0.4 dB. All scaling parameters are proportional to the supply voltage.

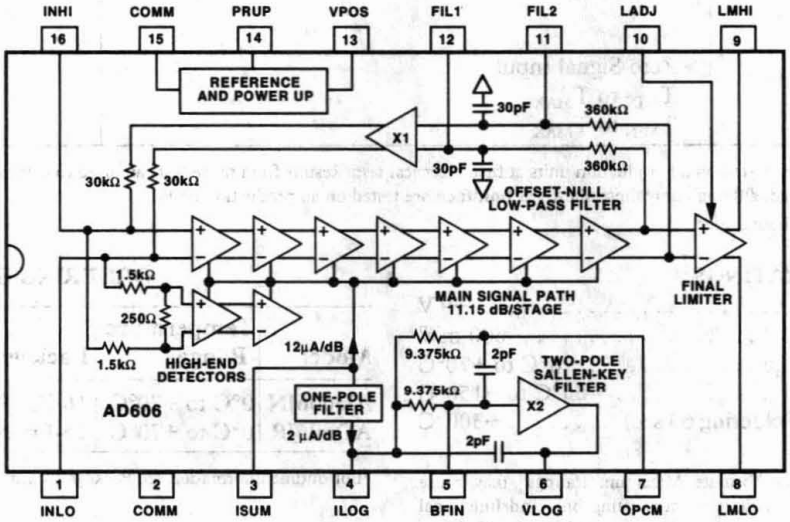
The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90 dB of conversion range. A second low-pass filter automatically nulls the input offset of the first stage down to the submicrovolt level. Adding external capacitors to both filters allows operation at input frequencies as low as a few hertz.

The AD606's limiter output provides a hard-limited signal output as a differential current of ±1.2 mA from open-collector outputs. In a typical application, both of these outputs are loaded by 200 Ω resistors to provide a voltage gain of more than 90 dB from the input. Transition times are 1.5 ns, and the phase is stable to within ±3° at 10.7 MHz for signals from –75 dBm to +5 dBm.

The logarithmic amplifier operates from a single +5 V supply and typically consumes 65 mW. It is enabled by a CMOS logic level voltage input, with a response time of <5 μs. When disabled, the standby power is reduced to <1 mW within 5 μs.

The AD606J is specified for the commercial temperature range of 0°C to +70°C and is available in 16-pin plastic DIPs or SOICs. Consult the factory for other packages and temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



AD606–SPECIFICATIONS (@ T_A = +25°C and supply = +5 V unless otherwise noted; dBm assumes 50 Ω)

Model / Parameter	Conditions	AD606J Min	Typ	Max	Units
SIGNAL INPUT					
Log Amp f_{MAX}	AC Coupled; Sinusoidal Input		50		MHz
Limiter f_{MAX}	AC Coupled; Sinusoidal Input		100		MHz
Dynamic Range			80		dB
Input Resistance	Differential Input	500	2,500		Ω
Input Capacitance	Differential Input		2		pF
SIGNAL OUTPUT					
Limiter Flatness	–75 dBm to +5 dBm Input Signal at 10.7 MHz With Pin 9 to V_{POS} via a 200 Ω Resistor and Pin 8 to V_{POS} via a 200 Ω Resistor	–1.5		+1.5	dB
Output Current	At Pins 8 or 9, Proportional to V_{POS}, LADJ Grounded		1.2		mA
	LADJ Open Circuited		0.48		mA
Phase Variation with Input Level	–75 dBm to +5 dBm Input Signal at 10.7 MHz		±3		°
LOG (RSSI) OUTPUT					
Nominal Slope	At 10.7 MHz; (0.0075 × V_{POS})/dB		37.5		mV/dB
	At 45 MHz		35		mV/dB
Slope Accuracy	Untrimmed at 10.7 MHz	–15	±5	+15	%
Intercept	Sinusoidal Input; Independent of V_{POS}		–88.33		dBm
Logarithmic Conformance	–75 dBm to +5 dBm Input Signal at 10.7 MHz	–1.5	0.4	+1.5	dB
Nominal Output	Input Level = –75 dBm		0.5		V
	Input Level = –35 dBm		2		V
	Input Level = +5 dBm		3.5		V
Accuracy over Temperature	After Calibration at –35 dBm at 10.7 MHz T_{MIN} to T_{MAX}	–3		3	dB
Video Response Time	From Onset of Input Signal Until Output Reaches 95% of Final Value		400		ns
POWER-DOWN INTERFACE					
Power-Up Response Time	Time Delay Following HI Transition Until Device Meets Full Specifications AC Coupled with 100 pF Coupling Capacitors		3.5		µs
Input Bias Current	Logical HI Input (See Figure 12)		1		nA
	Logical LO Input		4		µA
POWER SUPPLY					
Operating Range		4.5		5.5	V
Powered-Up Current	Zero Signal Input		13		mA
	T_{MIN} to T_{MAX}		13	20	mA
Powered-Down Current	T_{MIN} to T_{MAX}		65	200	µA

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage V_{POS} . . . . . +9 V
Internal Power Dissipation[2] . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
16-Pin Plastic DIP Package: θ_{JA} = 85°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD606JN	0°C to +70°C	16-Pin Plastic DIP (N-16)
AD606JR	0°C to +70°C	16-Pin Narrow-Body SOIC (R-16A)

*For outline information see Package Information section.

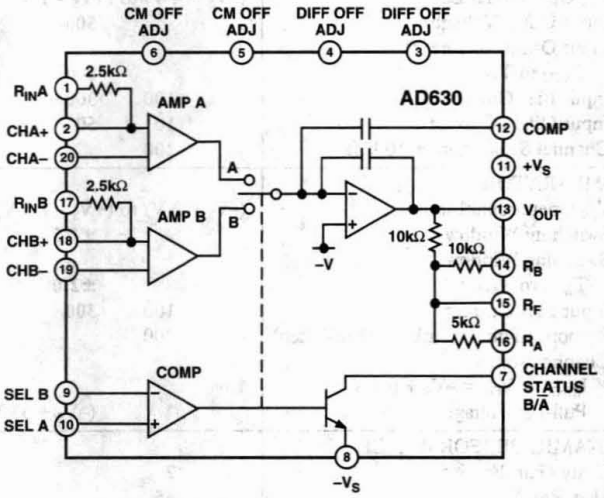
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100 dB Noise
2 MHz Channel Bandwidth
45 V/μs Slew Rate
–120 dB Crosstalk @ 1 kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100 μV Channel Offset Voltage (AD630BD)
350 kHz Full Power Bandwidth
Chips Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin-film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of –100 dB @ 10 kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100 dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1 kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common-mode and differential-offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active. This device is now available to Standard Military Drawing (DESC) numbers 5962-8980701RA and 5962-89807012A.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100 dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100 dB @ 10 kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

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AD630–SPECIFICATIONS (@ + 25°C and $\pm V_S = \pm 15$ V unless otherwise noted)

Model	AD630J/A			AD630K/B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm °C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S + 4\ V)$ to $(+V_S - 1\ V)$			$(-V_S + 4\ V)$ to $(+V_S - 1\ V)$			$(-V_S + 4\ V)$ to $(+V_S - 1\ V)$			Volts
Input Offset Voltage			500			100			500	µV
Input Offset Voltage T_{MIN} to T_{MAX}			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10 kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S + 3\ V)$ to $(+V_S - 1.5\ V)$			$(-V_S + 3\ V)$ to $(+V_S - 1.5\ V)$			$(-V_S + 3\ V)$ to $(+V_S - 1.3\ V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window T_{MIN} to T_{MAX}[2]			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (–5 mV to +5 mV Step)		200			200			200		ns
Channel Status I_{SINK} @ $V_{OL} = -V_S + 0.4\ V$[3]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S + 33\ V)$			$(-V_S + 33\ V)$			$(-V_S + 33\ V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[4]		45			45			45		V/µs
Settling Time to 0.1% (20 V Step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ $R_L = 2\ k\Omega$ T_{MIN} to T_{MAX}[2]	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance–N Package	0		+70	0		+70		N/A		°C
D Package	–25		+85	–25		+85	–55		+125	°C

NOTES

[1]If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2]These parameters are guaranteed but not tested for J and K grades. For A, B and S grades they are tested.

[3]I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4 mA.

[4]Pin 12 Open. Slew rate with Pins 12 and 13 shorted is typically 35 V/µs.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 600 mW
Output Short Circuit to Ground . . . . . Indefinite
Storage Temperature, Ceramic Package . . . . –65°C to +150°C
Storage Temperature, Plastic Package . . . . . –55°C to +125°C
Lead Temperature Range (Soldering, 10 sec) . . . . . +300°C
Max Junction Temperature . . . . . +150°C

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
20-Pin Plastic DIP (N)	24°C/W	61°C/W
20-Pin Ceramic DIP (D)	35°C/W	120°C/W
20-Pin Leadless Chip Carrier (E)	35°C/W	120°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD630JN	0°C to +70°C	Plastic DIP	N-20
AD630KN	0°C to +70°C	Plastic DIP	N-20
AD630AD	–25°C to +85°C	Side Brazed DIP	D-20
AD630BD	–25°C to +85°C	Side Brazed DIP	D-20
AD630SD	–55°C to +125°C	Side Brazed DIP	D-20
AD630SD/883B	–55°C to +125°C	Side Brazed DIP	D-20
5962-8980701RA	–55°C to +125°C	Side Brazed DIP	D-20
AD630SE/883B	–55°C to +125°C	LCC	E-20A
5962-89807012A	–55°C to +125°C	LCC	E-20A
AD630J Chip	0°C to +70°C	Chip	
AD630S Chip	–55°C to +125°C	Chip	

*For outline information see Package Information section.

ANALOG DEVICES

Low Cost Analog Multiplier

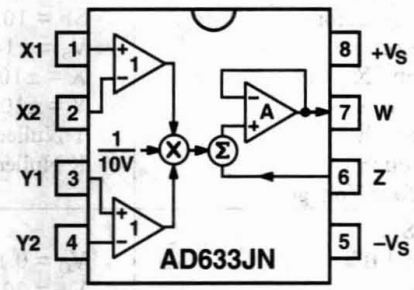
AD633

FEATURES
Four-Quadrant Multiplication
Low Cost 8-Pin Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

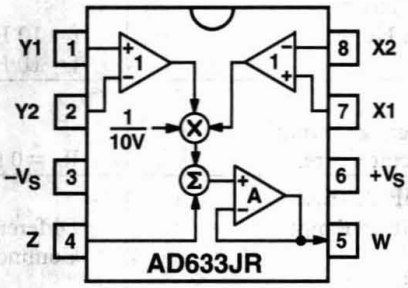
APPLICATIONS
Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/Filters

CONNECTION DIAGRAMS

8-Pin Plastic DIP (N) Package



8-Pin Plastic SOIC (R) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-pin plastic DIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

The AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0°C to +70°C commercial temperature range.

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-pin plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

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AD633—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model		AD633J			
TRANSFER FUNCTION		$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	–10 V ≤ X, Y ≤ +10 V		±1	**±2**	% Full Scale
T_{MIN} to T_{MAX}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5	**±50**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms,		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		μV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	**60**	80		dB
Bias Current X, Y, Z			0.8	**2.0**	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		**±8**		**±18**	V
Supply Current	Quiescent		4	**6**	mA

NOTES

Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Internal Power Dissipation[2] ..... 500 mW
Input Voltages[3] ..... ±18 V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C
ESD Rating ..... 1000 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

[2]8-Pin Plastic Package: θ_{JA} = 165°C/W; 8-Pin Small Outline Package: θ_{JA} = 155°C/W.

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

Model	Description	Package Option*
AD633JN	8-Pin Plastic DIP	N-8
AD633JR	8-Pin Plastic SOIC	R-8
AD633JR-REEL	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.

ANALOG DEVICES

Low Level, True RMS-to-DC Converter

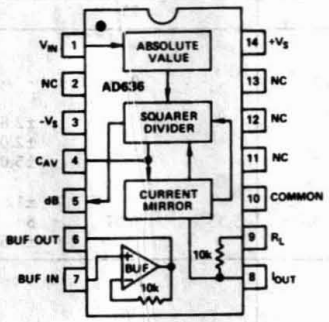
AD636

FEATURES

- True RMS-to-DC Conversion
- 200 mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes RMS of AC and DC Signals
  - 1 MHz –3 dB Bandwidth: V RMS>100 mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50 dB Range
- Low Power: 800 μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- Low Cost
- Available in Chip Form

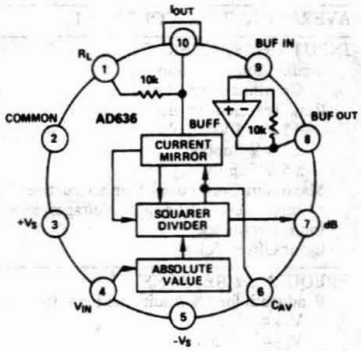
PIN CONNECTIONS & FUNCTIONAL BLOCK DIAGRAM

"D" Package (TO-116)



NC = NO CONNECT

"H" Package (TO-100)



PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 mV to 200 mV rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800 μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5 V to ±16.5 V or a single +5 V to +24 V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0 dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0 dBm (774.6 mV) to –20 dBm (77.46 mV). Frequency response ranges from 1.2 MHz at a 0 dBm level to over 10 kHz at –50 dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 200 mV rms. Thus no external trims are required to achieve full-rated accuracy.

AD636 is available in two accuracy grades; the AD636J total error of ±0.5 mV ±0.06% of reading, and the AD636K is accurate within ±0.2 mV to ±0.3% of reading. Both versions are specified for the 0°C to +70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full-scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10 MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5 V to +24 V or split ±2.5 V to ±16.5 V sources. A standard 9 V battery will provide several hundred hours of continuous operation.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD636JD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD636KD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD636JH	0°C to +70°C	Header	H-10A
AD636KH	0°C to +70°C	Header	H-10A
AD636JCHIP	0°C to +70°C	Chip	
AD636KCHIP	0°C to +70°C	Chip	

*For outline information see Package Information section.

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AD636—SPECIFICATIONS (@ +25°C, and $+V_S$ = +3 V, $-V_S$ = −5 V, unless otherwise noted)

Model	AD636J			AD636K			Units
	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{\text{avg.}\,(V_{IN})^2}$			$V_{OUT} = \sqrt{\text{avg.}\,(V_{IN})^2}$		
CONVERSION ACCURACY							
Total Error, Internal Trim[1, 2]			±0.5 ±1.0			±0.2 ±0.5	mV ±% of Reading
vs. Temperature, 0°C to +70°C			±0.1 ±0.01			±0.1 ±0.005	mV ±% of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01		mV ±% of Reading/V
dc Reversal Error at 200 mV		±0.2			±0.1		% of Reading
Total Error, External Trim[1]		±0.3 ±0.3			±0.1 ±0.2		mV ±% of Reading
ERROR VS. CREST FACTOR[3]							
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.2			−0.2		% of Reading
Crest Factor = 6		−0.5			−0.5		% of Reading
AVERAGING TIME CONSTANT		25			25		ms/μF CAV
INPUT CHARACTERISTICS							
Signal Range, All Supplies							
Continuous rms Level		0 to 200			0 to 200		mV rms
Peak Transient Inputs							
+3 V, −5 V Supply			±2.8			±2.8	V pk
±2.5 V Supply			±2.0			±2.0	V pk
±5 V Supply			±5.0			±5.0	V pk
Maximum Continuous Nondestructive							
Input Level (All Supply Voltages)			±12			±12	V pk
Input Resistance	5.33	6.67	8	5.33	6.67	8	kΩ
Input Offset Voltage			±0.5			±0.2	mV
FREQUENCY RESPONSE[2, 4]							
Bandwidth for 1% Additional Error (0.09 dB)							
V_{IN} = 10 mV		14			14		kHz
V_{IN} = 100 mV		90			90		kHz
V_{IN} = 200 mV		130			130		kHz
±3 dB Bandwidth							
V_{IN} = 10 mV		100			100		kHz
V_{IN} = 100 mV		900			900		kHz
V_{IN} = 200 mV		1.5			1.5		MHz
OUTPUT CHARACTERISTICS[2]							
Offset Voltage, V_{IN} = COM			±0.5			±0.2	mV
vs. Temperature		±10			±10		μV/°C
vs. Supply		±0.1			±0.1		mV/ V
Voltage Swing							
+3 V, −5 V Supply	0.3	0 to +1.0		0.3	0 to +1.0		V
±5 V to ±16.5 V Supply	0.3	0 to +1.0		0.3	0 to +1.0		V
Output Impedance	8	10	12	8	10	12	kΩ
dB OUTPUT							
Error, V_{IN} = 7 mV to 300 mV rms		±0.3	±0.5		±0.1	±0.2	dB
Scale Factor		−3.0			−3.0		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33		% of Reading/°C
		−0.033			−0.033		dB/°C
I_{REF} for 0 dB = 0.1 V rms	2	4	8	2	4	8	μA
I_{REF} Range	1		50	1		50	μA
I_{OUT} TERMINAL							
I_{OUT} Scale Factor		100			100		μA/V rms
I_{OUT} Scale Factor Tolerance	−20	±10	+20	−20	±10	+20	%
Output Resistance	8	10	12	8	10	12	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2 V)			$-V_S$ to ($+V_S$ −2 V)		V
BUFFER AMPLIFIER							
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2 V)			$-V_S$ to ($+V_S$ −2 V)			V
Input Offset Voltage, R_S = 10k		±0.8	±2		±0.5	±1	mV
Input Bias Current		100	300		100	300	nA
Input Resistance		10^8			10^8		Ω
Output Current	(+5 mA, −130 μA)			(+5 mA, −130 μA)			
Short Circuit Current		20			20		mA
Small Signal Bandwidth		1			1		MHz
Slew Rate[5]		5			5		V/μs
POWER SUPPLY							
Voltage, Rated Performance		+3, −5			+3, −5		V
Dual Supply	+2, −2.5		±16.5	+2, −2.5		±16.5	V
Single Supply	+5		+24	+5		+24	V
Quiescent Current[6]		0.80	1.00		0.80	1.00	mA
TEMPERATURE RANGE							
Rated Performance	0		+70	0		+70	°C
Storage	−55		+150	−55		+150	°C
TRANSISTOR COUNT		62			62		

NOTES

[1]Accuracy specified for 0 mV to 200 mV rms, dc or 1 kHz sine wave input. Accuracy is degraded at higher rms signal levels.

[2]Measured at Pin 8 of DIP (I_{OUT}), with Pin 9 tied to common.

[3]Error vs. crest factor is specified as additional error for a 200 mV rms rectangular pulse trim, pulse width = 200 μs.

[4]Input voltages are expressed in volts rms.

[5]With 10 kΩ pull down resistor from Pin 6 (BUF OUT) to $-V_S$.

[6]With BUF input tied to Common.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test and are used to calculate outgoing quality levels.

High Precision, Wide-Band RMS-to-DC Converter

AD637

FEATURES

High Accuracy
- 0.02% Max Nonlinearity, 0 V to 2 V RMS Input
- 0.10% Additional Error to Crest Factor of 3

Wide Bandwidth
- 8 MHz at 1 V RMS Input
- 600 kHz at 100 mV RMS

Computes:
- True RMS
- Square
- Mean Square
- Absolute Value

dB Output (60 dB Range)

Chip Select-Power Down Feature Allows:
- Analog "3-State" Operation
- Quiescent Current Reduction from 2.2 mA to 350 μA

Side-Brazed DIP, Low Cost Cerdip and SOIC

PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms-to-dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms-to-dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600 kHz with inputs of 200 mV rms and up to 8 MHz when the input levels are above 1 V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60 dB. An externally programmed reference current allows the user to select the 0 dB reference voltage to correspond to any level between 0.1 V and 2.0 V rms.

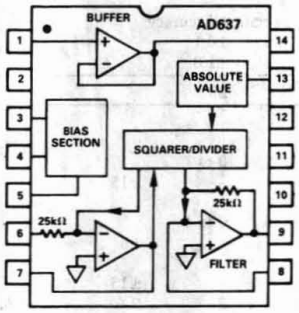
A chip select connection on the AD637 permits the user to decrease the supply current from 2.2 mA to 350 μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

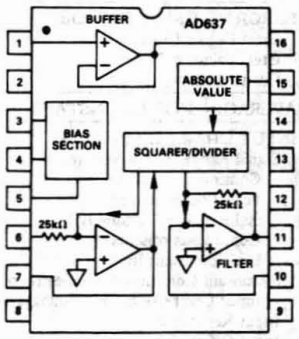
The AD637 is available in two accuracy grades (J, K) for commercial (0°C to +70°C) temperature range applications; two accuracy grades (A, B) for industrial (–40°C to +85°C) applications; and one (S) rated over the –55°C to +125°C temperature range. All versions are available in hermetically-sealed, 14-pin side-brazed ceramic DIPs as well as low cost cerdip packages. A 16-pin SOIC package is also available.

FUNCTIONAL BLOCK DIAGRAM

Ceramic DIP (D) and Cerdip (Q) Packages



SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option[3]
AD637AR	–40°C to +85°C	SOIC	R-16
AD637BR	–40°C to +85°C	SOIC	R-16
AD637AQ	–40°C to +85°C	Cerdip	Q-14
AD637BQ	–40°C to +85°C	Cerdip	Q-14
AD637JD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD637KD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD637JQ	0°C to +70°C	Cerdip	Q-14
AD637KQ	0°C to +70°C	Cerdip	Q-14
AD637JR	0°C to +70°C	SOIC	R-16
AD637JR-REEL	0°C to +70°C	SOIC	R-16
AD637JR-REEL7	0°C to +70°C	SOIC	R-16
AD637KR	0°C to +70°C	SOIC	R-16
AD637SD	–55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD637SD/883B	–55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD637SQ/883B	–55°C to +125°C	Cerdip	Q-14

NOTES
[1]"S" grade chips are also available.
[2]A Standard Microcircuit Drawing, 5962-8963701CA, is also available.
[3]For outline information see Package Information section.

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AD637—SPECIFICATIONS (@ + 25°C, and ±15 V dc unless otherwise noted)

Model	AD637J/A Min	AD637J/A Typ	AD637J/A Max	AD637K/B Min	AD637K/B Typ	AD637K/B Max	AD637S Min	AD637S Typ	AD637S Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 2)			±1 ± 0.5			±0.5 ± 0.2			±1 ± 0.5	mV ± % of Reading
T_{MIN} to T_{MAX}			±3.0 ± 0.6			±2.0 ± 0.3			±6 ± 0.7	mV ± % of Reading
vs. Supply, + V_{IN} = +300 mV		30	150		30	150		30	150	µV/V
vs. Supply, – V_{IN} = +300 mV		100	300		100	300		100	300	µV/V
DC Reversal Error at 2 V			0.25			0.1			0.25	% of Reading
Nonlinearity 2 V Full Scale[2]			0.04			0.02			0.04	% of FSR
Nonlinearity 7 V Full Scale			0.05			0.05			0.05	% of FSR
Total Error, External Trim		±0.5 ± 0.1			±0.25 ± 0.05			±0.5 ± 0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of Reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/µF C_{AV}
INPUT CHARACTERISTICS										
Signal Range, ±15 V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ±5 V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage			±0.5			±0.2			±0.5	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% Additional Error (0.09 dB)										
V_{IN} = 20 mV		11			11			11		kHz
V_{IN} = 200 mV		66			66			66		kHz
V_{IN} = 2 V		200			200			200		kHz
±3 dB Bandwidth										
V_{IN} = 20 mV		150			150			150		kHz
V_{IN} = 200 mV		1			1			1		MHz
V_{IN} = 2 V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs. Temperature		±0.05	±0.089		±0.04	±0.056		±0.04	±0.07	mV/°C
Voltage Swing, ±15 V Supply, 2 kΩ Load	0 to +12.0	+13.5		0 to +12.0	+13.5		0 to +12.0	+13.5		V
Voltage Swing, ±3 V Supply, 2 kΩ Load	0 to +2	+2.2		0 to +2	+2.2		0 to +2	+2.2		V
Output Current	6			6			6			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0.5			0.5			0.5		Ω
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7 mV to 7 V rms, 0 dB = 1 V rms		±0.5			±0.3			±0.5		dB
Scale Factor		–3			–3			–3		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33			+0.33		% of Reading/°C
		–0.033			–0.033			–0.033		dB/°C
I_{REF} for 0 dB = 1 V rms	5	20	80	5	20	80	5	20	80	µA
I_{REF} Range	1		100	1		100	1		100	µA
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to ($+V_S$ – 2.5 V)			$-V_S$ to ($+V_S$ – 2.5 V)			$-V_S$ to ($+V_S$ – 2.5 V)			V
Input Offset Voltage		±0.8	±2		±0.5	±1		±0.8	±2	mV
Input Current		±2	±10		±2	±5		±2	±10	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5 mA, –130 µA)			(+5 mA, –130 µA)			(+5 mA, –130 µA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/µs
DENOMINATOR INPUT										
Input Range		0 to +10			0 to +10			0 to +10		V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage		±0.2	±0.5		±0.2	±0.5		±0.2	±0.5	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level	Open or +2.4 V < V_C < $+V_S$			Open or +2.4 V < V_C < $+V_S$			Open or +2.4 V < V_C < $+V_S$			
rms "OFF" Level	V_C < +0.2 V			V_C < +0.2 V			V_C < +0.2 V			
I_{OUT} of Chip Select										
CS "LOW"	10			10			10			µA
CS "HIGH"	Zero			Zero			Zero			
On Time Constant	10 µs + ((25 kΩ) × C_{AV})			10 µs + ((25 kΩ) × C_{AV})			10 µs + ((25 kΩ) × C_{AV})			
Off Time Constant	10 µs + ((25 kΩ) × C_{AV})			10 µs + ((25 kΩ) × C_{AV})			10 µs + ((25 kΩ) × C_{AV})			
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3.0		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	µA

Specifications subject to change without notice.

DC Coupled Demodulating 120 MHz Logarithmic Amplifier

AD640

FEATURES

Complete, Fully Calibrated Monolithic System
Five Stages, Each Having 10 dB Gain, 350 MHz BW
Direct Coupled Fully Differential Signal Path
Logarithmic Slope, Intercept and AC Response are Stable Over Full Military Temperature Range
Dual Polarity Current Outputs Scaled 1 mA/Decade
Voltage Slope Options (1 V/Decade, 100 mV/dB, etc.)
Low Power Operation (Typically 220 mW at ±5 V)
Low Cost Plastic Packages Also Available

APPLICATIONS

Radar, Sonar, Ultrasonic and Audio Systems
Precision Instrumentation from DC to 120 MHz
Power Measurement with Absolute Calibration
Wide Range High Accuracy Signal Compression
Alternative to Discrete and Hybrid IF Strips
Replaces Several Discrete Log Amp ICs

PRODUCT DESCRIPTION

The AD640 is a complete monolithic logarithmic amplifier. A single AD640 provides up to 50 dB of dynamic range for frequencies from dc to 120 MHz. Two AD640s in cascade can provide up to 95 dB of dynamic range at reduced bandwidth. The AD640 uses a successive detection scheme to provide an output current proportional to the logarithm of the input voltage. It is laser calibrated to close tolerances and maintains high accuracy over the full military temperature range using supply voltages from ±4.5 V to ±7.5 V.

The AD640 comprises five cascaded dc coupled amplifier/limiter stages, each having a small signal voltage gain of 10 dB and a –3 dB bandwidth of 350 MHz. Each stage has an associated full-wave detector, whose output current depends on the absolute value of its input voltage. The five outputs are summed to provide the video output (when low-pass filtered) scaled at 1 mA per decade (50 μA per dB). On chip resistors can be used to convert this output current to a voltage with several convenient slope options. A balanced signal output at +50 dB (referred to input) is provided to operate AD640s in cascade.

The logarithmic response is absolutely calibrated to within ±1 dB for dc or square wave inputs from ±0.75 mV to ±200 mV, with an intercept (logarithmic offset) at 1 mV dc. An integral X10 attenuator provides an alternative input range of ±7.5 mV to ±2 V dc. Scaling is also guaranteed for sinusoidal inputs.

This device is now available to Standard Military Drawing (DESC) number 5962-9095501MRA and 5962-9095501M2A.

PRODUCT HIGHLIGHTS

1. Absolute calibration of a wideband logarithmic amplifier is unique. The AD640 is a high accuracy measurement device, not simply a logarithmic building block.
2. Advanced design results in unprecedented stability over the full military temperature range.
3. The fully differential signal path greatly reduces the risk of instability due to inadequate power supply decoupling and shared ground connections, a serious problem with commonly used unbalanced designs.
4. Differential interfaces also ensure that the appropriate ground connection can be chosen for each signal port. They further increase versatility and simplify applications. The signal input impedance is ~500 kΩ in shunt with ~2 pF.
5. The dc coupled signal path eliminates the need for numerous interstage coupling capacitors and simplifies logarithmic conversion of subsonic signals.
6. The low input offset voltage of 50 μV (200 μV max) ensures good accuracy for low level dc inputs.
7. Thermal recovery "tails," which can obscure the response when a small signal immediately follows a high level input, have been minimized by special attention to design details.
8. The noise spectral density of 2 nV/$\sqrt{\text{Hz}}$ results in a noise floor of ~23 μV rms (–80 dBm) at a bandwidth of 100 MHz. The dynamic range using cascaded AD640s can be extended to 95 dB by the inclusion of a simple filter between the two devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD640JN	0°C to +70°C	Plastic DIP	N-20
AD640JP	0°C to +70°C	Plastic Leaded Chip Carrier	P-20A
AD640BD	–40°C to +85°C	Side Brazed Ceramic DIP	D-20
AD640BE	–40°C to +85°C	Ceramic Leadless Chip Carrier	E-20A
AD640BP	–40°C to +85°C	Plastic Leaded Chip Carrier	P-20A
AD640TD/883B 5962-9095501MRA	–55°C to +125°C	Side Brazed Ceramic DIP	D-20
AD640TE/883B 5962-9095501M2A	–55°C to +125°C	Ceramic Leadless Chip Carrier	E-20A
AD640TCHIP	–55°C to +125°C	Chip	

*For outline information see Package Information section.

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AD640–SPECIFICATIONS

DC SPECIFICATIONS (V_S = ±5 V, T_A = +25°C, unless otherwise noted)

Model		AD640J			AD640B			AD640T			
Transfer Function		$I_{OUT} = I_Y \text{ LOG } \lvert V_{IN}/V_X \rvert$ for V_{IN} = ±0.75 mV to ±200 mV dc									
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
SIGNAL INPUTS (Pins 1, 20)											
Input Resistance	Differential		500			500			500		kΩ
Input Offset Voltage	Differential		50	**500**		50	**200**		50	**200**	µV
Input Bias Current			7	25		7	25		7	25	µA
Input Bias Offset			1			1			1		µA
Common-Mode Range		–2		+0.3	–2		+0.3	–2		+0.3	V
INPUT ATTENUATOR (Pins 2, 3, 4, 5 and 19)											
Attenuation	Pin 5 to Pin 19		20			20			20		dB
Input Resistance	Pins 5 to 3/4		300			300			300		Ω
SIGNAL OUTPUT (Pins 10, 11)											
Small Signal Gain			50			50			50		dB
Peak Differential Output			±180			±180			±180		mV
Output Resistance	Either Pin to COM		75			75			75		Ω
Quiescent Output Voltage	Either Pin to COM		–90			–90			–90		mV
LOGARITHMIC OUTPUT (Pin 14)											
Voltage Compliance Range		–0.3		$+V_S$ –1	–0.3		$+V_S$ –1	–0.3		V_S –1	V
Slope Current, I_Y		**0.95**	1.00	**1.05**	**0.98**	1.00	**1.02**	**0.98**	1.00	**1.02**	mA
Intercept Voltage, V_X		**0.85**	1.00	**1.15**	**0.95**	1.00	**1.05**	**0.95**	1.00	**1.05**	mV
Logarithmic Offset (Alt. Definition of V_X)		–61.5	–60.0	–58.7	–60.5	–60.0	–59.5	–60.5	–60.0	–59.5	dBV
Intercept Voltage Using Attenuator		**8.25**	10.0	**11.75**	**9.0**	10.0	**11.0**	**9.0**	10.0	**11.0**	mV
Zero Signal Output Current			–0.2			–0.2			–0.2		mA
ITC Disabled	Pin 8 to COM		–0.27			–0.27			–0.27		mA
Maximum Output Current			2.3			2.3			2.3		mA
DC LINEARITY											
V_{IN} = ±1 mV to ±100 mV			0.35	**1.2**		0.35	**0.6**		0.35	**0.6**	dB
TOTAL ABSOLUTE DC ACCURACY											
V_{IN} = ±1 mV to ±100 mV			0.55	**2**		0.55	**0.9**		0.55	**0.9**	dB
V_{IN} = ±0.75 mV to ±200 mV			1.0	**3**		1.0	**2.0**		1.0	**2.0**	dB
Using Attenuator											
V_{IN} = ±10 mV to ±1 V			0.4	**2.5**		0.4	**1.5**		0.4	**1.5**	dB
V_{IN} = ±7.5 mV to 2 V			1.2	**3.5**		1.2	**2.5**		1.2	**2.5**	dB
POWER REQUIREMENTS											
Voltage Supply Range		**±4.5**		**±7.5**	**±4.5**		**±7.5**	**±4.5**		**±7.5**	V
SIGNAL INPUTS (Pins 1, 20)											
Input Capacitance	Either Pin to COM		2			2			2		pF
Noise Spectral Density	1 kHz to 10 MHz		2			2			2		nV/√Hz
Tangential Sensitivity	BW = 100 MHz		–72			– 72			–72		dBm
3 dB BANDWIDTH											
Each Stage			350			350			350		MHz
All Five Stages	Pins 1 & 20 to 10 & 11		145			145			145		MHz
LOGARITHMIC OUTPUTS											
Slope Current, I_Y											
f< = 1 MHz		0.96	1.0	1.04	0.98	1.0	1.02	0.98	1.0	1.02	mA
f = 30 MHz		0.88	0.94	1.00	0.91	0.94	0.97	0.91	0.94	0.97	mA
f = 60 MHz		0.82	0.90	0.98	0.86	0.90	0.94	0.86	0.90	0.94	mA
f = 90 MHz			0.88			0.88			0.88		mA
f = 120 MHz			0.85			0.85			0.85		mA
Intercept, Dual AD640s											
f< = 1 MHz		–90.6	–88.6	–86.6	–89.6	–88.6	–87.6	–89.6	–88.6	–87.6	dBm
f = 30 MHz			–87.6			–87.6			–87.6		dBm
f = 60 MHz			–86.3			–86.3			–86.3		dBm
f = 90 MHz			–83.9			–83.9			–83.9		dBm
f = 120 MHz			–80.3			–80.3			–80.3		dBm
AC LINEARITY											
–40 dBm to –2 dBm	f = 1 MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
–35 dBm to –10 dBm	f = 1 MHz		0.25	1.0		0.25	0.5		0.25	0.5	dB
–75 dBm to 0 dBm	f = 1 MHz		0.75	3.0		0.75	1.5		0.75	1.5	dB
–70 dBm to –10 dBm	f = 1 MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
–75 dBm to +15 dBm	f = 10 kHz		0.5	3.0		0.5	1.5		0.5	1.5	dB

Specifications subject to change without notice.

250 MHz Demodulating Logarithmic Amplifier

AD641

FEATURES

Logarithmic Amplifier Performance
- Usable to 250 MHz
- 44 dB Dynamic Range
- ±2.0 dB Log Conformance
- 37.5 mV/dB Voltage Output
- Stable Slope and Intercepts

2.0 nV/√Hz Input Noise Voltage
50 μV Input Offset Voltage
Low Power
- ±5 V Supply Operation
- 9 mA ($+V_S$), 35 mA ($-V_S$) Quiescent Current

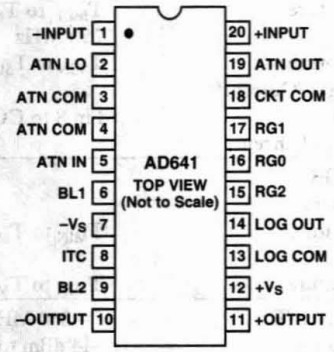
Onboard Resistors
Onboard 10X Attenuator
Dual Polarity Current Outputs
Direct Coupled Differential Signal Path

APPLICATIONS

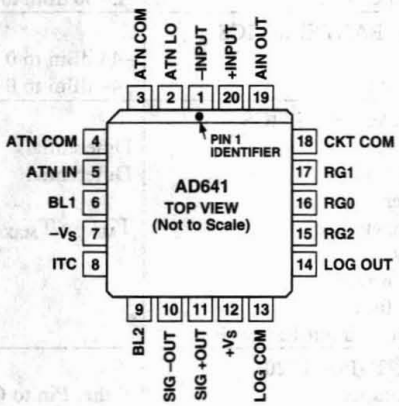
IF/RF Signal Processing
Received Signal Strength Indicator (RSSI)
High Speed Signal Compression
High Speed Spectrum Analyzer
ECM/Radar

PIN CONFIGURATIONS

20-Lead Plastic DIP (N)
20-Lead Cerdip (Q)



20-Lead PLCC (P)



PRODUCT DESCRIPTION

The AD641 is a 250 MHz, demodulating logarithmic amplifier with an accuracy of ±2.0 dB and 44 dB dynamic range. The AD641 uses a successive detection architecture to provide an output current that is logarithmically proportional to its input voltage. The output current can be converted to a voltage using one of several on-chip resistors to select the slope. A single AD641 provides up to 44 dB of dynamic range at speeds up to 250 MHz, and two cascaded AD641s together can provide 58 dB of dynamic range at speeds up to 250 MHz. The AD641 is fully stable and well characterized over either the industrial or military temperature ranges.

The AD641 is not a logarithmic building block, but rather a complete logarithmic solution for compressing and measuring wide dynamic range signals. The AD641 is comprised of five stages and each stage has a full wave rectifier, whose current depends on the absolute value of its input voltage. The output of these stages are summed together to provide the demodulated output current scaled at 1 mA per decade (50 μA/dB).

Without utilizing the 10× input attenuator, log conformance of 2.0 dB is maintained over the input range –44 dBm to 0 dBm. The attenuator offers the most flexibility without significantly impacting performance.

The 250 MHz bandwidth and temperature stability make this product ideal for high speed signal power measurement in RF/IF systems. ECM/Radar and Communication applications are routinely in the 100 MHz–180 MHz range for power measurement. The bandwidth and accuracy, as well as dynamic range, make this part ideal for high speed, wide dynamic range signals.

The AD641 is offered in industrial (–40°C to +85°C) and military (–55°C to +125°C) package temperature ranges. Industrial versions are available in plastic DIP and PLCC; MIL versions are packaged in cerdip.

ORDERING GUIDE

Model	Package Description	Package Option*
AD641AN	Plastic DIP	N-20
AD641AP	Plastic Leaded Chip Carrier	P-20A
5962-9559801MRA	Cerdip	Q-20

*For outline information see Package Information section.

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AD641–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = ±5 V; T_A = +25°C, unless otherwise noted)

Parameter	Conditions	AD641A Min	AD641A Typ	AD641A Max	AD641S Min	AD641S Typ	AD641S Max	Units
TRANSFER FUNCTION[1]			(I_{OUT} = I_Y LOG $\lvert V_{IN}/V_X \rvert$ for V_{IN} = 0.75 mV to ±200 mV dc)					
LOG AMPLIFIER PERFORMANCE								
3 dB Bandwidth			250			250		MHz
Voltage Compliance Range		–0.3		$+V_S - 1$	–0.3		$+V_S - 1$	V
Slope Current, I_Y		0.98	1.00	1.02	0.98	1.00	1.02	mA
Accuracy vs. Temperature			0.002			0.002		%/°C
Over Temperature	T_{MIN} to T_{MAX}				0.98		1.02	mA
Intercept dBm	250 MHz	–40.84	–40.43	–39.96	–40.84	–40.43	–39.96	dBm
Over Temperature	T_{MIN} to T_{MAX}, 250 MHz				–40.59		–39.47	dBm
Zero Signal Output Current[2]			–0.2			–0.2		mA
ITC Disabled	Pin 8 to COM		–0.27			–0.27		mA
Maximum Output Current.				2.3			2.3	mA
DYNAMIC RANGE								
Single Configuration			44			44		dB
Over Temperature	T_{MIN} to T_{MAX}		40			38		dB
Dual Configuration			58			58		dB
Over Temperature	T_{MIN} to T_{MAX}		52			52		dB
LOG CONFORMANCE	f = 250 MHz							
Single Configuration	–44 dBm to 0 dBm		±0.5	±2.0		±0.5	±2.0	dB
Over Temperature	S: –42 dBm to –4 dBm; A: –42 dBm to –2 dBm, T_{MIN} to T_{MAX}		±1.0	±2.5		±1.0	±2.5	dB
Dual Configuration	S: –60 dBm to –2 dBm;		±0.5	±2.0		±0.5	±2.0	dB
Over Temperature	A: –56 dBm to –4 dBm, T_{MIN} to T_{MAX}		±1.0	±2.5		±1.0	±2.5	dB
LIMITER CHARACTERISTICS								
Flatness	–44 dBm to 0 dBm @ 10.7 MHz		±1.6			±1.6		dB
Phase Variation	–44 dBm to 0 dBm @ 10.7 MHz		±2.0			±2.0		Degrees
INPUT CHARACTERISTICS								
Input Resistance	Differential		500			500		kΩ
Input Offset Voltage	Differential		50	200		50	200	µV
vs. Temperature			0.8			0.8		µV/°C
Over Temperature	T_{MIN} to T_{MAX}						300	µV
vs. Supply			2			2		µV/V
Input Bias Current			7	25		7	25	µA
Input Bias Offset			1			1		µA
Common Mode Input Range		–2		+0.3	–2		+0.3	V
SIGNAL INPUT (Pins 1, 20)								
Input Capacitance	Either Pin to COM		2			2		pF
Noise Spectral Density	1 kHz to 10 MHz		2			2		nV/√Hz
Tangential Sensitivity	BW = 100 MHz		–72			–72		dBm
INPUT ATTENUATOR (Pins 2, 3, 4, 5 & 19)								
Attenuation[3]	Pins 5 to Pin 19		20			20		dB
Input Resistance	Pins 5 to 3/4		300			300		Ω
APPLICATION RESISTORS (Pins 15, 16, 17)		0.995	1.000	1.005	0.995	1.000	1.005	kΩ
OUTPUT CHARACTERISTICS (Pins 10, 11)								
Peak Differential Output[4]			±180			±180		mV
Output Resistance	Either Pin to COM		75			75		Ω
Quiescent Output Voltage	Either Pin to COM		–90			–90		mV
POWER SUPPLY								
Voltage Supply Range		±4.5		±7.5	±4.5		±7.5	V
Quiescent Current								
$+V_S$ (Pin 12)	T_{MIN} to T_{MAX}		9	15		9	15	mA
$-V_S$ (Pin 7)	T_{MIN} to T_{MAX}		35	60		35	60	mA

NOTES

[1]Logarithms to base 10 are used throughout. The response is independent of the sign of V_{IN}.

[2]The zero-signal current is a function of temperature unless internal temperature compensation (ITC) pin is grounded.

[3]Attenuation ratio trimmed to calibrate intercept to 10 mV when in use. It has a temperature coefficient of +0.3%/°C.

[4]The fully limited signal output will appear to be a square wave; its amplitude is proportional to absolute temperature.

Specifications subject to change without notice.

10 MHz, 4-Quadrant Multiplier/Divider

AD734

FEATURES

High Accuracy
- **0.1% Typical Error**

High Speed
- **10 MHz Full-Power Bandwidth**
- **450 V/μs Slew Rate**
- **200 ns Settling to 0.1% at Full Power**

Low Distortion
- **–80 dBc from Any Input**
- **Third-Order IMD Typically –75 dBc at 10 MHz**

Low Noise
- **94 dB SNR, 10 Hz to 20 kHz**
- **70 dB SNR, 10 Hz to 10 MHz**

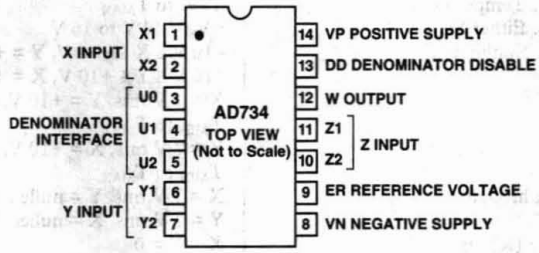
Direct Division Mode
- **2 MHz BW at Gain of 100**

APPLICATIONS

High Performance Replacement for AD534
Multiply, Divide, Square, Square Root
Modulator, Demodulator
Wideband Gain Control, RMS-DC Conversion
Voltage-Controlled Amplifiers, Oscillators, and Filters
Demodulator with 40 MHz Input Bandwidth

CONNECTION DIAGRAM

14-Pin DIP
(Q Package & N Package)



PRODUCT DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function W = XY/U. The AD734 provides a low-impedance voltage output with a full-power (20 V pk-pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of full scale. Distortion is typically less than –80 dBc and guaranteed. The low capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of –40°C to +85°C and come in a 14-pin ceramic DIP. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of –55°C to +125°C, is available in a 14-pin ceramic DIP.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD734AN	–40°C to +85°C	Plastic DIP	N-14
AD734BN	–40°C to +85°C	Plastic DIP	N-14
AD734AQ	–40°C to +85°C	Cerdip	Q-14
AD734BQ	–40°C to +85°C	Cerdip	Q-14
AD734SQ	–55°C to +125°C	Cerdip	Q-14
AD734SQ/883B	–55°C to +125°C	Cerdip	Q-14
AD734SCHIPS	–55°C to +125°C	Chip	

*For outline information see Package Information section.

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AD734—SPECIFICATIONS (T_A = +25°C, $+V_S$ = VP = +15 V, $-V_S$ = VN = −15 V, $R_L \geq 2$ kΩ)

TRANSFER FUNCTION

$$W = A_O\left\{\frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} - (Z_1 - Z_2)\right\}$$

Parameter	Conditions	A Min	A Typ	A Max	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
MULTIPLIER PERFORMANCE											
Transfer Function			W = XY/10			W = XY/10			W = XY/10		
Total Static Error[1]	−10 V ≤ X, Y ≤ 10 V		0.1	0.4		0.1	0.25		0.1	0.4	%
Over T_{MIN} to T_{MAX}				1			0.6			1.25	%
vs. Temperature	T_{MIN} to T_{MAX}		0.004			0.003			0.004		%/°C
vs. Either Supply	$\pm V_S$ = 14 V to 16 V		0.01	0.05		0.01	0.05		0.01	0.05	%/V
Peak Nonlinearity	−10 V ≤ X ≤ +10 V, Y = +10 V		0.05			0.05			0.05		%
	−10 V ≤ Y ≤ +10 V, X = +10 V		0.025			0.025			0.025		%
THD[2]	X = 7 V rms, Y = +10 V, f ≤ 5 kHz			−58			−66			−58	dBc
	T_{MIN} to T_{MAX}			−55			−63			−55	dBc
	Y = 7 V rms, X = +10 V, f ≤ 5 kHz			−60			−80			−60	dBc
	T_{MIN} to T_{MAX}			−57			−74			−57	dBc
Feedthrough	X = 7 V rms, Y = nulled, f ≤ 5 kHz		−85	−60		−85	−70		−85	−60	dBc
	Y = 7 V rms, X = nulled, f ≤ 5 kHz		−85	−66		−85	−76		−85	−66	dBc
Noise (RTO)	X = Y = 0										
Spectral Density	100 Hz to 1 MHz		1.0			1.0			1.0		$\mu V/\sqrt{Hz}$
Total Output Noise	10 Hz to 20 kHz		−94	−88		−94	−88		−94	−88	dBc
	T_{MIN} to T_{MAX}			−85			−85			−85	dBc
DIVIDER PERFORMANCE (Y = 10 V)											
Transfer Function			W = XY/U			W = XY/U			W = XY/U		
Gain Error	Y = 10 V, U = 100 mV to 10 V		1			1			1		%
X Input Clipping Level	Y ≤ 10 V		1.25 × U			1.25 × U			1.25 × U		V
U Input Scaling Error[3]				0.3			0.15			0.3	%
	T_{MIN} to T_{MAX}			0.8			0.65			1	%
(Output to 1%)	U = 1 V to 10 V Step, X = 1 V		100			100			100		ns
INPUT INTERFACES (X, Y, & Z)											
3 dB Bandwidth			40			40			40		MHz
Operating Range	Differential or Common Mode		±12.5			±12.5			±12.5		V
X Input Offset Voltage				15			5			15	mV
	T_{MIN} to T_{MAX}			25			15			25	mV
Y Input Offset Voltage				10			5			10	mV
	T_{MIN} to T_{MAX}			12			6			12	mV
Z Input Offset Voltage				20			10			20	mV
	T_{MIN} to T_{MAX}			50			50			90	mV
Z Input PSRR (Either Supply)	f ≤ 1 kHz	54	70		66	70		54	70		dB
	T_{MIN} to T_{MAX}	50			56			50			dB
CMRR	f = 5 kHz	70	85		70	85		70	85		dB
Input Bias Current (X, Y, Z Inputs)			50	300		50	150		50	300	nA
	T_{MIN} to T_{MAX}			400			300			500	nA
Input Resistance	Differential		50			50			50		kΩ
Input Capacitance	Differential		2			2			2		pF
DENOMINATOR INTERFACES (U0, U1, & U2)											
Operating Range			VN to VP-3			VN to VP-3			VN to VP-3		V
Denominator Range			1000:1			1000:1			1000:1		
Interface Resistor	U1 to U2		28			28			28		kΩ
OUTPUT AMPLIFIER (W)											
Output Voltage Swing	T_{MIN} to T_{MAX}	±12			±12			±12			V
Open-Loop Voltage Gain	X = Y = 0, Input to Z		72			72			72		dB
Dynamic Response	From X or Y Input, CL ≤ 20 pF										
3 dB Bandwidth	W ≤ 7 V rms	8	10		8	10		8	10		MHz
Slew Rate			450			450			450		V/μs
Settling Time	+20 V or −20 V Output Step										
To 1%			125			125			125		ns
To 0.1%			200			200			200		ns
Short-Circuit Current	T_{MIN} to T_{MAX}	20	50	80	20	50	80	20	50	80	mA
POWER SUPPLIES, $\pm V_S$											
Operating Supply Range		±8		±16.5	±8		±16.5	±8		±16.5	V
Quiescent Current	T_{MIN} to T_{MAX}	6	9	12	6	9	12	6	9	12	mA

NOTES
[1]Figures given are percent of full scale (e.g., 0.01% = 1 mV).
[2]dBc refers to deciBels relative to the full-scale input (carrier) level of 7 V rms.
[3]See Figure 10 for test circuit.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ANALOG DEVICES

Low Cost, Low Power, True RMS-to-DC Converter

AD736

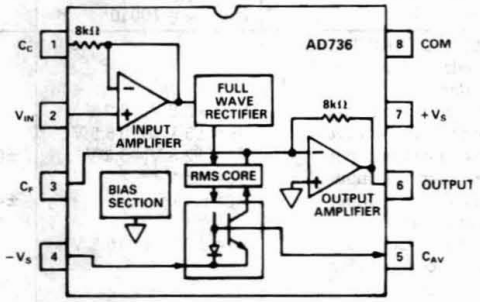
FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200 mV Full-Scale Input Range (Larger Inputs with Input Attenuator)
- High Input Impedance of 10^{12} Ω
- Low Input Bias Current: 25 pA max
- High Accuracy: ±0.3 mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8 V, –3.2 V to ±16.5 V
- Low Power: 200 μA max Supply Current
- Buffered Voltage Output
- No External Trims Needed for Specified Accuracy
- AD737—An Unbuffered Voltage Output Version with Chip Power Down Is Also Available

PIN CONFIGURATIONS

8-Pin Mini-DIP (N-8), 8-Pin SOIC (R-8), 8-Pin Cerdip (Q-8)



PRODUCT DESCRIPTION

The AD736 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.3 mV ±0.3% of reading with sine-wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD736 offers higher accuracy at equal or lower cost.

The AD736 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD736 can resolve input signal levels of 100 μV rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200 mV full-scale input level.

The AD736 has its own output buffer amplifier, thereby providing a great deal of design flexibility. Requiring only 200 μA of power supply current, the AD736 is optimized for use in portable multimeters and other battery powered applications.

The AD736 allows the choice of two signal input terminals: a high impedance (10^{12} Ω) FET input which will directly interface with high Z input attenuators and a low impedance (8 kΩ) input which allows the measurement of 300 mV input levels, while operating from the minimum power supply voltage of +2.8 V, –3.2 V. The two inputs may be used either singly or differentially.

The AD736 achieves a 1% of reading error bandwidth exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 1 mW.

The AD736 is available in four performance grades. The AD736J and AD736K grades are rated over the commercial temperature range of 0°C to +70°C. The AD736A and AD736B grades are rated over the industrial temperature range of –40°C to +85°C.

The AD736 is available in three low-cost, 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD736 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD736 to perform true rms measurement.
3. The low power consumption of 1 mW makes the AD736 suitable for many battery powered applications.
4. A high input impedance of 10^{12} Ω eliminates the need for an external buffer when interfacing with input attenuators.
5. A low impedance input is available for those applications requiring up to 300 mV rms input signal operating from low power supply voltages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD736JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD736KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD736JR	0°C to +70°C	Plastic SOIC	SO-8
AD736KR	0°C to +70°C	Plastic SOIC	SO-8
AD736AQ	–40°C to +85°C	Cerdip	Q-8
AD736BQ	–40°C to +85°C	Cerdip	Q-8
AD736JR-REEL	0°C to +70°C	Plastic SOIC	SO-8
AD736JR-REEL7	0°C to +70°C	Plastic SOIC	SO-8
AD736KR-REEL	0°C to +70°C	Plastic SOIC	SO-8
AD736KR-REEL7	0°C to +70°C	Plastic SOIC	SO-8

*For outline information see Package Information section.

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AD736—SPECIFICATIONS (@ +25°C ±5 V supplies, ac coupled with 1 kHz sine-wave input applied unless otherwise noted.)

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
TRANSFER FUNCTION			$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$		
CONVERSION ACCURACY	1 kHz Sine Wave							
Total Error, Internal Trim	ac Coupled Using C_C							
All Grades	0–200 mV rms		0.3/0.3	**0.5/0.5**		0.2/0.2	**0.3/0.3**	±mV/±% of Reading
	200 mV–1 V rms		–1.2	**±2.0**		–1.2	**±2.0**	% of Reading
dc Reversal Error, dc Coupled	@ 600 mV dc		1.3	2.5		1.3	2.5	% of Reading
Nonlinearity, 0 mV–200 mV	@ 100 mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0–200 mV rms		0.1/0.5			0.1/0.3		±mV/±% of Reading
ERROR vs. CREST FACTOR								
Crest Factor 1 to 3	C_{AV}, C_F = 100 µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100 µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, –3.2 V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8 V, –3.2 V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5 V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5 V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±3 V to ±16.5 V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, –3.2 V			300			300	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, –3.2 V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5 V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5 V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
OUTPUT CHARACTERISTICS								
Output Offset Voltage								
J&K Grades			±0.1	**±0.5**		±0.1	**±0.3**	mV
A&B Grades				**±0.5**			**±0.3**	mV
vs. Temperature			1	20		1	20	µV/°C
Output Voltage Swing								
2 kΩ Load	V_S = +2.8 V, –3.2 V	0 to +1.6	+1.7		0 to +1.6	+1.7		V
2 kΩ Load	V_S = ±5 V	0 to +3.6	+3.8		0 to +3.6	+3.8		V
2 kΩ Load	V_S = ±16.5 V	**0 to +4**	+5		**0 to +4**	+5		V
No Load	V_S = ±16.5 V	**0 to +4**	+12		**0 to +4**	+12		V
Output Current		2			2			mA
Short-Circuit Current			3			3		mA
Output Resistance	@ dc		0.2			0.2		Ω
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			37			37		kHz
V_{IN} = 200 mV rms			33			33		kHz
±3 dB Bandwidth	Sine-Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			170			170		kHz
V_{IN} = 200 mV rms			190			190		kHz
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			90			90		kHz
V_{IN} = 200 mV rms			90			90		kHz
±3 dB Bandwidth	Sine-Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			350			350		kHz
V_{IN} = 200 mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, –3.2	±5	±16.5	+2.8, –3.2	±5	±16.5	Volts
Quiescent Current	Zero Signal		160	**200**		160	**200**	µA
200 mV rms, No Load	Sine-Wave Input		230	270		230	270	µA

Specifications subject to change without notice.

Low Cost, Low Power, True RMS-to-DC Converter

AD737

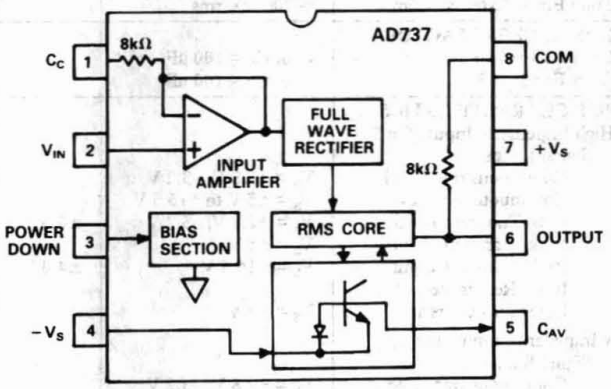
FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200 mV Full-Scale Input Range (Larger Inputs with Input Attenuator)
- Direct Interfacing with 3 1/2 Digit CMOS A/D Converters
- High Input Impedance: 10^{12} Ω
- Low Input Bias Current: 25 pA max
- High Accuracy: ±0.2 mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8 V, –3.2 V to ±16.5 V
- Low Power: 160 μA max Supply Current
- No External Trims Needed for Specified Accuracy
- AD736—A General Purpose, Buffered Voltage Output Version Also Available

PIN CONFIGURATIONS

8-Pin Mini-DIP (N-8), 8-Pin SOIC (R-8) and 8-Pin Cerdip (Q-8)



PRODUCT DESCRIPTION

The AD737 is a low power, precision, monolithic true rms-to-dc converter. It maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of 100 μV rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3. The AD737 is highly compatible with high input impedance A/D converters.

Requiring only 160 μA of power supply current, the AD737 is optimized for use in portable multimeters and other battery powered applications. This converter also provides a "power down" feature which reduces the power supply standby current to less than 30 μA.

The AD737 allows the choice of two signal input terminals: a high impedance (10^{12} Ω) FET input which will directly interface with high Z input attenuators and a low impedance (8 kΩ) input which allows the measurement of 300 mV input levels, while operating from the minimum power supply voltage of +2.8 V, –3.2 V. The two inputs may be used either singly or differentially.

The AD737 achieves a 1% of reading error bandwidth exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 0.72 mW.

PRODUCT HIGHLIGHTS

1. The AD737 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
3. The low power consumption of 0.72 mW makes the AD737 suitable for many battery powered applications.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD737JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737JR	0°C to +70°C	SOIC	R-8
AD737KR	0°C to +70°C	SOIC	R-8
AD737AQ	–40°C to +85°C	Cerdip	Q-8
AD737BQ	–40°C to +85°C	Cerdip	Q-8
AD737JR-Reel	–40°C to +85°C	SOIC	R-8
AD737KR-Reel	–40°C to +85°C	SOIC	R-8

*For outline information see Package Information section.

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AD737–SPECIFICATIONS (@ +25°C, ±5 V supplies, ac coupled with 1 kHz sine-wave input applied unless otherwise noted.)

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
TRANSFER FUNCTION	$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$		$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$					
CONVERSION ACCURACY	1 kHz Sine Wave							
Total Error, Internal Trim	ac Coupled Using C_C							
All Grades	0–200 mV rms		0.2/0.3	**0.4/0.5**		0.2/0.2	**0.2/0.3**	±mV/±% of Reading
	200 mV–1 V rms		–1.2	**±2.0**		–1.2	**±2.0**	% of Reading
T_{MIN}-T_{MAX}								
A&B Grades	@ 200 mV rms			**0.5/0.7**			**0.3/0.5**	±mV/±% of Reading
J&K Grades	@ 200 mV rms		0.007			0.007		±% of Reading/°C
DC Reversal Error, DC Coupled	@ 600 mV dc		1.3	**2.5**		1.3	**2.5**	% of Reading
Nonlinearity[2], 0–200 mV	@ 100 mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0–200 mV rms		0.1/0.2			0.1/0.2		±mV/±% of Reading
ERROR vs. CREST FACTOR								
Crest Factor 1 to 3	C_{AV}, C_F = 100 µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100 µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, –3.2 V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8 V, –3.2 V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5 V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5 V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±5 V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, –3.2 V			300			300	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, –3.2 V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5 V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5 V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous								
Nondestructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
No Load	V_S = +2.8 V, –3.2 V	0 to –1.6	–1.7		0 to –1.6	–1.7		V
No Load	V_S = ±5 V	0 to –3.3	–3.4		0 to –3.3	–3.4		V
No Load	V_S = ±16.5 V	**0 to –4**	–5		**0 to –4**	–5		V
Output Resistance	@ dc	6.4	8	9.6	6.4	8	9.6	kΩ
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			37			37		kHz
V_{IN} = 200 mV rms			33			33		kHz
±3 dB Bandwidth	Sine-Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			170			170		kHz
V_{IN} = 200 mV rms			190			190		kHz
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			90			90		kHz
V_{IN} = 200 mV rms			90			90		kHz
±3 dB Bandwidth	Sine-Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			350			350		kHz
V_{IN} = 200 mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, –3.2	±5	±16.5	+2.8, –3.2	±5	±16.5	V
Quiescent Current	Zero Signal		120	**160**		120	**160**	µA
V_{IN} = 200 mV rms, No Load	Sine-Wave Input		170	210		170	210	µA
Power Down Mode Current	Pin 3 Tied to +V_S		25	**40**		25	**40**	µA

Specifications subject to change without notice.

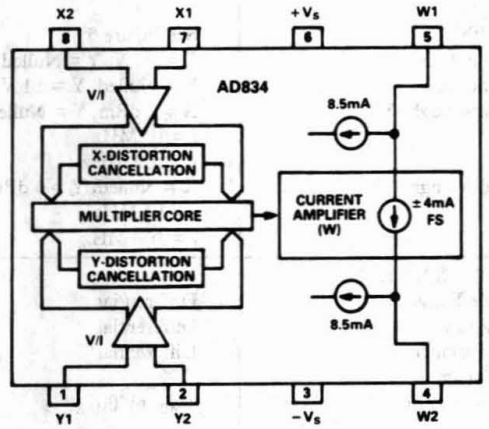
500 MHz Four-Quadrant Multiplier

AD834

FEATURES
DC to >500 MHz Operation
Differential ±1 V Full-Scale Inputs
Differential ±4 mA Full-Scale Output Current
Low Distortion (≤0.05% for 0 dBm Input)
Supply Voltages from ±4 V to ±9 V
Low Power (280 mW typical at V_S = ±5 V)

APPLICATIONS
High Speed Real Time Computation
Wideband Modulation and Gain Control
Signal Correlation and RF Power Measurement
Voltage Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having a transconductance bandwidth (R_L = 50 Ω) in excess of 500 MHz from either of the differential voltage inputs. In multiplier modes, the typical total full-scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single ended ground referenced voltage output, some form of external current to voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement) the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when X = Y = ±1 V, the differential output is ±4 mA. This absolute calibration allows the outputs of two or more AD834s to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J is specified for use over the commercial temperature range of 0°C to +70°C and is available in an 8-pin DIP package and an 8-pin plastic SOIC package. AD834A is available in cerdip for operation over the industrial temperature range of –40°C to +85°C. The AD834S/883B is specified for operation over the military temperature range of –55°C to +125°C and is available in the 8-pin cerdip package. S-Grade chips are also available.

Two application notes featuring the AD834 (AN-212 and AN-216) can now be obtained by calling 1-800-ANALOG-D. For additional applications circuits consult the AD811 data sheet.

PRODUCT HIGHLIGHTS

1. The AD834 combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited mainly by packaging and external board layout considerations. A large signal bandwidth of over 500 MHz is attainable under optimum conditions.
2. The AD834 can be used in many high speed nonlinear operations, such as square rooting, analog division, vector addition and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than –60 dB on either input) at high frequencies and low signal feedthrough (typically –65 dB up to 20 MHz).
4. The AD834 exhibits low differential phase error over the input range—typically 0.08° at 5 MHz and 0.8° at 50 MHz. The large signal transient response is free from overshoot, and has an intrinsic rise time of 500 ps, typically settling to within 1% in under 5 ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD834JN	0°C to +70°C	N-8
AD834JR	0°C to +70°C	R-8
AD834JR-REEL	0°C to +70°C	R-8
AD834AQ	–40°C to +85°C	Q-8
AD834SQ/883B	–55°C to +125°C	Q-8
AD834SCHIPS		Chips

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC) Package. For outline information see Package Information section.

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AD834—SPECIFICATIONS (T_A = +25°C and $\pm V_S$ = ±5 V, unless otherwise noted; dBm assumes 50 Ω load.)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834A, S Min	AD834A, S Typ	AD834A, S Max	Units
MULTIPLIER PERFORMANCE								
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4\,mA$			$W = \frac{XY}{(1V)^2} \times 4\,mA$		
Total Error[1] (Figure 6)	–1 V ≤ X, Y < +1 V		±0.5	**±2**		±0.5	**±2**	% FS
vs. Temperature	T_{MIN} to T_{MAX}					±1.5	**±3**	% FS
vs. Supplies[2]	±4 V to ±6 V		0.1	**0.3**		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**		±0.5	**±1**	% FS
Bandwidth[4]	See Figure 5	500			500			MHz
Feedthrough, X	X = ±1 V, Y = Nulled		0.2	**0.3**		0.2	**0.3**	% FS
Feedthrough, Y	X = Nulled, Y = ±1 V		0.1	**0.2**		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X = 0 dBm, Y = Nulled							
	f = 10 MHz		–65			–65		dB
	f = 100 MHz		–50			–50		dB
AC Feedthrough, Y[5]	X = Nulled, Y = 0 dBm							
	f = 10 MHz		–70			–70		dB
	f = 100 MHz		–50			–50		dB
INPUTS (X1, X2, Y1, Y2)								
Full-Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.1**	±1.3		**±1.1**	±1.3		V
Input Resistance	Differential		25			25		kΩ
Offset Voltage			0.5	**3**		0.5	**3**	mV
vs. Temperature	T_{MIN} to T_{MAX}		10			10		µV/°C
				4			**4**	mV
vs. Supplies[2]	±4 V to ±6 V		100	**300**		100	**300**	µV/V
Bias Current			45			45		µA
Common-Mode Rejection	f ≤ 100 kHz; 1 V p-p		70			70		dB
Nonlinearity, X	Y = 1 V; X = ±1 V		0.2	**0.5**		0.2	**0.5**	% FS
Nonlinearity, Y	X = 1 V; Y = ±1 V		0.1	**0.3**		0.1	**0.3**	% FS
Distortion, X	X = 0 dBm, Y = 1 V							
	f = 10 MHz		–60			–60		dB
	f = 100 MHz		–44			–44		dB
Distortion, Y	X = 1 V, Y = 0 dBm							
	f = 10 MHz		–65			–65		dB
	f = 100 MHz		–50			–50		dB
OUTPUTS (W1, W2)								
Zero Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X = 0, Y = 0		±20	**±60**		±20	**±60**	µA
vs. Temperature	T_{MIN} to T_{MAX}		40			40		nA/°C
							±60	µA
Scaling Current	Differential	3.96	4	4.04	3.96	4	4.04	mA
Output Compliance		4.75		9	4.75		9	V
Noise Spectral Density	f = 10 Hz to 1 MHz		16			16		nV/√Hz
	Outputs into 50 Ω Load							
POWER SUPPLIES								
Operating Range		±4		±9	±4		±9	V
Quiescent Current[6]	T_{MIN} to T_{MAX}							
$+V_S$			11	**14**		11	**14**	mA
$-V_S$			28	**35**		28	**35**	mA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0°C to +70°C)			AD834J, JR-REEL					
Military (–55°C to +125°C)						AD834S		
Industrial (–40°C to +85°C)						AD834A		
PACKAGE OPTIONS								
8-Pin SOIC (R)			AD834JR					
8-Pin Cerdip (Q)						AD834AQ		
8-Pin Plastic DIP (N)			AD834JN			AD834SQ/883B		

NOTES

[1]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full-scale output.

[2]Both supplies taken simultaneously; sinusoidal input at f ≤ 10 kHz.

[3]Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

[4]Bandwidth is guaranteed when configured in squarer mode. See Figure 5.

[5]Sine input; relative to full-scale output; zero input port nulled; represents feedthrough of the fundamental.

[6]Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

250 MHz, Voltage Output 4-Quadrant Multiplier

AD835

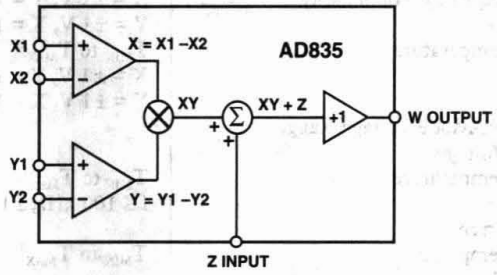
FEATURES

Simple: Basic Function is W = XY + Z
Complete: Minimal External Components Required
Very Fast: Settles to 0.1% of FS in 20 ns
DC-Coupled Voltage Output Simplifies Use
High Differential Input Impedance X, Y and Z Inputs
Low Multiplier Noise: 50 nV/$\sqrt{Hz}$

APPLICATIONS

Very Fast Multiplication, Division, Squaring
Wideband Modulation and Demodulation
Phase Detection and Measurement
Sinusoidal Frequency Doubling
Video Gain Control and Keying
Voltage Controlled Amplifiers and Filters

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

8-Pin Plastic DIP (N)
8-Pin Plastic SOIC (R)

PRODUCT DESCRIPTION

The AD835 is a complete four-quadrant voltage output analog multiplier fabricated on an advanced dielectrically isolated complementary bipolar process. It generates the linear product of its X and Y voltage inputs, with a –3 dB output bandwidth of 250 MHz (a small signal rise time of 1 ns). Full-scale (–1 V to +1 V) rise/fall times are 2.5 ns (with the standard R_L of 150 Ω) and the settling time to 0.1% under the same conditions is typically 20 ns.

Its differential multiplication inputs (X, Y) and its summing input (Z) are at high impedance. The low impedance output voltage (W) can provide up to ±2.5 V and drive loads as low as 25 Ω. Normal operation is from ±5 V supplies.

Though providing state-of-the-art speed, the AD835 is simple to use and versatile. For example, as well as permitting the addition of a signal at the output, the Z input provides the means to operate the AD835 with voltage gains up to about ×10. In this capacity, the very low product noise of this multiplier (50 nV$\sqrt{Hz}$) makes it much more useful than earlier products.

The AD835 is available in an 8-pin plastic mini-DIP package (N) and an 8-pin SOIC (R) and is specified to operate over the –40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD835 is the first monolithic 250 MHz four quadrant voltage output multiplier.
2. Minimal external components are required to apply the AD835 to a variety of signal processing applications.
3. High input impedances (100 kΩ‖2 pF) make signal source loading negligible.
4. High output current capability allows low impedance loads to be driven.
5. State of the art noise levels achieved through careful device optimization and the use of a special low noise bandgap voltage reference.
6. Designed to be easy to use and cost effective in applications which formerly required the use of hybrid or board level solutions.

ORDERING GUIDE

Model	Temperature Range	Package Options*
AD835AN	–40°C to +85°C	N-8
AD835AR	–40°C to +85°C	R-8

*N = Plastic DIP; R = Small Outline IC Plastic Package (SOIC). For outline information see Package Information section.

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AD835—SPECIFICATIONS (T_A = +25°C, V_S = ±5 V, R_L = 150 Ω, C_L ≤ 5 pF unless otherwise noted)

Model		AD835AN/AR			
TRANSFER FUNCTION		$W = \frac{(X1-X2)(Y1-Y2)}{U} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS (X, Y)					
Differential Voltage Range	V_{CM} = 0		±1		V
Differential Clipping Level		**±1.2**	±1.4		V
Low Frequency Nonlinearity	X = ±1 V, Y = 1 V		0.3	**0.5**	% FS
	Y = ±1 V, X = 1 V		0.1	**0.3**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]				
	X = ±1 V, Y = 1 V			0.7	% FS
	Y = ±1 V, X = 1 V			0.5	% FS
Common-Mode Voltage Range		–2.5		+3	V
Offset Voltage			±3	**±20**	mV
vs. Temperature	T_{MIN} to T_{MAX}[1]			±25	mV
CMRR	f ≤ 100 kHz; ±1 V p-p	**70**			dB
Bias Current			10	**20**	µA
vs. Temperature	T_{MIN} to T_{MAX}[1]			27	µA
Offset Bias Current			2		µA
Differential Resistance			100		kΩ
Single-Sided Capacitance			2		pF
Feedthrough, X	X = ±1 V, Y = 0 V			**–46**	dB
Feedthrough, Y	Y = ±1 V, X = 0 V			**–60**	dB
DYNAMIC CHARACTERISTICS					
–3 dB Small-Signal Bandwidth		150	250		MHz
–0.1 dB Gain Flatness Frequency			15		MHz
Slew Rate	W = –2.5 V to +2.5 V		1000		V/µs
Differential Gain Error, X	f = 3.58 MHz		0.3		%
Differential Phase Error, X	f = 3.58 MHz		0.2		Degrees
Differential Gain Error, Y	f = 3.58 MHz		0.1		%
Differential Phase Error, Y	f = 3.58 MHz		0.1		Degrees
Harmonic Distortion	X or Y = 10 dBm, 2nd and 3rd Harmonic				
	Fund = 10 MHz		–70		dB
	Fund = 50 MHz		–40		dB
Settling Time, X or Y	To 0.1%, W = 2 V p-p		20		ns
SUMMING INPUT (Z)					
Gain	From Z to W, f ≤ 10 MHz	0.990	0.995		
–3 dB Small-Signal Bandwidth			250		MHz
Differential Input Resistance			60		kΩ
Single Sided Capacitance			2		pF
Maximum Gain	X, Y to W, Z Shorted to W, f = 1 kHz		50		dB
Bias Current			50		µA
OUTPUT CHARACTERISTICS					
Voltage Swing		±2.2	±2.5		V
vs. Temperature	T_{MIN} to T_{MAX}[1]	±2.0			V
Voltage Noise Spectral Density	X = Y = 0, f < 10 MHz		50		nV/√Hz
Offset Voltage			±25	**±75**	mV
vs. Temperature[2]	T_{MIN} to T_{MAX}[1]			±10	mV
Short Circuit Current			75		mA
Scale Factor Error			±5	**±8**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]			±9	% FS
Linearity (Relative Error)[3]			±0.5	**±1.0**	% FS
vs. Temperature	T_{MIN} to T_{MAX}[1]			±1.25	% FS
POWER SUPPLIES					
Supply Voltage					
For Specified Performance		±4.5	±5	±5.5	V
Quiescent Supply Current			16	**25**	mA
vs. Temperature	T_{MIN} to T_{MAX}[1]			26	mA
PSRR at Output vs. Vp	+4.5 V to +5.5 V			**0.5**	%/V
PSRR at Output vs. Vn	–4.5 V to –5.5 V			**0.5**	%/V

NOTES
[1]T_{MIN} = –40°C, T_{MAX} = +85°C.
[2]Normalized to zero at +25°C.
[3]Linearity is defined as residual error after compensating for input offset, output voltage offset and scale factor errors.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

Four-Channel, Four-Quadrant Analog Multiplier

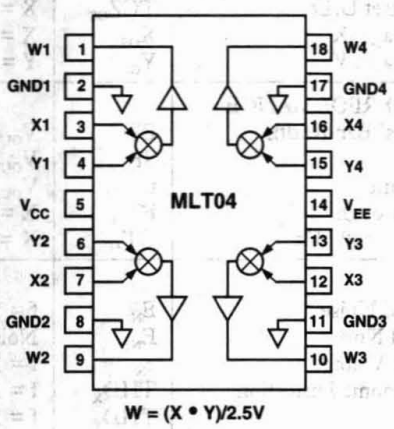
MLT04

FEATURES
- Four Independent Channels
- Voltage IN, Voltage OUT
- No External Parts Required
- 8 MHz Bandwidth
- Four-Quadrant Multiplication
- Voltage Output; W = (X × Y)/2.5 V
  - 0.2% Typical Linearity Error on X or Y Inputs
- Excellent Temperature Stability: 0.005%
- ±2.5 V Analog Input Range
- Operates from ±5 V Supplies
- Low Power Dissipation: 150 mW typ
- Spice Model Available

APPLICATIONS
- Geometry Correction in High-Resolution CRT Displays
- Waveform Modulation & Generation
- Voltage Controlled Amplifiers
- Automatic Gain Control
- Modulation and Demodulation

FUNCTIONAL BLOCK DIAGRAM

18-Lead Epoxy DIP (P Suffix)
18-Lead Wide Body SOIC (S Suffix)



GENERAL DESCRIPTION

The MLT04 is a complete, four-channel, voltage output analog multiplier packaged in an 18-pin DIP or SOIC-18. These complete multipliers are ideal for general purpose applications such as voltage controlled amplifiers, variable active filters, "zipper" noise free audio level adjustment, and automatic gain control. Other applications include cost-effective multiple-channel power calculations (I × V), polynomial correction generation, and low frequency modulation. The MLT04 multiplier is ideally suited for generating complex, high-order waveforms especially suitable for geometry correction in high-resolution CRT display systems.

Fabricated in a complementary bipolar process, the MLT04 includes four 4-quadrant multiplying cells which have been laser-trimmed for accuracy. A precision internal bandgap reference normalizes signal computation to a 0.4 scale factor. Drift over temperature is under 0.005%/°C. Spot noise voltage of 0.3 $\mu V/\sqrt{Hz}$ results in a THD + Noise performance of 0.02% (LPF = 22 kHz) for the lower distortion Y channel. The four 8 MHz channels consume a total of 150 mW of quiescent power.

The MLT04 is available in 18-pin plastic DIP, and SOIC-18 surface mount packages. All parts are offered in the extended industrial temperature range (–40°C to +85°C).

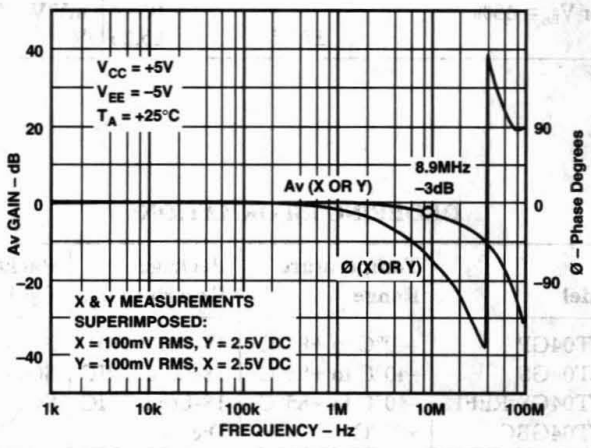


Figure 1. Gain & Phase vs. Frequency Response

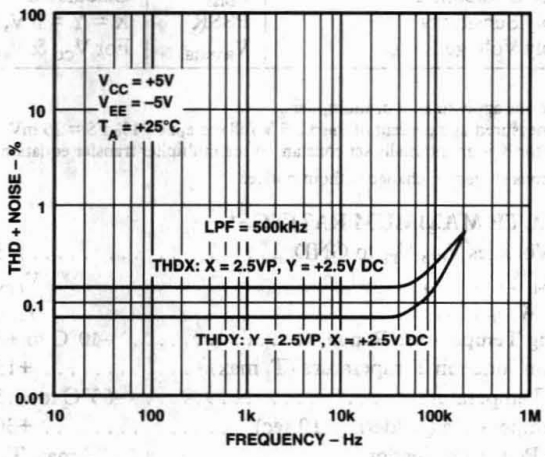


Figure 2. THD + Noise vs. Frequency

MLT04–SPECIFICATIONS (V_{CC} = +5 V, V_{EE} = –5 V, V_{IN} = ±2.5 V_P, R_L = 2 kΩ, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
MULTIPLIER PERFORMANCE[1]						
Total Error[2] X	E_X	–2.5 V < X < +2.5 V, Y = +2.5 V	–5	±2	5	% FS
Total Error[2] Y	E_Y	–2.5 V < Y < +2.5 V, X = +2.5 V	–5	±2	5	% FS
Linearity Error[2] X	LE_X	–2.5 V < X < +2.5 V, Y = +2.5 V	–1	±0.2	+1	% FS
Linearity Error[2] Y	LE_Y	–2.5 V < Y < +2.5 V, X = +2.5 V	–1	±0.2	+1	% FS
Total Error Drift	TCE_X	X = –2.5 V, Y = 2.5 V, T_A = –40°C to +85°C		0.005		%/°C
Total Error Drift	TCE_Y	Y = –2.5 V, X = 2.5 V, T_A = –40°C to +85°C		0.005		%/°C
Scale Factor[3]	K	X = ±2.5 V, Y = ±2.5 V, T_A = –40°C to +85°C	0.38	0.40	0.42	1/V
Output Offset Voltage	Z_{OS}	X = 0 V, Y = 0 V, T_A = –40°C to +85°C	–50	±10	50	mV
Output Offset Drift	TCZ_{OS}	X = 0 V, Y = 0 V, T_A = –40°C to +85°C		50		µV/°C
Offset Voltage, X	X_{OS}	X = 0 V, Y = ±2.5 V, T_A = –40°C to +85°C	–50	±10.5	50	mV
Offset Voltage, Y	Y_{OS}	Y = 0 V, X = ±2.5 V, T_A = –40°C to +85°C	–50	±10.5	50	mV
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	BW	V_{OUT} = 0.1 V rms		8		MHz
Slew Rate	SR	V_{OUT} = ±2.5 V	30	53		V/µs
Settling Time	t_S	V_{OUT} = Δ2.5 V to 1% Error Band		1		µs
AC Feedthrough	FT_{AC}	X = 0 V, Y = 1 V rms @ f = 100 kHz		–65		dB
Crosstalk @ 100 kHz	CT_{AC}	X = Y = 1 V rms Applied to Adjacent Channel		–90		dB
OUTPUTS						
Audio Band Noise	E_N	f = 10 Hz to 50 kHz		76		µV rms
Wide Band Noise	E_N	Noise BW = 1.9 MHz		380		µV rms
Spot Noise Voltage	e_N	f = 1 kHz		0.3		µV/√Hz
Total Harmonic Distortion	THD_X	f = 1 kHz, LPF = 22 kHz, Y = 2.5 V		0.1		%
	THD_Y	f = 1 kHz, LPF = 22 kHz, X = 2.5 V		0.02		%
Open Loop Output Resistance	R_{OUT}			40		Ω
Voltage Swing	V_{PK}	V_{CC} = +5 V, V_{EE} = –5 V	±3.0	±3.3		V_P
Short Circuit Current	I_{SC}			30		mA
INPUTS						
Analog Input Range	IVR	GND = 0 V	–2.5		+2.5	V
Bias Current	I_B	X = Y = 0 V		2.3	10	µA
Resistance	R_{IN}			1		MΩ
Capacitance	C_{IN}			3		pF
SQUARE PERFORMANCE						
Total Square Error	E_{SQ}	X = Y = 1		5		% FS
POWER SUPPLIES						
Positive Current	I_{CC}	V_{CC} = 5.25 V, V_{EE} = –5.25 V		15	20	mA
Negative Current	I_{EE}	V_{CC} = 5.25 V, V_{EE} = –5.25 V		15	20	mA
Power Dissipation	P_{DISS}	Calculated = 5 V × I_{CC} + 5 V × I_{EE}		150	200	mW
Supply Sensitivity	PSSR	X = Y = 0 V, V_{CC} = Δ5% or V_{EE} = Δ5%			10	mV/V
Supply Voltage Range	V_{RANGE}	For V_{CC} & V_{EE}	±4.75		±5.25	V

NOTES
[1]Specifications apply to all four multipliers.
[2]Error is measured as a percent of the ±2.5 V full scale, i.e., 1% FS = 25 mV.
[3]Scale Factor K is an internally set constant in the multiplier transfer equation W = K × X × Y.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages V_{CC}, V_{EE} to GND ..... ±7 V
Inputs X_I, Y_I ..... V_{CC}, V_{EE}
Outputs W_I ..... V_{CC}, V_{EE}
Operating Temperature Range ..... –40°C to +85°C
Maximum Junction Temperature (T_J max) ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... ($T_J$max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}
PDIP-18 (N-18) ..... 74°C/W
SOIC-18 (SOL-18) ..... 89°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification are not implied.

ORDERING INFORMATION[1]

Model	Temperature Range	Package Description	Package Option[2]
MLT04GP	–40°C to +85°C	18-Pin P-DIP	N-18
MLT04GS	–40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GS-REEL	–40°C to +85°C	18-Lead SOIC	SOL-18
MLT04GBC	+25°C	Die	

NOTES
[1]For die specifications contact your local Analog sales office. The MLT04 contains 211 transistors.
[2]For outline information see Package Information section.

Analog Switches & Multiplexers
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Analog Switches & Multiplexers–Selection Guides

Analog Multiplexers

Model	Over Supply Range Volts	R_{ON} Ohms	I_S Off ±nA	t_{ON} +25°C µs	Input Latch	# Pins	Page No.	Comments	Fax-code
$V_{SS} = V_{DD} = \pm 15$ V									
16-Channel Single Ended									
ADG406	0.3	100	0.5	0.12	No	28	4–9		1499
ADG426	0.3	100	0.5	0.12	Yes	28	4–9	With Latch & Enable Reset	1499
8-Channel Differential									
ADG407	0.3	100	0.5	0.12	No	28	4–9		1499
8-Channel Single Ended									
ADG408	2	40	0.5	0.09	No	16	4–11		1501
ADG428	2	40	0.5	0.09	Yes	18	4–19	With Latch & Enable Reset	1508
ADG438F	40	300	0.5	0.25	No	16	4–25	With Latch & Enable Reset	1855
ADG508F	20	300	1	0.25	No	16	4–31		1845
ADG528F	20	300	1	0.25	Yes	18	4–31	With Chip Address/Control	1845
ADG608	2	30	0.05	0.075	No	16	4–35		1912
ADG508A	2	500	1	0.25	No	16/20	4–29		1518
4-Channel Differential									
ADG409	2	40	0.5	0.12	No	16	4–11		1501
ADG429	2	40	0.5	0.09	Yes	18	4–19	With Latch & Enable Reset	1508
ADG439F	40	300	0.5	0.25	No	16	4–25		1855
ADG509F	20	300	1	0.25	No	16	4–31		1845
ADG509A	2	500	1	0.25	No	16/20	4–29		1518
$V_{SS} = V_{DD} = \pm 12$ V									
AD9300		NA	NA	0.050	No	16	4–5	Video 4 Channel	1459

Single Supply Multiplexers

Model	Over Supply Range Volts	R_{ON} Ohms	I_S Off ±nA	t_{ON} +25°C µs	Input Latch	# Pins	Page No.	Comments	Fax-code
8-Channel Single Ended									
ADG608	2	40	0.05	0.1	No	16	4–35	+5 V	1912
ADG608	2	90	0.05	0.17	No	16	4–35	+3 V	1912
4-Channel Differential									
ADG609	2	40	0.05	0.1	No	16	4–35	+5 V	1912
ADG609	2	90	0.05	0.17	No	16	4–35	+3 V	1912

CMOS Switches

Model	Type	Rail for Specs Volts	I_{DD} max mA	I_{SS} max mA	R_{ON} max Ohms	I_S Off nA	t_{ON} µs	t_{OFF} µs	# Pins	Page No.	Comments	Fax-code
ADG201A/ADG202A	4 SPST	±15	2	0.2	90	2	0.3	0.25	16	*		1492
ADG201HS	4 SPST	±15	6	2	50	1	0.075	0.075	16	*		1493
ADG211A/ADG212A	4 SPST	±15, +5	1	0.2	115	5	0.6	0.45	16	*		1495
ADG221/ADG222	4 SPST	±15	1.5	0.2	90	2	0.3	0.25	16	*	With Input Latch	1497

J-FET "Clickless" Switches

Model	Type	Rail for Specs Volts	I_{DD} max mA	I_{SS} max mA	R_{ON} max Ohms	I_S Off nA	t_{ON} µs	t_{OFF} µs	# Pins	Page No.	Comments	Fax-code
SSM2402/SSM2412	2 SPST	±12	6	7.	85		10/3.5 ms	4/1.5 ms	16	16–33	Off Isolation 120 dB	1801
SSM2404	4 SPST	±12	0.6	0.9	28			30 ms	16	16–33	THD+N = 0.0008%	1802

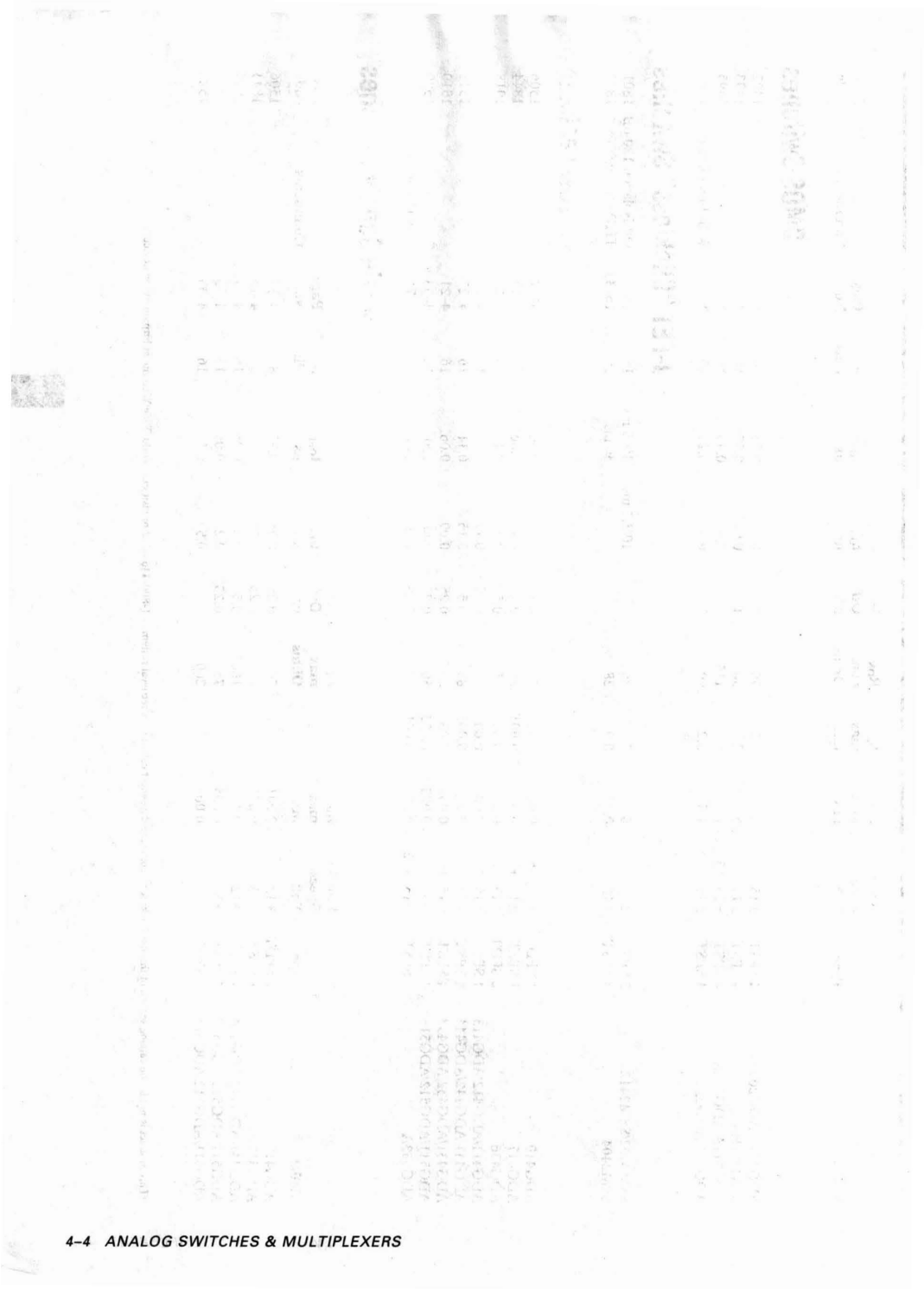
Low Leakage

Model	Type	Rail for Specs Volts	I_{DD} max mA	I_{SS} max mA	R_{ON} max Ohms	I_S Off nA	t_{ON} µs	t_{OFF} µs	# Pins	Page No.	Comments	Fax-code
ADG419	1 SPDT	±15, +5	0.001	0.001	25	0.1	0.1	0.06	8	4–17		1506
ADG417	1 SPST	±15, +5	0.001	0.001	25	0.1	0.1	0.06	8	4–15		1844
ADG436	2 SPDT	±15	0.25	0.05	15	0.5	0.11	0.1	16	4–23		1918
ADG411/ADG412/ADG413	4 SPST	±15, +5	0.005	0.00	35	0.25	0.11	0.1	16	4–13		1513
ADG441/ADG442/ADG444	4 SPST	±15	0.1	0.005	85	0.5	0.15	0.11	16	4–27		1513
ADG431/ADG432/ADG433	4 SPST	±15, +5	0.03	0.03	24	0.25	0.09	0.06	16	4–21		1510
ADG511/ADG512/ADG513	4 SPST	±5	0.005	0.005	50	0.25	200	120	16	4–33		1520
ADG333A	4 SPST	±15, +12	0.25	0.001	45	0.25	175	145	20	4–7	Low Distortion	1973

Single Supply Switches

Model	Type	Rail for Specs Volts	I_{DD} max mA	R_{ON} max Ohms	I_S Off nA	t_{ON} µs	t_{OFF} µs	# Pins	Page No.	Comments	Fax-code
ADG419	1 SPDT	+12	0.001	70	0.25	0.25	0.25	8	4–17		1506
ADG417	1 SPST	+12	0.001	70	0.25	0.150	0.085	8	4–15		1844
ADG441/ADG442/ADG444	4 SPST	+12	0.1	160	0.5	0.3	0.06	16	4–27		1513
ADG511/ADG512/ADG513	4 SPST	+5	0.005	75	0.25	0.2	0.05	16	4–33		1520
ADG511/ADG512/ADG513	4 SPST	+3	0.005	200		0.5	0.1	16	4–33		1520

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.



4 × 1 Wideband Video Multiplexer

AD9300

FEATURES

34 MHz Full Power Bandwidth
±0.1 dB Gain Flatness to 8 MHz
72 dB Crosstalk Rejection @ 10 MHz
0.03°/0.01% Differential Phase/Gain
Cascadable for Switch Matrices
MIL-STD-883 Compliant Versions Available

APPLICATIONS

Video Routing
Medical Imaging
Electro-Optics
ECM Systems
Radar Systems
Data Acquisition

GENERAL DESCRIPTION

The AD9300 is a monolithic high-speed video signal multiplexer useable in a wide variety of applications.

Its four channels of video input signals can be randomly switched at megahertz rates to the single output. In addition, multiple devices can be configured in either parallel or cascade arrangements to form switch matrices. This flexibility in using the AD9300 is possible because the output of the device is in a high-impedance state when the chip is not enabled; when the chip is enabled, the unit acts as a buffer with a high input impedance and low output impedance.

An advanced bipolar process provides fast, wideband switching capabilities while maintaining crosstalk rejection of 72 dB at 10 MHz. Full power bandwidth is a minimum 27 MHz. The device can be operated from ±10 V to ±15 V power supplies.

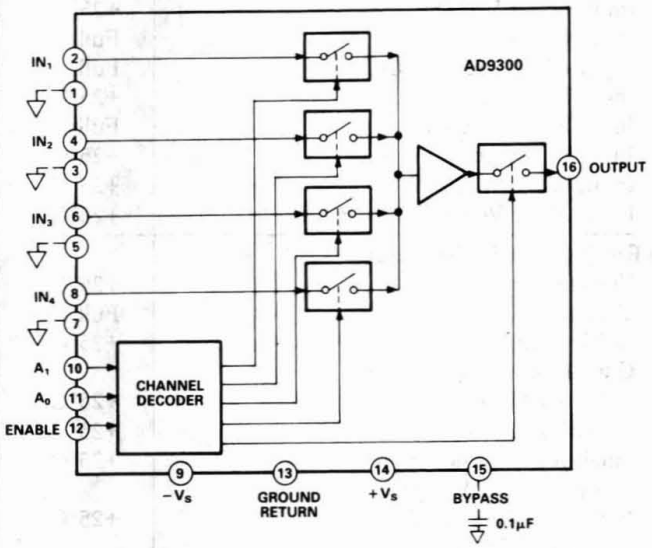
The AD9300K is available in a 16-pin ceramic DIP and a 20-pin PLCC and is designed to operate over the commercial temperature range of 0°C to +70°C. The AD9300TQ is a hermetic 16-pin ceramic DIP for military temperature range (–55°C to +125°C) applications. This part is also available processed to MIL-STD-883. The AD9300 is available in a 20-pin LCC as the model AD9300TE, which operates over a temperature range of –55°C to +125°C.

ORDERING GUIDE

Device	Temperature Range	Description	Package Option[1]
AD9300KQ	0°C to +70°C	16-Pin Cerdip, Commercial	Q-16
AD9300TE/883B[2]	–55°C to +125°C	20-Pin LCC, Military Temperature	E-20A
AD9300TQ/883B[2]	–55°C to +125°C	16-Pin Cerdip, Military Temperature	Q-16
AD9300KP	0°C to +70°C	20-Pin PLCC, Commercial	P-20A

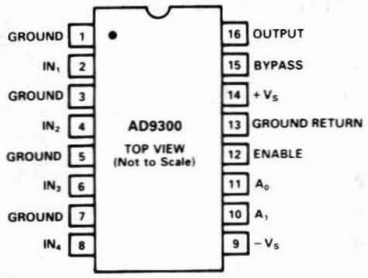
NOTES
[1]E = Ceramic Leadless Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.

FUNCTIONAL BLOCK DIAGRAM

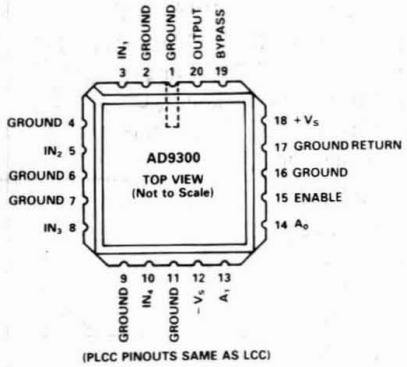


PIN DESIGNATIONS

DIP



LCC and PLCC



(PLCC PINOUTS SAME AS LCC)

AD9300–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 12$ V $\pm$ 5%; C_L = 10 pF; R_L = 2 kΩ, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9300KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Input Offset Voltage	+25°C	I		3	10	mV
Input Offset Voltage	Full	VI			14	mV
Input Offset Voltage Drift	Full	V		75		µV/°C
Input Bias Current	+25°C	I		15	37	µA
Input Bias Current	Full	VI			55	µA
Input Resistance	+25°C	V		3.0		MΩ
Input Capacitance	+25°C	V		2		pF
Input Noise Voltage (dc to 8 MHz)	+25°C	V		16		µV rms
TRANSFER CHARACTERISTICS						
Voltage Gain	+25°C	I	0.990	0.994		V/V
Voltage Gain	Full	VI	0.985			V/V
DC Linearity	+25°C	V		0.01		%
Gain Tolerance (V_{IN} = ±1 V)						
dc to 5 MHz	+25°C	I		0.05	0.1	dB
5 MHz to 8 MHz	+25°C	I		0.1	0.3	dB
Small-Signal Bandwidth (V_{IN} = 100 mV p-p)	+25°C	V		350		MHz
Full Power Bandwidth (V_{IN} = 2 V p-p)	+25°C	I	27	34		MHz
Output Swing	Full	VI	±2			V
Output Current (Sinking @ = 25°C)	+25°C	V		5		mA
Output Resistance	+25°C	IV, V		9	15	Ω
DYNAMIC CHARACTERISTICS						
Slew Rate	+25°C	I	170	215		V/µs
Settling Time (to 0.1% on ±2 V Output)	+25°C	IV		70	100	ns
Overshoot						
To T-Step	+25°C	V		<0.1		%
To Pulse	+25°C	V		<10		%
Differential Phase	+25°C	IV		0.03	0.1	°
Differential Gain	+25°C	IV		0.01	0.1	%
Crosstalk Rejection						
Three Channels	+25°C	IV	68	72		dB
One Channel	+25°C	IV	70	76		dB
SWITCHING CHARACTERISTICS						
A_X Input to Channel HIGH Time (t_{HIGH})	+25°C	I		40	50	ns
A_X Input to Channel LOW Time (t_{LOW})	+25°C	I		35	45	ns
Enable to Channel ON Time (t_{ON})	+25°C	I		35	45	ns
Enable to Channel OFF Time (t_{OFF})	+25°C	I		35	45	ns
Switching Transient	+25°C	V		60		mV
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	2			V
Logic "0" Voltage	Full	VI			0.8	V
Logic "1" Current	Full	VI			5	µA
Logic "0" Current	Full	VI			1	µA
POWER SUPPLY						
Positive Supply Current (+12 V)	Full	VI		13	16	mA
Negative Supply Current (–12 V)	Full	VI		12.5	16	mA
Power Dissipation (±12 V)	+25°C	V		306		mW

Specifications subject to change without notice.

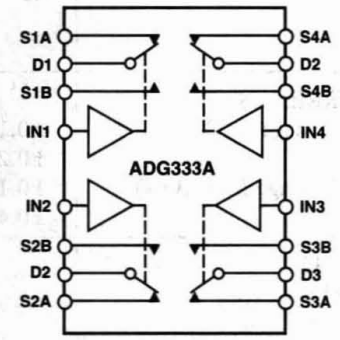
Quad SPDT Switch

ADG333A

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (45 Ω max)
- Low ΔR_{ON} (5 Ω max)
- Low R_{ON} Match (4 Ω max)
- Low Power Dissipation
- Fast Switching Times
  - t_{ON} < 175 ns
  - t_{OFF} < 145 ns
- Low Leakage Currents (5 nA max)
- Low Charge Injection (10 pC max)
- Break-Before-Make Switching Action

APPLICATIONS
- Audio and Video Switching
- Battery Powered Systems
- Test Equipment
- Communication Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

4

GENERAL DESCRIPTION

The ADG333A is a monolithic CMOS device comprising four independently selectable SPDT switches. It is designed on an LC^2MOS process which provides low power dissipation yet achieves a high switching speed and a low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the part ideally suited for portable, battery powered instruments.

When they are ON, each switch conducts equally well in both directions and has an input signal range which extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG333A is fabricated on an enhanced LC^2MOS process, giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG333A can be operated from a single rail power supply. The part is fully specified with a single +12 V supply.

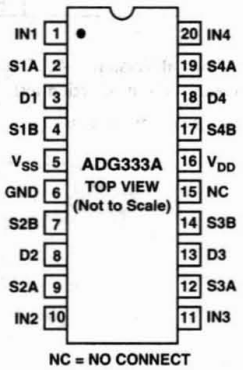
ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG333ABN	–40°C to +85°C	N-20
ADG333ABR	–40°C to +85°C	R-20
ADG333ABRS	–40°C to +85°C	RS-20

*N = Plastic DIP, R = Small Outline IC (SOIC). RS = Shrink Small Outline Package (SSOP). For outline information see Package Information section.

PIN CONFIGURATION

DIP/SOIC/SSOP



NC = NO CONNECT

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ADG333A–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	–40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	20		Ω typ	V_D = ±10 V, I_S = –1 mA
	45	45	Ω max	
ΔR_{ON}		5	Ω max	V_D = ±5 V, I_S = –10 mA
R_{ON} Match		4	Ω max	V_D = ±10 V, I_S = –10 mA
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V
	±0.25	±3	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		nA typ	V_S = V_D = ±15.5 V
	±0.4	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		±0.005	μA typ	V_{IN} = 0 V or V_{DD}
		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	90		ns typ	R_L = 300 Ω, C_L = 35 pF;
		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	80		ns typ	R_L = 300 Ω, C_L = 35 pF;
		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns min	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 5
Charge Injection	2		pC typ	V_D = 0 V, R_D = 0 Ω, C_L = 10 nF;
	10		pC max	V_{DD} = +15 V, V_{SS} = –15 V; Test Circuit 6
OFF Isolation	72		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz; V_S = 2.3 V rms, Test Circuit 7
Channel-to-Channel Crosstalk	85		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz; V_S = 2.3 V rms, Test Circuit 8
C_S (OFF)	5		pF typ	
C_D, C_S (ON)	20		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05		mA typ	Digital Inputs = 0 V or 5 V
	0.25	0.35	mA max	
I_{SS}	0.01		μA typ	
	1	5	μA max	
V_{DD}/V_{SS}		±3/±20	V min/V max	$\|V_{DD}\|$ = $\|V_{SS}\|$

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

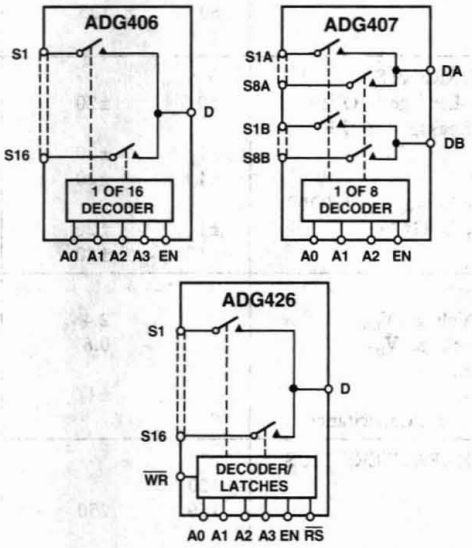
LC²MOS 8-/16-Channel High Performance Analog Multiplexers

ADG406/ADG407/ADG426

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (80 Ω max)
- Low Power
- Fast Switching
  - t_{ON} < 160 ns
  - t_{OFF} < 150 ns
- Break Before Make Switching Action
- Plug-In Upgrade for DG506A/ADG506A, DG507A/ADG507A, DG526/ADG526A
- ADG406/ADG407 are Plug-In Replacements for DG406/DG407

APPLICATIONS
- Audio and Video Routing
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems
- Avionics

FUNCTIONAL BLOCK DIAGRAMS



4

GENERAL DESCRIPTION

The ADG406, ADG407 and ADG426 are monolithic CMOS analog multiplexers. The ADG406 and ADG426 switch one of sixteen inputs to a common output as determined by the 4-bit binary address lines A0, A1, A2 and A3. The ADG426 has on-chip address and control latches that facilitate microprocessor interfacing. The ADG407 switches one of eight differential inputs to a common differential output as determined by the 3-bit binary address lines A0, A1 and A2. An EN input on all devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG406/ADG407/ADG426 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. These features make the parts suitable for high speed data acquisition systems and audio signal switching. Low power dissipation makes the parts suitable for battery powered systems. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG406/ADG407/ADG426 are fabricated on an enhanced LC²MOS process giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG406/ADG407/ADG426 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG406BN	–40°C to +85°C	N-28
ADG406BP	–40°C to +85°C	P-28A
ADG407BN	–40°C to +85°C	N-28
ADG407BP	–40°C to +85°C	P-28A
ADG426BN	–40°C to +85°C	N-28
ADG426BRS	–40°C to +85°C	RS-28

*N = Plastic DIP, P = Plastic Leaded Chip Carrier (PLCC), RS = Shrink Small Outline Package (SSOP). For outline information see Package Information section.

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ADG406/ADG407/ADG426–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	50		50		Ω typ	V_D = ±10 V, I_S = –1 mA
	80	125	80	125	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
R_{ON} Match	4		4		Ω typ	V_D = 0 V, I_S = –1 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.5	±20	±0.5	±50	nA max	V_D = ±10 V, V_S = ∓10 V, Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V, V_S = ∓10 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 3
ADG407	±1	±20	±1	±100	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 4
ADG407	±1	±20	±1	±100	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	120		120		ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	250	150	250	ns max	V_1 = ±10 V, V_2 = ∓10 V;
						Test Circuit 5
Break Before Make Delay, t_{OPEN}	10	10	10	10	ns min	R_L = 300 Ω, C_L = 35 pF;
						V_S = +5 V, Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	120	175	120	175	ns typ	R_L = 300 Ω, C_L = 35 pF;
	160	225	160	225	ns max	V_S = +5 V, Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	110	130	110	130	ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	180	150	180	ns max	V_S = +5 V, Test Circuit 7
ADG426 Only						
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	8		8		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF;
						Test Circuit 10
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, f = 100 kHz;
						V_{EN} = 0 V, Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz, Test Circuit 12
C_S (OFF)	5		5		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG406, ADG426	50		50		pF typ	
ADG407	25		25		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG406, ADG426	60		60		pF typ	
ADG407	40		40		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}		1		1	µA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	µA max	
I_{SS}		1		1	µA typ	
		5		5	µA max	
I_{DD}	100		100		µA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	µA max	
I_{SS}		1		1	µA typ	
		5		5	µA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

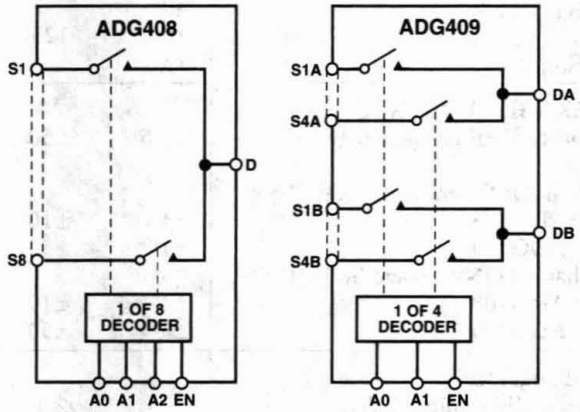
LC²MOS 4/8 Channel High Performance Analog Multiplexers

ADG408/ADG409

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (100 Ω max)
- Low Power (I_{SUPPLY} < 75 μA)
- Fast Switching
- Break-Before-Make Switching Action
- Plug-in Replacement for DG408/DG409

APPLICATIONS
- Audio and Video Routing
- Automatic Test Equipment
- Data Acquisition Systems
- Battery Powered Systems
- Sample and Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG408 and ADG409 are monolithic CMOS analog multiplexers comprising 8 single channels and four differential channels respectively. The ADG408 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG409 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG408/ADG409 are designed on an enhanced LC²MOS process which provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG408/ADG409 are improved replacements for the DG408/DG409 Analog Multiplexers.

PRODUCT HIGHLIGHTS

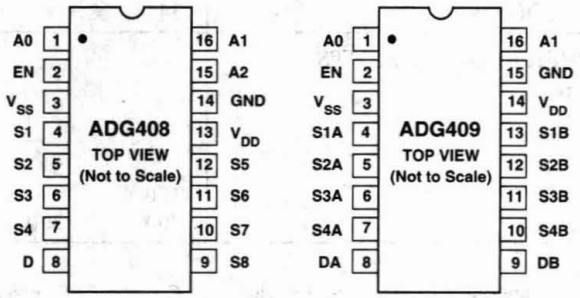
1. Extended Signal Range
   The ADG408/ADG409 are fabricated on an enhanced LC²MOS process giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG408/ADG409 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

ORDERING INFORMATION

Model[1]	Temperature Range	Package Option[2]
ADG408BN	–40°C to +85°C	N-16
ADG408BR	–40°C to +85°C	R-16A
ADG408TQ	–55°C to +125°C	Q-16
ADG409BN	–40°C to +85°C	N-16
ADG409BR	–40°C to +85°C	R-16A
ADG409TQ	–55°C to +125°C	Q-16

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATIONS (DIP/SOIC)



ADG408/ADG409–SPECIFICATIONS

DUAL SUPPLY[1] (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = ±10 V, I_S = –10 mA
	100	125	100	125	Ω max	
ΔR_{ON}	15		15		Ω max	V_D = +10 V, –10 V
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.5	±50	±0.5	±50	nA max	V_D = ±10 V, V_S = ∓10 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V; V_S = ∓10 V;
ADG408	±1	±100	±1	±100	nA max	Test Circuit 3
ADG409	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG408	±1	±100	±1	±100	nA max	Test Circuit 4
ADG409	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±10		±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$		120		120	ns typ	R_L = 300 Ω, C_L = 35 pF;
		250		250	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 5
t_{OPEN}	10	10	10	10	ns min	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 6
t_{ON} (EN)	85	125	85	125	ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	225	150	225	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN)		65		65	ns typ	R_L = 300 Ω, C_L = 35 pF;
		150		150	ns max	V_S = +5 V; Test Circuit 7
Charge Injection	20		20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 8
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, f = 100 kHz; V_{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 10
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						
I_{DD}		1		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	μA max	
I_{SS}		1		1	μA typ	
		5		5	μA max	
I_{DD}	100		100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	μA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

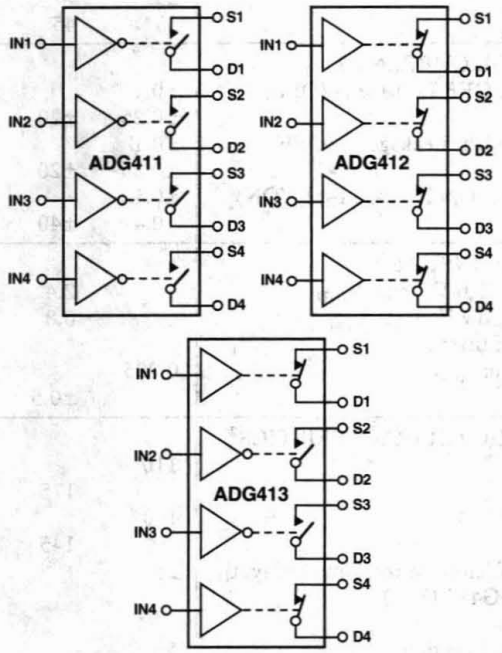
DI LC²MOS
Precision Quad SPST Switches

ADG411/ADG412/ADG413

FEATURES
- 44 V Supply Maximum Ratings
- ±15 V Analog Signal Range
- Low On Resistance (<35 Ω)
- Ultralow Power Dissipation (35 μW)
- Fast Switching Times
  - t_{ON} <175 ns
  - t_{OFF} <145 ns
- Latch-Up Proof
- TTL/CMOS Compatible
- Plug-In Replacement for DG411/DG412/DG413

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG411, ADG412 and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG411, ADG412 and ADG413 contain four independent SPST switches. The ADG411 and ADG412 differ only in that the digital control logic is inverted. The ADG411 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG412. The ADG413 has two switches with digital control logic similar to that of the ADG411 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG411, ADG412 and ADG413 are fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range which extends fully to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG411BN	–40°C to +85°C	N-16
ADG411BR	–40°C to +85°C	R-16A
ADG411TQ	–55°C to +125°C	Q-16
ADG412BN	–40°C to +85°C	N-16
ADG412BR	–40°C to +85°C	R-16A
ADG412TQ	–55°C to +125°C	Q-16
ADG413BN	–40°C to +85°C	N-16
ADG413BR	–40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ADG411/ADG412/ADG413–SPECIFICATIONS[1]

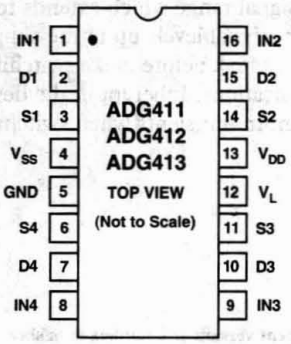
Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	25		25		Ω typ	V_D = ±8.5 V, I_S = –10 mA;
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±20	±0.25	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = ±15.5 V;
	±0.4	±40	±0.4	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	110		110		ns typ	R_L = 300 Ω, C_L = 35 pF;
		175		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		145		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_L	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

PIN CONFIGURATION (DIP/SOIC)



LC²MOS Precision Mini-DIP Analog Switch

ADG417

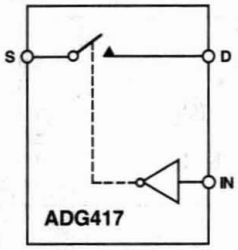
FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (<35 Ω)
- Ultralow Power Dissipation (<35 μW)
- Fast Switching Times
  - t_{ON} (145 ns max)
  - t_{OFF} (100 ns max)
- Break-Before-Make Switching Action
- Latch-Up Proof
- Plug-In Replacement for DG417

APPLICATIONS

- Precision Test Equipment
- Precision Instrumentation
- Battery Powered Systems
- Sample Hold Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCH SHOWN FOR A LOGIC "1" INPUT

4

GENERAL DESCRIPTION

The ADG417 is a monolithic CMOS SPST switch. This switch is designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents. Trench isolation gives all the benefits of dielectric isolation and ensures no latch-up even under extreme overvoltage conditions.

The on resistance profile of the ADG417 is very flat over the full analog input range ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG417 switch, which is turned ON with a logic low on the control input, conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG417 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital input.

PIN CONFIGURATION

DIP/SOIC

NC = NO CONNECT

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG417 is fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch-Up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG417 can be operated from a single rail power supply. The part is fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

Table I. Truth Table

Logic	Switch Condition
0	ON
1	OFF

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG417BN	–40°C to +85°C	N-8
ADG417BR	–40°C to +85°C	SO-8

*N = Plastic DIP, SO = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

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ADG417–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	25		25		Ω typ	V_D = ±12.5 V, I_S = –10 mA
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_S = V_D = ±15.5 V;
	±0.4	±5	±0.4	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF;
	145	200	145	200	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF;
	100	150	100	150	ns max	V_S = ±10 V; Test Circuit 4
Charge Injection	7		7		pC typ	V_S = 0 V, R_L = 0 Ω, C_L = 10 nF; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 6
C_S (OFF)	6		6		pF typ	
C_D (OFF)	6		6		pF typ	
C_D, C_S (ON)	55		55		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}	0.0001		0.0001		µA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	2.5	1	2.5	µA max	
I_L	0.0001		0.0001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

TRENCH ISOLATION

In the ADG417, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of the CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

Trench isolation also leads to lower leakage currents. The ADG417 has a leakage current of 0.25 nA as compared with a leakage current of several nanoamperes in non-trench isolated switches.

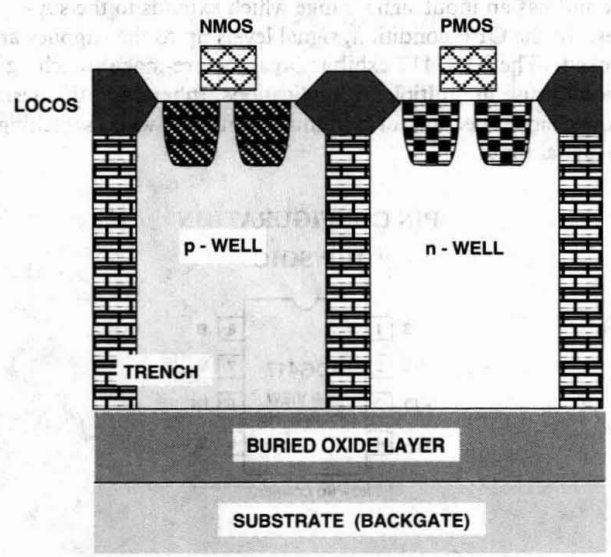


Figure 1. Trench Isolation

LC²MOS Precision Mini-DIP Analog Switch

ADG419

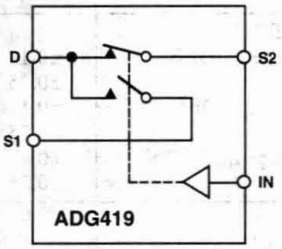
FEATURES

44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (< 35 Ω)
Ultralow Power Dissipation (< 35 μW)
Fast Transition Time (145 ns max)
Break-Before-Make Switching Action
Latch-Up Proof
Plug-In Replacement for DG419

APPLICATIONS

Precision Test Equipment
Precision Instrumentation
Battery Powered Systems
Sample Hold Systems

FUNCTIONAL BLOCK DIAGRAM



SWITCH SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG419 is a monolithic CMOS SPDT switch. This switch is designed on an enhanced LC²MOS process which provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

The on resistance profile of the ADG419 is very flat over the full analog input range ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

Each switch of the ADG419 conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG419 exhibits break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG419 is fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range that extends to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch Up
   A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG419 can be operated from a single rail power supply. The part is fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

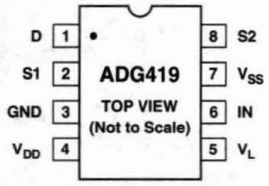
ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG419BN	–40°C to +85°C	N-8
ADG419BR	–40°C to +85°C	SO-8
ADG419TQ	–55°C to +125°C	Q-8

*N = Plastic DIP, Q = Cerdip, SO = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

PIN CONFIGURATION

DIP/SOIC



ADG419–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	25		25		Ω typ	V_D = ±12.5 V, I_S = –10 mA
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±5	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.4		±0.4		nA typ	V_S = V_D = ±15.5 V;
	±0.75	±5	±0.75	±30	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.005		±0.005	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	145	200	145	200	ns max	R_L = 300 Ω, C_L = 35 pF; V_{S1} = ±10 V, V_{S2} = ∓10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D	30		30		ns typ	R_L = 300 Ω, C_L = 35 pF;
	5		5		ns min	V_{S1} = V_{S2} = ±10 V; Test Circuit 5
OFF Isolation	80		80		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	70		70		dB typ	R_L = 50 Ω, f = 1 MHz; Test Circuit 7
C_S (OFF)	6		6		pF typ	f = 1 MHz
C_D, C_S (ON)	55		55		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}	0.0001		0.0001		µA typ	V_{IN} = 0 V or 5 V
	1	2.5	1	2.5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	2.5	1	2.5	µA max	
I_L	0.0001		0.0001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

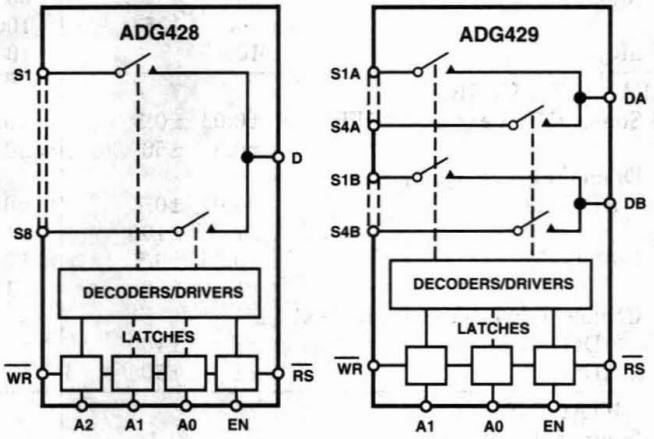
LC²MOS Latchable 4/8 Channel High Performance Analog Multiplexers

ADG428/ADG429

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (60 Ω typ)
- Low Power Consumption (1.6 mW max)
- Low Charge Injection (<4 pC typ)
- Fast Switching
- Break Before make Switching Action
- Plug-In Replacement for DG428/DG429

APPLICATIONS
- Automatic Test Equipment
- Data Acquisition Systems
- Communication Systems
- Avionics and Military Systems
- Microprocessor Controlled Analog Systems
- Medical Instrumentation

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG428 and ADG429 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels respectively. On-chip address and control latches facilitate microprocessor interfacing. The ADG428 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG429 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF. All the control inputs, address and enable inputs are TTL compatible over the full specified operating temperature range. This makes the part suitable for bus-controlled systems such as data acquisition systems, process controls, avionics and ATEs because the TTL compatible address latches simplify the digital interface design and reduce the board space required.

The ADG428/ADG429 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG428/ADG429 are improved replacements for the DG428/DG429 Analog Multiplexers.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG428/ADG429 are fabricated on an enhanced LC²MOS process giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG428/ADG429 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG428BN	–40°C to +85°C	N-18
ADG428BP	–40°C to +85°C	P-20A
ADG428TQ	–55°C to +125°C	Q-18
ADG429BN	–40°C to +85°C	N-18
ADG429BP	–40°C to +85°C	P-20A
ADG429TQ	–55°C to +125°C	Q-18

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ADG428/ADG429–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, $\overline{WR}$ = 0 V, $\overline{RS}$ = 2.4 V unless otherwise noted)

Parameter	B Version 25°C	B Version –40°C to +85°C	T Version 25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	60		60		Ω typ	V_D = ±10 V, I_S = –1 mA
	100	125	100	125	Ω max	
ΔR_{ON}	10		10		% max	–10 V < V_S < 10 V, I_S = –1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.03	±0.3	±0.03	±0.3	nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±50	±0.5	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V, V_S = ∓10 V;
ADG428	±0.07	±0.7	±0.07	±0.7	nA typ	Test Circuit 3
	±1	±100	±1	±100	nA max	
ADG429	±0.05	±0.5	±0.05	±0.5	nA typ	
	±1	±50	±1	±50	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG428	±1	±100	±1	±100	nA max	Test Circuit 4
ADG429	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	±0.1	±1	±0.1	±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	110		110		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	250	300	250	300	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V;
						Test Circuit 5
t_{OPEN}		10		10	ns min	R_L = 1 kΩ, C_L = 35 pF;
						V_S = +5 V; Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	115		115		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	225	150	225	ns max	V_S = +5 V; Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	105		105		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	300	150	300	ns max	V_S = +5 V; Test Circuit 7
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	4		4		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF;
						Test Circuit 10
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	–60		–60		dB min	V_S = 7 V rms, V_{EN} = 0 V; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
						Test Circuit 12
C_S (OFF)	11		11		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG428	40		40		pF typ	
ADG429	20		20		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG428	54		54		pF typ	
ADG429	34		34		pF typ	
POWER REQUIREMENTS						V_{IN} = 0 V, V_{EN} = 0 V
I_{DD}	20		20		μA typ	
	100		100		μA max	
I_{SS}	0.001		0.001		μA typ	
	5		5		μA max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

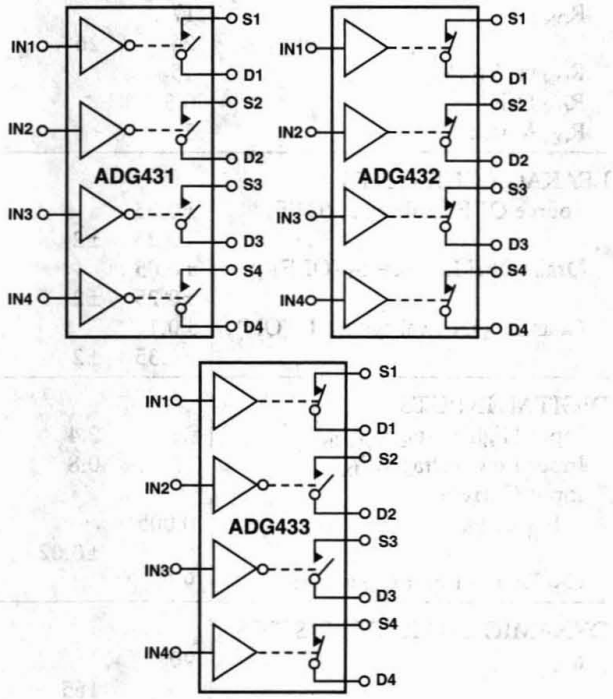
DI LC²MOS
Precision Quad SPST Switches

ADG431/ADG432/ADG433

FEATURES
- 44 V Supply Maximum Ratings
- ±15 V Analog Signal Range
- Low On Resistance (<24 Ω)
- Ultralow Power Dissipation (3.9 μW)
- Low Leakage (<0.25 nA)
- Fast Switching Times
  - t_{ON} <165 ns
  - t_{OFF} <130 ns
- Latch-up Proof
- Break-Before-Make Switching Action
- TTL/CMOS Compatible
- Plug-in Replacement for DG411/DG412/DG413

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

GENERAL DESCRIPTION

The ADG431, ADG432 and ADG433 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS, trench isolated process which provides low power dissipation yet gives high switching speed and low on resistance. Trench isolation gives all the benefits of dielectric isolation and ensures no latch up even under extreme overvoltage conditions.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG431, ADG432 and ADG433 contain four independent SPST switches. The ADG431 and ADG432 differ only in that the digital control logic is inverted. The ADG431 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG432. The ADG433 has two switches with digital control logic similar to that of the ADG431 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG431, ADG432 and ADG433 are fabricated on an enhanced LC²MOS, trench isolated process giving an increased signal range which extends fully to the supply rails.
2. Ultralow Power Dissipation
3. Low R_{ON}

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG431BN	–40°C to +85°C	N-16
ADG431BR	–40°C to +85°C	R-16A
ADG431TQ	–55°C to +125°C	Q-16
ADG432BN	–40°C to +85°C	N-16
ADG432BR	–40°C to +85°C	R-16A
ADG432TQ	–55°C to +125°C	Q-16
ADG433BN	–40°C to +85°C	N-16
ADG433BR	–40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip.
For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ADG431/ADG432/ADG433–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	17		17		Ω typ	V_D = ±8.5 V, I_S = –10 mA;
	24	26	24	27	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
R_{ON} vs. V_D (V_S)	15		15		% typ	
R_{ON} Drift	0.5		0.5		%/°C typ	
R_{ON} Match	5		5		% typ	V_D = 0 V, I_S = –10 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.05		±0.05		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±2	±0.25	±15	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		±0.05		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.25	±2	±0.25	±15	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = ±15.5 V;
	±0.35	±2	±0.35	±17	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.02		±0.02	µA max	
C_{IN} Digital Input Capacitance	9		9		pF typ	
DYNAMIC CHARACTERISTICS[2]						V_{DD} = +15 V, V_{SS} = –15 V
t_{ON}	90		90		ns typ	R_L = 300 Ω, C_L = 35 pF;
		165		175	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	60		60		ns typ	R_L = 300 Ω, C_L = 35 pF;
		130		145	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG433 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Test Circuit 5
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V Digital Inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		µA typ	
	0.1	0.2	0.1	0.2	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	0.1	0.2	0.1	0.2	µA max	
I_L	0.0001		0.0001		µA typ	
	0.1	0.2	0.1	0.2	µA max	
Power Dissipation		7.7		7.7	µW max	

NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ANALOG DEVICES

Dual SPDT Switch

ADG436

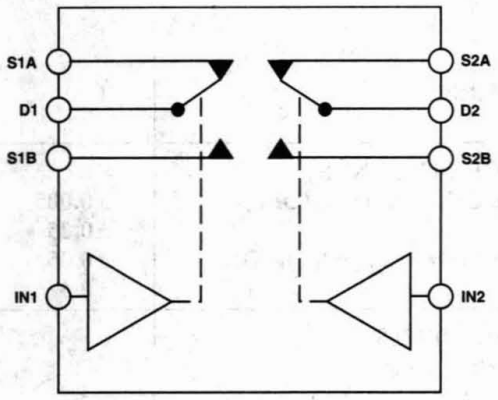
FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (12 Ω typ)
- Low ΔR_{ON} (3 Ω max)
- Low R_{ON} Match (2.5 Ω max)
- Low Power Dissipation
- Fast Switching Times
  - t_{ON} < 175 ns
  - t_{OFF} < 145 ns
- Low Leakage Currents (5 nA max)
- Low Charge Injection (10 pC max)
- Break-Before-Make Switching Action

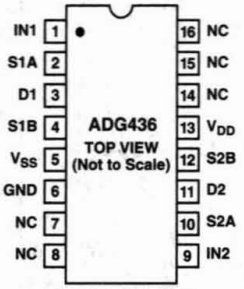
APPLICATIONS

- Audio and Video Switching
- Battery Powered Systems
- Test Equipment
- Communications Systems

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (DIP/SOIC)



NC = NO CONNECT

GENERAL DESCRIPTION

The ADG436 is a monolithic CMOS device comprising two independently selectable SPDT switches. It is designed on an LC²MOS process which provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the part suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the part ideally suited for portable and battery powered instruments.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG436 is fabricated on an enhanced LC²MOS process, giving an increased signal range which extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG436 can be operated from a single rail power supply.

ADG436 Truth Table

Logic	Switch A	Switch B
0	OFF	ON
1	ON	OFF

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG436BN	−40°C to +85°C	N-16
ADG436BR	−40°C to +85°C	R-16A

*N = Plastic DIP, R-16A = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

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ADG436–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	–40°C to +85°C	Units	Test Conditions/ Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
R_{ON}	12		Ω typ	V_D = ±10 V, I_S = –1 mA
		25	Ω max	
ΔR_{ON}	1		Ω typ	V_D = –5 V, 5 V, I_S = –10 mA
		3	Ω max	
R_{ON} Match	1		Ω typ	V_D = ±10 V, I_S = –10 mA
		2.5	Ω max	
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.005		nA typ	V_D = ±15.5 V, V_S = ±15.5 V
	±0.25	±5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_S = V_D = ±15.5 V
	±0.4	±5	nA max	Test Circuit 3
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}		±0.005	μA typ	V_{IN} = 0 V or V_{DD}
		±0.5	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	70		ns typ	R_L = 300 Ω, C_L = 35 pF;
		125	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF;
		120	ns max	V_S = ±10 V; Test Circuit 4
Break-Before-Make Delay, t_{OPEN}	10		ns min	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V; Test Circuit 5
Charge Injection	10		pC typ	V_D = 0 V, R_D = 0 Ω, C_L = 10 nF; Test Circuit 6;
OFF Isolation	72		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz; V_S = 2.3 V rms, Test Circuit 7
Channel-to-Channel Crosstalk	90		dB typ	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz; V_S = 2.3 V rms, Test Circuit 8
C_S (OFF)	10		pF typ	
C_D, C_S (ON)	30		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05		mA typ	Digital Inputs = 0 V or 5 V
		0.35	mA max	
I_{SS}	0.01		μA typ	
	1	5	μA max	
V_{DD}/V_{SS}		±3/±20	V min/V max	$\|V_{DD}\| = \|V_{SS}\|$

NOTES

[1]Temperature Range is as follows: B Version, –40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

High Performance 4/8 Channel Fault-Protected Analog Multiplexers

ADG438F/ADG439F*

FEATURES

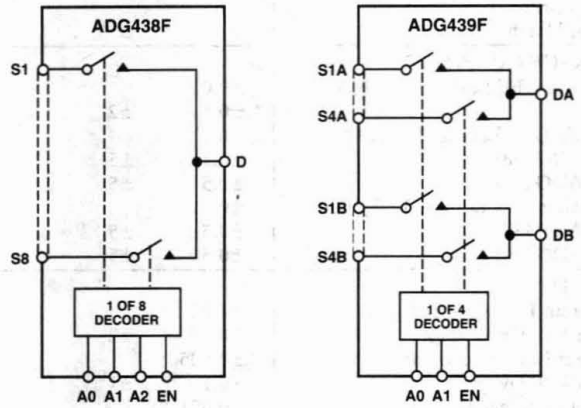
Fast Switching Times
- t_{ON} 250 ns max
- t_{OFF} 150 ns max

Fault and Overvoltage Protection (–35 V, +55 V)
All Switches OFF with Power Supply OFF
Analog Output of ON Channel Clamped Within Power Supplies If an Overvoltage Occurs
Latch-Up Proof Construction
Break Before Make Construction
TTL and CMOS Compatible Inputs

APPLICATIONS

Data Acquisition Systems
Industrial and Process Control Systems
Avionics Test Equipment
Signal Routing Between Systems
High Reliability Control Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG438F/ADG439F are CMOS analog multiplexers, the ADG438F comprising 8 single channels and the ADG439F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from –35 V to +55 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ADG438F switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG439F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

*Patent pending.

PRODUCT HIGHLIGHTS

1. Fault Protection.
   The ADG438F/ADG439F can withstand continuous voltage inputs up to –35 V or +55 V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. ON channel turns OFF while fault exists.
3. Low R_{ON}.
4. Fast Switching Times.
5. Break-Before-Make Switching.
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Eliminates Latch-up.
   A dielectric trench separates the p- and n-channel MOSFETs thereby preventing latch-up.
7. Improved OFF Isolation.
   Trench isolation enhances the channel-to-channel isolation of the ADG438F/ADG439F.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG438FBN	–40°C to +105°C	N-16
ADG438FBR	–40°C to +105°C	R-16A
ADG439FBN	–40°C to +105°C	N-16
ADG439FBR	–40°C to +105°C	R-16A

*N = Plastic DIP; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

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ADG438F/ADG439F–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	B Version –40°C to +85°C	–40°C to +105°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range		V_{SS} + 1.2	V_{SS} + 1.2	V min	
		V_{DD} – 0.8	V_{DD} – 0.8	V max	
R_{ON}		400	400	Ω max	–10 V ≤ V_S ≤ +10 V, I_S = 1 mA;
ΔR_{ON}		5	5	% max	–5 V ≤ V_S ≤ +5 V, I_S = 1 mA;
R_{ON} Drift	0.6			%/°C typ	V_S = 0 V, I_S = 1 mA
R_{ON} Match	3	3	3	% max	V_S = ±10 V, I_S = 1 mA
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±2	±5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG438F	±0.5	±5	±30	nA max	Test Circuit 3
ADG439F	±0.5	±5	±15	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = ±10 V;
ADG438F	±0.5	±5	±30	nA max	Test Circuit 4
ADG439F	±0.5	±5	±15	nA max	
FAULT					
Output Leakage Current	±0.02			nA typ	V_S = –33 V, +33 V or +50 V, V_D = 0 V, Test Circuit 3
(With Overvoltage)	±0.1	±2	±10	µA max	
Input Leakage Current	±0.005			µA typ	V_S = ±25 V, V_D = ∓10 V, Test Circuit 5
(With Overvoltage)	±0.1	±1	±2	µA max	
Input Leakage Current	±0.001			µA typ	V_S = ±25 V, V_D = V_{EN} = A0, A1, A2 = 0 V
(With Power Supplies OFF)	±0.1	±1	±4	µA max	Test Circuit 6
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.4	2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8	V max	
Input Current					
I_{INL} or I_{INH}		±1	±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
$t_{TRANSITION}$	170			ns typ	R_L = 1 MΩ, C_L = 35 pF;
	220	300	320	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 7
t_{OPEN}	10	10	10	ns min	R_L = 1 kΩ, C_L = 35 pF;
					V_S = +5 V; Test Circuit 8
t_{ON} (EN)	200			ns typ	R_L = 1 kΩ, C_L = 35 pF;
	250	300	300	ns max	V_S = +5 V; Test Circuit 9
t_{OFF} (EN)	110			ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	180	180	ns max	V_S = +5 V; Test Circuit 9
t_{SETT}, Settling Time					
0.1%		0.5	0.5	µs typ	R_L = 1 kΩ, C_L = 35 pF;
0.01%		1.7	1.7	µs typ	V_S = +5 V
Charge Injection	4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 10
OFF Isolation	80			dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
					V_S = 7 V rms; Test Circuit 11
Channel-to-Channel Crosstalk	85			dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
					V_S = 7 V rms; Test Circuit 12
C_S (OFF)	5			pF typ	
C_D (OFF)					
ADG438F	50			pF typ	
ADG439F	25			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.05			mA typ	V_{IN} = V_{INL}, V_{INH}, 0 V or 5 V
	0.15	0.25	0.25	mA max	
I_{SS}	0.01			mA typ	
	0.02	0.04	0.04	mA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +105°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

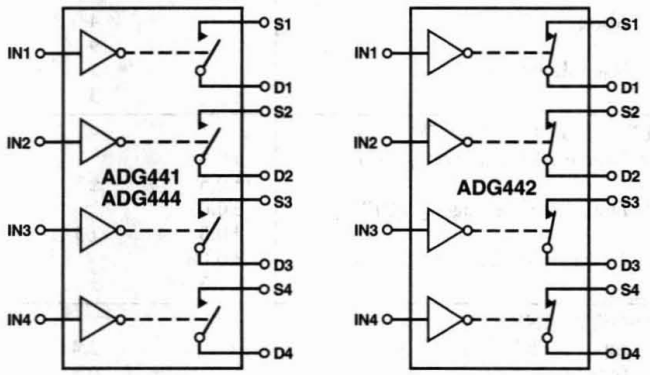
LC²MOS Quad SPST Switches

ADG441/ADG442/ADG444

FEATURES
- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (< 70 Ω)
- Low ΔR_{ON} (9 Ω max)
- Low R_{ON} Match (3 Ω max)
- Low Power Dissipation
- Fast Switching Times
  - t_{ON} < 110 ns
  - t_{OFF} < 60 ns
- Low Leakage Currents (3 nA max)
- Low Charge Injection (6 pC max)
- Break-Before-Make Switching Action
- Latch-Up Proof
- Plug-In Upgrade for DG201A/ADG201A, DG202A/ADG202A, DG211/ADG211A
- Plug in Replacement for DG441/DG442/DG444

APPLICATIONS
- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

4

GENERAL DESCRIPTION

The ADG441, ADG442 and ADG444 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG441, ADG442 and ADG444 contain four independent SPST switches. Each switch of the ADG441 and ADG444 turns on when a logic low is applied to the appropriate control input. The ADG442 switches are turned on with a logic high on the appropriate control input. The ADG441 and ADG444 switches differ in that the ADG444 requires a 5 V logic power supply which is applied to the V_L pin. The ADG441 and ADG442 do not have a V_L pin, the logic power supply being generated internally by an on-chip voltage generator.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG441/ADG442/ADG444 are fabricated on an enhanced LC²MOS, trench-isolated process, giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG441BN	–40°C to +85°C	N-16
ADG441BR	–40°C to +85°C	R-16A
ADG441TQ	–55°C to +125°C	Q-16
ADG442BN	–40°C to +85°C	N-16
ADG442BR	–40°C to +85°C	R-16A
ADG444BN	–40°C to +85°C	N-16
ADG444BR	–40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP, R = 0.15" Small Outline IC (SOIC), Q = Cerdip. For outline information see Package Information section.

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ADG441/ADG442/ADG444–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, V_L = +5 V ± 10% (ADG444), GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	40		40		Ω typ	V_D = ±8.5 V, I_S = –10 mA
	70	85	70	85	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
ΔR_{ON}		4		4	Ω typ	–8.5 V ≤ V_D ≤ +8.5 V
		9		9	Ω max	
R_{ON} Match		1		1	Ω typ	V_D = 0 V, I_S = –10 mA
		3		3	Ω max	
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.01		±0.01		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.5	±3	±0.5	±20	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01		±0.01		nA typ	V_D = ±15.5 V, V_S = ∓15.5 V;
	±0.5	±3	±0.5	±20	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.08		±0.08		nA typ	V_S = V_D = ±15.5 V;
	±0.5	±3	±0.5	±40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±0.00001		±0.00001	µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	85		85		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	110	170	110	170	ns max	V_S = ±10 V; Test Circuit 4
t_{OFF}	45		45		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	60	80	60	80	ns max	V_S = ±10 V; Test Circuit 4
t_{OPEN}	30		30		ns typ	R_L = 1 kΩ, C_L = 35 pF;
Charge Injection	1		1		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF;
	6		6		pC max	V_{DD} = +15 V, V_{SS} = –15 V; Test Circuit 5
OFF Isolation	60		60		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; Test Circuit 6
Channel-to-Channel Crosstalk	100		100		dB typ	R_L = 50 Ω, C_L = 5 pF; f = 1 MHz; Test Circuit 7
C_S (OFF)	4		4		pF typ	f = 1 MHz
C_D (OFF)	4		4		pF typ	f = 1 MHz
C_D, C_S (ON)	16		16		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}						Digital Inputs = 0 V or 5 V
ADG441/ADG442		80		80	µA max	
ADG444	0.001		0.001		µA typ	
	1	2.5	1	2.5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	2.5	1	2.5	µA max	
I_L (ADG444 Only)	0.001		0.001		µA typ	V_L = +5.5 V
	1	2.5	1	2.5	µA max	

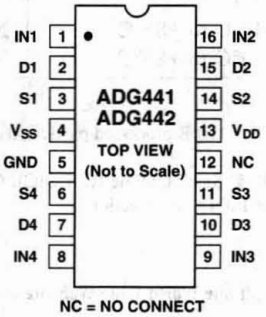
NOTES

[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

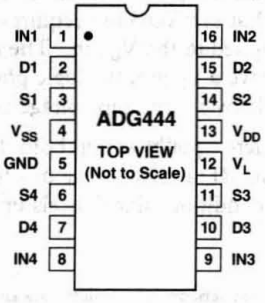
Specifications subject to change without notice.

ADG441/ADG442 PIN CONFIGURATION (DIP/SOIC)



NC = NO CONNECT

ADG444 PIN CONFIGURATION (DIP/SOIC)

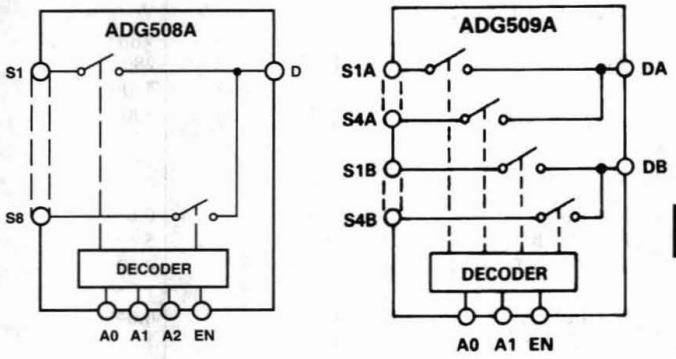


CMOS 4/8 Channel Analog Multiplexers

ADG508A/ADG509A

FEATURES
- 44 V Supply Maximum Rating
- V_{SS} to V_{DD} Analog Signal Range
- Single/Dual Supply Specifications
- Wide Supply Ranges (10.8 V to 16.5 V)
- Extended Plastic Temperature Range (–40°C to +85°C)
- Low Power Dissipation (28 mW max)
- Low Leakage (20 pA typ)
- Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
- Superior Alternative to:
  - DG508A, HI-508
  - DG509A, HI-509

FUNCTIONAL BLOCK DIAGRAMS



4

GENERAL DESCRIPTION

The ADG508A and ADG509A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. The ADG508A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG509A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic compatible digital inputs.

The ADG508A and ADG509A are designed on an enhanced LC^{2}MOS process which gives an increased signal capability of V_{SS} to V_{DD} and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8 V to 16.5 V single or dual supply range. These multiplexers also feature high switching speeds and low R_{ON}.

PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8 V to 16.5 V range for both single and dual supplies.
2. Extended Signal Range:
   The enhanced LC^{2}MOS processing results in a high break down and an increased analog signal range of V_{SS} to V_{DD}.
3. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
4. Low Leakage:
   Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

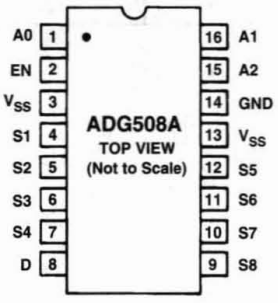
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG508AKN	–40°C to +85°C	N-16
ADG508AKR	–40°C to +85°C	R-16A
ADG508AKP	–40°C to +85°C	P-20A
ADG508ABQ	–40°C to +85°C	Q-16
ADG508ATQ	–55°C to +125°C	Q-16
ADG508ATE	–55°C to +125°C	E-20A
ADG509AKN	–40°C to +85°C	N-16
ADG509AKR	–40°C to +85°C	R-16A
ADG509AKP	–40°C to +85°C	P-20A
ADG509ABQ	–40°C to +85°C	Q-16
ADG509ATQ	–55°C to +125°C	Q-16
ADG509ATE	–55°C to +125°C	E-20A

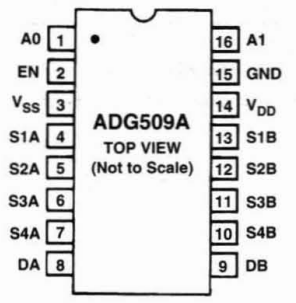
NOTES
[1] To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2] E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

PIN CONFIGURATIONS

DIP and SOIC



DIP and SOIC



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ADG508A/ADG509A–SPECIFICATIONS

DUAL SUPPLY (V_{DD} = +10.8 V to +16.5 V, V_{SS} = –10.8 V to –16.5 V unless otherwise specified)

Parameter	ADG508A ADG509A K Version +25°C	ADG508A ADG509A K Version –40°C to +85°C	ADG508A ADG509A B Version +25°C	ADG508A ADG509A B Version –40°C to +85°C	ADG508A ADG509A T Version +25°C	ADG508A ADG509A T Version –55°C to +125°C	Units	Comments
ANALOG SWITCH								
Analog Signal Range	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V min	
	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V max	
R_{ON}	280		280		280		Ω typ	–10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA; Test Circuit 1
	450	600	450	600	450	600	Ω max	
	300	400	300	400			Ω max	V_{DD} = 15 V (±10%), V_{SS} = –15 V (±10%)
					300	400	Ω max	V_{DD} = 15 V (±5%), V_{SS} = –15 V (±5%)
R_{ON} Drift	0.6		0.6		0.6		%/°C typ	V_S = 0, I_{DS} = 1 mA
R_{ON} Match	5		5		5		% typ	–10 V ≤ V_S ≤ +10 V, I_{DS} = 1 mA
I_S(OFF), Off Input Leakage	0.02		0.02		0.02		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 2
	1	50	1	50	1	50	nA max	
I_D(OFF), Off Output Leakage	0.04		0.04		0.04		nA typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 3
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_D(ON), On Channel Leakage	0.04		0.04		0.04		nA typ	V1 = V2 = ±10 V; Test Circuit 4
ADG508A	1	100	1	100	1	100	nA max	
ADG509A	1	50	1	50	1	50	nA max	
I_{DIFF}, Differential Off Output Leakage (ADG509A only)		25		25		25	nA max	V1 = ±10 V, V2 = ∓10 V; Test Circuit 5
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	µA max	V_{IN} = 0 to V_{DD}
C_{IN} Digital Input Capacitance	8		8		8		pF max	
DYNAMIC CHARACTERISTICS								
$t_{TRANSITION}$[1]	200		200		200		ns typ	V1 = ±10 V, V2 = ∓10 V; Test Circuit 6
	300	400	300	400	300	400	ns max	
t_{OPEN}[1]	50		50		50		ns typ	Test Circuit 7
	25	10	25	10	25	10	ns min	
t_{ON}(EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
t_{OFF}(EN)[1]	200		200		200		ns typ	Test Circuit 8
	300	400	300	400	300	400	ns max	
OFF Isolation	68		68		68		dB typ	V_{EN} = 0.8 V, R_L = 1 kΩ, C_L = 15 pF,
	50		50		50		dB min	V_S = 7 V rms, f = 100 kHz
C_S(OFF)	5		5		5		pF typ	V_{EN} = 0.8 V
C_D(OFF)								
ADG508A	22		22		22		pF typ	V_{EN} = 0.8 V
ADG509A	11		11		11		pF typ	
Q_{INJ}, Charge Injection	4		4		4		pC typ	R_S = 0 Ω, V_S = 0; Test Circuit 9
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	V_{IN} = V_{INL} or V_{INH}
		1.5		1.5		1.5	mA max	
I_{SS}	20		20		20		µA typ	V_{IN} = V_{INL} or V_{INH}
		0.2		0.2		0.2	mA max	
Power Dissipation	10		10		10		mW typ	
		28		28		28	mW max	

NOTE

[1]Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

4/8 Channel Fault-Protected Analog Multiplexers

ADG508F/ADG509F/ADG528F*

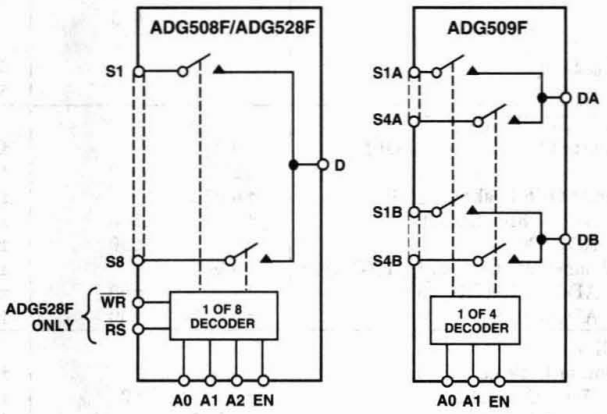
FEATURES

- Low On Resistance (300 Ω typ)
- Fast Switching Times
  - t_{ON} 250 ns max
  - t_{OFF} 250 ns max
- Low Power Dissipation (3.3 mW max)
- Fault and Overvoltage Protection
- All Switches OFF with Power Supply OFF
- Analog Output of ON Channel Clamped Within Power Supplies If an Overvoltage Occurs
- Latch-Up Proof Construction
- Break Before Make Construction
- TTL and CMOS Compatible Inputs

APPLICATIONS

- Existing Multiplexer Applications (Both Fault-Protected and Non-Fault-Protected)
- New Designs Requiring Multiplexer Functions

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG508F, ADG509F and ADG528F are CMOS analog multiplexers, the ADG508F and ADG528F comprising 8 single channels and the ADG509F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs up to ±35 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ADG508F and ADG528F switch one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG509F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. The ADG528F has on-chip address and control latches that facilitate microprocessor interfacing. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

PRODUCT HIGHLIGHTS

1. Fault Protection.
   The ADG508F/ADG509F/ADG528F can withstand continuous voltage inputs up to ±35 V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. ON channel turns off while fault exists.
3. Low R_{ON}.
4. Fast Switching Times.
5. Break-Before-Make Switching.
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Eliminates Latch-up.
   A dielectric trench separates the p and n-channel MOSFETs thereby preventing latch-up.

***Patent pending.**

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG508FBN	–40°C to +85°C	N-16
ADG508FBRN	–40°C to +85°C	R-16N
ADG508FBRW	–40°C to +85°C	R-16W
ADG508FTQ	–55°C to +125°C	Q-16
ADG509FBN	–40°C to +85°C	N-16
ADG509FBRN	–40°C to +85°C	R-16N
ADG509FBRW	–40°C to +85°C	R-16W
ADG509FTQ	–55°C to +125°C	Q-16
ADG528FBN	–40°C to +85°C	N-18
ADG528FBP	–40°C to +85°C	P-20A
ADG528FTQ	–55°C to +125°C	Q-18

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; RN = 0.15" Small Outline IC (SOIC), RW = 0.3" Small Outline IC (SOIC). For outline information see Package Information section.

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ADG508F/ADG509F/ADG528F–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} + 3		V_{SS} + 3	V min	
		V_{DD} – 1.5		V_{DD} – 1.5	V max	
R_{ON}	300	350	300	400	Ω typ	–10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%
		400		450	Ω max	–10 V ≤ V_S ≤ +10 V, I_S = 1 mA; V_{DD} = +15 V ± 5%, V_{SS} = –15 V ± 5%
R_{ON} Drift	0.6		0.6		%/°C typ	V_S = 0 V, I_S = 1 mA
R_{ON} Match	5		5		% max	V_S = 0 V, I_S = 1 mA
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	±0.02		±0.02		nA typ	V_D = ±10 V, V_S = ∓10 V;
	±1	±50	±1	±50	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.04		±0.04		nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG508F/ADG528F	±1	±60	±1	±200	nA max	Test Circuit 3
ADG509F	±1	±30	±1	±100	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.04		±0.04		nA typ	V_S = V_D = ±10 V;
ADG508F/ADG528F	±1	±60	±1	±200	nA max	Test Circuit 4
ADG509F	±1	±30	±1	±100	nA max	
FAULT						
Output Leakage Current	±0.02		±0.02		nA typ	V_S = ±33 V, V_D = 0 V, Test Circuit 3
(With Overvoltage)	±2	±2	±2		µA max	
Input Leakage Current	±0.005		±0.005		µA typ	V_S = ±25 V, V_D = ∓10 V, Test Circuit 5
(With Overvoltage)	±2		±2		µA max	
Input Leakage Current	±0.001		±0.001		µA typ	V_S = ±25 V, V_D = V_{EN} = A0, A1, A2 = 0 V
(With Power Supplies OFF)	±2		±2		µA max	Test Circuit 6
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5		5		pF typ	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	200		200		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	300	400	300	400	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 7
t_{OPEN}	50		50		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	25	10	25	10	ns min	V_S = +5 V; Test Circuit 8
t_{ON} (EN, $\overline{WR}$)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	250	400	250	400	ns max	V_S = +5 V; Test Circuit 9
t_{OFF} (EN, $\overline{RS}$)	200		200		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	250	400	250	400	ns max	V_S = +5 V; Test Circuit 9
t_{SETT}, Settling Time						
0.1%		1		1	µs typ	R_L = 1 kΩ, C_L = 35 pF;
0.01%		2.5		2.5	µs typ	V_S = +5 V
ADG528F Only						
t_W, Write Pulse Width	100	120	100	200	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	
Charge Injection	4		4		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 12
OFF Isolation	68		68		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
	50		50		dB min	V_S = 7 V rms; Test Circuit 13
C_S (OFF)	5		5		pF typ	
C_D (OFF)						
ADG508F/ADG528F	50		50		pF typ	
ADG509F	25		25		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.05		0.05		mA typ	V_{IN} = V_{INL} or V_{INH}
	0.2	0.5	0.2	0.5	mA max	
I_{SS}	0.01		0.01		mA typ	
	0.1	0.1	0.1	0.2	mA max	
I_{DD}	0.1	0.2	0.1	0.2	mA max	V_{IN} = 0 V or 5 V
I_{SS}	0.1	0.1	0.1	0.1	mA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ANALOG DEVICES

DI LC²MOS
Precision 5 V/3 V Quad SPST Switches

ADG511/ADG512/ADG513

FEATURES
+3 V, +5 V or ±5 V Power Supplies
Ultralow Power Dissipation (<0.5 μW)
Low Leakage (<100 pA)
Low On Resistance (<50 Ω)
Fast Switching Times
Low Charge Injection
Latch-Up Proof
TTL/CMOS Compatible
16-Pin DIP or SOIC Package

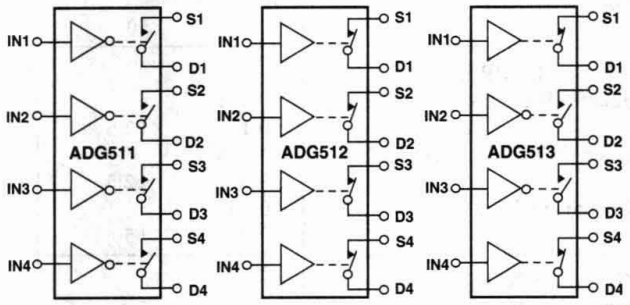
APPLICATIONS
Battery Powered Instruments
Single Supply Systems
Remote Powered Equipment
+5 V Supply Systems
Computer Peripherals such as Disk Drives
Precision Instrumentation
Audio and Video Switching
Automatic Test Equipment
Precision Data Acquisition
Sample Hold Systems
Communication Systems
Compatible with ±5 V Supply DACs and ADCs such as AD7840/8, AD7870/1/2/4/5/6/8

GENERAL DESCRIPTION

The ADG511, ADG512 and ADG513 are monolithic CMOS ICs containing four independently selectable analog switches. These switches feature low, well-controlled on resistance and wide analog signal range, making them ideal for precision analog signal switching.

These switch arrays are fabricated using Analog Devices' advanced linear compatible CMOS (LC²MOS) process which offers the additional benefits of low leakage currents, ultralow power dissipation and low capacitance for fast switching speeds with minimum charge injection. These features make the ADG511, ADG512 and ADG513 the optimum choice for a wide variety of signal switching tasks in precision analog signal processing and data acquisition systems.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

The ability to operate from single +3 V, +5 V or ±5 V bipolar supplies make the ADG511, ADG512 and ADG513 perfect for use in battery-operated instruments, 4–20 mA loop systems and with the new generation of DACs and ADCs from Analog Devices. The use of 5 V supplies and reduced operating currents give much lower power dissipation than devices operating from ±15 V supplies.

The ADG511, ADG512 and ADG513 contain four independent SPST switches. The ADG511 and ADG512 differ only in that the digital control logic is inverted. The ADG511 switch is turned on with a logic low on the appropriate control input, while a logic high is required for the ADG512. The ADG513 contains two switches whose digital control logic is similar to that of the ADG511 while the logic is inverted in the remaining two switches.

PRODUCT HIGHLIGHTS

1. +5 Volt Single Supply Operation
   The ADG511/ADG512/ADG513 offers high performance, including low on resistance and wide signal range, fully specified and guaranteed with +3 V, ±5 V as well as +5 V supply rails.
2. Ultralow Power Dissipation
   CMOS construction ensures ultralow power dissipation.
3. Low R_{ON}

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Option[3]
ADG511BN	–40°C to +85°C	N-16
ADG511BR	–40°C to +85°C	R-16A
ADG511TQ	–55°C to +125°C	Q-16
ADG512BN	–40°C to +85°C	N-16
ADG512BR	–40°C to +85°C	R-16A
ADG512TQ	–55°C to +125°C	Q-16
ADG513BN	–40°C to +85°C	N-16
ADG513BR	–40°C to +85°C	R-16A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.
[2]3.3 V specifications apply over 0°C to +70°C temperature range.
[3]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); Q = Cerdip. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ADG511/ADG512/ADG513–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +5 V ± 10%, V_{SS} = –5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	30		30		Ω typ	V_D = ±3.5 V, I_S = –10 mA;
		50		50	Ω max	V_{DD} = +4.5 V, V_{SS} = –4.5 V
LEAKAGE CURRENTS						V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.025		±0.025		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.025		±0.025		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.1	±2.5	±0.1	±2.5	nA max	Test Circuit 2
Channel ON Leakage I_D, I_S (ON)	±0.05		±0.05		nA typ	V_D = V_S = ±4.5 V;
	±0.2	±5	±0.2	±5	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1		±0.1	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	200		200		ns typ	R_L = 300 Ω. C_L = 35 pF;
		375		375	ns max	V_S = ±3 V; Test Circuit 4
t_{OFF}	120		120		ns typ	R_L = 300 Ω, C_L = 35 pF;
		150		150	ns max	V_S = ±3 V; Test Circuit 4
Break-Before-Make Time Delay, t_D (ADG513 Only)	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +3 V; Test Circuit 5
Charge Injection	11		11		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Test Circuit 6
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						
V_{DD}		+4.5/5.5		+4.5/5.5	V min/max	
V_{SS}		–4.5/–5.5		–4.5/–5.5	V min/max	
I_{DD}	0.0001		0.0001		µA typ	V_{DD} = +5.5 V, V_{SS} = –5.5 V
		1		1	µA max	Digital Inputs = 0 V or 5 V
I_{SS}	0.0001		0.0001		µA typ	
		1		1	µA max	

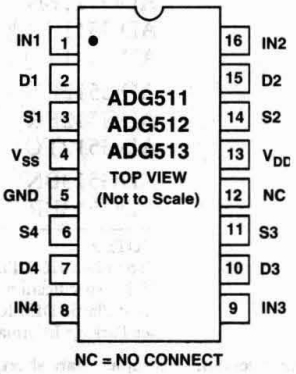
NOTES

[1]Temperature ranges are as follows: B Versions –40°C to +85°C; T Versions –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

PIN CONFIGURATION (DIP/SOIC)



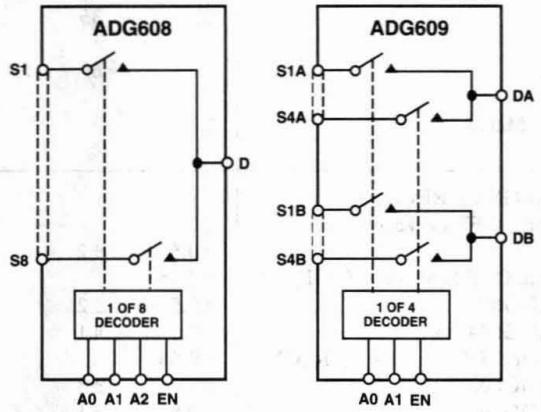
3 V/5 V, 4/8 Channel High Performance Analog Multiplexers

ADG608/ADG609

FEATURES
+3 V, +5 V, ±5 V Power Supplies
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (30 Ω max)
Fast Switching Times
t_{ON} 75 ns max
t_{OFF} 45 ns max
Low Power Dissipation (1.5 μW max)
Break-Before-Make Construction
ESD > 5000 V as per Military Standard 3015.7
TTL and CMOS Compatible Inputs

APPLICATIONS
Automatic Test Equipment
Data Acquisition Systems
Communication Systems
Avionics and Military Systems
Microprocessor Controlled Analog Systems
Medical Instrumentation
Battery Powered Instruments
Remote Powered Equipment
Compatible with ±5 V DACs and ADCs such as AD7840/8, AD7870/1/2/4/5/6/8

FUNCTIONAL BLOCK DIAGRAMS



The ability to operate from single +3 V, +5 V or ±5 V bipolar supplies makes the ADG608 and ADG609 perfect for use in battery operated instruments and with the new generation of DACs and ADCs from Analog Devices. The use of 5 V supplies and reduced operating currents gives much lower power dissipation than devices operating from ±15 V supplies.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG608/ADG609 are fabricated on an enhanced LC^2MOS process giving an increased signal range which extends to the supplies.
2. Low Power Dissipation
3. Low R_{ON}
4. Fast Switching Times
5. Break-Before-Make Switching
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Single/Dual Supply Operation

GENERAL DESCRIPTION

The ADG608 and ADG609 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels respectively, fully specified for ±5 V, +5 V and +3 V power supplies. The ADG608 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG609 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF. All the address and enable inputs are TTL compatible over the full specified operating temperature range, making the parts suitable for bus-controlled systems such as data acquisition systems, process controls, avionics and ATEs since the TTL compatible address inputs simplify the digital interface design and reduce the board space requirements.

The ADG608/ADG609 are designed on an enhanced LC^2MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG608BN	–40°C to +85°C	N-16
ADG608BR	–40°C to +85°C	R-16A
ADG608BRU	–40°C to +85°C	RU-16
ADG608TRU	–55°C to +125°C	RU-16
ADG609BN	–40°C to +85°C	N-16
ADG609BR	–40°C to +85°C	R-16A
ADG609BRU	–40°C to +85°C	RU-16

*N = Plastic DIP; RU = Thin Shrink Small Outline Package (TSSOP); R = 0.15" Small Outline IC (SOIC). For outline information see Package Information section.

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ADG608/ADG609–SPECIFICATIONS

DUAL SUPPLY[1] (V_{DD} = +5 V ± 10%, V_{SS} = –5 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/ Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	22		22		Ω typ	–3.5 V ≤ V_S ≤ +3.5 V, I_S = –1 mA;
	30	35	30	40	Ω max	V_{DD} = +4.5 V, V_{SS} = –4.5 V; Test Circuit 1
ΔR_{ON}	5	6	5	6	Ω max	–3 V ≤ V_S ≤ +3 V, I_{DS} = –1 mA; V_{DD} = +5 V, V_{SS} = –5 V
R_{ON} Match	2	3	2	3	Ω max	V_S = 0 V, I_{DS} = –1 mA; V_{DD} = +5 V, V_{SS} = –5 V
LEAKAGE CURRENTS						V_{DD} = +5.5 V, V_{SS} = –5.5 V
Source OFF Leakage I_S (OFF)	±0.05		±0.05		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
	±0.5	±2	±0.5	±10	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		±0.05		nA typ	V_D = ±4.5 V, V_S = ∓4.5 V;
ADG608	±0.5	±2	±0.5	±10	nA max	Test Circuit 3
ADG609	±0.5	±1	±0.5	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		±0.05		nA typ	V_S = V_D = ±4.5 V;
ADG608	±0.5	±3	±0.5	±20	nA max	Test Circuit 4
ADG609	±0.5	±1.5	±0.5	±10	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5		5		pF typ	
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	50		50		ns typ	R_L = 300 Ω, C_L = 35 pF;
	75	90	75	100	ns max	V_{S1} = ±3.5 V, V_{S8} = ∓3.5 V; Test Circuit 5
t_{OPEN}	10		10		ns min	R_L = 300 Ω, C_L = 35 pF; V_S = +3.5 V; Test Circuit 6
t_{ON} (EN)	50		50		ns typ	R_L = 300 Ω, C_L = 35 pF;
	75	90	75	100	ns max	V_S = +3.5 V; Test Circuit 7
t_{OFF} (EN)	30		30		ns typ	R_L = 300 Ω, C_L = 35 pF;
	45	60	45	75	ns max	V_S = +3.5 V; Test Circuit 7
Charge Injection	6		6		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 8
OFF Isolation	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz; V_S = 3 V rms; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz; Test Circuit 10
C_S (OFF)	9		9		pF typ	
C_D (OFF)						
ADG608	40		40		pF typ	
ADG609	20		20		pF typ	
C_D (ON)						
ADG608	54		54		pF typ	
ADG609	34		34		pF typ	
POWER REQUIREMENTS						
I_{DD}	0.05	0.2	0.05	0.2	μA typ	V_{IN} = 0 V or V_{DD}
	0.2	2	0.2	2	μA max	
I_{SS}	0.01	0.1	0.01	0.1	μA typ	
	0.1	1	0.1	1	μA max	

NOTES

[1]Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Comparators
Contents

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Comparators–Selection Guides

Model	# Comp	Output Stage Type	Power Supply Requirements $+V_{CC}$ Volts	E_{OS} @ +25°C ± mV	Latch Enable Pin	Prop Delay +25°C ns	Prop Delay T_{MAX} ns	# Pins	Page No.	Comments	Fax-code
Singles: Dual Supply											
AD790	1	Open Collector	±15 @ 10/5 mA	0.25–1	Yes	45	50	8	5–3	Large CMV Range	1386
AD9696	1	DIFF/TTL	±5 @ 32/4 mA	2	Yes	4.5	7	8	5–5		1472
AD96685	1	DIFF/ECL	±5 @ 9/18 mA	2	Yes	3.5	NS	16	5–7		1470
Duals: Dual Supply											
AD9698	2	DIFF/TTL	±5 @ 64/8 mA	2	Yes	4.5	7	8	5–5		1472
AD96687	2	DIFF/ECL	±5 @ 18/36 mA	2	Yes	3.5	NS	16	5–7		1470
Singles: Single Supply											
AD790	1	Open Collector	+15 @ 12 mA	0.6	Yes	45	50	8	5–3	Precision, with Internal Hysteresis	1386
AD9696	1	DIFF/TTL	+5 @ 32 mA	2	Yes	4.5	7	8	5–5		1472
Duals: Single Supply											
AD9698	2	DIFF/TTL	+5 @ 64 mA	2	Yes	4.5	7	8	5–5		1472
Quads: Single Supply											
CMP04	4	Open Collector	+15 @ 2 mA	1	No	300	NS	14	5–9		1616
CMP401†	4	TTL +3 V or +5 V	+5 @ 7.5 mA	3	No	23	27	16	5–11	For Recovering Digital Signals	1872
CMP402†	4	TTL +3 V or +5 V	+5 @ 12.4 mA	3	No	40	45	16	5–11	For Recovering Digital Signals	1872

†Also specified @ ±5 V rails.

ANALOG DEVICES

Fast, Precision Comparator

AD790

FEATURES

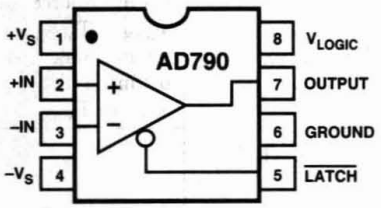
- 45 ns max Propagation Delay
- Single +5 V or Dual ±15 V Supply Operation
- CMOS or TTL Compatible Output
- 250 μV max Input Offset Voltage
- 500 μV max Input Hysteresis Voltage
- 15 V max Differential Input Voltage
- Onboard Latch
- 60 mW Power Dissipation
- Available in 8-Pin Plastic and Hermetic Cerdip Packages
  - MIL-STD-883B Processing Available
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

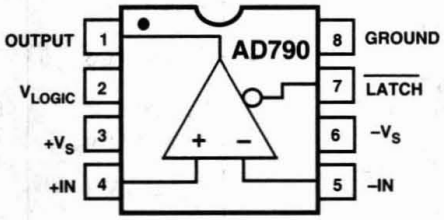
- Zero-Crossing Detectors
- Overvoltage Detectors
- Pulse-Width Modulators
- Precision Rectifiers
- Discrete A/D Converters
- Delta-Sigma Modulator A/Ds

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and Cerdip (Q) Packages



8-Pin SOIC (R) Package



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PRODUCT DESCRIPTION

The AD790 is a fast (45 ns), precise voltage comparator, with a number of features that make it exceptionally versatile and easy to use. The AD790 may operate from either a single +5 V supply or a dual ±15 V supply. In the single-supply mode, the AD790's inputs may be referred to ground, a feature not found in other comparators. In the dual-supply mode it has the unique ability of handling a maximum differential voltage of 15 V across its input terminals, easing their interfacing to large amplitude and dynamic signals.

To preserve its speed and accuracy, the AD790 incorporates a "low glitch" output stage that does not exhibit the large current spikes normally found in TTL or CMOS output stages. Its controlled switching reduces power supply disturbances that can feed back to the input and cause undesired oscillations. The AD790 also has a latching function which makes it suitable for applications requiring synchronous operation.

PRODUCT HIGHLIGHTS

1. The AD790's combination of speed, precision, versatility and low cost makes it suitable as a general purpose comparator in analog signal processing and data acquisition systems.
2. Built-in hysteresis and a low-glitch output stage minimize the chance of unwanted oscillations, making the AD790 easier to use than standard open-loop comparators.
3. The hysteresis combined with a wide input voltage range enables the AD790 to respond to both slow, low level (e.g., 10 mV) signals and fast, large amplitude (e.g., 10 V) signals.
4. A wide variety of supply voltages are acceptable for operation of the AD790, ranging from single +5 V to dual +5 V/–12 V, ±5 V, or +5 V/±15 V supplies.
5. The AD790's power dissipation is the lowest of any comparator in its speed range.
6. The AD790's output swing is symmetric between V_{LOGIC} and ground, thus providing a predictable output under a wide range of input and output conditions.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD790JN	0°C to +70°C	Plastic DIP	N-8
AD790JR	0°C to +70°C	SOIC	R-8
AD790JR-REEL	0°C to +70°C	Reel	
AD790JR-REEL7	0°C to +70°C	SOIC	R-8
AD790KN	0°C to +70°C	Plastic DIP	N-8
AD790AQ	–40°C to +85°C	Cerdip	Q-8
AD790BQ	–40°C to +85°C	Cerdip	Q-8
AD790SQ	–55°C to +125°C	Cerdip	Q-8
AD790SQ/883B	–55°C to +125°C	Cerdip	Q-8
AD790SCHIPS	–55°C to +125°C	Die	

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD790–SPECIFICATIONS

DUAL SUPPLY (Operation @ +25°C and $+V_S$ = +15 V, $-V_S$ = –15 V, V_{LOGIC} = +5 V unless otherwise noted)

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		40	45		40	45		40	45	ns
	T_{MIN} to T_{MAX}			45/50			45/50			60	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{MIN} to T_{MAX}	4.3/**4.3**			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{MIN} to T_{MAX}			0.5/**0.5**			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[1]			0.2	**1.0**		0.05	**0.25**		0.2	**1.0**	mV
	T_{MIN} to T_{MAX}			1.5			**0.5**			**1.5**	mV
Hysteresis[2]	T_{MIN} to T_{MAX}	0.3	0.4	0.6	**0.3**	0.4	**0.5**	**0.3**	0.4	**0.65**	mV
Bias Current	Either Input		2.5	5		1.8	**3.5**		2.5	**5**	µA
	T_{MIN} to T_{MAX}			6.5			**4.5**			**7**	µA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	µA
	T_{MIN} to T_{MAX}			0.3			**0.2**			**0.4**	µA
Power Supply											
Rejection Ratio DC	V_S ± 20%	**80**	90		**88**	100		**80**	90		dB
	T_{MIN} to T_{MAX}	76	88		**85**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage	$V_S \leq \pm 15$ V			**±V_S**			**±V_S**			**±V_S**	V
Common Mode		$-V_S$		$+V_S$ – 2 V	$-V_S$		$+V_S$ – 2 V	$-V_S$		$+V_S$ – 2 V	V
Common Mode											
Rejection Ratio	–10 V < V_{CM} <+10 V	**80**	95		**88**	105		**80**	95		dB
	T_{MIN} to T_{MAX}	76	90		**85**	100		**76**	88		dB
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{MIN} to T_{MAX}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{MIN} to T_{MAX}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	5		2.3	**3.5**		2.3	5	µA
	T_{MIN} to T_{MAX}			7			**5**			**8**	µA
SUPPLY CHARACTERISTICS											
Diff Supply Voltage[3]	V_{LOGIC} = 5 V										
	T_{MIN} to T_{MAX}	4.5		33	**4.5**		**33**	**4.7**		**33**	V
Logic Supply	T_{MIN} to T_{MAX}	4.0		7	**4.0**		7	**4.2**		7	V
Quiescent Current											
$+V_S$	$+V_S$ = 15 V		8	**10**		8	**10**		8	**10**	mA
$-V_S$	$-V_S$ = –15 V		4	**5**		4	**5**		4	**5**	mA
V_{LOGIC}	V_{LOGIC} = 5 V		2	**3.3**		2	**3.3**		2	**3.3**	mA
Power Dissipation				**242**			**242**			**242**	mW
TEMPERATURE RANGE											
Rated Performance	T_{MIN} to T_{MAX}	0 to +70/–40 to +85			0 to +70/–40 to +85			–55 to +125			°C

NOTES

For single +5 V specifications, request the complete data sheet.

[1]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[2]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]$+V_S$ must be no lower than (V_{LOGIC} –0.5 V) in any supply operating conditions, except during power up.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

Ultrafast TTL Comparators

AD9696/AD9698

FEATURES
4.5 ns Propagation Delay
200 ps Maximum Propagation Delay Dispersion
Single +5 V or ±5 V Supply Operation
Complementary Matched TTL Outputs

APPLICATIONS
High Speed Line Receivers
Peak Detectors
Window Comparators
High Speed Triggers
Ultrafast Pulse Width Discriminators

GENERAL DESCRIPTION

The AD9696 and AD9698 are ultrafast TTL-compatible voltage comparators able to achieve propagation delays previously possible only in high performance ECL devices. The AD9696 is a single comparator providing 4.5 ns propagation delay, 200 ps maximum delay dispersion and 1.7 ns setup time. The AD9698 is a dual comparator with equally high performance; both devices are ideal for critical timing circuits in such applications as ATE, communications receivers and test instruments.

Both devices allow the use of either a single +5 V supply or ±5 V supplies. The choice of supplies determines the common mode input voltage range available: –2.2 V to +3.7 V for ±5 V operation, +1.4 V to +3.7 V for single +5 V supply operation.

The differential input stage features high precision, with offset voltages which are less than 2 mV and offset currents less than 1 µA. A latch enable input is provided to allow operation in either sample-and-hold or track-and-hold applications.

The AD9696 and AD9698 are both available as commercial temperature range devices operating from ambient temperatures of 0°C to +70°C, and as extended temperature range devices for ambient temperatures from –55°C to +125°C. Both versions are available qualified to MIL-STD-883 class B.

Package options for the AD9696 include a 10-pin TO-100 metal can, an 8-pin ceramic DIP, an 8-pin plastic DIP, and an 8-lead small outline plastic package. The AD9698 is available in a 16-pin ceramic DIP, a 16-lead ceramic gullwing, a 16-pin plastic DIP, and a 16-lead small outline plastic package. Military qualified versions of the AD9696 come in the TO-100 can and ceramic DIP; the dual AD9698 comes in ceramic DIP.

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ORDERING GUIDE

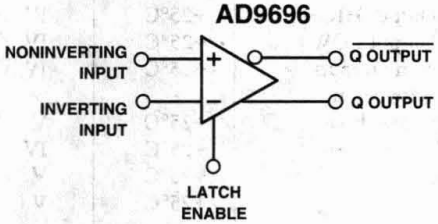
Model	Package	Temperature	Package Option[1]
AD9696KN	Plastic DIP	0°C to +70°C	N-8
AD9696KR	SOIC	0°C to +70°C	R-8
AD9696KQ	Cerdip	0°C to +70°C	Q-8
AD9696TQ/883B	Cerdip	–55°C to +125°C	Q-8
AD9696TZ/883B[2]	Gullwing	–55°C to +125°C	Z-8A
AD9698KN	Plastic DIP	0°C to +70°C	N-16
AD9698KR	SOIC	0°C to +70°C	R-16A
AD9698KQ	Cerdip	0°C to +70°C	Q-16
AD9698TQ/883B	Cerdip	–55°C to +125°C	Q-16
AD9698TZ/883B[3]	Gullwing	–55°C to +125°C	Z-16

NOTES
[1]N = Plastic DIP, Q = Cerdip, R = Small Outline (SOIC), Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]Refer to AD9696TZ/883B military data sheet.
[3]Refer to AD9698TZ/883B military data sheet.

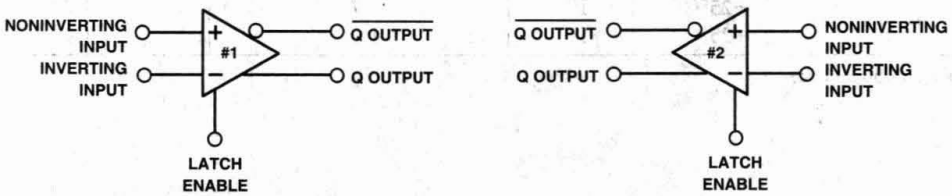
FUNCTIONAL BLOCK DIAGRAMS

AD9696/AD9698 Architecture

AD9696



AD9698



AD9696/AD9698–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S/-V_S$)	+7 V/–7 V
Input Voltage Range	±5 V
Differential Input Voltage	5.4 V
Latch Enable Voltage	–0.5 V to $+V_S$
Output Current (Continuous)	20 mA
Power Dissipation	600 mW
Operating Temperature Range[2]	
AD9696/AD9698KN/KQ/KR[3]	0°C to +70°C
AD9696/AD9698TQ[3]	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	
KQ/TQ Suffixes	+175°C
KN/KR Suffixes	+150°C
Lead Soldering Temperature (10 sec)	+300°C

ELECTRICAL CHARACTERISTICS

(Supply Voltages = –5.2 V and +5.0 V; load as specified in Note 4, unless otherwise indicated)

Parameter	Temp	Test Level	0°C to +70°C AD9696/AD9698 KN/KQ/KR[3] Min	Typ	Max	–55°C to +125°C AD9696/AD9698 TQ[3] Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Input Offset Voltage[5]	+25°C	I		1.0	2.0		1.0	2.0	mV
	Full	VI			3.0			3.0	mV
Input Offset Voltage Drift	Full	V		10			10		µV/°C
Input Bias Current	+25°C	I		16	55		16	55	µA
	Full	VI			110			110	µA
Input Offset Current	+25°C	I		0.4	1.0		0.4	1.0	µA
	Full	VI			1.3			1.3	µA
Input Capacitance	+25°C	V		3			3		pF
Input Voltage Range									
±5.0 V	Full	VI	–2.2		+3.7	–2.2		+3.7	V
±5.0 V	Full	VI	+1.4		+3.7	+1.4		+3.7	V
Common-Mode Rejection Ratio									
±5.0 V	Full	VI	80	85		80	85		dB
±5.0 V	Full	VI	57	63		57	63		dB
LATCH ENABLE INPUT									
Logic "1" Voltage Threshold	Full	VI	2.0			2.0			V
Logic "0" Voltage Threshold	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			10			10	µA
Logic "0" Current	Full	VI			1			1	µA
DIGITAL OUTPUTS									
Logic "1" Voltage (Source 4 mA)	Full	VI	2.7	3.5		2.7	3.5		V
Logic "0" Voltage (Sink 10 mA)	Full	VI		0.4	0.5		0.4	0.5	V
SWITCHING PERFORMANCE									
Propagation Delay (t_{PD})[6]									
Input to Output HIGH	Full	IV		4.5	7.0		4.5	7.0	ns
Input to Output LOW	Full	IV		4.5	7.0		4.5	7.0	ns
Latch Enable to Output HIGH	+25°C	IV		6.5	8.5		6.5	8.5	ns
Latch Enable to Output LOW	+25°C	IV		6.5	8.5		6.5	8.5	ns
Delta Delay Between Outputs	+25°C	IV		0.5	1.5		0.5	1.5	ns
Propagation Delay Dispersion									
20 mV to 100 mV Overdrive	+25°C	V		100			100		ps
100 mV to 1.0 V Overdrive	+25°C	IV		100	200		100	200	ps
Rise Time[11]	+25°C	V		1.85			1.85		ns
Fall Time[11]	+25°C	V		1.35			1.35		ns
Latch Enable									
Pulse Width [$t_{PW(E)}$]	+25°C	IV	3.5	2.5		3.5	2.5		ns
Setup Time (t_S)	+25°C	IV	3	1.7		3	1.7		ns
Hold Time (t_H)	+25°C	IV	3	1.9		3	1.9		ns

Specifications subject to change without notice.

ANALOG DEVICES

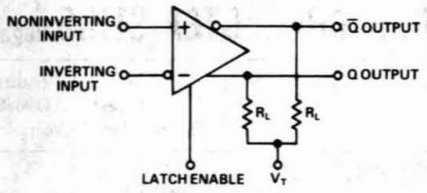
Ultrafast Comparators

AD96685/AD96687

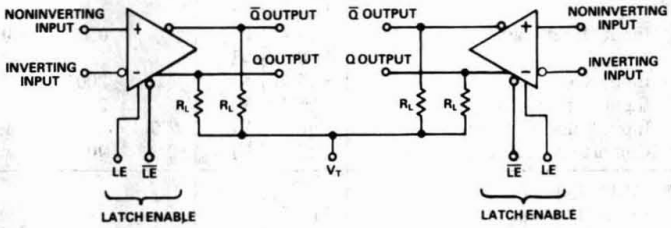
FEATURES
Fast: 2.5 ns Propagation Delay
Low Power: 118 mW per Comparator
Packages: DIP, TO-100, SOIC, PLCC
Power Supplies: +5 V, –5.2 V
Logic Compatibility: ECL
MIL-STD-883 Versions Available
50 ps Delay Dispersion

APPLICATIONS
High Speed Triggers
High Speed Line Receivers
Threshold Detectors
Window Comparators
Peak Detectors

AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO –2.0V, OR 200Ω – 2000Ω

5

GENERAL DESCRIPTION

The AD96685 and AD96687 are ultrafast voltage comparators. The AD96685 is a single comparator with 2.5 ns propagation delay; the AD96687 is an equally fast dual comparator. Both devices feature 50 ps propagation delay dispersion which is a particularly important characteristic of high speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from –2.5 V to +5 V. Outputs are complementary digital signals fully compatible with ECL 10K and 10KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to –2 V. A level sensitive latch input is included which permits tracking, track-hold, or sample-hold modes of operation.

The AD96685 and AD96687 are available in both industrial, –25°C to +85°C, and military temperature ranges. Industrial range devices are available in 16-pin DIP, SOIC, and 20-lead PLCC; additionally, the AD96685 is available in a 10-pin, TO-100 metal can.

ORDERING GUIDE

Model	Type	Temperature Range	Description	Package Options*
AD96685BH	Single	–25°C to +85°C	10-Pin Can, Industrial	H-10A
AD96685BP	Single	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685BQ	Single	–25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96685BR	Single	–25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96685BP-REEL	Single	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685TQ	Single	–55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16
AD96687BP	Dual	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96687BQ	Dual	–25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96687BR	Dual	–25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96687BR-REEL	Dual	–25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96687TQ	Dual	–55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD96685/AD96687–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) ..... +6.5 V
Negative Supply Voltage ($-V_S$) ..... –6.5 V
Input Voltage Range[2] ..... ±5 V
Differential Input Voltage ..... 5.5 V
Latch Enable Voltage ..... $-V_S$ to 0 V
Output Current ..... 30 mA

Operating Temperature Ranges[3]
AD96685/87/BH/BQ/BP/BR ..... –25°C to +85°C
AD96685/87/TQ ..... –55°C to +125°C
Storage Temperature Range ..... –55°C to +150°C
Junction Temperature ..... +175°C
Lead Soldering Temperature (10 sec) ..... +300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0 V; Negative Supply Voltage = –5.2 V, unless otherwise noted)

Parameter	Temp	Test Level	Industrial Temp. Range –25°C to +85°C AD96685BH/BQ/BP/BR Min	Typ	Max	AD96687BQ/BP/BR Min	Typ	Max	Military Temp. Range –55°C to +125°C AD96685TQ Min	Typ	Max	AD96687TQ Min	Typ	Max	Units
INPUT CHARACTERISTICS															
Input Offset Voltage[4]	+25°C	I		1	2		1	2		1	2		1	2	mV
	Full	VI			3			3			3			3	mV
Input Offset Drift	Full	V		20			20			20			20		µV/°C
Input Bias Current	+25°C	I		7	10		7	10		7	10		7	10	µA
	Full	VI			13			13			16			16	µA
Input Offset Current	+25°C	I		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	µA
	Full	VI			1.2			1.2			1.2			1.2	µA
Input Resistance	+25°C	V		200			200			200			200		kΩ
Input Capacitance	+25°C	V		2			2			2			2		pF
Input Voltage Range[5]	Full	VI	–2.5		+5.0	–2.5		+5.0	–2.5		+5.0	–2.5		+5.0	V
Common-Mode Rejection Ratio	Full	VI	80	90		80	90		80	90		80	90		dB
ENABLE INPUT															
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5			–1.5	V
Logic "1" Voltage	Full	VI			40			40			40			40	µA
Logic "0" Voltage	Full	VI			5			5			5			5	µA
DIGITAL OUTPUTS[6]															
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5			–1.5	V
SWITCHING PERFORMANCE[6]															
Propagation Delays[7]															
Input to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Input to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Dispersion[8]	+25°C	V		50			50			50			50		ps
Latch Enable															
Minimum Pulse Width	+25°C	IV		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[9]															
Positive Supply Current (+5.0 V)	Full	VI		8	9		15	18		8	9		15	18	mA
Negative Supply Current (–5.2 V)	Full	VI		15	18		31	36		15	18		31	36	mA
Power Supply Rejection Ratio[10]	Full	VI	60	70		60	70		60	70		60	70		dB

NOTES

[1]Absolute maximum ratings are limiting values, be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under no circumstances should the input voltages exceed the supply voltages.

[3]Typical thermal impedances . . .

AD96685 Metal Can	θ_{JA} = 172°C/W; θ_{JC} = 52°C/W
AD96685 Ceramic	θ_{JA} = 115°C/W; θ_{JC} = 57°C/W
AD96685 SOIC	θ_{JA} = 170°C/W; θ_{JC} = 60°C/W
AD96685 PLCC	θ_{JA} = 88°C/W; θ_{JC} = 45°C/W
AD96687 Ceramic	θ_{JA} = 115°C/W; θ_{JC} = 57°C/W
AD96687 SOIC	θ_{JA} = 92°C/W; θ_{JC} = 47°C/W
AD96687 PLCC	θ_{JA} = 81°C/W; θ_{JC} = 45°C/W

[4]R_S= 100 Ω.

[5]Input Voltage Range can be extended to –3.3 V if $-V_S$ = –6.0 V.

[6]Outputs terminated through 50 Ω to –2.0 V.

[7]Propagation delays measured with 100 mV pulse (10 mV overdrive), to 50% transition point of the output.

[8]Change in propagation delay from 100 mV to 1 V input overdrive.

[9]Supply voltages should remain stable within ±5% for normal operation.

[10]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C; 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

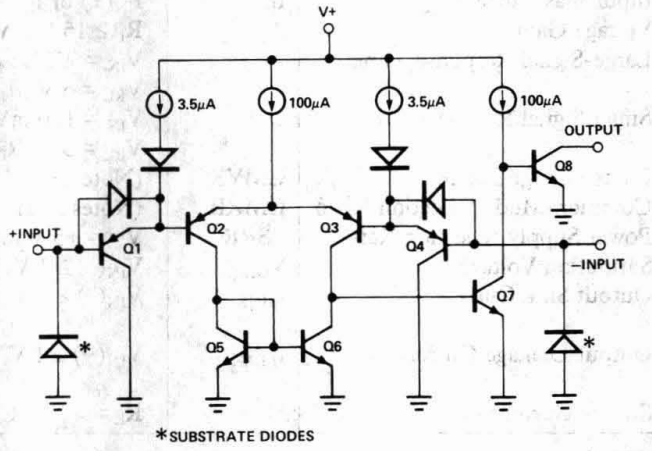
Quad Low Power, Precision Comparator

CMP04

FEATURES

- High Gain: 200 V/mV typ
- Single or Dual Supply Operation
- Input Voltage Range Includes Ground
- Low Power Consumption (1.5 mW/Comparator)
- Low Input Bias Current: 100 nA max
- Low Input Offset Current: 10 nA max
- Low Offset Voltage: 1 mV max
- Low Output Saturation Voltage: 250 mV @ 4 mA
- Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS
- Directly Replaces LM139/239/339 Comparators
- Available in Die Form

SIMPLIFIED SCHEMATIC (1/4 CMP-04)



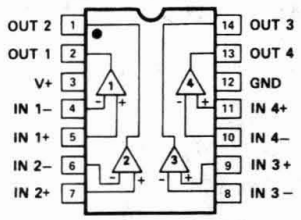
5

GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2 mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

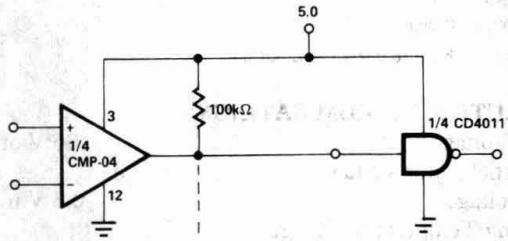
PIN CONNECTIONS

14-Pin Hermetic DIP (Y Suffix)
14-Pin Epoxy DIP (P Suffix)
14-Pin SO (S Suffix)

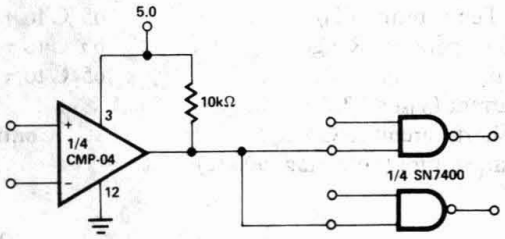


TYPICAL INTERFACE

Driving CMOS



Driving TTL



CMP04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V+ = +5 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 0 Ω, R_L = 5.1 kΩ, V_O = 1.4 V[1]		0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+)$ – $I_{IN}(-)$, R_L = 5.1 kΩ V_O = 1.4 V		2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		25	100	nA
Voltage Gain	A_V	$R_L \geq 15$ kΩ, V+ = 15 V[5]	80	200		V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V[4] V_{RL} = 5 V, R_L = 5.1 kΩ		300		ns
Small-Signal Response Time	t_r	V_{IN} = 100 mV Step[4], 5 mV Overdrive V_{RL} = 5 V, R_L = 5.1 kΩ		1.3		µs
Input Voltage Range	CMVR	(Note 2)	0		V+ – 1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100		dB
Power Supply Rejection Ratio	PSRR	V+ = +5 V to +18 V[5]	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA		250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+) = 0$, $V_O \leq 1.5$ V	6	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1$ V, $V_{IN}(-) = 0$, V_O = 30 V		0.1	100	nA
Supply Current	I+	$R_L = \infty$, All Comps, V+ = 30 V		0.8	2.0	mA

NOTES
[1]At output switch point, V_O = 1.4 V, R_S = 0 Ω with V+ from 5 V; and over the full input common-mode range (0 V to V+ – 1.5 V).
[2]The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ – 1.5 V, but either or both inputs can go to +30 V without damage.
[3]$R_L \geq 15$ kΩ, V+ = 15 V, V_{CM} = 1.5 V to 13.5 V.
[4]Sample tested.
[5]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 36 V or ±18 V
Differential Input Voltage . . . . . 36 Vdc
Input Voltage . . . . . –0.3 V to +36 V
Operating Temperature Range
  CMP04FY . . . . . –40°C to +85°C
  CMP04BY . . . . . –55°C to +125°C
  CMP04FP, FS . . . . . –40°C to +85°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
  (P Suffix) . . . . . –65°C to +125°C
Input Current (V_{IN} < –3.0 V) . . . . . 50 mA
Output Short-Circuit to GND . . . . . Continuous
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for Cerdip and Plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE[1]

Model	T_A = +25°C V_{OS}	Temperature Range	Package Descriptions	Package Options[2]
CMP04BY/883C	1 mV	–55°C to +125°C	14-Contact LCC	Q-14
CMP04FP	1 mV	–40°C to +85°C	14-Pin P-DIP	N-14
CMP04FS	1 mV	–40°C to +85°C	14-Pin SO	SO-14

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in Cerdip and plastic DIP packages.
[2]For outline information see Package Information section.

ANALOG DEVICES

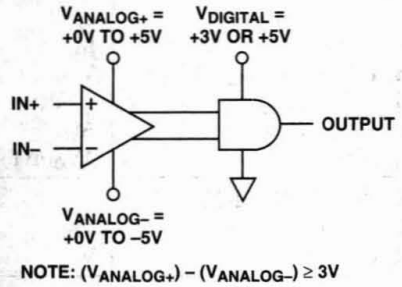
23 ns and 65 ns Low Voltage Comparators

CMP401/CMP402

FEATURES
23 ns or 65 ns Propagation Delay
Single-Supply Operation
Compatible with +3 V and +5 V Logic
Separate Input and Output Sections
Low Power
Wide Input Range: –5 V to +3.9 V

APPLICATIONS
Battery Operated Instrumentation
Line Receivers
Level Translators
Read Channel Detection

FUNCTIONAL BLOCK DIAGRAM



NOTE: $(V_{ANALOG+}) - (V_{ANALOG–}) \geq 3V$

5

GENERAL DESCRIPTION

The CMP401 and CMP402 are 23 ns and 65 ns quad comparators with separate input and output supplies. Separate supplies enable the input stage to be operated from +3 volts to as high as ±6 volts. The output can be supplied with either +3 volts or +5 volts as determined by the interface logic or available supplies. Independent input and output supplies combined with fast propagation make the CMP401 and CMP402 excellent choices for interfacing to portable instrumentation.

The CMP401 and CMP402 are specified over the extended industrial (–40°C to +125°C) temperature range. Both are available in 16-pin plastic DIP or narrow SO-16 surface mount packages. Consult factory for 16-lead TSSOP availability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
CMP401GP	–40°C to +125°C	16-Pin Plastic DIP	N-16
CMP401GS	–40°C to +125°C	16-Pin SOIC	R-16A
CMP401GS-REEL	–40°C to +125°C	16-Pin SOIC	R-16A
CMP401GRU-REEL	–40°C to +125°C	16-Lead TSSOP	RU-16
CMP402GP	–40°C to +125°C	16-Pin Plastic DIP	N-16
CMP402GS	–40°C to +125°C	16-Pin SOIC	R-16A
CMP402GS-REEL	–40°C to +125°C	16-Pin SOIC	R-16A
CMP402GRU-REEL	–40°C to +125°C	16-Lead TSSOP	RU-16

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

Total Analog Supply Voltage ..... +16 V
Digital Supply Voltage ..... +7 V
Analog Positive Supply—Digital Positive Supply .... –200 mV
Input Voltage[2] ..... ±7 V
Differential Input Voltage ..... ±9 V
Output Short-Circuit Duration to GND ..... Indefinite
Storage Temperature Range
P, S, RU Package ..... –65°C to +150°C
Operating Temperature Range
CMP401G, CMP402G ..... –40°C to +125°C
Junction Temperature Range
P, S, RU Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
16-Pin Plastic DIP (P)	90	47	°C/W
16-Pin SO (S)	113	37	°C/W
16-Lead TSSOP (RU)	180	37	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The analog input voltage is equal to ±7 volts or the analog supply voltage, whichever is less.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

CMP401/CMP402–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ $V+_{ANA} = V+_{DIG} = +5.0$ V, $V_{CM} = 0.1$ V, $-40°C \le T_A \le +125°C$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}	$T_A = +25°C$			3	mV
Offset Voltage[1]	V_{OS}				4	mV
Hysteresis				2		mV
Input Bias Current	I_B	$T_A = +25°C$			3	µA
	I_B				4	µA
Input Offset Current	I_{OS}				±3	µA
Input Common-Mode Voltage Range	V_{CM}		0		+4.0	V
Common-Mode Rejection	CMRR	$0.1 V \le V_{CM} \le 3.9 V$	60			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10 k\Omega$		10		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	$I_{OH} = -3.2$ mA	4.6			V
Output Low Voltage	V_{OL}	$I_{OL} = 3.2$ mA			0.2	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V+_{ANA}$ and $V+_{DIG}$ +2.7 V to +6 V	60			dB
Analog Supply Current – CMP401	I_{ANA}	$T_A = +25°C$			6.5	mA
Digital Supply Current – CMP401	I_{DIG}	$V_O = 0$ V, $R_L = \infty$, $T_A = +25°C$			2.0	mA
Analog Supply Current – CMP401	I_{ANA}				8.0	mA
Digital Supply Current – CMP401	I_{DIG}	$V_O = 0$ V, $R_L = \infty$			2.25	mA
Analog Supply Current – CMP402	I_{ANA}	$T_A = +25°C$			1.4	mA
Digital Supply Current – CMP402	I_{DIG}	$V_O = 0$ V, $R_L = \infty$, $T_A = +25°C$			2.0	mA
Analog Supply Current – CMP402	I_{ANA}				1.75	mA
Digital Supply Current – CMP402	I_{DIG}	$V_O = 0$ V, $R_L = \infty$			2.25	mA
DYNAMIC PERFORMANCE						
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD, $T_A = +25°C$		17	23	ns
Propagation Delay – CMP401	t_P	100 mV Step with 5 mV OD, $T_A = +25°C$		33		ns
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD			30	ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD, $T_A = +25°C$		54	65	ns
Propagation Delay – CMP402	t_P	100 mV Step with 5 mV OD, $T_A = +25°C$		60		ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD			75	ns

ELECTRICAL SPECIFICATIONS (@ $V_{ANA} = V_{DIG} = +3.0$ V, $V_{CM} = 0.1$ V, $T_A = +25°C$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}				4.5	mV
Input Common-Mode Voltage Range	V_{CM}		0		+2.0	V
Input Differential Voltage Range	V_{DIFF}		±2.0			V
Common-Mode Rejection	CMRR	$0.1 V \le V_{CM} \le 1.9 V$	60			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	$I_{OH} = -3.2$ mA	2.6			V
Output Low Voltage	V_{OL}	$I_{OL} = 3.2$ mA			0.25	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V+_{ANA}$ and $V+_{DIG}$ +2.7 V to +6 V	60			dB
Analog Supply Current – CMP401	I_{ANA}				6	mA
Digital Supply Current – CMP401	I_{DIG}	$V_O = 0$ V, $R_L = \infty$			1	mA
Analog Supply Current – CMP402	I_{ANA}				1.2	mA
Digital Supply Current – CMP402	I_{DIG}	$V_O = 0$ V, $R_L = \infty$			1	mA
DYNAMIC PERFORMANCE						
Propagation Delay – CMP401	t_P	100 mV Step with 20 mV OD		32		ns
Propagation Delay – CMP402	t_P	100 mV Step with 20 mV OD		70		ns

Specifications subject to change without notice.

D/A Converters
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Low Power

Singles

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	V or I Out	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD7524	8	+5	1	I	1/2		$\pm V_{REF}$	P8	1	16	6–59	Inverted R/2R, 4-Quad Mult	1297
AD7391	10	+2.7	0.1	+1.2 V	TBD	+1.2		S	2	8	6–57	With Readback	1957
AD7390	12	+2.7	0.1	+1.2 V	TBD	+1.2		S	2	8	6–57	With Readback	1957
AD7943	12	+5	0.2	I	1/2		$\pm V_{REF}$	S	1	16	6–91	Inverted R/2R, 4-Quad Mult, Fast I/O	1389
AD7945	12	+5	0.2	I	1/2		$\pm V_{REF}$	P12	1	20	6–91	Inverted R/2R, 4-Quad Mult, Fast I/O	1389
AD7948	12	+5	0.2	I	1/2		$\pm V_{REF}$	P8	1	20	6–91	Inverted R/2R, 4-Quad Mult, Fast I/O	1389
AD8300	12	+3	1.7	+2 V	2	+2.048		S	2	8	6–93	16 MHz Serial Clk., with Reset	1808
DAC8043	12	+5	0.5	I	1/2		$\pm V_{REF}$	S	2	8	6–127	Inverted R/2R, 4-Quad Mult	1624
DAC8143	12	+5	2	I	1/2–1		$\pm V_{REF}$	S	2	16	6–129	With Serial Output & Reset	1625
DAC8512	12	+5	1	+4.096 V	2	+2.5		S	1	8	6–143	14 MHz Serial Clk., with Reset, I_Q = 2.7 mA with CMOS	1895
DAC8562	12	+5	1	+4.096 V	1/2	+2.5		P12	1	20	6–145	I_Q = 1 mA with CMOS, 6 mA with TTL, with Reset	1896
AD7534	14	+12/15	2	I	1		$\pm V_{REF}$	P8	2	20	*	Inverted R/2R, 4-Quad Mult	1300
AD7535	14	+12/15	2	I	2		$\pm V_{REF}$	P16	2	28	*	Inverted R/2R, 4-Quad Mult	1301
AD7536	14	+12/15	2	I	1		$\pm V_{REF}$	P8/14	2	28	*	Inverted R/2R, 4-Quad Mult	1302
AD7538	14	+12/15	2	I	1		$\pm V_{REF}$	P14	2	24	6–65	Inverted R/2R, 4-Quad Mult	1304

Duals

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	V or I Out	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD7528	8	+5/15	2	I	1/2		2 @ $\pm V_{REF}$	P8	2	20	6–61	Inverted R/2R, 4-Quad Mult, Not TTL @ +15 V	1297
AD7628	8	+12/15	2	I	1/2		2 @ $\pm V_{REF}$	P8	2	20	*	Inverted R/2R, 4-Quad Mult, TTL Com. @ 15 V	1329
AD8402	8	+3	5 µA	$+V_{REF}$	1 1/2		$+V_{REF}$	S	2	14	6–97	3-Terminal Pot Function 10/50/100K, I_Q = 2.7 mA with TTL, I_Q = 3 µA with CMOS, 10 MHz I/O, with Reset	1867
AD7537	12	+12/15	2	I	1/2		2 @ V_{REF}	P8	2	24	6–63	Inverted R/2R, 4-Quad Mult	1303
AD7547	12	+15	2	I	1/2		2 @ V_{REF}	P8	1	24	6–67	Inverted R/2R, 4-Quad Mult	1310
AD7549	12	+15	5	I	1/2		4 @ V_{REF}	P4	2	20	*	Inverted R/2R, 4-Quad Mult	1312
DAC8512	12	+5/15	2	I	1/2		2 @ V_{REF}	P12	1	24	6–143	Inverted R/2R, 4-Quad Mult	1895
AD8303	12	+2.7	2	+2.0475 V	2	+2.048		S	2	8	6–95	With Shutdown, I_S = 50 µA	1846
AD8522	12	+5	2	+4.096 V	2	+2.5		S	1	14	6–99	14.2 MHz Serial Clk, I_Q = 5 mA with TTL	1427
AD8582	12	+5	2	+4.096 V	2	+2.5		P12	1	24	6–101	I_Q = 5 mA with TTL, with Reset	1428
DAC8221	12	+5/15	2	I	1/2		2 @ V_{REF}	P12	1	24	*	Inverted R/2R, 4-Quad Mult	1626
DAC8222	12	+5/15	2	I	1/2		2 @ V_{REF}	P12	2	24	6–131	Inverted R/2R, 4-Quad Mult	1627
DAC8248	12	+5/15	2	I	1/2		2 @ V_{REF}	P8	2	24	6–133	Inverted R/2R, 4-Quad Mult with Reset to Zero	1630

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D/A Converters–Selection Guides

Low Power

Quads

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	V or I Out	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD8403	8	+5	0.05	+V_{REF}	1 1/2		+V_{REF}	S	1	14	6–97	3-Terminal Pot Function 10/50/100K, I_Q = 4 mA, with TTL, I_Q = 3 µA with CMOS, 10 MHz I/O, with Reset	1867
DAC8408	8	+5	1.5	I	1/2		4 @ V_{REF}	P8	1	28	6–135	With Readback	1631
AD7804	10	+3.3	12	$V_{BIAS} - V_{SWING}$	2–3	+1.2		S	2	16/28	6–73	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD7805	10	+3.3	12	$V_{BIAS} - V_{SWING}$	2–3	+1.2		P8	2	16/28	6–73	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD7564	12	+5	1.75	I	1/2		4 @ ±V_{REF}	S	2	44	6–69	Inverted R/2R, 4-Quad Mult, with Readback & Reset	1313

Octals

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	V or I Out	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD8801	8	+5 or ±5	4	V_{REFH}	1 1/5		1 V_H	S	1	16	6–105	30 MHz I/O, Reset to V_{REF}/2	1876
AD8803	8	+5 or ±5	4	V_{REFH-L}	1 1/5		1 V_H & 1 V_L	S	1	16	6–105	30 MHz I/O, Reset to V_{REFL}	1876
AD7808	10	+5.5	8	$V_{BIAS} - V_{SWING}$	2–3		+1.2	S	2	20/44	6–75	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD7809	10	+5	8	$V_{BIAS} - V_{SWING}$	2–3		+1.2	P	2	20/44	6–75	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD7568	12	+5	3.5	I	1/2		8 @ ±V_{REF}	S	2	44	6–71	Inverted R/2R, 4-Quad Mult, with Readback & Reset	1314

12 Channel

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	V or I Out	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD8802	8	+5 or ±5	4	V_{REFH}	1 1/2		1 V_H	S	1	20	6–107	30 MHz I/O, Reset to V_{REF}/2	1933
AD8804	8	+5 or ±5	4	V_{REFH-L}	1 1/2		1 V_H & 1 V_L	S	1	20	6–107	30 MHz I/O, Reset to V_{REFL}	1933

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Precision: Bipolar Output

Singles

Model	# Bits	Power Supply Requirements +V_{CC} +Volts	+I_{CC} +mA	–V_{EE} –Volts	–I_{EE} –mA	V_{OUT} Volts	I_{OUT} mA	Linearity LSBs +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD7224	8	+15	6	–5	5	$\pm V_{REF}$	5	1/2–1		+10	P8	2	18	6–37		1257
AD667	12	+15	12	–15	25	±2.5	5	1/4–1/2	+10		P4/8/12	2	28	*		1917
AD767	12	+15	12	–15	23	±2.5	5	1/2–1	+10		P12	1	24	6–33		1332
AD7233	12	+15	10	–15	3	±5	5	1/2–1	+5		S	1	8	6–45	5 MHz I/O	1262
AD7243	12	+15	9	–15	2	+5	5	1/2–1	+5		S	1	16	6–51	5 MHz I/O, with Readback, Reset	1265
AD7245A	12	+12	9	–12	5	5	5	1/2–1	+5		P12	2	24	6–53		1268
AD7248A	12	+12	9	–12	5	5	5	1/2–1	+5		P8	2	24	6–53		1271
AD7845	12	+15	10	–15	4	$\pm V_{REF}$	5	1/2–1		$\pm V_{REF}$	P12	1	24	6–85	With On Chip 4-Quadrant Mult Resistors	1364
AD7848	12	+5	13	–5	6	±3	5	1/2–1	+3		P12	8	28	*	With 8 Deep FIFO Memory	1367
AD7849A	14	+12/15	5	–12/15	5	±10	5	4–6		$\pm V_{REF}$	S	2	20	6–89	Output Control on Powerup/ Powerdown, +5 V Logic Req. with Readback, Reset	1831
AD7840	14	+5	14	–5	6	±3	5	1/2–2	+3		P14	2	24/28	6–83		1363
AD569	16	+12	13	–12	13	±5	5	16–26		±5	P8/16	2	28	*		1167
AD660	16	+15	18	–15	18	10, ±10	5	1–2	+10		P8/S	2	24	6–23	Require a +5 V Logic Supply, with Readback, Reset	4001
AD669	16	+15	18	–15	18	10, ±10	5	1–2	+10		P16	2		6–29	Require a +5 V Logic Supply	1221
AD760	16/18	+15	18	–15	18	±10, +10	5	3/4	+10		P8	2	28	6–31	Self-Calibrating, 10 MHz I/O	1827
AD766	16	+5	12	–5	15	±3.0		2	2.5		S	2		*	12.5 MHz I/O, DSP Interface	1330
AD7846	16	+15	5	–15	5	±10	5	4–16		+5	P16	2	28	6–87		1365
AD7849B	16	+5	2.5					4–6		$\pm V_{REF}$				6–89	Output Control on Powerup/ Powerdown, +5 V Logic Req. with Readback, Reset	1831
AD420	16	+24/32	5			0 to +5	4–20	8	+5		S	1	20	6–13	Output Ranges 4 to 20 mA, or 0 to 20 mA, or 0 to 25 mA	1135
AD421	16	+24	5			0 to +5	4–20	8	+1.25/2.5		S	1	16	6–15	Loop Powered, Output Ranges 4 to 20 mA, 0 to 20 mA, 0 to 25 mA, with Readback, Reset	1707

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D/A Converters–Selection Guides

Precision: Bipolar Output

Duals

Model	# Bits	Power Supply Requirements +V_{CC} +Volts	+I_{CC} +mA	−V_{EE} −Volts	−I_{EE} −mA	V_{OUT} Volts	I_{OUT} mA	Linearity LSBs +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
DAC8229	8	+12–15	6	–5	5	–10/2.5	5	1/2		–10/+2.5	P8	1	20	*	Pins with AD7528	1629
AD7237A	12	+12	18	–15	18	±5	5	1/2–1	+5		P8	2	24	6–47		1263
AD7247A	12	+12	18	–15	18	±5	5	1/2–1	+5		P12	2	24	6–47		1263
AD7242	12	+5	12	–5	27	±3	5	1/2–1	+3		S	2	24	6–49	5 MHz Serial	1264
AD7244	14	+5	12	–5	27	+5 V	12	5	+3		S	2	24	6–49	5 MHz Serial	1266
AD7249	12	+12–15	27	–15	12	±5/10	5	1/2–1			S	1	24	6–55	2 MHz Serial	1272
AD7837	12	+15	10	–15	6	±V_{REF}	5	1/2–1		±V_{REF}	P8	2	24	6–81	With Reset, 4 QM (4 Quadrant Multiplying)	1362
AD7847	12	+15	10	–15	6	±V_{REF}	5	1/2–1		±V_{REF}	P12	1	24	6–81	With Reset, 4 QM (4 Quadrant Multiplying)	1362

Quads

Model	# Bits	Power Supply Requirements +V_{CC} +Volts	+I_{CC} +mA	−V_{EE} −Volts	−I_{EE} −mA	V_{OUT} Volts	I_{OUT} mA	Linearity LSBs +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD7225	8	+15	10	–5	9	±5	5	1/2–1		4 @ V_H	P8	2	24 or	6–39	Single Supply Mode	1258
AD7226	8	+12–15	13	–5	11	±5	5	1/2–1		1 @ V_H	P8	1	20/24	6–41	Single Supply Mode	1259
DAC8426	8	+15	14	–5	10	±5	10, 0	1–2	+10		P8	1	20	6–141	AD7226 with Internal Reference	1635
AD664	12	+15	15	–15	19	±V_{REF}	5	3/4		±V_{REF}	P4/8/12	2	28/44	6–25	Requires a +5 V Logic Supply & 1 mA, with Readback, Reset, 4 QM	1218
AD7564	12	+5	1.75	±V_{REF}		±V_{REF}		1/2		4 @ ±V_{REF}	S	2	44	6–69	With Readback, Reset, 4 QM	1313
DAC8412	12	+5 or ±15	12	15	10	V_H/V_L	5	1–2		1 @ V_H	P12	2	28	6–137	With Readback, Resets to Midscale	1632
DAC8413	12	+5 or ±15	12	15	10	V_H/V_L	5	1–2		1 @ V_H	P12	2	28	6–137	With Readback, Resets to Zero	1633
DAC8420	12	15	12	15	12	V_L/V_H	5	1–2		1 @ V_H	S	2	16	6–139	10 MHz I/O	1634
AD783x Series, Has Power on Reset Function																
AD7834	14	+15	10	–15	10	±8.192	5	2		1 V_H 1 V_L	S	2	28	6–77	10 MHz I/O, Requires a +5 V Logic Supply	1859
AD7835	14	+15	10	–15	10	±8.192	5	1		2 V_H 2 V_L	P8/16	2	44	6–77	Requires a +5 V Logic Supply	1859
AD7836	14	+15	10	–15	10	±10	5	2–1		2 V_H 2 V_L		2	44	6–79	Requires a +5 V Logic Supply	1859
AD75004	14	+12	30	–12	30	±5	5	1/2	+5		P8	2	24/28	6–119		

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Precision: Bipolar Output

Octals

Model	# Bits	Power Supply Requirements +V_{CC} +Volts	+I_{CC} +mA	−V_{EE} −Volts	−I_{EE} −mA	V_{OUT} Volts	I_{OUT} mA	Linearity LSBs +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD7228A	8	+15	16	−5	14	±5	5	1		+2 > 10	P8	1	20	6–43		1261
DAC8800	8	12	2	−5	0.2		$V_H/V_L/R_{FB}$	1/2		2 @ V_H/V_L	S	1	20	6–147	8 MHz Serial	1636
DAC8840	8	+5	26	−5	26	±3	±5	1		8 @ $\pm V_{REF}$	S	1	24	6–149	6 MHz Serial, with Reset, 1 MHz 4 QM	1637
AD8842	8	+5	14	−5	13	±3	±5	1		8 @ $\pm V_{REF}$	S	1	24	6–109	6 MHz Serial, with Reset, 50 kHz 4 QM	1433

16 Channel

Model	# Bits	Power Supply Requirements +V_{CC} +Volts	+I_{CC} +mA	−V_{EE} −Volts	−I_{EE} −mA	V_{OUT} Volts	I_{OUT} mA	Linearity LSBs +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD8600	8	+5	35	−5	35	±3	2	1		+2.5	P8	2	44	6–103	With Readback	1429

D/A Converters–Selection Guides

True Single Supply

Singles

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	Output Voltage +5 V_{DD} Volts	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O 4	# Buff	# Pins	Page No.	Comments	Fax-code
AD557	7	+5	23	2.56	1	+1.2		P8	1	16	6–17		1159
AD558	8	+5–15	23	2.56–10	1/2	+1.2		P8	1	16	6–19		1160
AD7224	8	+15	6	+10	1/2		$\pm V_{REF}$	P8	2	18	6–37		1257
AD7391	10	+2.7	0.1	+1.2	TBD	+1.2		S	2	8	6–57	With Readback	1957
AD7390	12	+2.7	0.1	+1.2	TBD	+1.2		S	2	8	6–57	With Readback	1957
AD7243	12	+12–15	10	5–12	1/2–1	+3		S	2	16	6–51	3 MHz I/O with Readback & Reset	1265
AD8300	12	+3	1.7	+2	2	+2.05		S	2	8	6–93	16 MHz Serial Clk., with Reset	1808
DAC8512	12	+5	1	+4.096	2	+2.5		S	1	8	6–143	14 MHz Serial Clk., with Reset, I_Q = 2.7 mA with CMOS	1895
DAC8562	12	+5	1	+4.096	1/2	+2.5		P12	1	20	6–145	I_Q = 1 mA with CMOS, 6 mA with TTL, with Reset	1896
AD420	16	+24–32		5–10	1/2–1	+5		S	1		6–13	0/4-to-20 mA Output, with Readback & Reset	1135
AD421	16	+5	0.3	5–10	1/2–1	+5		S	1	16	6–15	0/4-to-20 mA Output, with Readback & Reset	1892

Dual

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	Output Voltage +5 V_{DD} Volts	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O 4	# Buff	# Pins	Page No.	Comments	Fax-code
AD8402	8	+3	5 µA	+V_{REF}	1 1/2		+V_{REF}	S	2	14	6–97	3 Terminal Pot. Function 10/50/100 K, I_Q = 2.7 mA, with TTL, I_Q = 3 µA with CMOS, 10 MHz I/O, with Reset	1867
AD7237A	12	+12	18	+10	1/2–1	+3		P8	2	24	6–47	Dual Supply Mode	1263
AD7247A	12	+12	18	+10	1/2–1	+3		P12	2	24	6–47	Dual Supply Mode	1263
AD7249	12	+12–15	2	+5/10	1/2–1	+3		S	1	24	6–55	2 MHz Serial, with Reset	1272
AD8303	12	+2.7	2	2.0475	2	+2.05		S	2	8	6–95	With Shutdown, I_S = 50 µA	1846
AD8522	12	+5	2	4.096	2	+2.5		S	1	14	6–99	14.2 MHz Serial Clk., I_Q = 5 mA with TTL	1427
AD8582	12	+5	2	4.096	2	+2.5		P12	1	24	6–101	I_Q = 5 mA with TTL, with Reset	1428

True Single Supply

Quad

Model	# Bits	Power Supply Requirements $+V_S$ +Volts	$+I_S$ +mA	Output Voltage +5 V_{DD}	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O 4	# Buff	# Pins	Page No.	Comments	Fax-code
AD7225	8	+15	10	+10 V	1		4 @ $+V_{REF}$	P8	2	24	6–39		1258
AD7226	8	+15	13	+10 V	1		1 @ $+V_{REF}$	P8	2	20	6–41		1259
AD7804	10	+3.3	12	V_{BIAS}–V_{SWING}	2–3	+1.2		S	2	16/28	6–73	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD7805	10	+3.3	12	V_{BIAS}–V_{SWING}	2–3	+1.2		P8	2	16/28	6–73	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD8403	8	+5	0.05	$+V_{REF}$	1 1/2		1 @ $+V_{REF}$	S	1	14	6–97	3-Terminal Pot. Function 10/50/100 K, I_Q = 4 mA, with TTL, I_Q = 3 µA with CMOS, 10 MHz I/O, with Reset	1867
DAC8420	12	+5		V_L–V_H	2–4		1 V_H & 1V_L	S	2		6–139	With Reset	1634

Octal

Model	# Bits	Power Supply Requirements $+V_S$ +Volts	$+I_S$ +mA	Output Voltage +5 V_{DD}	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O 4	# Buff	# Pins	Page No.	Comments	Fax-code
AD7228A	8	+5–15	14	+10 V	1–2	+10		P8	1	24	6–43		1261
DAC8841	8	+5	26	+1.5 V	1–3		8 @ $+V_{REF}$	S	1	24	6–151	6 MHz I/O with Readback & Reset	1638
AD7808	10	+5.5	8	V_{BIAS}–V_{SWING}	2–3	+1.2		S	2	20/44	6–75	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884
AD7809	10	+5	8	V_{BIAS}–V_{SWING}	2–3	+1.2			2	20/44	6–75	10 MHz I/O, with Reset, I_Q = 230 µA in Shutdown	1884

16 Channel

Model	# Bits	Power Supply Requirements $+V_S$ +Volts	$+I_S$ +mA	Output Voltage +5 V_{DD}	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O 4	# Buff	# Pins	Page No.	Comments	Fax-code
AD8600	8	+5	32	0–+2.3 V	1	+2.3		P8	2	44	6–103	With Readback & Reset	1429

D/A Converters–Selection Guides

High Speed Current Output

Model	# Bits	Power Supply Volts	Power Supply mA	I_{OUT} mA	Settling Time ns 0.1	Settling Time ns 0.01%	Update Rate MHz	Linearity +25°C LSBs	# Pins	Page No.	Comments	Fax-code
AD9768	8	±5	3.6	20	5		100	1/2	18/20	6–117	ECL, 400 V/µs Slew Rate	1481
AD9701	8	–5	160	–26.87	6		250	1	22/28	6–111	Complete Composite Video	1474
DAC08	8	+5/–15	3.8	2.04	135			1/2	16	*	Industry Standard	1618
AD561	10	±15	10/1.5	–2.4	250			NS	16	*	Internal V_{REF}	1161
ADV7128	10	+5	125	15			30, 50, 80	1/2	40	6–121	Very High Speed	1598
AD9720	10	–5.2	280	20.48 typ	4.5			3/4	28	6–115	ECL, Excellent SFDR	1479
AD9721	10	±5	30/290	20.48	4.5			3/4	28	6–115	TTL, Excellent SFDR	1480
AD9712B	12	–5.2	178	20.48		30		1.5	28	6–113	ECL, Good SFDR	1476
AD9713B	12	±5	12/184	20.48		30		1.5	28	6–113	TTL, Good SFDR	1476
AD565A	12	±12	5/18	–2.4		400		3/4	24	6–21	Internal V_{REF}	1164
AD566A	12	±12	5/18	–2.4		400		3/4	24	6–21	External V_{REF}	1164
AD568	12	±15	32/8	10.24	23	35		1	24	*	350 pV-sec Glitch	1166
AD668	12	±12	32/9	10.24	90	120		1	24	6–27	350 pV-sec Glitch	1220
AD7943	12	+5	0.2	$\pm V_{REF}/5K$		500		1	16	6–91	4 Quadrant Multiplying	1389
AD7945	12	+5	0.2	$\pm V_{REF}/5K$		500		1	20	6–91	4 Quadrant Multiplying	1389
AD7948	12	+5	0.2	$\pm V_{REF}/5K$		500		1	20	6–91	4 Quadrant Multiplying	1389
DAC312	12	±5, ±15	7/16	4		500		1/2–1	20	6–125	12-Bit Version of DAC08	1622
AD768	14/16	±5		20.48		35	30	6	44	6–35	35 pV-sec Glitch, 83 dB SFDR @ 1 MHz	1334
DAC16	16	+5, –15	20/10	4		500		1.5	24	6–123		1621

DDS Functions

Model	# Bits	Power Supply Volts	Power Supply mA	I_{OUT} mA	Settling Time ns 0.1	Settling Time ns 0.01%	Update Rate MHz	Linearity +25°C	# Pins	Page No.	Comments	Fax-code
AD7008	10	+5	160				20/40		44	17–13	AD7008 (Complete 32-Bit DDS with Quadrature Modulator)	1240
AD7350	10	+5	15				50		48	*	Complete 32-Bit DDS with Frequency and Phase Modulators, Sine Lookup	1993
AD7351	10	+3	12				5		48	*	Complete 32-Bit DDS with Frequency and Phase Modulators, Sine Lookup	1994

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Digital Potentiometers

Dual

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	Output Voltage Range	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD8402	8	+3	5 µA	0 to +V_{REF}	1 1/2		1 @ +V_{REF}	S	2	14	6–97	3-Terminal Pot. Function 10/50/100K, I_Q = 2.7 mA, with TTL, I_Q = 3 µA with CMOS, 10 MHz I/O, with Reset	1867

Quad

Model	# Bits	Power Supply Requirements +V_S +Volts	+I_S +mA	Output Voltage Range	Linearity +25°C	Voltage Reference–Volts Int	Ext	I/O	# Buff	# Pins	Page No.	Comments	Fax-code
AD8403	8	+5	0.05	0 to +V_{REF}	1 1/2		1 @ +V_{REF}	S		14	6–97	3-Terminal Pot. Function 10/50/100K, I_Q = 4 mA, with TTL, I_Q = 3 µA with CMOS, 10 MHz I/O, with Reset	1867

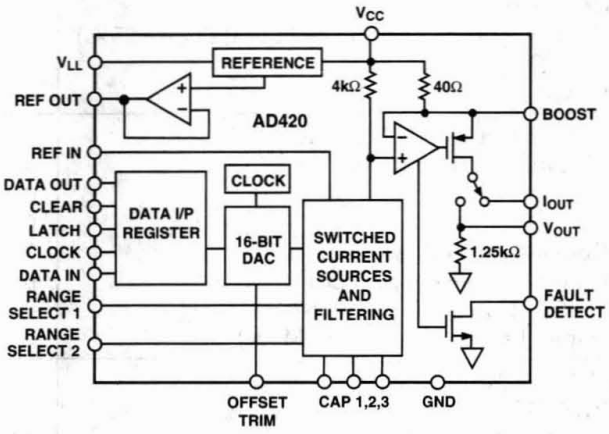
Serial Input 16-Bit 4–20 mA, 0–20 mA DAC

AD420

FEATURES

4–20 mA, 0–20 mA or 0–24 mA Current Output
16-Bit Resolution and Monotonicity
±0.012% max Integral Nonlinearity
±0.05% max Offset (Trimmable)
±0.15% max Total Output Error (Trimmable)
Flexible Serial Digital Interface (3.3 MBPS)
On-Chip Loop Fault Detection
On-Chip 5 V Reference (25 ppm/°C max)
Asynchronous CLEAR Function
Maximum Power Supply Range of 32 V
Output Loop Compliance of 0 V to V_{CC} – 2.5 V
24-Pin SOIC and PDIP Packages

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD420 is a complete digital to current loop output converter, designed to meet the needs of the industrial control market. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop signals in a compact 24-pin SOIC or PDIP package.

The output current range can be programmed to 4 mA–20 mA, 0 mA–20 mA or an overrange function of 0 mA–24 mA. The AD420 can alternatively provide a voltage output from a separate pin that can be configured to provide 0 V–5 V, 0 V–10 V, ±5 V or ±10 V with the addition of a single external buffer amplifier.

The 3.3M Baud serial input logic design minimizes the cost of galvanic isolation and allows for simple connection to commonly used microprocessors. It can be used in three-wire or asynchronous mode and a serial-out pin is provided to allow daisy chaining of multiple DACs on the current loop side of the isolation barrier.

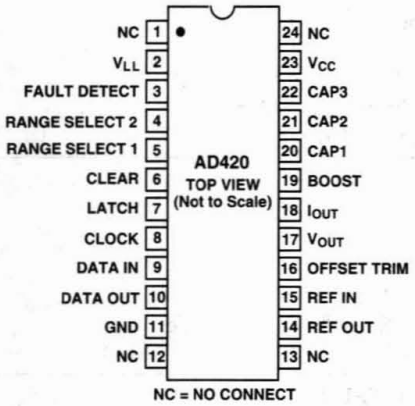
The AD420 uses sigma-delta (ΣΔ) DAC technology to achieve 16-bit monotonicity at very low cost. Full-scale settling to 0.1% occurs within 3 ms. The only external components that are required (in addition to normal transient protection circuitry) are three low cost capacitors which are used in the DAC output filter.

If the AD420 is going to be used at extreme temperatures and supply voltages, an external output transistor can be used to minimize power dissipation on the chip via the "BOOST" pin.

The FAULT DETECT pin signals when an open circuit occurs in the loop. The on-chip voltage reference can be used to supply a precision +5 V to external components in addition to the AD420 or, if the user desires temperature stability exceeding 25 ppm/°C, an external precision reference such as the AD586 can be used as the reference.

The AD420 is available in a 24-pin SOIC and PDIP over the industrial temperature range of –40°C to +85°C.

PIN DESIGNATIONS



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Max Operating Voltage	Package Option*
AD420AN-32	–40°C to +85°C	32 V	N-24
AD420AR-32	–40°C to +85°C	32 V	R-24

*N = Plastic DIP, R = Plastic SOIC. For outline information see Package Information section.

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AD420—SPECIFICATIONS ($T_A = T_{MIN}$–T_{MAX}, V_{CC} = + 24 V, R_L = 500 Ω, unless otherwise noted)

Parameter	AX-32 Versions[1] Min	Typ	Max	Units	Comments
RESOLUTION	16			Bits	
ACCURACY[2]					
Monotonicity	16			Bits	
Integral Nonlinearity		±0.002	±0.012	%	
Offset (0 mA or 4 mA) (T_A = +25°C)			±0.05	%	
Offset Drift		20	50	ppm/°C	
Total Output Error (20 mA or 24 mA) (T_A = +25°C)			±0.15	%	
Total Output Error Drift		20	50	ppm/°C	
PSRR[3]		5	10	μA/V	
OUTPUT CHARACTERISTICS					
Operating Current Ranges	4		20	mA	
	0		20	mA	
	0		24	mA	
Current Loop Voltage Compliance	0		V_{CC} – 2.5 V	V	
Output Voltage Range (Pin 17)	0		5	V	
Settling Time (to 0.1% of FS)[4]		2.5	3	ms	
Output Impedance (Current Mode)		25		MΩ	
VOLTAGE REFERENCE					
REF OUT					
Output Voltage (T_A = +25°C)	4.995	5.0	5.005	V	
Drift			±25	ppm/°C	
Externally Available Current		5		mA	
Short Circuit Current		7		mA	
REF IN					
Resistance		30		kΩ	
V_{LL}					
Output Voltage		4.5		V	
Externally Available Current		5		mA	
Short Circuit Current		20		mA	
DIGITAL INPUTS					
V_{IH} (Logic 1)	2.4			V	
V_{IL} (Logic 0)			0.8	V	
I_{IH} (V_{IN} = 5.0 V)			±10	μA	
I_{IL} (V_{IN} = 0 V)			±10	μA	
Data Input Rate ("3-Wire" Mode)	No Minimum		3.3	MBPS	
Data Input Rate ("Asynchronous" Mode)	No Minimum		150	kBPS	
DIGITAL OUTPUTS					
FAULT DEFECT					
V_{OH} (10 kΩ Pull-Up Resistor to V_{LL})	3.6	4.5		V	
V_{OL} (10 kΩ Pull-Up Resistor to V_{LL})		0.2	0.4	V	
V_{OL} @ 2.5 mA		0.6		V	
DATA OUT					
V_{OH} (I_{OH} = –0.8 mA)	3.6	4.3		V	
V_{OL} (I_{OL} = 1.6 mA)		0.3	0.4	V	
POWER SUPPLY					
Operating Range V_{CC}	12		32	V	
Quiescent Current		4.2	5.0	mA	
Quiescent Current (External V_{LL})		3		mA	
TEMPERATURE RANGE					
Specified Performance	–40		+85	°C	

NOTES

[1]X refers to the package designator, R or N.

[2]Total Output Error includes Offset and Gain Error. Total Output Error and Offset Error are with respect to the Full-Scale Output and are measured with an ideal +5 V reference. If the internal reference is used, the reference errors must be added to the Offset and Total Output Errors.

[3]PSRR is measured by varying V_{CC} from 12 V to its maximum 32 V.

[4]External capacitor selection must be as described in Figure 5.

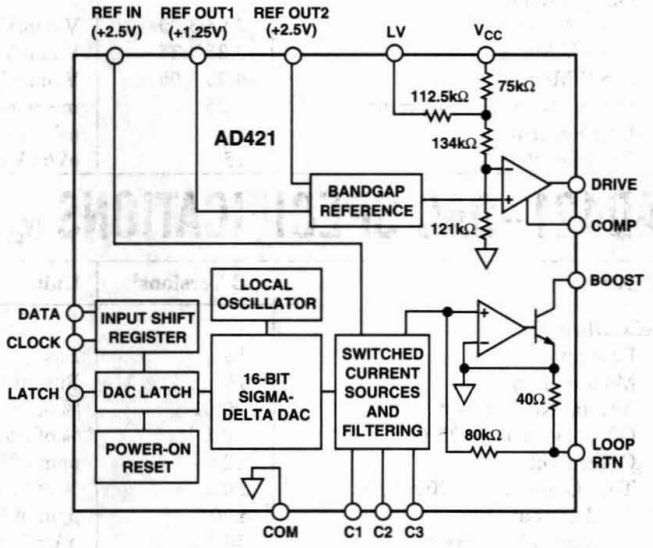
Specifications subject to change without notice.

Loop-Powered 4–20 mA DAC

AD421

FEATURES
4–20 mA Current Output
HART* Compatible
16-Bit Resolution and Monotonicity
±0.01% Integral Nonlinearity
5 V or 3 V Regulator Output
2.5 V and 1.25 V Precision Reference
750 μA Quiescent Current max
Programmable Alarm Current Capability
Flexible High Speed Serial Interface
16-Pin TSSOP, SOIC and PDIP Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD421 is a complete, loop-powered, digital to 4–20 mA converter, designed to meet the needs of smart transmitter manufacturers in the Industrial Control industry. It provides a high precision, fully integrated, low cost solution in a compact 16-pin package. The AD421 is ideal for extending the resolution of smart 4–20 mA transmitters at very low cost.

The AD421 includes a selectable regulator that is used to power itself and other devices in the transmitter. This regulator provides either a +5 V, +3.3 V or +3 V regulated output voltage. The part also contains +1.25 V and +2.5 V precision references. The AD421 thus eliminates the need for a discrete regulator and voltage reference. The only external components required are a number of passive components and a pass transistor to span large loop voltages.

The AD421 can be used with standard HART FSK protocol communication circuitry without any degradation in specified performance. The high speed serial interface is capable of operating at 10 Mbps and allows for simple connection to commonly-used microprocessors and microcontrollers via a standard three-wire serial interface.

The sigma-delta architecture of the DAC guarantees 16-bit monotonicity while the integral nonlinearity for the AD421 is ±0.01%. The part provides a zero scale 4 mA output current with ±0.1% offset error and a 20 mA full-scale output current with ±0.2% gain error.

The AD421 is available in a 16-pin, 0.3 inch-wide, plastic DIP and in a 16-lead, 0.3 inch-wide, SOIC package. The part is specified over the industrial temperature range of –40°C to +85°C.

***HART is a trademark of the HART Communication Foundation.**

PRODUCT HIGHLIGHTS

1. The AD421 is a single chip, high performance, low cost solution for generating 4–20 mA signals for smart industrial control transmitters.
2. The AD421's regulated supply voltage can be used to power any additional circuits in the transmitter. The regulated output value is pin selectable as either +3 V, +3.3 V or +5 V.
3. The AD421's on-chip references can provide a precision reference voltage to other devices in the system. This reference voltage can be either +1.25 V or +2.5 V.
4. The AD421 is fully compatible with standard HART circuitry or other similar FSK protocols.
5. With the addition of a single discrete transistor, the AD421 can be operated from V_{CC} + 2 V min to a maximum of the breakdown voltage of the pass transistor.
6. The AD421 converts the digital data to current with 16-bit resolution and monotonicity. Full-scale settling time to ±0.1% typically occurs within 8 ms.
7. The AD421 features a programmable alarm current capability that allows the transmitter to send out of range currents to indicate a transducer fault.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD421–LOOP-POWERED SPECIFICATIONS (Using DN25D[1] as pass transistor; REF IN = REF OUT2; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Versions[2]	Units	Conditions/Comments
OUTPUT CHARACTERISTICS			
Current Loop Voltage Compliance[3]	V_{CC} + 2	V min	
	350	V max	DN25D Breakdown Voltage
Full-Scale Settling Time	8	ms typ	Settling Time to ±0.1%, C1 = C2 = 10 nF, C3 = 3.3 nF
Output Impedance	25	MΩ typ	
AC Loop Voltage Sensitivity	2	µA/V typ	1200 Hz to 2200 Hz
VOLTAGE REGULATOR			
Output Voltage (V_{CC})			
3 V Mode	2.95/3.05	V min/V max	3 V Nominal. LV Pin Connected to V_{CC}
3.3 V Mode	3.25/3.35	V min/V max	3.3 V Nominal. LV Pin Connected Through 0.01 µF to V_{CC}
5 V Mode	4.95/5.05	V min/V max	5 V Nominal. LV Pin Connected to COM
Externally Available Current	3.25	mA min	Assuming 4 mA Flowing in the Loop
Line Regulation	1	µV/V typ	
Load Regulation	15	µV/mA typ	

AD421–DAC SPECIFICATIONS (V_{CC} = +3 V to +5 V; REF IN = REF OUT2; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	B Versions[2]	Units	Conditions/Comments
ACCURACY			
Resolution	16	Bits	
Monotonicity	16	Bits min	
Integral Nonlinearity	±0.01	% of FS max	FS = Full-Scale Output Current
Offset (4 mA) @ +25°C[4]	±0.1	% of FS max	V_{CC} = 5 V
Offset Drift	±25	ppm of FS/°C max	Includes On-Chip Reference Drift
Total Output Error (20 mA) @ +25°C[4]	±0.2	% of FS max	V_{CC} = 5 V
Total Output Drift	±50	ppm of FS/°C max	Includes On-Chip Reference Drift
V_{CC} Supply Sensitivity	50	nA/mV max	25 nA/mV Typical
VOLTAGE REFERENCE			
REF OUT2			
Output Voltage	2.49/2.51	V min/V max	2.5 V Nominal
Drift	±40	ppm/°C max	20 ppm/°C Typical from –40°C to +25°C and –2.5 ppm/°C Typical from +25°C to +85°C
Externally Available Current	0.5	mA min	
V_{CC} Supply Sensitivity	150	µV/V max	15 µV/V Typical
Output Impedance	3	Ω typ	
Noise (0.1 Hz – 10 Hz)	6	µV (p-p) typ	
REF OUT1			
Output Voltage	1.24/1.26	V min/V max	1.25 V Nominal, 100 kΩ Load to COM[5]
Drift	±50	ppm/°C max	20 ppm/°C Typical from –40°C to +25°C and 2 ppm/°C Typical from +25°C to +85°C
Externally Available Current	0.5	mA min	
V_{CC} Supply Sensitivity	150	µV/V max	15 µV/V Typical
Output Impedance	3	Ω typ	
Noise (0.1 Hz–10 Hz)	4	µV (p-p) typ	
REF IN			
Input Resistance	40	kΩ typ	
DIGITAL INPUTS			
V_{IH} (Logic 1)	0.75 × V_{CC}	V min	
V_{IL} (Logic 0)	0.25 × V_{CC}	V max	
I_{IH}	±10	µA max	$V_{IN} = V_{CC}$
I_{IL}	±10	µA max	V_{IN} = 0 V
Data Coding	Binary		
Data Rate	10	Mbps max	
POWER SUPPLIES			
Operating Range	+2.95 to +5.05	V min to V max	Functional to 7 V
Quiescent Current			
@ V_{CC} = 3 V	650	µA max	475 µA Typical
@ V_{CC} = 5 V	750	µA max	575 µA Typical

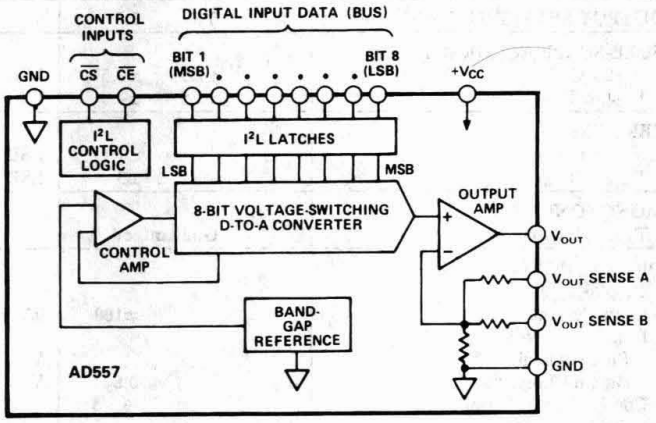
NOTES
[1]The DN25D is available from Supertex, Inc., 1350 Bordeaux Drive, Sunnyvale, CA 94089.
[2]Temperature range is –40°C to +85°C.
[3]The max current loop voltage compliance is determined by the pass transistor breakdown voltage and is 350 V for the DN25D.
[4]With V_{CC} = 3 V, the transfer function shifts negative by typically 0.25%; a 16 kΩ resistor connected between COM and LOOPRTN will approximately compensate for the V_{CC} supply sensitivity in moving from 5 V to 3 V by skewing the gain of the AD421.
[5]100 kΩ resistor only required if this reference is being used in application circuits.
Specifications subject to change without notice.

DACPORT Low Cost, Complete µP-Compatible 8-Bit DAC

AD557*

FEATURES
Complete 8-Bit DAC
Voltage Output—0 V to 2.56 V
Internal Precision Band-Gap Reference
Single-Supply Operation: +5 V (±10%)
Full Microprocessor Interface
Fast: 1 µs Voltage Settling to ±1/2 LSB
Low Power: 75 mW
No User Trims Required
Guaranteed Monotonic Over Temperature
All Errors Specified T_{MIN} to T_{MAX}
Small 16-Pin DIP or 20-Pin PLCC Package
Low Cost

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD557 DACPORT® is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The low cost and versatility of the AD557 DACPORT are the result of continued development in monolithic bipolar technologies.

The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5 V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while laser-wafer trimming of these thin-film resistors permits absolute calibration at the factory to within ±2.5 LSB; thus, no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2 LSB for a full-scale step in 800 ns.

The AD557 is available in two package configurations. The AD557JN is packaged in a 16-pin plastic, 0.3"-wide DIP. For surface mount applications, the AD557JP is packaged in a 20-pin JEDEC standard PLCC. Both versions are specified over the operating temperature range of 0°C to +70°C.

DACPORT is a registered trademark of Analog Devices, Inc.

***Protected by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; other patents pending.**

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD557 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The AD557 is designed and specified to operate from a single +4.5 V to +5.5 V power supply.
5. Low digital input currents, 100 µA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible.
6. The single-chip, low power I^2L design of the AD557 is inherently more reliable than hybrid multichip or conventional single-chip bipolar designs.

AD557—SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +5 V unless otherwise noted)

Model	Min	Typ	Max	Units
RESOLUTION			8	Bits
RELATIVE ACCURACY				
0°C to +70°C		±1/2	1	LSB
OUTPUT				
Ranges		0 to +2.56		V
Current Source	+5			mA
Sink		Internal Passive Pull-Down to Ground[2]		
OUTPUT SETTLING TIME[3]		0.8	1.5	µs
FULL-SCALE ACCURACY[4]				
@ +25°C		±1.5	±2.5	LSB
T_{MIN} to T_{MAX}		±2.5	±4.0	LSB
ZERO ERROR				
@ +25°C			±1	LSB
T_{MIN} to T_{MAX}			±3	LSB
MONOTONICITY[5]				
T_{MIN} to T_{MAX}		**Guaranteed**		
DIGITAL INPUTS				
T_{MIN} to T_{MAX}				
Input Current			±100	µA
Data Inputs, Voltage				
Bit On—Logic "1"	2.0			V
Bit On—Logic "0"	0		0.8	V
Control Inputs, Voltage				
On—Logic "1"	2.0			V
On—Logic "0"	0		0.8	V
Input Capacitance		4		pF
TIMING[6]				
t_W Strobe Pulse Width	225			ns
T_{MIN} to T_{MAX}	**300**			ns
t_{DH} Data Hold Time	10			ns
T_{MIN} to T_{MAX}	**10**			ns
t_{DS} Data Setup Time	225			ns
T_{MIN} to T_{MAX}	**300**			ns
POWER SUPPLY				
Operating Voltage Range (V_{CC})				
2.56 Volt Range	**+4.5**		**+5.5**	V
Current (I_{CC})		15	**25**	mA
Rejection Ratio			**0.03**	%/%
POWER DISSIPATION, V_{CC} = 5 V		75	125	mW
OPERATING TEMPERATURE RANGE	0		+70	°C

NOTES
[1]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error" on the AD558 data sheet.
[2]Passive pull-down resistance is 2 kΩ.
[3]Settling time is specified for a positive-going full-scale step to ±1/2 LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.
[4]The full-scale output voltage is 2.55 V and is guaranteed with a +5 V supply.
[5]A monotonic converter has a maximum differential linearity error of ±1 LSB.
[6]See Figure 7.

Specifications shown in **boldface** are tested on all production units at electrical test.
Specifications subject to change without notice.

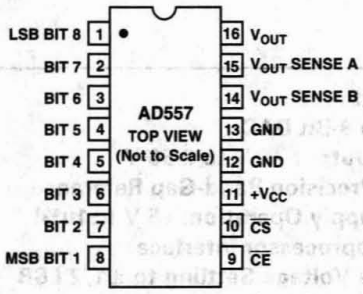
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD557JN	0°C to +70°C	N-16
AD557JP	0°C to +70°C	P-20A

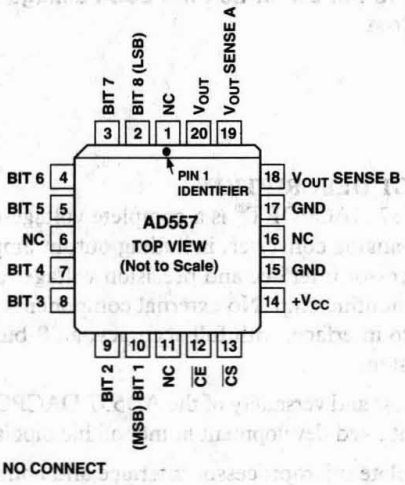
*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATIONS

DIP



PLCC



NC = NO CONNECT

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground ..... 0 V to +18 V
Digital Inputs (Pins 1–10) ..... 0 V to +7.0 V
V_{OUT} ..... Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation ..... 450 mW
Storage Temperature Range
N/P (Plastic) Packages ..... –25°C to +100°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
N/P (Plastic) Packages ..... 140/55°C/W

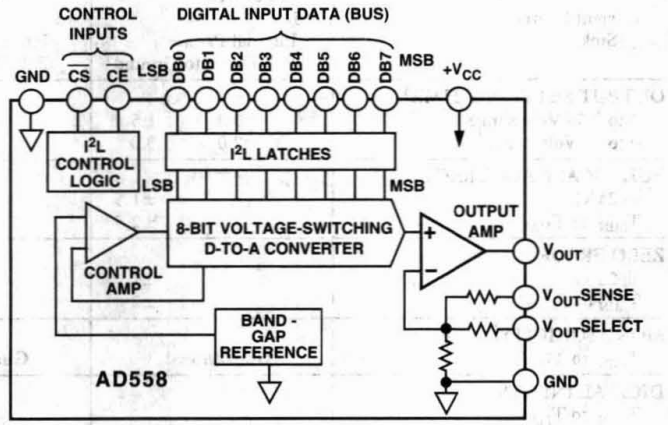
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DACPORT Low Cost, Complete µP-Compatible 8-Bit DAC

AD558*

FEATURES
- Complete 8-Bit DAC
- Voltage Output–2 Calibrated Ranges
- Internal Precision Bandgap Reference
- Single-Supply Operation: +5 V to +15 V
- Full Microprocessor Interface
- Fast: 1 µs Voltage Settling to ±1/2 LSB
- Low Power: 75 mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{MIN} to T_{MAX}
- Small 16-Pin DIP and 20-Pin PLCC Packages
- Single Laser-Wafer-Trimmed Chip for Hybrids
- Low Cost
- MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD558 DACPORT® is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low voltage bandgap circuit which permits full-accuracy performance on a single +5 V to +15 V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1 LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2 LSB for a full-scale step in 800 ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0°C to +70°C temperature range, while the AD558S and T grades are specified for –55°C to +125°C operation. The "J" and "K" grades are available either in 16-pin plastic (N) or hermetic ceramic (D) DIPS. They are also available in 20-pin JEDEC standard PLCC packages. The "S" and "T" grades are available in the 16-pin hermetic ceramic DIP package.

***Protected by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; Patents Pending.**

DACPORT is a registered trademark of Analog Devices, Inc.

ORDERING GUIDE

Model[1]	Temperature	Relative Accuracy Error Max T_{MIN} to T_{MAX}	Full-Scale Error, Max T_{MIN} to T_{MAX}	Package Option[2]
AD558JN	0°C to +70°C	±1/2 LSB	±2.5 LSB	Plastic (N-16)
AD558JP	0°C to +70°C	±1/2 LSB	±2.5 LSB	PLCC (P-20A)
AD558JD	0°C to +70°C	±1/2 LSB	±2.5 LSB	TO-116 (D-16)
AD558KN	0°C to +70°C	±1/4 LSB	±1 LSB	Plastic (N-16)
AD558KP	0°C to +70°C	±1/4 LSB	±1 LSB	PLCC (P-20A)
AD558KD	0°C to +70°C	±1/4 LSB	±1 LSB	TO-116 (D-16)
AD558SD	–55°C to +125°C	±3/4 LSB	±2.5 LSB	TO-116 (D-16)
AD558TD	–55°C to +125°C	±3/8 LSB	±1 LSB	TO-116 (D-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD558/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD558—SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +5 V to +15 V unless otherwise noted)

Model	AD558J Min	AD558J Typ	AD558J Max	AD558K Min	AD558K Typ	AD558K Max	AD558S[1] Min	AD558S[1] Typ	AD558S[1] Max	AD558T[1] Min	AD558T[1] Typ	AD558T[1] Max	Units
RESOLUTION			8			8			8			8	Bits
RELATIVE ACCURACY[2]													
0°C to +70°C			±1/2			±1/4			±1/2			±1/4	LSB
−55°C to +125°C									±3/4			±3/8	LSB
OUTPUT													
Ranges[3]		0 to +2.56			0 to +2.56			0 to +2.56			0 to +2.56		V
		0 to +10			0 to +10			0 to +10			0 to +10		V
Current Source		+5			+5			+5			+5		mA
Sink		Internal Passive Pull-Down to Ground[4]			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground		
OUTPUT SETTLING TIME[5]													
0 to 2.56 Volt Range		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	µs
0 to 10 Volt Range[4]		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	µs
FULL-SCALE ACCURACY[6]													
@ 25°C			±1.5			±0.5			±1.5			±0.5	LSB
T_{MIN} to T_{MAX}			±2.5			±1			±2.5			±1	LSB
ZERO ERROR													
@ 25°C			±1			±1/2			±1			±1/2	LSB
T_{MIN} to T_{MAX}			±2			±1			±2			±1	LSB
MONOTONICITY[7]													
T_{MIN} to T_{MAX}		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
DIGITAL INPUTS													
T_{MIN} to T_{MAX}													
Input Current			±100			±100			±100			100	µA
Data Inputs, Voltage													
Bit On-Logic "1"	2.0			2.0			2.0			2.0			V
Bit On-Logic "0"	0		0.8	0			0			0			V
Control Inputs, Voltage													
On-Logic "1"	2.0			2.0			2.0			2.0			V
On-Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
Input Capacitance		4			4			4			4		pF
TIMING[8]													
t_W, Strobe Pulse Width	200			200			200			200			ns
T_{MIN} to T_{MAX}	270			270			270			270			ns
t_{DH} Data Hold Time	10			10			10			10			ns
T_{MIN} to T_{MAX}	10			10			10			10			ns
t_{DS} Data Set-Up Time	200			200			200			200			ns
T_{MIN} to T_{MAX}	270			270			270			270			ns
POWER SUPPLY													
Operating Voltage Range (V_{CC})													
2.56 Volt Range	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	V
10 Volt Range	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	V
Current (I_{CC})		15	25		15	25		15	25		15	25	mA
Rejection Ratio			0.03			0.03			0.03			0.03	%/%
POWER DISSIPATION, V_{CC} = 5 V		75	125		75	125		75	125		75	125	mW
V_{CC} = 15 V		225	375		225	375		225	375		225	375	mW
OPERATING TEMPERATURE RANGE	0		+70	0		+70	−55		+125	−55		+125	°C

NOTES

[1]The AD558 S & T grades are available processed and screened to MIL-STD-883 Class B. Consult Analog Devices' Military Databook for details.

[2]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the offset to the full scale of the device. See "Measuring Offset Error".

[3]Operation of the 0 volt to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4]Passive pull-down resistance is 2 kΩ for 2.56 volt range, 10 kΩ for 10 volt range.

[5]Settling time is specified for a positive-going full-scale step to ±1/2 LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6]The full range output voltage for the 2.56 range is 2.55 V and is guaranteed with a +5 V supply, for the 10 V range, it is 9.960 V guaranteed with a +15 V supply.

[7]A monotonic converter has a maximum differential linearity error of ±1 LSB.

[8]See Figure 7.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Ground . . . . . 0 V to +18 V

Digital Inputs (Pins 1–10) . . . . . 0 V to +7.0 V

V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}

Power Dissipation . . . . . 450 mW

Storage Temperature Range

N/P (Plastic) Packages . . . . . −25°C to +100°C

D (Ceramic) Package . . . . . −55°C to +150°C

Lead Temperature (soldering, 10 sec) . . . . . +300°C

Thermal Resistance

Junction to Ambient/Junction to Case

D (Ceramic) Package . . . . . 100°C/W/30°C/W

N/P (Plastic) Packages . . . . . 140°C/W/55°C/W

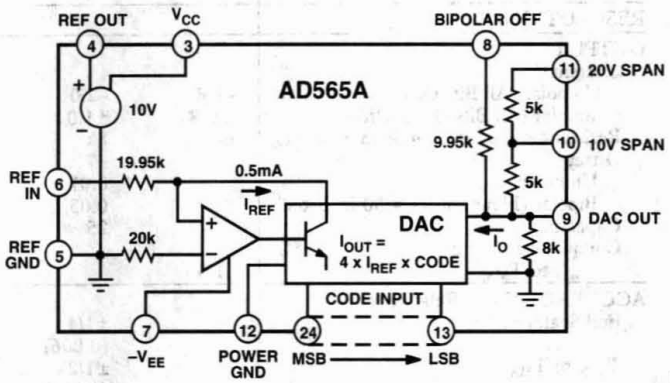
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

High Speed 12-Bit Monolithic D/A Converters

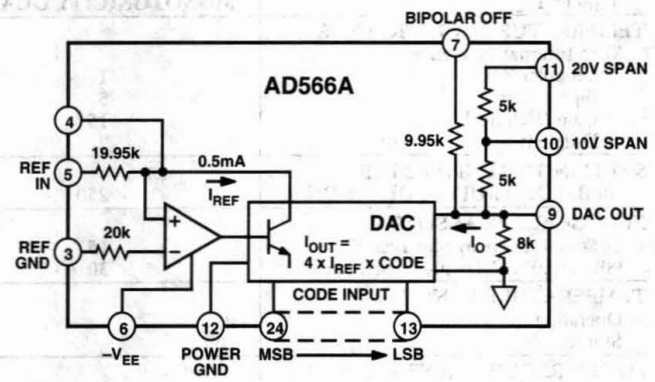
AD565A*/AD566A*

FEATURES
- Single Chip Construction
- Very High-Speed Settling to 1/2 LSB
  - AD565A: 250 ns max
  - AD566A: 350 ns max
- Full-Scale Switching Time: 30 ns
- Guaranteed for Operation with ±12 V Supplies:
  - AD565A with –12 V Supply: AD566A
- Linearity Guaranteed Over Temperature:
  - 1/2 LSB max (K, T Grades)
- Monotonicity Guaranteed Over Temperature
- Low Power: AD566A = 180 mW max;
  - AD565A = 225 mW max
- Use with On-Board High-Stability Reference (AD565A)
  - or with External Reference (AD566A)
- Low Cost
- MIL-STD-883-Compliant Versions Available

AD565A FUNCTIONAL BLOCK DIAGRAM



AD566A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters which incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high-speed bipolar current-steering switches, control amplifier and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried Zener reference that features low-noise, long-term stability and temperature drift characteristics comparable to the best discrete reference diodes.

The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10–90% full-scale transition time less than 35 ns and settle to within ±1/2 LSB in 250 ns max (350 ns for AD566A). Both are laser-trimmed at the wafer level to ±1/8 LSB typical linearity and are specified to ±1/4 LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD565A and AD566A the ideal choice for high-speed display drivers as well as fast analog-to-digital converters.

The laser trimming process which provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A resulting in a typical full-scale gain TC of 10 ppm/°C. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

AD565A and AD566A are available in four performance grades. The J and K are specified for use over the 0°C to +70°C temperature range while the S and T grades are specified for the –55°C to +125°C range. The D grades are all packaged in a 24-pin, hermetically sealed, ceramic, dual-in-line package. The JR grade is packaged in a 28-pin plastic SOIC.

PRODUCT HIGHLIGHTS

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562/3 with very fast switching times and an optimally-damped settling characteristic.
3. The devices also contain SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.
4. The AD565A and AD566A are available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current /883B data sheet for detailed specifications.

*Protected by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349; 4,020,486; 3,747,088.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD565A–SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = +15 V, unless otherwise noted.)

Model	AD565AJ Min	AD565AJ Typ	AD565AJ Max	AD565AK Min	AD565AK Typ	AD565AK Max	Units
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (All Bits On)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
Bipolar (All Bits On or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R2 = 50 Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{MIN} to T_{MAX}	−1.5		+10	−1.5		+10	V
ACCURACY (Error Relative to Full Scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
All Bits ON-to-OFF or OFF-to-ON		250	400		250	400	ns
FULL-SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5 V dc		3	5		3	5	mA
V_{EE}, −11.4 to −16.5 V dc		−12	−18		−12	−18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5 V dc		3	10		3	10	ppm of F.S./%
V_{EE} = −11.4 to −16.5 V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE							
(see Figures 2, 3, 4)		0 to +5			0 to +5		V
		−2.5 to +2.5			−2.5 to +2.5		V
		0 to +10			0 to +10		V
		−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1]The digital inputs are guaranteed but not tested over the operating temperature range.

[2]The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15 V dc.

[3]For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

ANALOG DEVICES

Monolithic 16-Bit Serial/Byte DACPORT

AD660

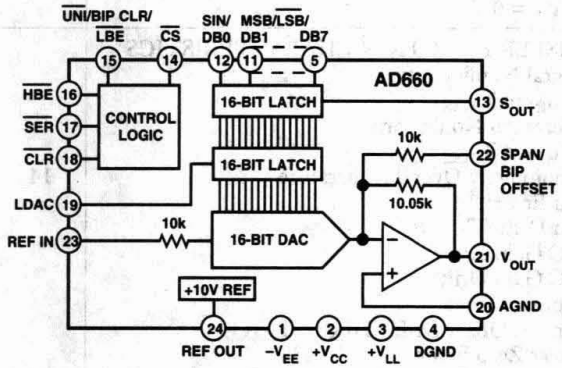
FEATURES

Complete 16-Bit D/A Function
- On-Chip Output Amplifier
- On-Chip Buried Zener Voltage Reference

±1 LSB Integral Linearity
15-Bit Monotonic over Temperature
Microprocessor Compatible
- Serial or Byte Input
- Double Buffered Latches
- Fast (40 ns) Write Pulse

Asynchronous Clear (to 0 V) Function
Serial Output Pin Facilitates Daisy Chaining
Unipolar or Bipolar Output
Low Glitch: 15 nV-s
Low THD+N: 0.009%

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD660 DACPORT® is a complete 16-bit monolithic D/A converter with an on-board voltage reference, double buffered latches and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry.

The AD660's architecture ensures 15-bit monotonicity over time and temperature. Integral and differential nonlinearity is maintained at ±0.003% max. The on-chip output amplifier provides a voltage output settling time of 10 µs to within 1/2 LSB for a full-scale step.

The AD660 has an extremely flexible digital interface. Data can be loaded into the AD660 in serial mode or as two 8-bit bytes. This is made possible by two digital input pins which have dual functions. The serial mode input format is pin selectable to be MSB or LSB first. The serial output pin allows the user to daisy chain several AD660s by shifting the data through the input latch into the next DAC thus minimizing the number of control lines required to SIN, $\overline{CS}$ and LDAC. The byte mode input format is also flexible in that the high byte or low byte data can be loaded first. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system.

DACPORT is a registered trademark of Analog Devices, Inc.

ORDERING GUIDE

Model	Temperature Range	Linearity Error Max $T_{MIN} - T_{MAX}$	Package Option[1]
AD660AN	–40°C to +85°C	±4 LSB	N-24
AD660AR	–40°C to +85°C	±4 LSB	R-24
AD660BN	–40°C to +85°C	±2 LSB	N-24
AD660BR	–40°C to +85°C	±2 LSB	R-24
AD660SQ	–55°C to +125°C	±4 LSB	Q-24
AD660SQ/883B[2]	–55°C to +125°C	(Note 2)	(Note 2)

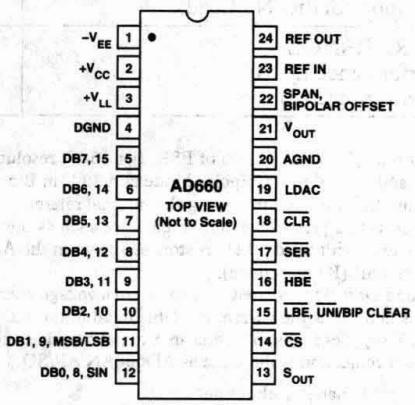
NOTES
[1]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[2]Refer to AD660/883B military data sheet.

The AD660 is available in five grades. AN and BN versions are specified from –40°C to +85°C and are packaged in a 24-pin 300 mil plastic DIP. AR and BR versions are also specified from –40°C to +85°C and are packaged in a 24-pin SOIC. The SQ version is packaged in a 24-pin 300 mil cerdip package and is also available compliant to MIL-STD-883. Refer to the AD660/883B data sheet for specifications and test conditions.

PRODUCT HIGHLIGHTS

1. The AD660 is a complete 16-bit DAC, with a voltage reference, double buffered latches and output amplifier on a single chip.
2. The internal buried Zener reference is laser trimmed to 10.000 volts with a ±0.1% maximum error and a temperature drift performance of ±15 ppm/°C. The reference is available for external applications.
3. The output range of the AD660 is pin programmable and can be set to provide a unipolar output range of 0 V to +10 V or a bipolar output range of –10 V to +10 V. No external components are required.
4. The AD660 is both dc and ac specified. DC specifications include ±1 LSB INL and ±1 LSB DNL errors. AC specifications include 0.009% THD+N and 83 dB SNR.

PIN CONNECTION



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AD660–SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = –15 V, V_{LL} = +5 V unless otherwise noted)

Parameter	AD660AN/AR/SQ Min	Typ	Max	AD660BN/BR Min	Typ	Max	Units
RESOLUTION	16			16			Bits
DIGITAL INPUTS (T_{MIN} to T_{MAX})							
V_{IH} (Logic "1")	2.0		5.5	*		*	Volts
V_{IL} (Logic "0")	0		0.8	*		*	Volts
I_{IH} (V_{IH} = 5.5 V)			±10			*	μA
I_{IL} (V_{IL} = 0 V)			±10			*	μA
TRANSFER FUNCTION CHARACTERISTICS[1]							
Integral Nonlinearity			±2			±1	LSB
T_{MIN} to T_{MAX}			±4			±2	LSB
Differential Nonlinearity			±2			±1	LSB
T_{MIN} to T_{MAX}			±4			±2	LSB
Monotonicity Over Temperature	14			15			Bits
Gain Error[2, 3]			±0.10			*	% of FSR
Gain Drift (T_{MIN} to T_{MAX})			25			15	ppm/°C
DAC Gain Error[4]			±0.05			*	% of FSR
DAC Gain Drift[4]			10			*	ppm/°C
Unipolar Offset			±2.5			*	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			3			*	ppm/°C
Bipolar Zero Error			±7.5			*	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			5			*	ppm/°C
REFERENCE INPUT							
Input Resistance	7	10	13	*	*	*	kΩ
Bipolar Offset Input Resistance	7	10	13	*	*	*	kΩ
REFERENCE OUTPUT							
Voltage	9.99	10.00	10.01	*	*	*	Volts
Drift			25			15	ppm/°C
External Current[5]	2	4		*	*		mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
OUTPUT CHARACTERISTICS							
Output Voltage Range							
Unipolar Configuration	0		+10	*		*	Volts
Bipolar Configuration	–10		+10	*		*	Volts
Output Current	5			*			mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
POWER SUPPLIES							
Voltage							
V_{CC}[6]	+13.5		+16.5	*		*	Volts
V_{EE}[6]	–13.5		–16.5	*		*	Volts
V_{LL}	+4.5		+5.5	*		*	Volts
Current (No Load)							
I_{CC}		+12	+18		*	*	mA
I_{EE}		–12	–18		*	*	mA
I_{LL}							
@ V_{IH}, V_{IL} = 5, 0 V		0.3	2		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4 V		3	7.5		*	*	mA
Power Supply Sensitivity		1	2		*	*	ppm/%
Power Dissipation (Static, No Load)		365	625		*	*	mW
TEMPERATURE RANGE							
Specified Performance (A, B)	–40		+85	*		*	°C
Specified Performance (S)	–55		+125				°C

NOTES

[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR. For 14-bit resolution, 1 LSB = 0.006% of FSR. FSR stands for Full-Scale Range and is 10 V in a Unipolar Mode and 20 V in Bipolar Mode.

[2]Gain error and gain drift are measured using the internal reference. The internal reference is the main contributor to gain drift. If lower gain drift is required, the AD660 can be used with a precision external reference such as the AD587, AD586 or AD688.

[3]Gain Error is measured with fixed 50 Ω resistors as shown in the Application section. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar mode) or 0.50% of FSR (Bipolar mode).

[4]DAC Gain Error and Drift are measured with an external voltage reference. They represent the error contributed by the DAC alone, for use with an external reference.

[5]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD660.

[6]Operation on ±12 V supplies is possible using an external reference such as the AD586 and reducing the output range. Refer to the Internal/External Reference section.

*Indicates that the specification is the same as AD660AN/AR/SQ.

Specifications subject to change without notice.

ANALOG DEVICES

Monolithic 12-Bit Quad DAC

AD664

FEATURES
Four Complete Voltage Output DACs
Data Register Readback Feature
"Reset to Zero" Override
Multiplying Operation
Double-Buffered Latches
Surface Mount and DIP Packages
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Automatic Test Equipment
Robotics
Process Control
Disk Drives
Instrumentation
Avionics

PRODUCT DESCRIPTION

The AD664 is four complete 12-bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double-buffered input latch structure and a data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accommodates 4-, 8- or 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response by the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, with a gain of one or two times the reference voltage. All DACs are operated from a single external reference.

The functional completeness of the AD664 results from the combination of Analog Devices' BiMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

PRODUCT HIGHLIGHTS

1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.
2. The output range of each DAC is fully and independently programmable.
3. Readback capability allows verification of contents of the internal data registers.
4. The asynchronous RESET control returns all D/A outputs to zero volts.
5. DAC-to-DAC matching performance is specified and tested.
6. Linearity error is specified to be 1/2 LSB at room temperature and 3/4 LSB maximum for the K, B and T grades.
7. DAC performance is guaranteed to be monotonic over the full operating temperature range.
8. Readback buffers have three-state outputs.
9. Multiplying-mode operation allows use with fixed or variable, positive or negative external references.
10. The AD664 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD664/883B data sheet for detailed specifications.

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ORDERING GUIDE

Model[1]	Temperature Range	Output Range	Gain Error	Linearity Error	Package Options[2]
AD664JN-UNI	0°C to +70°C	0 to $+V_{REF}$	±7 LSB	±0.75 LSB	N-28
AD664JN-BIP	0°C to +70°C	$-V_{REF}$ to $+V_{REF}$	±7 LSB	±0.75 LSB	N-28
AD664JP	0°C to +70°C	Programmable	±7 LSB	±0.75 LSB	P-44A
AD664KN-UNI	0°C to +70°C	0 to $+V_{REF}$	±5 LSB	±0.5 LSB	N-28
AD664KN-BIP	0°C to +70°C	$-V_{REF}$ to $+V_{REF}$	±5 LSB	±0.5 LSB	N-28
AD664KP	0°C to +70°C	Programmable	±5 LSB	±0.5 LSB	P-44A
AD664AD-UNI	–40°C to +85°C	0 to $+V_{REF}$	±7 LSB	±0.75 LSB	D-28
AD664AD-BIP	–40°C to +85°C	$-V_{REF}$ to $+V_{REF}$	±7 LSB	±0.75 LSB	D-28
AD664AJ	–40°C to +85°C	Programmable	±7 LSB	±0.75 LSB	J-44
AD664BD-UNI	–40°C to +85°C	0 to $+V_{REF}$	±5 LSB	±0.5 LSB	D-28
AD664BD-BIP	–40°C to +85°C	$-V_{REF}$ to $+V_{REF}$	±5 LSB	±0.5 LSB	D-28
AD664BJ	–40°C to +85°C	Programmable	±5 LSB	±0.5 LSB	J-44
AD664BE	–40°C to +85°C	Programmable	±5 LSB	±0.5 LSB	E-44A
AD664SD-UNI	–55°C to +125°C	0 to $+V_{REF}$	±7 LSB	±0.75 LSB	D-28
AD664SD-BIP	–55°C to +125°C	$-V_{REF}$ to $+V_{REF}$	±7 LSB	±0.75 LSB	D-28
AD664TD-UNI	–55°C to +125°C	0 to $+V_{REF}$	±5 LSB	±0.5 LSB	D-28
AD664TD-BIP	–55°C to +125°C	$-V_{REF}$ to $+V_{REF}$	±5 LSB	±0.5 LSB	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD664/883B data sheet.
[2]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier; J = Leaded Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

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AD664—SPECIFICATIONS (V_{LL} = +5 V, V_{CC} = +15 V, V_{EE} = −15 V, V_{REF} = +10 V, T_A = +25°C unless otherwise noted)

Model	JN/JP/AD/AJ/SD			KN/KP/BD/BJ/BE/TD/TE			Units
	Min	Typ	Max	Min	Typ	Max	
RESOLUTION		12	12		*	*	Bits
ANALOG OUTPUT							
Voltage Range[1]							
UNI Versions	0		V_{CC} − 2.0[2]	*		*	Volts
BIP Versions	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	*		*	Volts
Output Current	5			*			mA
Load Resistance		2			*		kΩ
Load Capacitance			500			*	pF
Short-Circuit Current		25	40		*	*	mA
ACCURACY							
Gain Error	**−7**	±3	7	**−5**	±2	5	LSB
Unipolar Offset	**−2**	±1/2	2	**−1**	±1/4	1	LSB
Bipolar Zero[3]	**−3**	±3/4	3	**−2**	±1/2	2	LSB
Linearity Error[4]	**−3/4**	±1/2	3/4	**−1/2**	±1/4	1/2	LSB
Linearity T_{MIN} to T_{MAX}	**−1**	±3/4	1	**−3/4**	±1/2	3/4	LSB
Differential Linearity	**−3/4**		3/4	**−1/2**		1/2	LSB
Differential Linearity T_{MIN} to T_{MAX}	**Monotonic @ All Temperatures**			**Monotonic @ All Temperatures**			
Gain Error Drift							
Unipolar 0 V to +10 V Mode	**−12**	±7	12	**−10**	±5	10	ppm of FSR[5]/°C
Bipolar −5 V to +5 V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Bipolar −10 V to +10 V Mode	**−12**	±7	12	**−10**	±5	10	ppm of FSR/°C
Unipolar Offset Drift							
Unipolar 0 V to +10 V Mode	**−3**	±1.5	3	**−2**	±1	2	ppm of FSR/°C
Bipolar Zero Drift							
Bipolar −5 V to +5 V Mode	−12	±7	12	−10	±5	10	ppm of FSR/°C
Bipolar −10 V to +10 V Mode	**−12**	±7	12	**−10**	±5	10	ppm of FSR/°C
REFERENCE INPUT							
Input Resistance	1.3		2. 6	*		*	kΩ
Voltage Range[6]	V_{EE} + 2.0[2]		V_{CC} − 2.0[2]	*		*	Volts
POWER REQUIREMENTS							
V_{LL}	**4.5**	5.0	5.5	*	*	*	Volts
I_{LL}							
@ V_{IH}, V_{IL} = 5 V, 0 V		0.1	**1**		*	*	mA
@ V_{IH}, V_{IL} = 2.4 V, 0.4 V		3	**6**		*	*	mA
V_{CC}/V_{EE}	**±11.4**		**±16.5**	*		*	Volts
I_{CC}		12	**15**		*	*	mA
I_{EE}		15	**19**		*	*	mA
Total Power		**400**	525		*	*	mW
ANALOG GROUND CURRENT[7]	−600	±400	+600	*	*	*	µA
MATCHING PERFORMANCE							
Gain[8]	**−6**	±3	6	**−4**	±2	4	LSB
Offset[9]	**−2**	±1/2	2	**−1**	±1/4	1	LSB
Bipolar Zero[10]	**−3**	±1	3	**−2**	±1	2	LSB
Linearity[11]	**−1.5**	±1/2	1.5	**−1**	±1/2	1	LSB
CROSSTALK							
Analog			−90			*	dB
Digital			−60			*	dB
DYNAMIC PERFORMANCE (R_L = 2 kΩ, C_L = 500 pF)							
Settling Time to ±1/2 LSB							
Off←Bits→On, GAIN = 1, V_{REF} = 10		8	10		*	*	µs
Settling Time to ±1/2 LSB							
−10←V_{REF}→10 V, GAIN = 1, Bits On		10			*		µs
Glitch Impulse			500			*	nV-sec
MULTIPLYING MODE PERFORMANCE							
Reference Feedthrough @ 1 kHz		−75			*		dB
Reference −3 dB Bandwidth		70			*		kHz
POWER SUPPLY GAIN SENSITIVITY							
11.4 V←V_{CC}→16.5 V		±2	±5		*	*	ppm/%
−16.5 V←V_{EE}→−11.4 V		±2	±5		*	*	ppm/%
4.5 V←V_{LL}→5.5 V		±2	±5		*	*	ppm/%

Specifications subject to change without notice.

ANALOG DEVICES

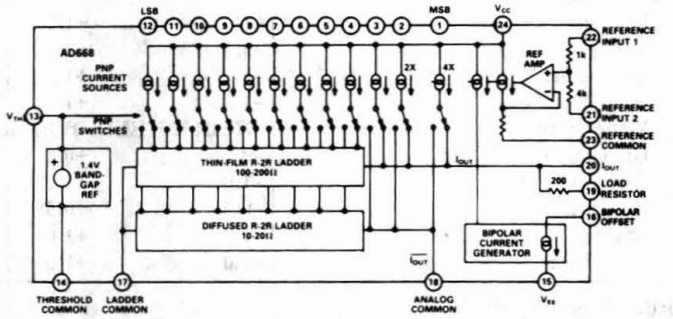
12-Bit Ultrahigh Speed Multiplying D/A Converter

AD668

FEATURES

Ultrahigh Speed: Current Settling to 1 LSB in 90 ns for a Full-Scale Change in Digital Input. Voltage Settling to 1 LSB in 120 ns for a Full-Scale Change in Analog Input
15 MHz Reference Bandwidth
Monotonicity Guaranteed over Temperature
10.24 mA Current Output or 1.024 V Voltage Output
Integral and Differential Linearity Guaranteed over Temperature
0.3" "Skinny DIP" Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD668 is an ultrahigh speed, 12-bit, multiplying digital-to-analog converter, providing outstanding accuracy and speed performance in responding to both analog and digital inputs. The AD668 provides a level of performance and functionality in a monolithic device that exceeds that of many contemporary hybrid devices. The part is fabricated using Analog Devices' Complementary Bipolar (CB) Process, which features vertical NPN and PNP devices on the same chip without the use of dielectric isolation. The AD668's design capitalizes on this proprietary process in combination with standard low impedance circuit techniques to provide its unique combination of speed and accuracy in a monolithic part.

The wideband reference input is buffered by a high gain, closed loop reference amplifier. The reference input is essentially a 1 V, high impedance input, but trimmed resistive dividers are provided to readily accommodate 5 V and 1.25 V references. The reference amplifier features an effective small signal bandwidth of 15 MHz and an effective slew rate of 3% of full scale/ns.

Multiple matched current sources and thin film ladder techniques are combined to produce bit weighting. The output range can nominally be taken as a 10.24 mA current output or a 1.024 V voltage output. Varying the analog input can provide modulation of the DAC full scale from 10% to 120% of its nominal value. Bipolar outputs can be realized through pin-strapping to provide two-quadrant operation without additional external circuitry.

Laser wafer trimming insures full 12-bit linearity and excellent gain accuracy. All grades of the AD668 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100 Ω ± 1.0%.

The AD668 is available in four performance grades. The AD668JQ and KQ are specified for operation from 0°C to +70°C, the AD668AQ is specified for operation from –40°C to +85°C, and the AD668SQ specified for operation from –55°C to +125°C. All grades are available in a 24-pin cerdip (0.3" package.

PRODUCT HIGHLIGHTS

1. The fast settling time of the AD668 provides suitable performance for waveform generation, graphics display, and high speed A/D conversion applications.
2. The high bandwidth reference channel allows high frequency modulation between analog and digital inputs.
3. The AD668's design is configured to allow wide variation of the analog input, from 10% to 120% of its nominal value.
4. The AD668's combination of high performance and tremendous flexibility makes it an ideal building block for a variety of high speed, high accuracy instrumentation applications.
5. The digital inputs are readily compatible with both TTL and 5 V CMOS logic families.

ORDERING GUIDE

Model[1]	Temperature Range	Linearity Error Max @ 25°C	Voltage Gain T.C. Max ppm/°C	Package Option[2]
AD668JQ	0°C to +70°C	±1/2	±30	Q-24
AD668KQ	0°C to +70°C	±1/4	±15	Q-24
AD668AQ	–40°C to +85°C	±1/2	±30	Q-24
AD668SQ	–55°C to +125°C	±1/2	±40	Q-24

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD668/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.

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AD668—SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +15 V, V_{EE} = –15 V, unless otherwise noted)

Parameter	AD668J/A Min	AD668J/A Typ	AD668J/A Max	AD668K Min	AD668K Typ	AD668K Max	AD668S Min	AD668S Typ	AD668S Max	Units
RESOLUTION	12			12			12			Bits
LSB WEIGHT (At Nominal FSR)										
Current		2.5			*			*		μA
Voltage (Current into R_L)		250			*			*		μV
ACCURACY[1]										
Linearity	–1/2		+1/2	–1/4		+1/4	*		*	LSB
T_{MIN} to T_{MAX}	–3/4		+3/4	–1/2		+1/2	*		*	LSB
Differential Nonlinearity	–1		+1	–1/2		+1/2	*		*	LSB
T_{MIN} to T_{MAX}	–1		+1	–1/2		+1/2	*		*	LSB
Monotonicity	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE									
Unipolar Offset (Digital)	–0.2		+0.2	*		*	*		*	% of FSR
Bipolar Offset	–1.0		+1.0	–0.6		+0.6	*		*	% of FSR
Bipolar Zero	–0.5		+0.5	–0.2		+0.2	*		*	% of FSR
Analog Offset	–1.0		+1.0	–0.7		+0.7	*		*	% of V_{NOM}
Gain Error	–1.0		+1.0	*		*	*		*	% of FSR
REFERENCE INPUT										
Input Resistance										
5.0 V Range		5			*			*		kΩ
1.25 V Range		5			*			*		kΩ
1.0 V Range		1			*			*		MΩ
Reference Range (T_{MIN} to T_{MAX})	10	100	120	*	*	*	*	*	*	% of V_{NOM}
CODING	BINARY, OFFSET BINARY									
CURRENT OUTPUT RANGES	0 to 10.24, ± 5.12									mA
VOLTAGE OUTPUT RANGES	0 to 1.024, ± 0.512									V
OUTPUT COMPLIANCE	–2		+1.2	*		*	*		*	V
OUTPUT RESISTANCE										
Exclusive of R_L	160	200	240	*	*	*	*	*	*	Ω
Inclusive of R_L	99	100	101	*	*	*	*	*	*	Ω
REFERENCE AMPLIFIER										
Input Bias Current		1.5			*			*		μA
Slew Rate		3			*			*		% of FS/ns
Large Signal Bandwidth		10			*			*		MHz
Small Signal Bandwidth		15			*			*		MHz
Undervoltage Recovery Time										
V_{REF}/V_{NOM} to 0%		35			*			*		ns
AC CHARACTERISTICS										
Analog Settling Time										
(10% to 120% Step)										
to ±1%		60			*			*		ns to 1% of FSR
to ±0.1%		90			*			*		ns to 0.1% of FSR
to ±0.025%		120			*			*		ns to 0.025% of FSR
Digital Settling Time										
Current										
to ±1%		30			*			*		ns to 1% of FSR
to ±0.025%		90			*			*		ns to 0.025% of FSR
Voltage (100 Ω Internal R_L)[3]										
to 1%		50			*			*		ns to 1% of FSR
to 0.1%		75			*			*		ns to 0.1% of FSR
to 0.025%		110			*			*		ns to 0.025% of FSR
Glitch Impulse[4]		350			*			*		pV-sec
Peak Amplitude		20			*			*		% of FSR
Total Harmonic Distortion[5]		–75			*			*		dB
Multiplying Feedthrough Error[6]		–62			*			*		dB

NOTES
*Same as AD668J/A
Specifications subject to change without notice.

Monolithic 16-Bit DACPORT

AD669

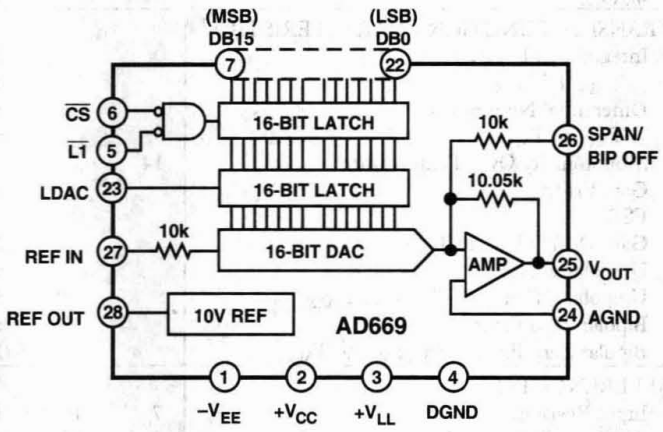
FEATURES

Complete 16-Bit D/A Function
- **On-Chip Output Amplifier**
- **High Stability Buried Zener Reference**

Monolithic BiMOS II Construction
±1 LSB Integral Linearity Error
15-Bit Monotonic over Temperature
Microprocessor Compatible
- **16-Bit Parallel Input**
- **Double-Buffered Latches**

Fast 40 ns Write Pulse
Unipolar or Bipolar Output
Low Glitch: 15 nV-s
Low THD+N: 0.009%
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD669 DACPORT® is a complete 16-bit monolithic D/A converter with an on-board reference and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD669 chip includes current switches, decoding logic, an output amplifier, a buried Zener reference and double-buffered latches.

The AD669's architecture insures 15-bit monotonicity over temperature. Integral nonlinearity is maintained at ±0.003%, while differential nonlinearity is ±0.003% max. The on-chip output amplifier provides a voltage output settling time of 10 µs to within 1/2 LSB for a full-scale step.

Data is loaded into the AD669 in a parallel 16-bit format. The double-buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system. Three TTL/LSTTL/5 V CMOS compatible signals control the latches: $\overline{CS}$, $\overline{L1}$ and LDAC.

The output range of the AD669 is pin programmable and can be set to provide a unipolar output range of 0 V to +10 V or a bipolar output range of –10 V to +10 V.

The AD669 is available in seven grades: AN and BN versions are specified from –40°C to +85°C and are packaged in a 28-pin plastic DIP. The AR and BR versions are specified for –40°C to +85°C operation and are packaged in a 28-pin SOIC. The SQ version is specified from –55°C to +125°C and is packaged in a hermetic 28-pin cerdip package. The AD669 is also available compliant to MIL-STD-883. Refer to the AD669/883B data sheet for specifications and test conditions.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The AD669 is a complete voltage output 16-bit DAC with voltage reference and digital latches on a single IC chip.
2. The internal buried Zener reference is laser trimmed to 10.000 volts with a ±0.2% maximum error. The reference voltage is also available for external applications.
3. The AD669 is both dc and ac specified. DC specs include ±1 LSB INL error and ±1 LSB DNL error. AC specs include 0.009% THD+N and 83 dB SNR. The ac specifications make the AD669 suitable for signal generation applications.
4. The double-buffered latches on the AD669 eliminate data skew errors while allowing simultaneous updating of DACs in multi-DAC systems.
5. The output range is a pin-programmable unipolar 0 V to +10 V or bipolar –10 V to +10 V output. No external components are necessary to set the desired output range.
6. The AD669 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD669/883B data sheet for detailed specifications.

ORDERING GUIDE

Model	Temperature Range	Linearity Error Max T_{MIN}–T_{MAX}	Gain TC max ppm/°C	Package Description	Package Option*
AD669AN	–40°C to +85°C	±4 LSB	25	Plastic DIP	N-28
AD669AR	–40°C to +85°C	±4 LSB	25	SOIC	R-28
AD669BN	–40°C to +85°C	±2 LSB	15	Plastic DIP	N-28
AD669BR	–40°C to +85°C	±2 LSB	15	SOIC	R-28
AD669AQ	–40°C to +85°C	±4 LSB	15	Cerdip	Q-28
AD669BQ	–40°C to +85°C	±2 LSB	15	Cerdip	Q-28
AD669SQ	–55°C to +125°C	±4 LSB	15	Cerdip	Q-28
AD669/883B**	–55°C to +125°C	**	**	**	**

NOTES
*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
**Refer to AD669/883B military data sheet.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD669–SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +15 V, V_{EE} = –15 V, V_{LL} = +5 V, unless otherwise noted)

Model	AD669AN/AR Min	AD669AN/AR Typ	AD669AN/AR Max	AD669AQ/SQ Min	AD669AQ/SQ Typ	AD669AQ/SQ Max	AD669BN/BQ/BR Min	AD669BN/BQ/BR Typ	AD669BN/BQ/BR Max	Units
RESOLUTION	16			16			16			Bits
DIGITAL INPUTS (T_{MIN} to T_{MAX})										
V_{IH} (Logic "1")	**2.0**		**5.5**	*		*	*		*	Volts
V_{IL} (Logic "0")	**0**		**0.8**	*		*	*		*	Volts
I_{IH} (V_{IH} = 5.5 V)			**±10**			*			*	µA
I_{IL} (V_{IL} = 0 V)			**±10**			*			*	µA
TRANSFER FUNCTION CHARACTERISTICS[1]										
Integral Nonlinearity			**±2**			*			**±1**	LSB
T_{MIN} to T_{MAX}			**±4**			*			**±2**	LSB
Differential Nonlinearity			**±2**			*			**±1**	LSB
T_{MIN} to T_{MAX}			**±4**			*			**±2**	LSB
Monotonicity Over Temperature	**14**			**14**			**15**			Bits
Gain Error[2, 5]			**±0.15**			**±0.10**			**±0.10**	% of FSR
Gain Drift[2] (T_{MIN} to T_{MAX})			**25**			**15**			**15**	ppm/°C
Unipolar Offset			**±5**			**±5**			**±2.5**	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			**5**			**3**			**3**	ppm/°C
Bipolar Zero Error			**±15**			**±15**			**±10**	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			**12**			**10**			**5**	ppm/°C
REFERENCE INPUT										
Input Resistance	7	10	13	*	*	*	*	*	*	kΩ
Bipolar Offset Input Resistance	7	10	13	*	*	*	*	*	*	kΩ
REFERENCE OUTPUT										
Voltage	**9.98**	10.00	**10.02**	*	*	*	*	*	*	Volts
Drift			**25**			**15**			**15**	ppm/°C
External Current[3]	2	4		*	*		*	*		mA
Capacitive Load			1000			*			*	pF
Short Circuit Current		25			*			*		mA
OUTPUT CHARACTERISTICS										
Output Voltage Range										
Unipolar Configuration	0		+10	*		*	*		*	Volts
Bipolar Configuration	–10		+10	*		*	*		*	Volts
Output Current	5			*			*			mA
Capacitive Load			1000			*			*	pF
Short Circuit Current		25			*			*		mA
POWER SUPPLIES										
Voltage										
V_{CC}[4]	**+13.5**		**+16.5**	*		*	*		*	Volts
V_{EE}[4]	**–13.5**		**–16.5**	*		*	*		*	Volts
V_{LL}	**+4.5**		**+5.5**	*		*	*		*	Volts
Current (No Load)										
I_{CC}		+12	**+18**		*	*		*	*	mA
I_{EE}		–12	**–18**		*	*		*	*	mA
I_{LL}										
@ V_{IH}, V_{IL} = 5, 0 V		0.3	**2**		*	*		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4 V		3	**7.5**		*	*		*	*	mA
Power Supply Sensitivity		1	**3**		*	*		*	*	ppm/%
Power Dissipation (Static, No Load)		365	625		*			*		mW
TEMPERATURE RANGE										
Specified Performance (A, B)	–40		+85	–40		+85	–40		+85	°C
Specified Performance (S)				–55		+125				°C

NOTES

[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR = 15 ppm of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR = 30 ppm of FSR. For 14-bit resolution 1 LSB = 0.006% of FSR = 60 ppm of FSR. FSR stands for Full-Scale Range and is 10 V for a 0 V to + 10 V span and 20 V for a –10 V to +10 V span.

[2]Gain error and gain drift measured using the internal reference. Gain drift is primarily reference related. See the Using the AD669 with the AD688 Reference section for further information.

[3]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD669.

[4]Operation on ±12 V supplies is possible using an external reference like the AD586 and reducing the output range. Refer to the Internal/External Reference Use section.

[5]Measured with fixed 50 Ω resistors. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar Mode) or 0.50% of FSR (Bipolar Mode). Refer to the Analog Circuit Connections section.

*Same as AD669AN/AR specification.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Those shown in **boldface** are tested on all production units.

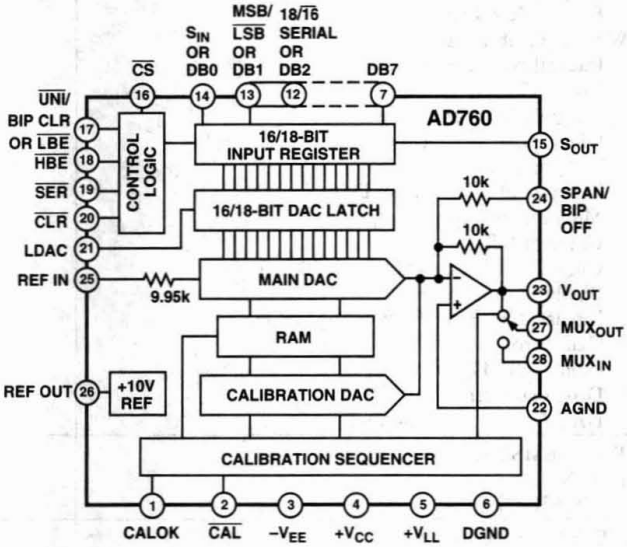
16/18-Bit Self-Calibrating Serial/Byte DACPORT

AD760

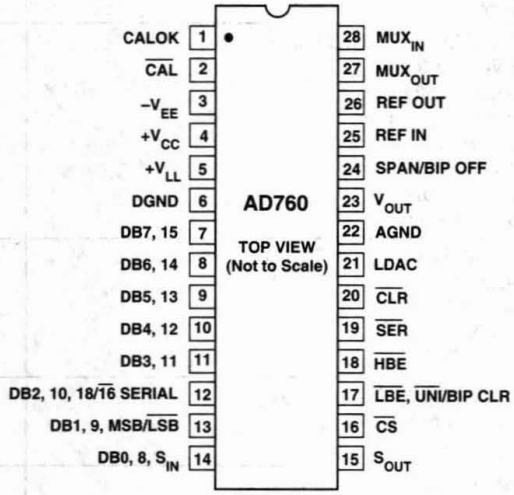
FEATURES

±0.2 LSB (±0.00031%) Typ Peak DNL and INL
±0.5 LSB (±0.00076%) Typ Unipolar Offset, Bipolar Zero
17-Bit Monotonicity Guaranteed
18-Bit Resolution (in Serial Mode)
Complete 16/18-Bit D/A Function
On-Chip Output Amplifier
On-Chip Buried Zener Voltage Reference
Microprocessor Compatible
Serial or Byte Input
Double Buffered Latches
Asynchronous Clear Function
Serial Output Pin Facilitates Daisy Chaining
Pin Strappable Unipolar or Bipolar Output
Low THD+N: 0.005%
MUX Output Control on Power-Up and Supply Glitches

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
DIP



PRODUCT DESCRIPTION

The AD760 is a complete 16/18-bit self-calibrating monolithic DAC (DACPORT®) with onboard voltage reference, double buffered latches and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry.

Self-calibration is initiated by simply pulsing the $\overline{CAL}$ pin low. The CALOK pin indicates when calibration has been successfully completed. The output multiplexer (MUX_{OUT}) can be used to send the output to the bottom of the output range during calibration.

Data can be loaded into the AD760 as straight binary, serial data or as two 8-bit bytes. In serial mode, 16-bit or 18-bit data can be used and the serial mode input format is pin selectable, to be MSB or LSB first. This is made possible by three digital input pins which have dual functions (Pins 12, 13, and 14). In byte mode the user can similarly define whether the high byte or low byte is loaded first. The serial output (S_{OUT}) pin allows the user to daisy chain several AD760s by shifting the data through the input latch into the next DAC thus minimizing the number of control lines required in a multiple DAC application. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system.

The asynchronous $\overline{CLR}$ function can be configured to clear the output to minus full-scale or midscale depending on the state of Pin 17 when $\overline{CLR}$ is strobed. The AD760 also powers up with the MUX output in a predetermined state by means of a digital and analog power supply detection circuit. This is particularly useful for robotic and industrial control applications.

The AD760 is available in a 28-pin, 600 mil cerdip package. The AQ version is specified from –40°C to +85°C.

DACPORT is a registered trademark of Analog Devices, Inc.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD760AQ	–40°C to +85°C	Cerdip	Q-28

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD760—SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +15 V, V_{EE} = –15 V, V_{LL} = + 5 V, unless otherwise noted)

Model	AD760AQ Min	Typ	Max	Units
RESOLUTION	16/18			Bits
TRANSFER FUNCTION CHARACTERISTICS				
With Calibration @ T_{CAL}; –40°C ≤ T_{CAL} ≤ +85°C				
Integral Nonlinearity		±0.2	±0.75	16-Bit LSB
Differential Nonlinearity		±0.2	±0.5	16-Bit LSB
Monotonicity	17	18		Bits
Unipolar Offset		±0.5	±1	16-Bit LSB
Bipolar Zero Error		±0.5	±1	16-Bit LSB
Without Calibration				
Integral Nonlinearity			±2	16-Bit LSB
T_{MIN} to T_{MAX}			±4	16-Bit LSB
Integral Nonlinearity Drift		0.015		16-Bit LSB/°C
Differential Nonlinearity			±2	16-Bit LSB
T_{MIN} to T_{MAX}			±4	16-Bit LSB
Differential Nonlinearity Drift		0.015		16-Bit LSB/°C
Monotonicity Over Temperature	14			Bits
Unipolar Offset			±2.5	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			3	ppm/°C
Bipolar Zero Error			±10	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			5	ppm/°C
Gain Error			±0.10	% of FSR
Gain Drift (T_{MIN} to T_{MAX})			25	ppm/°C
DAC Gain Error			±0.05	% of FSR
DAC Gain Drift (T_{MIN} to T_{MAX})			10	ppm/°C
INPUT RESISTANCE				
REFIN	7	10	13	kΩ
SPAN/BIP OFF	7	10	13	kΩ
REFERENCE OUTPUT				
Voltage	9.99	10.00	10.01	V
Drift			25	ppm/°C
External Current	2	4		mA
Capacitive Load			1000	pF
Short Circuit Current		25		mA
Long-Term Stability		50		ppm/1000 Hrs
OUTPUT CHARACTERISTICS				
Output Voltage Range				
Unipolar Configuration	0		+10	V
Bipolar Configuration	–10		+10	V
Output Current	5			mA
Capacitive Load			1000	pF
Short Circuit Current		25		mA
MUX_{OUT} Resistance	0.9		7	kΩ
DIGITAL INPUTS (T_{MIN} to T_{MAX})				
V_{IH} (Logic "1")	2.0		V_{LL}	V
V_{IL} (Logic "0")	0		0.8	V
I_{IH} (V_{IH} = V_{LL})			±10	µA
I_{IL} (V_{IL} = 0 V)			±10	µA
DIGITAL OUTPUT (T_{MIN} to T_{MAX})				
V_{OH} (I_{OH} = –0.6 mA)	2.4			V
V_{OL} (I_{OL} = 1.6 mA)			0.4	V
POWER SUPPLIES				
Voltage				
V_{CC}	+14.25		+15.75	V
V_{EE}	–15.75		–14.25	V
V_{LL}	+4.75		+5.25	V
Current (No Load)				
I_{CC}		+18	+21	mA
I_{EE}	–21	–18		mA
I_{LL}				
@ V_{IH}, V_{IL} = 5.0 V, 0 V		2	3	mA
@ V_{IH}, V_{IL} = 2.4 V, 0.4 V		3	7.5	mA
Power Supply Sensitivity with V_{OUT} = 10 V			1	ppm/%
Power Dissipation (Static, No Load)		600	725	mW
TEMPERATURE RANGE				
Specified Performance (A)	–40		+85	°C

Specifications subject to change without notice.

ANALOG DEVICES

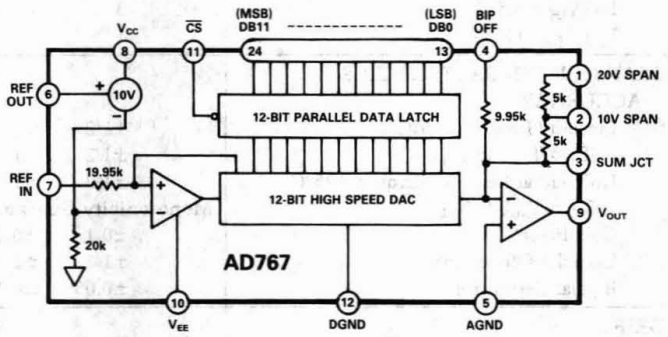
Microprocessor-Compatible 12-Bit D/A Converter

AD767*

FEATURES

Complete 12-Bit D/A Function
On-Chip Output Amplifier
High Stability Buried Zener Reference
Fast 40 ns Write Pulse
0.3" Skinny DIP and PLCC Packages
Single Chip Construction
Monotonicity Guaranteed Over Temperature
Settling Time: 3 μs max to 1/2 LSB
Guaranteed for Operation with ±12 V or ±15 V Supplies
TTL/5 V CMOS Compatible Logic Inputs
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD767 is a complete voltage output 12-bit digital-to-analog converter including a high stability buried Zener reference and input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser-trimmed thin-film resistor network to provide high accuracy.

Microprocessor compatibility is achieved by the on-chip latch. The design of the input latch allows direct interface to 12-bit buses. The latch responds to strobe pulses as short as 40 ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance of the AD767 result from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology.

The subsurface (buried) Zener diode on the chip provides a low noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim the absolute value of the reference as well as its temperature coefficient. The AD767 is thus well suited for wide temperature range performance with ±1/2 LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full-scale gain T.C. is 5 ppm/°C.

***Protected by U.S. Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground ..... 0 V to +18 V
V_{EE} to Power Ground ..... 0 V to –18 V
Digital Inputs (Pins 11, 13–24)
to Power Ground ..... –1.0 V to +7.0 V
Ref In to Reference Ground ..... ±12 V
Bipolar Offset to Reference Ground ..... ±12 V
10 V Span R to Reference Ground ..... ±12 V
20 V Span R to Reference Ground ..... ±24 V
Ref Out, V_{OUT} (Pins 6, 9) ... Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation ..... 1000 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Package	Temperature Range °C	Linearity Error Max T_{MIN}–T_{MAX}	Gain T.C. Max ppm/°C
AD767JN	Plastic DIP (N-24)	0 to +70	±1 LSB	30
AD767JP	PLCC (P-28A)	0 to +70	±1 LSB	30
AD767KN	Plastic DIP (N-24)	0 to +70	±1/2 LSB	15
AD767KP	PLCC (P-28A)	0 to +70	±1/2 LSB	15
AD767AD	Ceramic DIP (D-24A)	–25 to +85	±1 LSB	30
AD767BD	Ceramic DIP (D-24A)	–25 to +85	±1/2 LSB	15
AD767SD/883B	Ceramic DIP (D-24A)	–55 to +125	Note 2	Note 2
AD767ACHIPS	N/A	–25 to +85	±1 LSB	30

NOTES
[1]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[2]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD767/883B data sheet.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD767—SPECIFICATIONS (T_A = +25°C, ±15 volt power supplies, Unipolar Mode, unless otherwise noted.)

Model	AD767J/A/S[1]			AD767K/B			AD767A[2] Chips			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIGITAL INPUTS										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible, T_{MIN}–T_{MAX})[3]										
V_{IH} (Logic "1")	**+2.0**		+5.5	**+2.0**		+5.5	**+2.0**		+5.5	V
V_{IL} (Logic "0") J, K, A, B	0		**+0.8**	0		**+0.8**	0		**+0.8**	V
V_{IL} (Logic "0") S	0		**+0.7**							V
I_{IH} (V_{IH} = 5.5 V)		3	**10**		3	**10**		3	**10**	µA
I_{IL} (V_{IL} = 0.8 V)		1	5		1	5		1	5	µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/2	**±1**		±1/8	**±1/2**		±1/2	**±1**	LSB
T_A = T_{MIN} to T_{MAX}		±1/2	**±1**		±1/4	**±1/2**		±1/2	**±1**	LSB
Differential Linearity Error @ +25°C		±1/2	**±1**		±1/4	**±1**		±1/2	**±1**	LSB
T_A = T_{MIN} to T_{MAX}	**Monotonicity Guaranteed**			**Monotonicity Guaranteed**			**Monotonicity Guaranteed**			LSB
Gain Error[4]		±0.1	**±0.2**		±0.1	**±0.2**		±0.1	**±0.2**	% of FSR[5]
Unipolar Offset Error[4]		±1	**±2**		±1	**±2**		±1	**±2**	LSB
Bipolar Zero Error[4]		±0.05	**±0.1**		±0.05	**±0.1**		±0.05	**±0.1**	% of FSR
DRIFT										
Gain T_A = 25°C to T_{MIN} or T_{MAX}		±5	±30		±5	±15		±5	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{MIN} or T_{MAX}		±1	±3		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Zero T_A = 25°C to T_{MIN} or T_{MAX}		±5	±10			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for										
FSR change (2 kΩ‖500 pF Load)										
with 10 kΩ Feedback		3	4		3	4		3	4	µs
with 5 kΩ Feedback		2	3		2	3		2	3	µs
For LSB Change		1			1			1		µs
Slew Rate	10			10			10			V/µs
ANALOG OUTPUT										
Ranges[6]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (DC)		0.05			0.05			0.05		Ω
Short-Circuit Current			40			40			40	mA
REFERENCE OUTPUT	**9.90**	10.00	**10.10**	**9.90**	10.00	**10.10**	**9.90**	10.00	**10.10**	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 to +16.5 V dc		5	**10**		5	**10**		5	**10**	ppm of FS/%
V_{EE} = –11.4 to –16.5 V dc		5	**10**		5	**10**		5	**10**	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±12, ±15			±12, ±15			±12, ±15		V
Range[6]	**±11.4**		**±16.5**	**±11.4**		**±16.5**	**±11.4**		**±16.5**	V
Supply Current										
+11.4 to +16.5 V dc		9	**13**		9	**13**		9	**13**	mA
–11.4 to –16.5 V dc		18	**23**		18	**23**		18	**23**	mA
Total Power Consumption		400	600		400	600		400	600	mW
TEMPERATURE RANGE										
J/K	0		+70	0		+70				°C
A/B	–25		+85	–25		+85	–25		+85	°C
S	–55		+125	–55		+125				°C
Operating	–55		+125	–55		+125				°C
Storage (All Grades)	–65		+125	–65		+125	–65		+125	°C

NOTES

[1]AD767 "S" specifications shown for information only. Consult Analog Devices Military Databook or contact factory for a controlled specification sheet.

[2]AD767A Chips specifications are tested at +25°C and, when in boldface, at +85°C. They are typical at –25°C.

[3]The digital input specifications are 100% tested at +25°C, and guaranteed but not tested over the full temperature range.

[4]Adjustable to zero.

[5]FSR means "Full-Scale Range" and is 20 V for ±10 V range and 10 V for the ±5 V range.

[6]A minimum power supply of ±12.5 V is required for a ±10 V full-scale output and ±11.4 V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test (except per Notes 1 and 2). Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ANALOG DEVICES

16-Bit, 30 MSPS D/A Converter

AD768

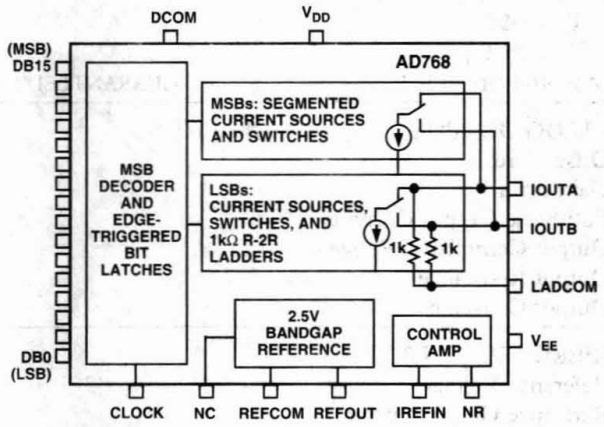
FEATURES

30 MSPS Update Rate
16-Bit Resolution
Linearity: 1/2 LSB DNL @ 14 Bits
1 LSB INL @ 14 Bits
Fast Settling: 25 ns Full-Scale Settling to 0.025%
SFDR @ 1 MHz Output: 86 dBc
THD @ 1 MHz Output: 71 dBc
Low Glitch Impulse: 35 pV-s
Power Dissipation: 465 mW
On-Chip 2.5 V Reference
Edge-Triggered Latches
Multiplying Reference Capability

APPLICATIONS

Arbitrary Waveform Generation
Communications Waveform Reconstruction
Vector Stroke Display

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD768 is a 16-bit, high speed digital-to-analog converter (DAC) that offers exceptional ac and dc performance. The AD768 is manufactured on ADI's Advanced Bipolar CMOS (ABCMOS) process, combining the speed of bipolar transistors, the accuracy of laser-trimmable thin film resistors, and the efficiency of CMOS logic. A segmented current source architecture is combined with a proprietary switching technique to reduce glitch energy and maximize dynamic accuracy. Edge triggered input latches and a temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution.

The AD768 is a current-output DAC with a nominal full-scale output current of 20 mA and a 1 kΩ output impedance. Differential current outputs are provided to support single-ended or differential applications. The current outputs may be tied directly to an output resistor to provide a voltage output, or fed to the summing junction of a high speed amplifier to provide a buffered voltage output. Also, the differential outputs may be interfaced to a transformer or differential amplifier.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD768 can be driven by the on-chip reference or by a variety of external reference voltages based on the selection of an external resistor. An external capacitor allows the user to optimally trade off reference bandwidth and noise performance.

The AD768 operates on ±5 V supplies, typically consuming 465 mW of power. The AD768 is available in a 28-pin SOIC package and is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The low glitch and fast settling time provide outstanding dynamic performance for waveform reconstruction or digital synthesis requirements, including communications.
2. The excellent dc accuracy of the AD768 makes it suitable for high speed A/D conversion applications.
3. On-chip, edge-triggered input CMOS latches interface readily to CMOS logic families. The AD768 can support update rates up to 40 MSPS.
4. A temperature compensated, 2.5 V bandgap reference is included on-chip allowing for generation of the reference input current with the use of a single external resistor. An external reference may also be used.
5. The current output(s) of the AD768 may be used singly or differentially, either into a load resistor, external op amp summing junction or transformer.
6. Proper selection of an external resistor and compensation capacitor allow the performance-conscious user to optimize the AD768 reference level and bandwidth for the target application.

ORDERING GUIDE

Model	Package Description	Package Option*
AD768AR	28-Pin 300 mil SOIC	R-28
AD768ACHIPS	Die	
AD768-EB	AD768 Evaluation Board	

*For outline information see Package Information section.

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AD768–SPECIFICATIONS

(T_{MIN} to T_{MAX}, V_{DD} = +5.0 V, V_{EE} = –5.0 V, LADCOM, REFCOM, DCOM = 0 V, IREFIN = 5 mA, CLOCK = 10 MHz, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	16			Bits
DC ACCURACY[1]				
Linearity Error				
T_A = +25°C	–8	±4	+8	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Differential Nonlinearity				
T_A = +25°C	–6	±2	+6	LSB
T_{MIN} to T_{MAX}	–8		+8	LSB
Monotonicity (13-Bit)	GUARANTEED OVER RATED SPECIFICATION TEMPERATURE RANGE			
ANALOG OUTPUT				
Offset Error	–0.2		+0.2	% of FSR
Gain Error	–1.0		+1.0	% of FSR
Full-Scale Output Current[2]		20		mA
Output Compliance Range	–1.2		+5.0	V
Output Resistance	0.8	1.0	1.2	kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	2.475	2.5	2.525	V
Reference Output Current[3]		+5.0	+15	mA
REFERENCE INPUT				
Reference Input Current	1	5	7	mA
Reference Bandwidth (IBEF = 4 mA ±2 mA)		9		MHz
DYNAMIC PERFORMANCE[7]				
Maximum Output Update Rate	30	40		MSPS
Output Settling Time (t_{ST}) (to 0.025%)		25	35	ns
Output Propagation Delay (t_{PD})		10		ns
Glitch Impulse		35		pV-s
Output Rise Time (10% to 90%)		5		ns
Output Fall Time (10% to 90%)		5		ns
Output Noise (DB0–DB15 High, into 50 Ω)		3		nV/√Hz
AC LINEARITY[7]				
Spurious-Free Dynamic Range (SFDR)				
F_{OUT} = 1.002 MHz; CLOCK = 10 MHz; 2 MHz Span		86	–79	dB
F_{OUT} = 1.002 MHz; CLOCK = 20 MHz; 2 MHz Span		85		dB
F_{OUT} = 5.002 MHz; CLOCK = 30 MHz; 10 MHz Span		78		dB
Total Harmonic Distortion (THD)				
F_{OUT} = 1.002 MHz; CLOCK = 10 MHz		–71	–68	dB
F_{OUT} = 1.002 MHz; CLOCK = 20 MHz		–66		dB
F_{OUT} = 5.002 MHz; CLOCK = 30 MHz		–61		dB

Specifications subject to change without notice.

WAFER TEST LIMITS (T_A = +25°C, V_{DD} = +5.0 V, V_{EE} = –5.0 V, I_{REFIN} = 5 mA, unless otherwise noted)

Parameter	AD768ACHIPS Limit	Units
Integral Nonlinearity[2]	±8	LSB max
Differential Nonlinearity[2]	±6	LSB max
Offset Error	±0.2	% FSR max
Gain Error	±1.0	% FSR max
Reference Voltage	±1.0	% of nom. 2.5 V max
Positive Supply Current	40	mA max
Negative Supply Current	73	mA max
Power Dissipation	600	mW max

ANALOG DEVICES

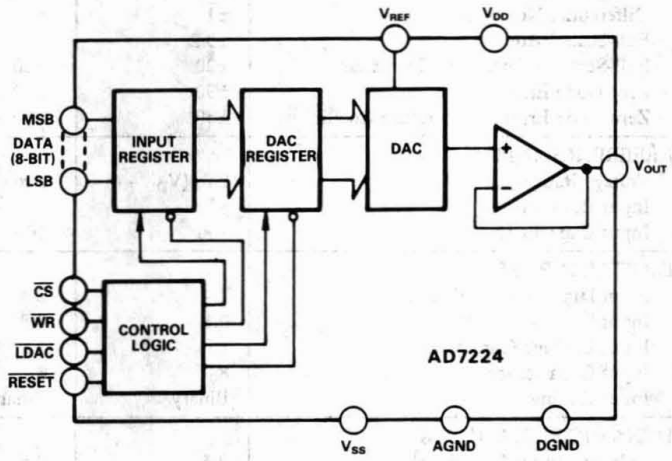
LC²MOS 8-Bit DAC with Output Amplifier

AD7224

FEATURES

8-Bit CMOS DAC with Output Amplifiers
Operates with Single or Dual Supplies
Low Total Unadjusted Error:
Less Than 1 LSB Over Temperature
Extended Temperature Range Operation
µP-Compatible with Double Buffered Inputs
Standard 18-Pin DIPs, and 20-Terminal Surface Mount Package and SOIC Package

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD7224 is a precision 8-bit voltage-output, digital-to-analog converter, with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers–an input register and a DAC register. Only the data held in the DAC registers determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224s. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5 V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 V to +12.5 V when using dual supplies. The part is also specified for single supply operation using a reference of +10 V. The output amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35 mW typical with single supply).
2. Low Total Unadjusted Error
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC²MOS) process coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1 LSB over the full operating temperature range.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7224KN	–40°C to +85°C	±2 max	N-18
AD7224LN	–40°C to +85°C	±1 max	N-18
AD7224KP	–40°C to +85°C	±2 max	P-20A
AD7224LP	–40°C to +85°C	±1 max	P-20A
AD7224KR-1	–40°C to +85°C	±2 max	R-20
AD7224LR-1	–40°C to +85°C	±1 max	R-20
AD7224KR-18	–40°C to +85°C	±2 max	R-18
AD7224LR-18	–40°C to +85°C	±1 max	R-18
AD7224BQ	–40°C to +85°C	±2 max	Q-18
AD7224CQ	–40°C to +85°C	±1 max	Q-18
AD7224TQ	–55°C to +125°C	±2 max	Q-18
AD7224UQ	–55°C to +125°C	±1 max	Q-18
AD7224TE	–55°C to +125°C	±2 max	E-20A
AD7224UE	–55°C to +125°C	±1 max	E-20A

NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

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AD7224–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4 V to 16.5 V, V_{SS} = –5 V ± 10%; AGND = DGND = 0 V; V_{REF} = +2 V to (V_{DD} – 4 V)[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15 V ± 5%, V_{REF} = +10 V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±3/2	±1	LSB max	
Full-Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14 V to 16.5 V, V_{REF} = +10 V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±50	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	V min to V max	
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1s.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]				
Positive Full-Scale Change	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Negative Full-Scale Change	7	7	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough	50	50	nV secs typ	V_{REF} = 0 V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V min/V max	For Specified Performance
V_{SS} Range	4.5/5.5	4.5/5.5	V min/V max	For Specified Performance
I_{DD}				
@ 25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{MIN} to T_{MAX}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}				
@ 25°C	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{MIN} to T_{MAX}	5	5	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3, 4]				
t_1				
@ 25°C	90	90	ns min	Chip Select/Load DAC Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_2				
@ 25°C	90	90	ns min	Write/Reset Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_3				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_4				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_5				
@ 25°C	90	90	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	ns min	
t_6				
@ 25°C	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	ns min	

NOTES

[1]Maximum possible reference voltage.

[2]Temperature ranges are as follows:
K, L Versions: –40°C to +85°C
B, C Versions: –40°C to +85°C
T, U Versions: –55°C to +125°C

[3]Sample Tested at 25°C by Product Assurance to ensure compliance.

[4]Switching characteristics apply for single and dual supply operation.

Specifications subject to change without notice.

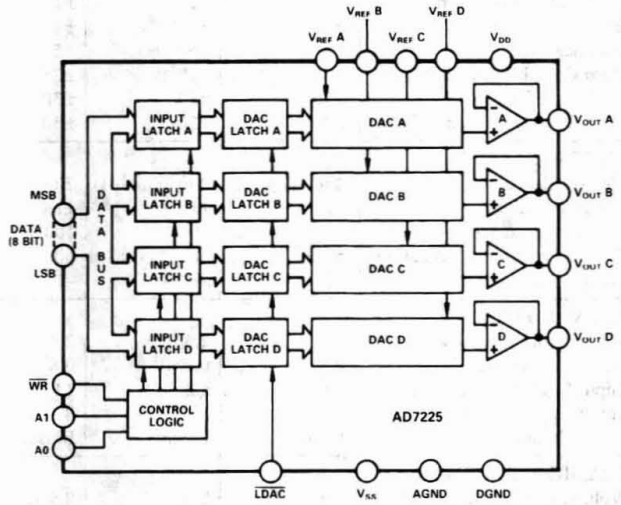
LC²MOS Quad 8-Bit DAC with Separate Reference Inputs

AD7225

FEATURES

- Four 8-Bit DACs with Output Amplifiers
- Separate Reference Input for Each DAC
- µP Compatible with Double-Buffered Inputs
- Simultaneous Update of All Four Outputs
- Operates with Single or Dual Supplies
- Extended Temperature Range Operation
- No User Trims Required
- Skinny 24-Pin DIP, SOIC and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each D/A converter has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel–an input register and a DAC register. Control inputs A0 and A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5 V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 V to +12.5 V when using dual supplies. The part is also specified for single supply operation using a reference of +10 V. Each output buffer amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7225 is fabricated on an all ion-implanted high-speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7225 allows single supply operation. The part can also be operated with dual supplies giving enhanced performance for some parameters.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7225KN	–40°C to +85°C	±2 LSB	N-24
AD7225LN	–40°C to +85°C	±1 LSB	N-24
AD7225KP	–40°C to +85°C	±2 LSB	P-28A
AD7225LP	–40°C to +85°C	±1 LSB	P-28A
AD7225KR	–40°C to +85°C	±2 LSB	R-24
AD7225LR	–40°C to +85°C	±1 LSB	R-24
AD7225BQ	–40°C to +85°C	±2 LSB	Q-24
AD7225CQ	–40°C to +85°C	±1 LSB	Q-24
AD7225TQ	–55°C to +125°C	±2 LSB	Q-24
AD7225UQ	–55°C to +125°C	±1 LSB	Q-24
AD7225TE	–55°C to +125°C	±2 LSB	E-28A
AD7225UE	–55°C to +125°C	±1 LSB	E-28A

NOTES

[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.

[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

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AD7225–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4 V to 16.5 V, V_{SS} = –5 V ± 10%; AGND = DGND = 0 V; V_{REF} = +2 V to (V_{DD} – 4 V)[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	V_{DD} = +15 V ± 5%, V_{REF} = +10 V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±1	±1/2	±1	±1/2	LSB max	
Full-Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C typ	V_{DD} = 14 V to 16.5 V, V_{REF} = +10 V
Zero Code Error @ 25°C	±25	±15	±25	±15	mV max	
T_{MIN} to T_{MAX}	±30	±20	±30	±20	mV max	
Zero Code Error Temp Coeff.	±30	±30	±30	±30	µV/°C typ	
REFERENCE INPUT						
Voltage Range	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	V min to V max	
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[3]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1s.
Channel-to-Channel Isolation[3]	60	60	60	60	dB min	V_{REF} = 10 V p-p Sine Wave @ 10 kHz
AC Feedthrough[3]	–70	–70	–70	–70	dB max	V_{REF} = 10 V p-p Sine Wave @ 10 kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[3]	2.5	2.5	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]						
Positive Full-Scale Change	5	5	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Negative Full-Scale Change	5	5	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough[3]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES						
V_{DD} Range	11.4/16.5	11.4/16.5	11.4/16.5	11.4/16.5	V min to V max	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	10	10	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3,4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{MIN} to T_{MAX}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{MIN} to T_{MAX}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{MIN} to T_{MAX}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{MIN} to T_{MAX}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: –40°C to +85°C
B, C Versions: –40°C to +85°C
T, U Versions: –55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS Quad 8-Bit D/A Converter

AD7226

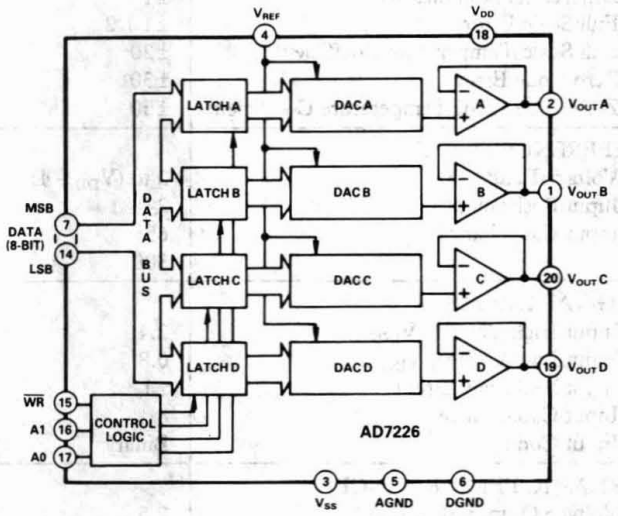
FEATURES

Four 8-Bit DACs with Output Amplifiers
Skinny 20-Pin DIP, SOIC and 20-Terminal Surface Mount Packages
Microprocessor Compatible
TTL/CMOS Compatible
No User Trims
Extended Temperature Range Operation
Single Supply Operation Possible

APPLICATIONS

Process Control
Automatic Test Equipment
Automatic Calibration of Large System Parameters, e.g., Gain/Offset

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7226 contains four 8-bit voltage-output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS (5 V) compatible input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed-compatible with most 8-bit microprocessors.

Each D/A converter includes an output buffer amplifier capable of driving up to 5 mA of output current. The amplifiers' offsets are laser-trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2 V to +12.5 V with dual supplies. The part is also specified for single supply operation at a reference of +10 V.

The AD7226 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching
   Since all four DACs are fabricated on the same chip at the same time, precise matching and tracking between the DACs is inherent.
2. Single Supply Operation
   The voltage mode configuration of the DACs allows the AD7226 to be operated from a single power supply rail.
3. Microprocessor Compatibility
   The AD7226 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7226KN	–40°C to +85°C	±2 LSB	N-20
AD7226KP	–40°C to +85°C	±2 LSB	P-20A
AD7226KR	–40°C to +85°C	±2 LSB	R-20
AD7226BQ	–40°C to +85°C	±2 LSB	Q-20
AD7226TQ	–55°C to +125°C	±2 LSB	Q-20
AD7226TE	–55°C to +125°C	±2 LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for Military data sheet, for U.S. Standard Military Drawing (SMD), see DESC drawing #5962–87802.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7226–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4 V to 16.5 V, V_{SS} = –5 V ± 10%; AGND = DGND = 0 V; V_{REF} = +2 V to (V_{DD} – 4 V)[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error	±2	LSB max	V_{DD} = +15 V ± 5%, V_{REF} = +10 V
Relative Accuracy	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Full Scale Error	±1 1/2	LSB max	
Full Scale Temperature Coefficient	±20	ppm/°C typ	V_{DD} = 14 V to 16.5 V, V_{REF} = +10 V
Zero Code Error	±30	mV max	
Zero Code Error Temperature Coefficient	±50	µV/°C typ	
REFERENCE INPUT			
Voltage Range	2 to (V_{DD} – 4)	V min to V max	
Input Resistance	2	kΩ min	
Input Capacitance[3]	65	pF min	Occurs when each DAC is loaded with all 0s.
	300	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[4]	2.5	V/µs min	
Voltage Output Settling Time[4]			
Positive Full Scale Change	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Negative Full Scale Change	7	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Crosstalk	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES			
V_{DD} Range	11.4/16.5	V min/V max	For Specified Performance
I_{DD}	13	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	11	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4, 5]			
Address to Write Setup Time, t_{AS}			
@ 25°C	0	ns min	
T_{MIN} to T_{MAX}	0	ns min	
Address to Write Hold Time, t_{AH}			
@ 25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Data Valid to Write Setup Time, t_{DS}			
@ 25°C	90	ns min	
T_{MIN} to T_{MAX}	100	ns min	
Data Valid to Write Hold Time, t_{DH}			
@ 25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Write Pulse Width, t_{WR}			
@ 25°C	150	ns min	
T_{MIN} to T_{MAX}	200	ns min	

NOTES

[1]Maximum possible reference voltage.

[2]Temperature ranges are as follows:
K Version: –40°C to +85°C
B Version: –40°C to +85°C
T Version: –55°C to +125°C

[3]Guanteed by design. Not production tested.

[4]Sample Tested at 25°C to ensure compliance.

[5]Switching Characteristics apply for single and dual supply operation.

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS Octal 8-Bit DAC

AD7228A

FEATURES
- Eight 8-Bit DACs with Output Amplifiers
- Operates with Single +5 V, +12 V or +15 V or Dual Supplies
- µP Compatible (95 ns $\overline{WR}$ Pulse)
- No User Trims Required
- Skinny 24-Pin DIPs, SOIC, and 28-Terminal Surface Mount Packages

GENERAL DESCRIPTION

The AD7228A contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5 V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

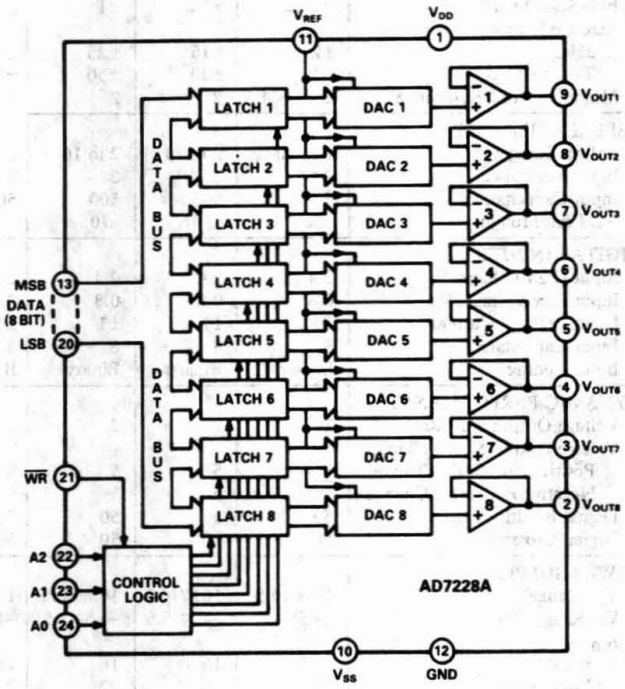
Specified performance is guaranteed for input reference voltages from +2 to +10 V when using dual supplies. The part is also specified for single supply +15 V operation using a reference of +10 V and single supply +5 V operation using a reference of +1.23 V. Each output buffer amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7228A is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. Eight DACs and Amplifiers in Small Package
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228A. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Microprocessor Compatibility
   The AD7228A has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high performance 8-bit microprocessors.

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7228ABN	–40°C to +85°C	±2 max	N-24
AD7228ACN	–40°C to +85°C	±1 max	N-24
AD7228ABP	–40°C to +85°C	±2 max	P-28A
AD7228ACP	–40°C to +85°C	±1 max	P-28A
AD7228ABR	–40°C to +85°C	±2 max	R-24
AD7228ACR	–40°C to +85°C	±1 max	R-24
AD7228ABQ	–40°C to +85°C	±2 max	Q-24
AD7228ACQ	–40°C to +85°C	±1 max	Q-24
AD7228ATQ[3]	–55°C to +125°C	±2 max	Q-24
AD7228AUQ[3]	–55°C to +125°C	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]These grades will be available to /883B processing only.

AD7228A–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 10.8 V to 16.5 V; V_{SS} = –5 V ± 10%; GND = 0 V; V_{REF} = +2 V to +10 V[1]; R_L = 2 kΩ, C_L = 100 pF unless otherwise noted.) All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Parameter	B Version[2]	C Version	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	V_{DD} = +15 V ± 10%, V_{REF} = +10 V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error[4]	±1	±1/2	±1	±1/2	LSB max	Typical tempco is 5 ppm/°C with V_{REF} = +10 V
Zero Code Error						
@ 25°C	±25	±15	±25	±15	mV max	Typical tempco is 30 µV/°C
T_{MIN} to T_{MAX}	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10 V
REFERENCE INPUT						
Voltage Range[1]	2 to 10	2 to 10	2 to 10	2 to 10	V min/V max	
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
AC Feedthrough	–70	–70	–70	–70	dB typ	V_{REF} = 8 V p-p Sine Wave @ 10 kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[5]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/µs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Negative Full-Scale Change	5	5	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0 V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = +10 V; $\overline{WR}$ = 0 V
POWER SUPPLIES						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	For Specified Performance
V_{SS} Range	–4.5/–5.5	–4.5/–5.5	–4.5/–5.5	–4.5/–5.5	V min/V max	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@ 25°C	16	16	16	16	mA max	
T_{MIN} to T_{MAX}	20	20	22	22	mA max	
I_{SS}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@ 25°C	14	14	14	14	mA max	
T_{MIN} to T_{MAX}	18	18	20	20	mA max	

SINGLE SUPPLY

(V_{DD} = +15 V ± 10%, V_{SS} = GND = 0 V; V_{REF} = +10 V; R_L = 2 kΩ, C_L = 100 pF unless otherwise noted.) All specifications T_{MIN} to T_{MAX} unless otherwise noted.

STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10 V
REFERENCE INPUT						
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS	As per Dual Supply Specifications					
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/µs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	µs max	Settling Time to ±1/2 LSB
Negative Full-Scale Change	7	7	7	7	µs max	Settling Time to ±1/2 LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = 0 V; $\overline{WR}$ = V_{DD}
Digital Crosstalk[6]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. V_{REF} = +10 V; $\overline{WR}$ = 0 V
POWER SUPPLIES						
V_{DD} Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V min/V max	For Specified Performance
I_{DD}						Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
@ 25°C	16	16	16	16	mA max	
T_{MIN} to T_{MAX}	20	20	22	22	mA max	

NOTES

[1]V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.

[2]Temperature ranges are as follows:
B, C Versions; –40°C to +85°C
T, U Versions; –55°C to +125°C

[3]Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.

[4]Calculated after zero code error has been adjusted out.

[5]Sample tested at 25°C to ensure compliance.

[6]The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.

Specifications subject to change without notice.

LC²MOS 12-Bit Serial Mini-DIP DACPORT

AD7233

FEATURES

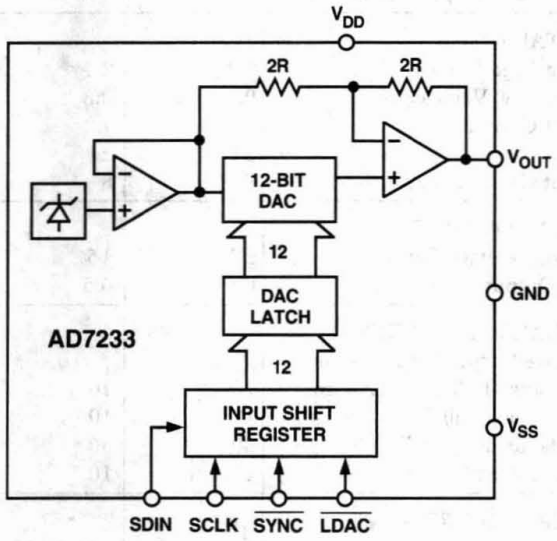
12-Bit CMOS DAC with
- **On-Chip Voltage Reference**
- **Output Amplifier**
- **–5 V to +5 V Output Range**

Serial Interface
300 kHz DAC Update Rate
Small Size: 8-Pin Mini-DIP
Nonlinearity: ±1/2 LSB T_{MIN} to T_{MAX}
Low Power Dissipation: 100 mW typ

APPLICATIONS

Process Control
Industrial Automation
Digital Signal Processing Systems
Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7233 is a complete 12-bit, voltage-output, digital-to-analog converter with output amplifier and Zener voltage reference all in an 8-pin package. No external trims are required to achieve full specified performance. The data format is 2s complement, and the output range is –5 V to +5 V.

The AD7233 features a fast, versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. When the $\overline{SYNC}$ input is taken low, data on the SDIN pin is clocked into the input shift register on each falling edge of SCLK. On completion of the 16-bit data transfer, bringing $\overline{LDAC}$ low updates the DAC latch with the lower 12 bits of data and updates the output. Alternatively, $\overline{LDAC}$ can be tied permanently low, and in this case the DAC register is automatically updated with the contents of the shift register when all sixteen data bits have been clocked in. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz.

For applications which require greater flexibility and unipolar output ranges with single supply operation, please refer to the AD7243 data sheet.

The AD7233 is fabricated on Linear Compatible CMOS (LC^2MOS), an advanced, mixed-technology process. It is packaged in an 8-pin DIP package.

DACPORT is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT®.
2. The AD7233 is a complete, voltage output, 12-bit DAC on a single chip. This single-chip design is inherently more reliable than multichip designs.
3. Simple 3-wire interface to most microcontrollers and DSP processors.
4. DAC Update Rate—300 kHz.
5. Space Saving 8-Pin Package.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7233AN	–40°C to +85°C	±1 LSB	N-8
AD7233BN	–40°C to +85°C	±1/2 LSB	N-8

*N = Plastic DIP. For outline information see Package Information section.

AD7233–SPECIFICATIONS[1] (V_{DD} = +12 V to +15 V,[2] V_{SS} = –12 V to –15 V,[2] GND = 0 V, R_L = 2 kΩ, C_L = 100 pF to GND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A	B	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error[3]	±6	±6	LSB max	DAC Latch Contents 0000 0000 0000
Full-Scale Error[3]	±8	±8	LSB max	
Full-Scale Temperature Coefficient	±30	±30	ppm of FSR/°C typ	
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Current				
I_{IN}	±1	±1	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[4]	8	8	pF max	
ANALOG OUTPUTS				
Output Voltage Range	±5	±5	V	
DC Output Impedance	0.5	0.5	Ω typ	
AC CHARACTERISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	µs max	Typically 3 µs; DAC Latch 100. . .000 to 011. . .111
Negative Full-Scale Change	10	10	µs max	Typically 5 µs; DAC Latch 011. . .111 to 100. . .000
Digital-to-Analog Glitch Impulse[3]	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and all 1s
Digital Feedthrough[3]	10	10	nV secs typ	$\overline{LDAC}$ = High
POWER REQUIREMENTS				
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range	–10.8/–16.5	–11.4/–15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	10	10	mA max	Output Unloaded; Typically 7 mA
I_{SS}	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Temperature Ranges are as follows: A, B Versions: –40°C to +85°C.
[2]Power Supply Tolerance: A Version: ±10%; B Version: ±5%.
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

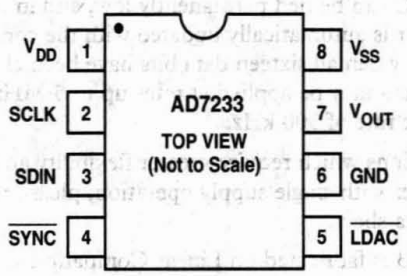
ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +17 V
V_{SS} to GND ..... +0.3 V to –17 V
V_{OUT}[2] to GND ..... –6 V to V_{DD} + 0.3 V
Digital Inputs to GND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A, B Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation to +75°C ..... 450 mW
Derates above +75°C by ..... 10 mW/°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]The output may be shorted to voltages in this range provided the power dissipation of the package is not exceeded. Short circuit current is typically 80 mA.

PIN CONFIGURATION



LC²MOS Dual 12-Bit DACPORTs

AD7237A/AD7247A

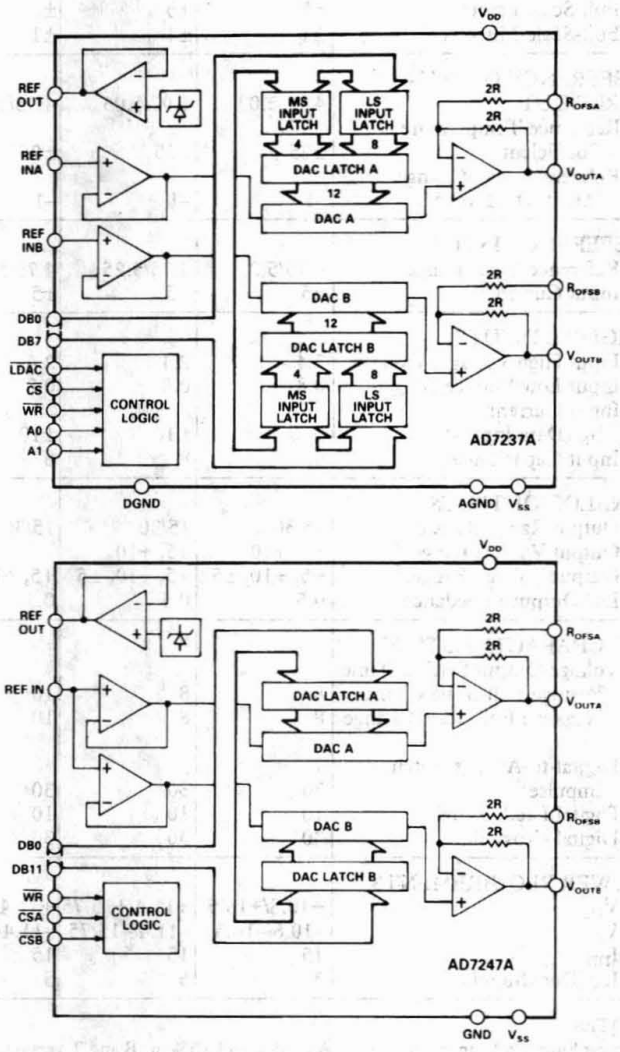
FEATURES

Complete Dual 12-Bit DAC Comprising
- **Two 12-Bit CMOS DACs**
- **On-Chip Voltage Reference**
- **Output Amplifiers**
- **Reference Buffer Amplifiers**

Improved AD7237/AD7247:
- **12 V to 15 V Operation**
- **Faster Interface –30 ns typ Data Setup Time**

Parallel Loading Structure: AD7247A
(8+4) Loading Structure: AD7237A
Single or Dual Supply Operation
Low Power—165 mW typ in Single Supply

FUNCTIONAL BLOCK DIAGRAMS



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GENERAL DESCRIPTION

The AD7237A/AD7247A is an enhanced version of the industry standard AD7237/AD7247. Improvements include operation from 12 V to 15 V supplies, faster interface times and better reference variations with V_{DD}. Additional features include faster settling times.

The AD7237A/AD7247A is a complete, dual, 12-bit, voltage output digital-to-analog converter with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7247A accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7237A has a double buffered interface structure and an 8-bit wide data bus with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7237A updates the DAC latches and analog outputs.

A REF OUT/REF IN function is provided which allows either the on-chip 5 V reference or an external reference to be used as a reference voltage for the part. For single supply operation, two output ranges of 0 V to +5 V and 0 V to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7237A/AD7247A is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3" wide plastic and hermetic dual-in-line package (DIP) and are also packaged in a 24-lead small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. The AD7237A/AD7247A is a dual 12-bit DACPORT® on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. The improved interface times of the parts allow easy, direct interfacing to most modern microprocessors, whether they have 8-bit or 16-bit data bus structures.
3. The AD7237A/AD7247A features a wide power supply range allowing operation from 12 V supplies.

DACPORT is a registered trademark of Analog Devices, Inc.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7237A/AD7247A–SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or –12 V to –15 V,[1] AGND = DGND = 0 V [AD7237A], GND = 0 V [AD7247A], REF IN = +5 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A[2]	B[2]	T[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±3	±3	±4	LSB max	V_{SS} = 0 V or –12 V to –15 V[4]. DAC Latch Contents All 0s
Bipolar Zero Error[3]	±6	±4	±6	LSB max	V_{SS} = –12 V to –15 V[4]. DAC Latch Contents 1000 0000 0000
Full-Scale Error[3, 5]	±5	±5	±6	LSB max	
Full-Scale Mismatch[5]	±1	±1	±1	LSB typ	
REFERENCE OUTPUT					
REF OUT	4.97/5.03	4.97/5.03	4.95/5.05	V min/max	
Reference Temperature Coefficient	±25	±25	±25	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	–1	mV max	Reference Load Current Change (0-100 μA)
REFERENCE INPUT					
Reference Input Range	4.75/5.25	4.75/5.25	4.75/5.25	V min/max	5 V ± 5%
Input Current[6]	±5	±5	±5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN} (Data Inputs)	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[6]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/max	
Output Voltage Ranges[7]	+5, +10	+5, +10		V	Single Supply; (V_{SS} = 0 V)
Output Voltage Ranges[7]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5		Dual Supply; (V_{SS} = –12 V to –15 V[4])
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[6]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	8	8	10	μs max	DAC Latch all 0s to all 1s. Typically 5 μs
Negative Full-Scale Change	8	8	10	μs max	DAC Latch all 1s to all 0s. Typically 5 μs V_{SS} = –12 V to –15 V[4].
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between all 0s and all 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	
Digital Crosstalk[3]	30	30	30	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/max	For Specified Performance Unless Otherwise Stated
V_{SS}	–10.8/–16.5	–11.4/–15.75	–11.4/–15.75	V min/max	For Specified Performance Unless Otherwise Stated
I_{DD}	15	15	15	mA max	Output Unloaded. Typically 10 mA
I_{SS} (Dual Supplies)	5	5	5	mA max	Output Unloaded. Typically 3 mA

NOTES
[1]Power Supply tolerance is ±10% for A version and ±5% for B and T versions.
[2]Temperature ranges are as follows: A, B Versions, –40°C to +85°C; T Version, –55°C to +125°C.
[3]See Terminology.
[4]With appropriate power supply tolerances.
[5]Measured with respect to REF IN and includes unipolar/bipolar offset error.
[6]Sample tested @ +25°C to ensure compliance.
[7]0 V to +10 V range is only available with $V_{DD} \geq 14.25$ V.

Specifications subject to change without notice.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Option[2]
AD7237AAN	–40°C to +85°C	±1 max	N-24
AD7237ABN	–40°C to +85°C	±1/2 max	N-24
AD7237AAR	–40°C to +85°C	±1 max	R-24
AD7237ABR	–40°C to +85°C	±1/2 max	R-24
AD7237ATQ	–55°C to +125°C	±1/2 max	Q-24
AD7247AAN	–40°C to +85°C	±1 max	N-24
AD7247ABN	–40°C to +85°C	±1/2 max	N-24
AD7247AAR	–40°C to +85°C	±1 max	R-24
AD7247ABR	–40°C to +85°C	±1/2 max	R-24
AD7247ATQ	–55°C to +125°C	±1/2 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet and availability.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC).
For outline information see Package Information section.

LC²MOS Dual, Complete, 12-Bit/14-Bit Serial DACs

AD7242/AD7244

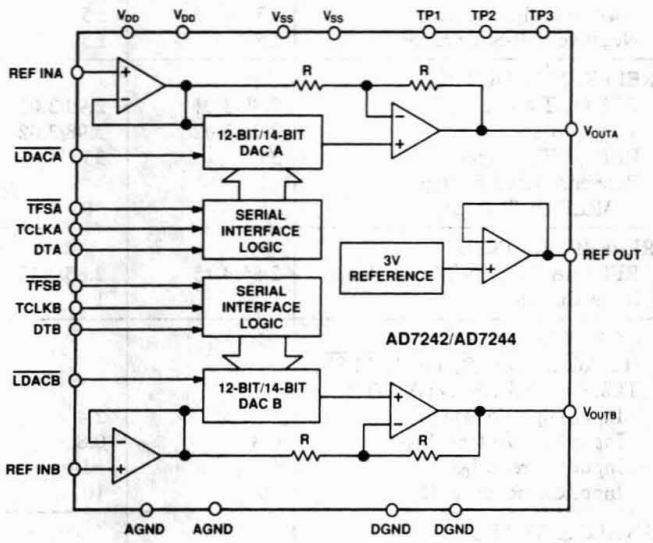
FEATURES

Two 12-Bit/14-Bit DACs with Output Amplifiers
- **AD7242: 12-Bit Resolution**
- **AD7244: 14-Bit Resolution**

On-Chip Voltage Reference
Fast Settling Time
- **AD7242: 3 μs to ±1/2 LSB**
- **AD7244: 4 μs to ±1/2 LSB**

High Speed Serial Interface
Operates from ±5 V Supplies
Specified Over –40°C to +85°C in Plastic Packages
Low Power – 130 mW typ

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7242/AD7244 is a fast, complete, dual 12-bit/14-bit voltage output D/A converter. It consists of a 12-bit/14-bit DAC, 3 V buried Zener reference, DAC output amplifiers and high speed serial interface logic.

Interfacing to both DACs is serial, minimizing pin count and allowing a small package size. Standard control signals allow interfacing to most DSP processors and microcontrollers. Asynchronous control of DAC updating for both DACs is made possible with a separate LDAC input for each DAC.

The AD7242/AD7244 operates from ±5 V power supplies, providing an analog output range of ±3 V. A REF OUT/REF IN function allows the DACs to be driven from the on-chip 3 V reference or from an external reference source.

The AD7242/AD7244 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced mixed technology process that combines precision bipolar circuits with low power CMOS logic. Both parts are available in a 24-pin, 0.3 inch wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin, plastic small outline (SOIC) package. The AD7242 and AD7244 are available in the same pinout to allow easy upgrade from 12-bit to 14-bit performance.

PRODUCT HIGHLIGHTS

1. Complete, Dual 12-Bit/14-Bit DACs
   The AD7242/AD7244 provides the complete function for generating voltages to 12-bit/14-bit resolution. The part features an on-chip reference, output buffer amplifiers and two 12-bit/14-bit D/A converters.
2. High Speed Serial Interface
   The AD7242/AD7244 provides a high speed, easy-to-use, serial interface allowing direct interfacing to DSP processors and microcontrollers. A separate serial port is provided for each DAC.
3. Small Package Size
   The AD7242/AD7244 is available in a 24-pin DIP and a 28-pin SOIC package offering considerable space saving over comparable solutions.

AD7242 ORDERING GUIDE

Model	Temperature Range	Integral Nonlinearity	Package Option*
AD7242JN	–40°C to +85°C	±1 LSB max	N-24
AD7242KN	–40°C to +85°C	±1/2 LSB max	N-24
AD7242JR	–40°C to +85°C	±1 LSB max	R-28
AD7242KR	–40°C to +85°C	±1/2 LSB max	R-28
AD7242AQ	–40°C to +85°C	±1 LSB max	Q-24
AD7242BQ	–40°C to +85°C	±1/2 LSB max	Q-24

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

AD7244 ORDERING GUIDE

Model[1]	Temperature Range	Integral Nonlinearity	Package Option[2]
AD7244JN	–40°C to +85°C	±2 LSB max	N-24
AD7244JR	–40°C to +85°C	±2 LSB max	R-28
AD7244AQ	–40°C to +85°C	±2 LSB max	Q-24
AD7244SQ[3]	–55°C to +125°C	±2 LSB max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet and availablility.
[2]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]This grade will be available to /883B processing only.

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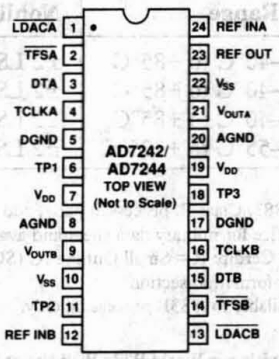
AD7242/AD7244–SPECIFICATIONS (V_{DD} = +5 V ± 5% V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, REF INA = REF INB = +3 V. V_{OUTA}, V_{OUTB} load to AGND: R_L = 2 kΩ, C_L = 100 pF. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7242 J, A Versions[1]	AD7242 K, B Versions[1]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±5	±5	LSB max	
Positive Full-Scale Error[2]	±5	±5	LSB max	
Negative Full-Scale Error[2]	±5	±5	LSB max	
REFERENCE OUTPUT[3]				
REF OUT @ +25°C	2.99/3.01	2.99/3.01	V min/V max	
T_{MIN} to T_{MAX}	2.98/3.02	2.98/3.02	V min/V max	
REF OUT Tempco	35	35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	mV max	Reference Load Current Change (0-500 μA)
REFERENCE INPUTS				
RFF INA, REF INB Input Range	2.85/3.15	2.85/3.15	V min/V max	3 V ± 5%
Input Current	1	1	μA max	
LOGIC INPUTS ($\overline{LDACA}$, $\overline{LDACB}$, $\overline{TFSA}$, $\overline{TFSB}$, TCLKA, TCLKB, DTA, DTB)				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
ANALOG OUTPUTS (V_{OUTA}, V_{OUTB})				
Output Voltage Range	±3	±3	V nom	
DC Output Impedance	0.1	0.1	Ω typ	
Short Circuit Current	20	20	mA typ	
AC CHARACTERTISTICS[4]				
Voltage Output Settling Time				Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	3	3	μs max	Typically 2 μs
Negative Full-Scale Change	3	3	μs max	Typically 2 μs
Digital-to-Analog Glitch Impulse	10	10	nV secs typ	DAC Code Change All 1s to All 0s
Digital Feedthrough	2	2	nV secs typ	
Channel-to-Channel Isolation	110	110	dB typ	V_{OUT} = 10 kHz Sine Wave
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	V nom	±5% for Specified Performance
I_{DD}	27	27	mA max	Cumulative Current from the Two V_{DD} Pins
I_{SS}	15	15	mA max	Cumulative Current from the Two V_{SS} Pins
Total Power Dissipation	195	195	mW max	Typically 130 mW

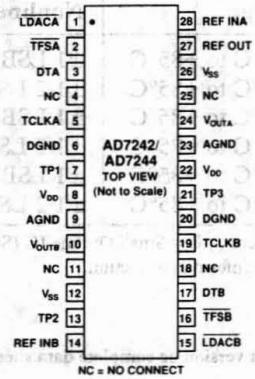
NOTES
[1]Temperature ranges are as follows: J, K Versions: –40°C to +85°C; A, B Versions: –40°C to +85°C.
[2]Measured with respect to REF IN and includes bipolar offset error.
[3]For capacitive loads greater than 50 pF a series resistor is required (see Internal Reference section).
[4]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

PIN CONFIGURATIONS

DIP



SOIC



ANALOG DEVICES

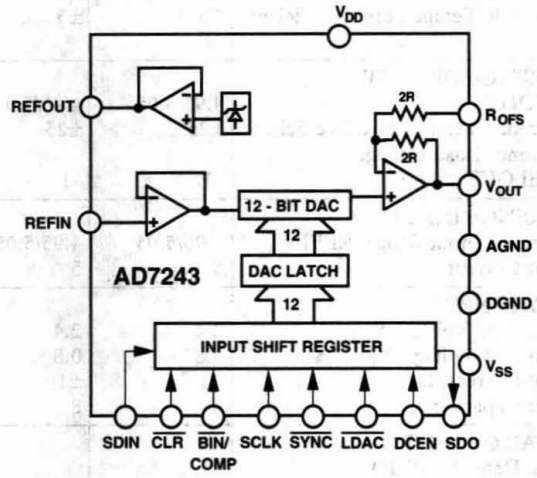
LC²MOS 12-Bit Serial DACPORT

AD7243

FEATURES
- 12-Bit CMOS DAC with
  - On-Chip Voltage Reference
  - Output Amplifier
- 3 Selectable Output Ranges
  - –5 V to +5 V, 0 V to +5 V, 0 V to +10 V
- Serial Interface
- 300 kHz DAC Update Rate
- Small Size: 16-Pin DIP or SOIC
- Nonlinearity: ±1/2 LSB T_{MIN} to T_{MAX}
- Low Power Dissipation: 100 mW typical

APPLICATIONS
- Process Control
- Industrial Automation
- Digital Signal Processing Systems
- Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7243 is a complete 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance.

The output amplifier is capable of developing +10 V across a 2 kΩ load. The output voltage ranges with single supply operation are 0 V to +5 V or 0 V to +10 V, while an additional bipolar ±5 V output range is available with dual supplies. The ranges are selected using the internal gain resistor.

The data format is natural binary in both unipolar ranges, while either offset binary or 2s complement format may be selected in the bipolar range. A $\overline{CLR}$ function is provided which sets the output to 0 V in both unipolar ranges and in the 2s complement bipolar range, while with offset binary data format, the output is set to –REFIN. This function is useful as a power-on reset as it allows the output to be set to a known voltage level.

The AD7243 features a fast versatile serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. The serial data may be applied at rates up to 5 MHz allowing a DAC update rate of 300 kHz. A serial data output capability is also provided which allows daisy chaining in multi-DAC systems. This feature allows any number of DACs to be used in a system with a simple 4-wire interface. All DACs may be updated simultaneously using $\overline{LDAC}$.

The AD7243 is fabricated on Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process. It is packaged in 16-pin DIP and 16-pin SOIC packages.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit DACPORT®
   The AD7243 is a complete, voltage output, 12-bit DAC on a single chip. The single chip design is inherently more reliable than multichip designs.
2. Single or Dual Supply Operation.
3. Minimum 3-wire interface to most DSP processors.
4. DAC Update Rate–300 kHz.
5. Serial Data Output allows easy daisy-chaining in multiple DAC systems.

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ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD7243AN	–40°C to +85°C	±1 LSB	N-16
AD7243BN	–40°C to +85°C	±1/2 LSB	N-16
AD7243AR	–40°C to +85°C	±1 LSB	R-16
AD7243BR	–40°C to +85°C	±1/2 LSB	R-16
AD7243AQ	–40°C to +85°C	±1 LSB	Q-16
AD7243BQ	–40°C to +85°C	±1/2 LSB	Q-16
AD7243SQ[2]	–55°C to +125°C	±1 LSB	Q-16

NOTES
[1]N = Plastic DIP; R = SOIC; Q = Cerdip. For outline information see Package Information section.
[2]Available to /883B processing only. Contact your local sales office for military data sheet.

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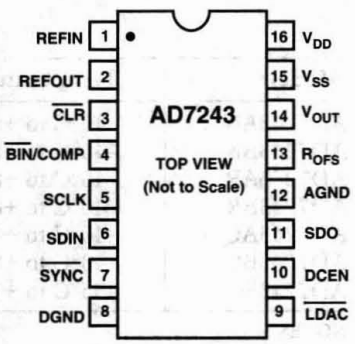
AD7243–SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or –12 V to –15 V,[1] AGND = DGND = 0 V, REFIN = +5 V R_L = 2 kΩ, C_L = 100 pF to AGND. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A[2]	B[2]	S[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±4	±4	±5	LSB max	V_{SS} = 0 V or –12 V to –15 V[1]; DAC Latch Contents All 0s
Bipolar Zero Error[3]	±5	±5	±6	LSB max	V_{SS} = –12 V to –15 V[1]; DAC Latch Contents A
Full-Scale Error[3, 4]	±6	±6	±7	LSB max	
Full-Scale Temperature Coefficient	±5	±5	±5	ppm of FSR/°C typ	
REFERENCE OUTPUT					
REFOUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔREFOUT vs. I_L)	–1	–1	–1	mV max	Reference Load Current (I_L) Change (0–100 µ
REFERENCE INPUT					
Reference Input Range, REFIN	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	5 V ±1% for Specified Performance
Input Current	5	5	5	µA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±1	±1	±1	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[5]	8	8	8	pF max	
DIGITAL OUTPUT					
Serial Data Out (SDO)					
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.0 mA
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 400 µA
ANALOG OUTPUT					
Output Range Resistor, R_{OFS}	15/30	15/30	15/30	kΩ min/max	
Output Voltage Ranges[6]	+5, +10	+5, +10	+5, +10	V	Single Supply; V_{SS} = 0 V
Output Voltage Ranges[6]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	Dual Supply; V_{SS} = –12 V to –15 V
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Val
Positive Full-Scale Change	10	10	12	µs max	Typically 3 µs
Negative Full-Scale Change	10	10	10	µs max	Typically 5 µs; V_{SS} = –12 V to –15 V[1]
Negative Full-Scale Change	10	10	10	µs typ	V_{SS} = 0 V
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and All 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	$\overline{LDAC}$ = High
POWER REQUIREMENTS					
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise S
V_{SS} Range (Dual Supplies)	–10.8/–16.5	–11.4/–15.75	–11.4/–15.75	V min/V max	For Specified Performance Unless Otherwise S
I_{DD}	10	10	12	mA max	Output Unloaded; Typically 7 mA
I_{SS} (Dual Supplies)	4	4	4	mA max	Output Unloaded; Typically 2 mA

NOTES
[1]Power Supply Tolerance A Version: ±10%; B, S Versions: ±5%.
[2]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.
[3]See terminology.
[4]Measured with respect to REFIN and includes unipolar/bipolar offset error.
[5]Sample tested @ +25°C to ensure compliance.
[6]0 V to +10 V output range is available only with $V_{DD} \geq$ +14.25 V.
Specifications subject to change without notice.

PIN CONFIGURATION
DIP and SOIC



ANALOG DEVICES

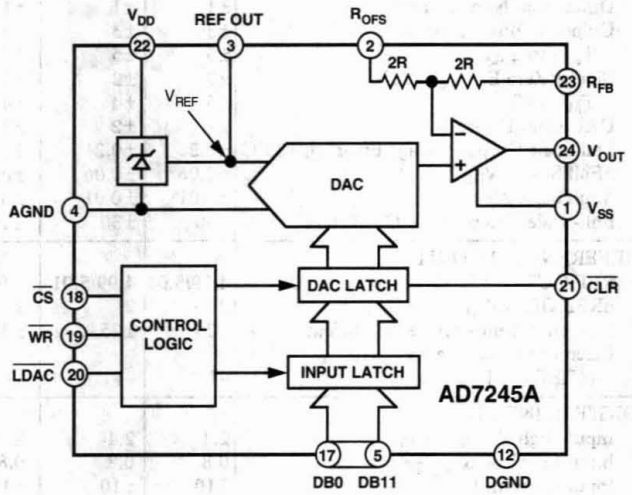
LC²MOS 12-Bit DACPORTs

AD7245A/AD7248A

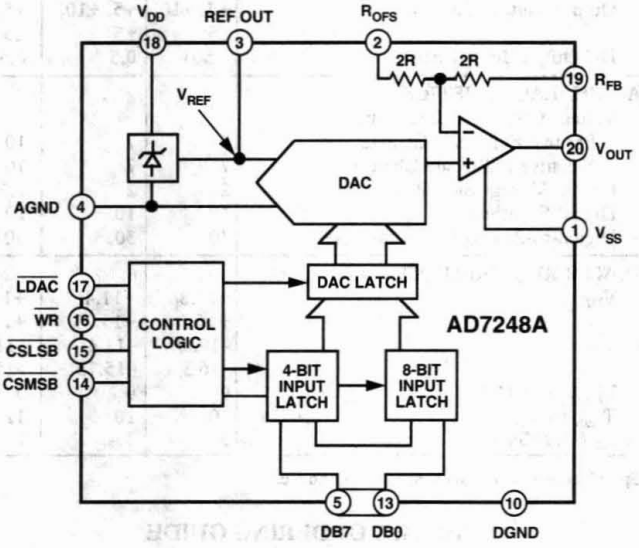
FEATURES

12-Bit CMOS DAC with Output Amplifier and Reference
Improved AD7245/AD7248:
12 V to 15 V Operation
±1/2 LSB Linearity Grade
Faster Interface–30 ns typ Data Setup Time
Extended Plastic Temperature Range (–40°C to +85°C)
Single or Dual Supply Operation
Low Power–65 mW typ in Single Supply
Parallel Loading Structure: AD7245A
(8+4) Loading Structure: AD7248A

AD7245A FUNCTIONAL BLOCK DIAGRAM



AD7248A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7245A/AD7248A is an enhanced version of the industry standard AD7245/AD7248. Improvements include operation from 12 V to 15 V supplies, a ±1/2 LSB linearity grade, faster interface times and better full scale and reference variations with V_{DD}. Additional features include extended temperature range operation for commercial and industrial grades.

The AD7245A/AD7248A is a complete, 12-bit, voltage output, digital-to-analog converter with output amplifier and Zener voltage reference on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and double-buffered interface logic. The AD7245A accepts 12-bit parallel data which is loaded into the input latch on the rising edge of $\overline{CS}$ or $\overline{WR}$. The AD7248A has an 8-bit wide data bus with data loaded to the input latch in two write operations. For both parts, an asynchronous $\overline{LDAC}$ signal transfers data from the input latch to the DAC latch and updates the analog output. The AD7245A also has a $\overline{CLR}$ signal on the DAC latch which allows features such as power-on reset to be implemented.

The on-chip 5 V buried Zener diode provides a low noise, temperature compensated reference for the DAC. For single supply operation, two output ranges of 0 V to +5 V and 0 V to +10 V are available, while these two ranges plus an additional ±5 V range are available with dual supplies. The output amplifiers are capable of developing +10 V across a 2 kΩ load to GND.

The AD7245A/AD7248A is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The AD7245A is available in a small, 0.3" wide, 24-pin DIP and SOIC and in 28-terminal surface mount packages. The AD7248A is packaged in a small, 0.3" wide, 20-pin DIP and SOIC and in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. The AD7245A/AD7248A is a 12-bit DACPORT® on a single chip. This single chip design and small package size offer considerable space saving and increased reliability over multichip designs.
2. The improved interface times on the part allows easy, direct interfacing to most modern microprocessors.
3. The AD7245A/AD7248A features a wide power supply range allowing operation from 12 V supplies.

DACPORT is a registered trademark of Analog Devices, Inc.

AD7245A/AD7248A–SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or –12 V to –15 V,[1] AGND = DGND = 0 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A[2] Version	B[2] Version	T[2] Version	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy @ +25°C[3]	±3/4	±1/2	±1/2	LSB max	
T_{MIN} to T_{MAX}	±1	±3/4	±3/4	LSB max	
T_{MIN} to T_{MAX}		±1/2		LSB max	V_{DD} = 15 V ± 5%
Differential Nonlinearity[3]	±1	±1	±1	LSB max	Guaranteed Monotonic
Unipolar Offset Error @ +25°C[3]	±3	±3	±3	LSB max	V_{SS} = 0 V or –12 V to –15 V[4]
T_{MIN} to T_{MAX}	±5	±5	±5	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
Bipolar Zero Error @ +25°C[3]	±3	±2	±2	LSB max	R_{OFS} connected to REF OUT; V_{SS} = –12 V to –15 V[4]
T_{MIN} to T_{MAX}	±5	±4	±4	LSB max	Typical Tempco is ±3 ppm of FSR[5]/°C.
DAC Gain Error[3, 6]	±2	±2	±2	LSB max	
Full-Scale Output Voltage Error[7] @ +25°C	±0.2	±0.2	±0.2	% of FSR max	V_{DD} = +15 V
ΔFull Scale/ΔV_{DD}	±0.06	±0.06	±0.06	% of FSR/V max	V_{DD} = +12 V to +15 V[4]
ΔFull Scale/ΔV_{SS}	±0.01	±0.01	±0.01	% of FSR/V max	V_{SS} = –12 V to –15 V[4]
Full-Scale Temperature Coefficient[8]	±30	±30	±40	ppm of FSR/°C max	V_{DD} = +15 V
REFERENCE OUTPUT					
REF OUT @ +25°C	4.99/5.01	4.99/5.01	4.99/5.01	V min/V max	V_{DD} = +15 V
ΔREF OUT/ΔV_{DD}	2	2	2	mV/V max	V_{DD} = +12 V to +15 V[4]
Reference Temperature Coefficient	±25	±25	±35	ppm/°C typ	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	–1	mV max	Referenee Load Current Change (0–100 μA)
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[9]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistors	15/30	15/30	15/30	kΩ min/kΩ max	
Output Voltage Ranges[10]	+5, +10	+5, +10	+5, +10	V	V_{SS} = 0 V; Pin Strappable
Output Voltage Ranges[10]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	V_{SS} = –12 V to –15 V;[4] Pin Strappable
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[9]					
Voltage Output Settling Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	7	7	10	μs max	DAC Latch All 0s to All 1s
Negative Full-Scale Change	7	7	10	μs max	DAC Latch All 1s to All 0s; V_{SS} = –12 V to –15 V[4]
Output Voltage Slew Rate	2	2	1.5	V/μs min	
Digital Feedthrough[3]	10	10	10	nV-s typ	
Digital-to-Analog Glitch Impulse	30	30	30	nV-s typ	
POWER REQUIREMENTS					
V_{DD}	+10.8/ +16.5	+11.4/ +15.75	+11.4/ +15.75	V min/ V max	For Specified Performance Unless Otherwise Stated
V_{SS}	–10.8/ –16.5	–11.4/ –15.75	–11.4/ –15.75	V min/ V max	For Specified Performance Unless Otherwise Stated
I_{DD} @ +25°C	9	9	9	mA max	Output Unloaded; Typically 5 mA
T_{MIN} to T_{MAX}	10	10	12	mA max	Output Unloaded
I_{SS} (Dual Supplies)	3	3	5	mA max	Output Unloaded; Typically 2 mA

Specifications subject to change without notice.

AD7245A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7245AAN	–40°C to +85°C	±3/4 LSB	N-24
AD7245ABN	–40°C to +85°C	±1/2 LSB	N-24
AD7245AAQ	–40°C to +85°C	±3/4 LSB	Q-24
AD7245ATQ[3]	–55°C to +125°C	±3/4 LSB	Q-24
AD7245AAP	–40°C to +85°C	±3/4 LSB	P-28A
AD7245AAR	–40°C to +85°C	±3/4 LSB	R-24
AD7245ABR	–40°C to +85°C	±1/2 LSB	R-24
AD7245ATE[3]	–55°C to +125°C	±3/4 LSB	E-28A

NOTES
[1]To order MIL-STD-883, Class B. processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section
[3]This grade will be available to /883B processing only.

AD7248A ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7248AAN	–40°C to +85°C	±3/4 LSB	N-20
AD7248ABN	–40°C to +85°C	±1/2 LSB	N-20
AD7248AAQ	–40°C to +85°C	±3/4 LSB	Q-20
AD7248ATQ[3]	–55°C to +125°C	±3/4 LSB	Q-20
AD7248AAP	–40°C to +85°C	±3/4 LSB	P-20A
AD7248AAR	–40°C to +85°C	±3/4 LSB	R-20
AD7248ABR	–40°C to +85°C	±1/2 LSB	R-20

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact our local sales office for military data sheet and availability.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section
[3]This grade will be available to /883B processing only.

LC²MOS Dual 12-Bit Serial DACPORT

AD7249

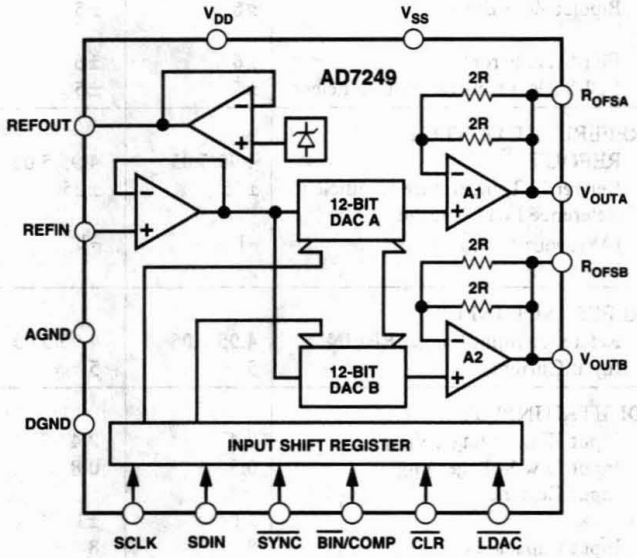
FEATURES

Two 12-Bit CMOS DAC Channels with
On-Chip Voltage Reference
Output Amplifiers
Three Selectable Output Ranges per Channel
–5 V to +5 V, 0 V to +5 V, 0 V to +10 V
Serial Interface
125 kHz DAC Update Rate
Small Size: 16-Pin DIP or SOIC
Low Power Dissipation

APPLICATIONS

Process Control
Industrial Automation
Digital Signal Processing Systems
Input/Output Ports

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7249 DACPORT® contains a pair of 12-bit, voltage-output, digital-to-analog converters with output amplifiers and Zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance.

The output amplifiers are capable of developing +10 V across a 2 kΩ load. The output voltage ranges with single supply operation are 0 V to +5 V or 0 V to +10 V, while an additional bipolar ±5 V output range is available with dual supplies. The ranges are selected using the internal gain resistor.

Interfacing to the AD7249 is serial, minimizing pin count and allowing a small package size. Standard control signals allow interfacing to most DSP processors and microcontrollers. The data stream consists of 16 bits, DB15 to DB13 are don't care bits, the 13th bit (DB12) is used as the channel select bit and the remaining 12 bits (DB11 to DB0) contain the data to update the DAC. The 16-bit data word is clocked into the input register on each falling SCLK edge.

The data format is natural binary in both unipolar ranges, while either offset binary or twos complement format may be selected in the bipolar range. A $\overline{\text{CLR}}$ function is provided which sets the output to 0 V in both unipolar ranges and in the twos complement bipolar range, while with offset binary data format, the output is set to –REFIN. This function is useful as a power-on reset as it allows the outputs to be set to a known voltage level.

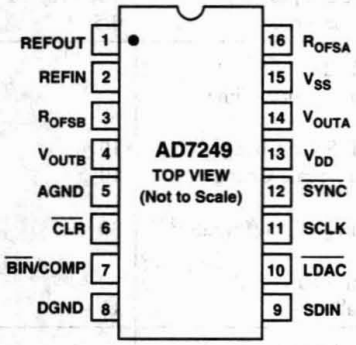
The AD7249 features a serial interface which allows easy connection to both microcomputers and 16-bit digital signal processors with serial ports. The serial data may be applied at rates up to 2 MHz allowing a DAC update rate of 125 kHz.

The AD7249 is fabricated on linear compatible CMOS (LC²MOS), an advanced, mixed technology process. It is packaged in 16-pin DIP and 16-pin SOIC packages.

DACPORT is a registered trademark of Analog Devices, Inc.

PIN CONFIGURATIONS

(DIP and SOIC)



ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option[1]
AD7249AN	–40°C to +85°C	±1 LSB	N-16
AD7249BN	–40°C to +85°C	±1/2 LSB	N-16
AD7249AR	–40°C to +85°C	±1 LSB	R-16
AD7249BR	–40°C to +85°C	±1/2 LSB	R-16
AD7249SQ[2]	–55°C to +125°C	±1 LSB	Q-16

NOTES
[1]For outline information see Package Information section.
[2]Available to /883B processing only. Contact your local sales office for military data sheet.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7249—SPECIFICATIONS (V_{DD} = +12 V to +15 V,[1] V_{SS} = 0 V or −12 V to −15 V,[1] AGND = DGND = 0 V, REFIN = +5 V, R_L = 2 kΩ, C_L = 100 pF to AGND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[2]	B Version[2]	S Version[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Unipolar Offset Error[3]	±5	±5	±6	LSB max	V_{SS} = 0 V or −12 V to −15 V[1]; DAC Latch Contents All 0s
Bipolar Zero Error[3]	±6	±5	±7	LSB max	V_{SS} = −12 V to −15 V[1] DAC Latch Contents All 0s
Full-Scale Error[3, 4]	±6	±6	±7	LSB max	
Full-Scale Temperature Coefficient	±5	±5	±5	ppm of FSR/°C typ	
REFERENCE OUTPUT					
REFOUT	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	
Reference Temperature Coefficient	±25	±25	±30	ppm/°C typ	
Reference Load Change (ΔV_{REFOUT} vs. I_L)	−1	−1	−1	mV max	Reference Load Current (I_L) Change (0 μA–100 μA)
REFERENCE INPUT					
Reference Input Range, REFIN	4.95/5.05	4.95/5.05	4.95/5.05	V min/V max	5 V ± 1%
Input Current	5	5	5	μA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current					
I_{IN}	±1	±1	±1	μA max	V_{IN} = 0 V to V_{DD}
Input Capacitance[5]	8	8	8	pF max	
ANALOG OUTPUTS					
Output Range Resistor, R_{OFSA} & R_{OFSB}	15/30	15/30	15/30	kΩ min/ max	
Output Voltage Ranges[6]	+5, +10	+5, +10	+5, +10	V	Single Supply; V_{SS} = 0 V
Output Voltage Ranges[6]	+5, +10, ±5	+5, +10, ±5	+5, +10, ±5	V	Dual Supply; V_{SS} = −12 V or −15 V
DC Output Impedance	0.5	0.5	0.5	Ω typ	
AC CHARACTERISTICS[5]					
Voltage Output Settling-Time					Settling Time to Within ±1/2 LSB of Final Value
Positive Full-Scale Change	10	10	10	μs max	Typically 3 μs
Negative Full-Scale Change	10	10	10	μs max	Typically 5 μs. V_{SS} = −12 V to −15 V
	10	10	10	μs typ	V_{SS} = 0 V
Digital-to-Analog Glitch Impulse[3]	30	30	30	nV secs typ	DAC Latch Contents Toggled Between All 0s and All 1s
Digital Feedthrough[3]	10	10	10	nV secs typ	
Digital Crosstalk[3]	10	10	10	nV secs typ	
POWER REQUIREMENTS					
V_{DD} Range	+10.8/+16.5	+11.4/+15.75	+11.4/+15.75	V min/V max	For Specified Performance Unless Otherwise Stated
V_{SS} Range (Dual Supplies)	−10.8/−16.5	−11.4/−15.75	−11.4/−15.75	V min/V max	For Specified Performance Unless Otherwise Stated
I_{DD}	15	15	15	mA max	Output Unloaded; Typically 11 mA
I_{SS} (Dual Supplies)	5	5	5	mA max	Output Unloaded; Typically 3 mA

NOTES
[1]Power supply tolerance, A Version: ±10%; B, S Versions: ±5%.
[2]Temperature ranges are as follows: A, B Versions: −40°C to +85°C; S Version: −55°C to +125°C.
[3]See Terminology.
[4]Measured with respect to REFIN and includes unipolar/bipolar offset error.
[5]Guaranteed by design not production tested.
[6]0 V to 10 V output range available only with $V_{DD} \geq 14.25$ V.
Specifications subject to change without notice.

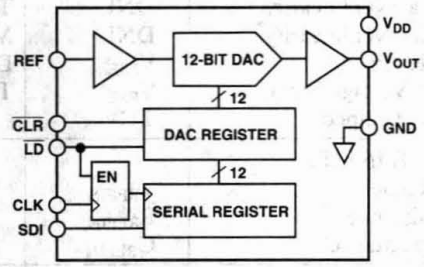
+3 V, Serial Input Micropower 10- and 12-Bit DACs

AD7390/AD7391

FEATURES
Micropower: 100 μA
Single-Supply +2.7 V to +5.5 V Operation
Compact 1.75 mm Height SO-8 Package
AD7390/12-Bit Resolution
AD7391/10-Bit Resolution
SPI and QSPI Serial Interface Compatible

APPLICATIONS
Automotive 0.5 V to 4.5 V Output Span Voltage
Portable Communications
Digitally Controlled Calibration
Servo Controls
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



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PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7390/AD7391 family of 10- and 12-bit voltage-output digital-to-analog converters are designed to operate from a single +3 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in single-supply +3 V systems. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V consuming less than 100 μA making this device ideal for battery operated applications.

The full-scale voltage output is determined by the external reference input voltage applied. The rail-to-rail REF_{IN} to DAC_{OUT} allows for a full-scale voltage set equal the positive supply V_{DD} or any value in between.

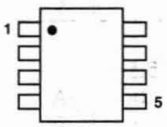
A doubled-buffered serial-data interface offers high speed, three-wire, SPI and microcontroller compatible inputs using data in (SDI), clock (CLK) and load strobe (LD) pins. Additionally, a CLR input sets the output to zero scale at power on or upon user demand.

Both parts are offered in the same pinout to allow the user to select the amount of resolution appropriate for their application without circuit card redesign.

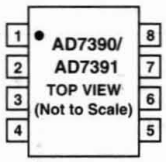
The AD7390/AD7391 are specified over the extended industrial (–40°C to +85°C) temperature range. AD7390/AD7391 are available in plastic DIP, and low profile 1.75 mm height SO-8 surface mount packages. For ultracompact applications the thin 1.1 mm TSSOP-8 package will be available.

PIN CONFIGURATIONS

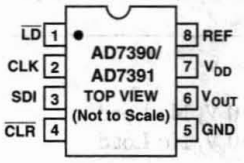
TSSOP-8



SO-8



P-DIP-8



ORDERING GUIDE

Model	RES	Temperature[1]	Package Description	Package Option[2]
AD7390AN	12	XIND	8-Pin P-DIP	N-8
AD7390AR	12	XIND	8-Lead SOIC	SO-8
AD7391AN	10	XIND	8-Pin P-DIP	N-8
AD7391AR	10	XIND	8-Lead SOIC	SO-8
AD7391ARU	10	XIND	TSSOP-8	RU-8

NOTES
[1]XIND = –40°C to +85°C. The AD7390 contains 558 transistors. The die size measures 70 mil × 68 mil.
[2]For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7390/AD7391–SPECIFICATIONS

+3 V Operation (12-Bit and 10-Bit Rail-to-Rail Voltage Out DAC)

(@ V_{DD} = +2.7 V to +3.6 V, V_{REF}IN = 2.5 V, –40°C < T_A < +85°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ[1]	Max	Units
STATIC PERFORMANCE						
Resolution[2]	N	AD7391	10			Bits
	N	AD7390	12			Bits
Relative Accuracy[3]	INL	T_A = +25°C	–1.5	±1/2	+1.5	LSB
Differential Nonlinearity[3]	DNL	T_A = +25°C, Monotonic	–3/4	±1/4	+3/4	LSB
Differential Nonlinearity[3]	DNL	Monotonic	–1	±1/2	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		1.5		mV
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, Data = FFF_H (or BFF_H)		±2		LSB
Full-Scale Tempco[4]	TCV_{FS}			3		ppm/°C
REFERENCE INPUT						
V_{REF}IN Range	V_{REFIN}		GND		V_{DD}	V
Input Resistance	R_{REFIN}			2		MΩ
Input Capacitance[4]	C_{REFIN}			5		pF
ANALOG OUTPUTS						
Output Current (Source)	I_{OUT}	Data = 800_H, (or $A00_H$), ΔV_{OUT} = 5 LSB		1		mA
Output Current (Sink)	I_{OUT}	Data = 800_H, (or $A00_H$), ΔV_{OUT} = 5 LSB		3		mA
Capacitive Load[4]	C_L	No Oscillation		100		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.6	V
Logic Input High Voltage	V_{IH}		V_{DD} – 0.6			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[4]	C_{IL}				10	pF
INTERFACE TIMING SPECIFICATIONS[4, 5]						
Clock Width High	t_{CH}		40			ns
Clock Width Low	t_{CL}		40			ns
Load Pulse Width	t_{LDW}		50			ns
Data Setup	t_{DS}		15			ns
Data Hold	t_{DH}		15			ns
Clear Pulse Width	t_{CLRW}		40			ns
Load Setup	t_{LD1}		15			ns
Load Hold	t_{LD2}		40			ns
Select	t_{CSS}		40			ns
Deselect	t_{CSH}		40			ns
AC CHARACTERISTICS[6]						
Output Slew Rate	SR	Data = 000_H to FFF_H (or BFF_H), to 000_H		0.05		V/µs
Settling Time	t_S	To ±0.1% of Full Scale		75		µs
DAC Glitch	Q			15		nV s
Digital Feedthrough	Q			15		nV s
Feedthrough	V_{OUT}/V_{REF}	Data = 000_H, V_{REF} = 1.5 V dc +1 Vp-p, f = 100 kHz		–65		dB
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7		5.5	V
Positive Supply Current	I_{DD}	V_{DD} = 5 V, V_{IL} = 0 V, No Load		50	100	µA
Power Dissipation	P_{DISS}	V_{DD} = 5 V, V_{IL} = 0 V, No Load		150	300	µW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±10%		0.001	0.006	%/%

PRELIMINARY TECHNICAL DATA

NOTES

[1]Typicals represent average readings measured at +25°C.

[2]One LSB = V_{REF}/4096 V for the 12-bit AD7390, and 1 LSB = V_{REF}/1024 V for the 10-bit AD7391.

[3]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

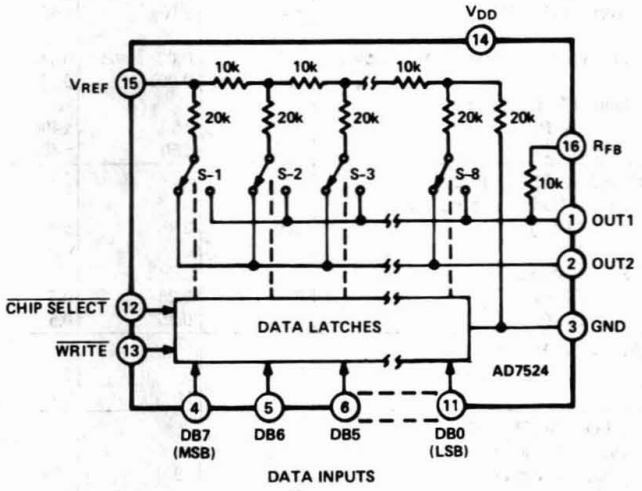
CMOS 8-Bit Buffered Multiplying DAC

AD7524

FEATURES
Microprocessor Compatible (6800, 8085, Z80, etc.)
TTL/CMOS Compatible Inputs
On-Chip Data Latches
Endpoint Linearity
Low Power Consumption
Monotonicity Guaranteed (Full Temperature Range)
Latch Free (No Protection Schottky Required)

APPLICATIONS
Microprocessor Controlled Gain Circuits
Microprocessor Controlled Attenuator Circuits
Microprocessor Controlled Function Generation
Precision AGC Circuits
Bus Structured Instruments

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

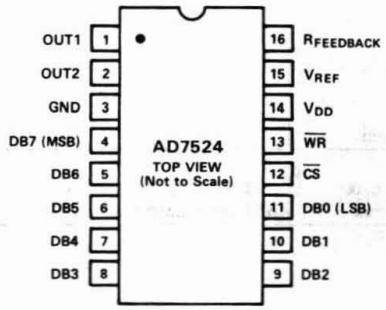
Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8 LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5 V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5 V to +15 V, the AD7524 interfaces directly to most microprocessor buses or output ports.

Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

PIN CONFIGURATION



ORDERING GUIDE

Model[1]	Temperature Range	Nonlinearity (V_{DD} = +15 V)	Package Option[2]
AD7524JN	–40°C to +85°C	±1/2 LSB	N-16
AD7524KN	–40°C to +85°C	±1/4 LSB	N-16
AD7524LN	–40°C to +85°C	±1/8 LSB	N-16
AD7524JP	–40°C to +85°C	±1/2 LSB	P-20A
AD7524KP	–40°C to +85°C	±1/4 LSB	P-20A
AD7524LP	–40°C to +85°C	±1/8 LSB	P-20A
AD7524JR	–40°C to +85°C	±1/2 LSB	R-16A
AD7524AQ	–40°C to +85°C	±1/2 LSB	Q-16
AD7524BQ	–40°C to +85°C	±1/4 LSB	Q-16
AD7524CQ	–40°C to +85°C	±1/8 LSB	Q-16
AD7524SQ	–55°C to +125°C	±1/2 LSB	Q-16
AD7524TQ	–55°C to +125°C	±1/4 LSB	Q-16
AD7524UQ	–55°C to +125°C	±1/8 LSB	Q-16
AD7524SE	–55°C to +125°C	±1/2 LSB	E-20A
AD7524TE	–55°C to +125°C	±1/4 LSB	E-20A
AD7524UE	–55°C to +125°C	±1/8 LSB	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC drawing #5962-87700.
[2]E = Leadless Ceramic Chip Carrier: N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7524—SPECIFICATIONS (V_{REF} = +10 V, V_{OUT1} = V_{OUT2} = 0 V, unless otherwise noted)

Parameter	Limit, T_A = +25°C V_{DD} = +5 V	Limit, T_A = +25°C V_{DD} = +15 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = 5 V	Limit, T_{MIN}, T_{MAX}[1] V_{DD} = +15 V	Units	Test Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy						
J, A, S Versions	±1/2	±1/2	±1/2	±1/2	LSB max	
K, B, T Versions	±1/2	±1/4	±1/2	±1/4	LSB max	
L, C, U Versions	±1/2	±1/8	±1/2	±1/8	LSB max	
Monotonicity	Guaranteed	Guaranteed	Guaranteed	Guaranteed		
Gain Error[2]	±2 1/2	±1 1/4	±3 1/2	±1 1/2	LSB max	
Average Gain TC[3]	±40	±10	±40	±10	ppm/°C	Gain TC Measured from +25°C to T_{MIN} or from +25°C to T_{MAX}
DC Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08	0.02	0.16	0.04	% FSR/% max	ΔV_{DD} = ±10%
	0.002	0.001	0.01	0.005	% FSR/% typ	
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V; V_{REF} = ±10 V
DYNAMIC PERFORMANCE						
Output Current Settling Time[3] (to 1/2 LSB)	400	250	500	350	ns max	OUT1 Load = 100 Ω, C_{EXT} = 13 pF; $\overline{WR}$, $\overline{CS}$ = 0 V; DB0–DB7 = 0 V to V_{DD} to 0 V.
AC Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10 V, 100 kHz Sine Wave; DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
at OUT2	0.25	0.25	0.5	0.5	% FSR max	
REFERENCE INPUT						
R_{IN} (Pin 15 to GND)[4]	5	5	5	5	kΩ min	
	20	20	20	20	kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (Pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	30	30	30	30	pF max	
C_{OUT1} (Pin 1)	30	30	30	30	pF max	DB0–DB7 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT2} (Pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement						
V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement						
V_{IL}	+0.8	+1.5	+0.5	+1.5	V max	
Input Current						
I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0 V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0 V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[5]						See Timing Diagram
t_{CS}						t_{WR} = t_{CS}
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Chip Select to Write Hold Time						
t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t_{WR}						$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
AD7524J, K, L, A, B, C	170	100	220	130	ns min	
AD7524S, T, U	170	100	240	150	ns min	
Data Setup Time						
t_{DS}						
AD7524J, K, L, A, B, C	135	60	170	80	ns min	
AD7524S, T, U	135	60	170	100	ns min	
Data Hold Time						
t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	μA max	All Digital Inputs 0 V or V_{DD}

NOTES

[1]Temperature ranges as follows: J, K, L versions: –40°C to +85°C
A, B, C versions: –40°C to +85°C
S, T, U versions: –55°C to +125°C

[2]Gain error is measured using internal feedback resistor. Full-Scale Range (FSR) = V_{REF}.

[3]Guaranteed not tested.

[4]DAC thin-film resistor temperature coefficient is approximately –300 ppm/°C.

[5]AC parameter, sample tested @ +25°C to ensure conformance to specification.

Specifications subject to change without notice.

ANALOG DEVICES

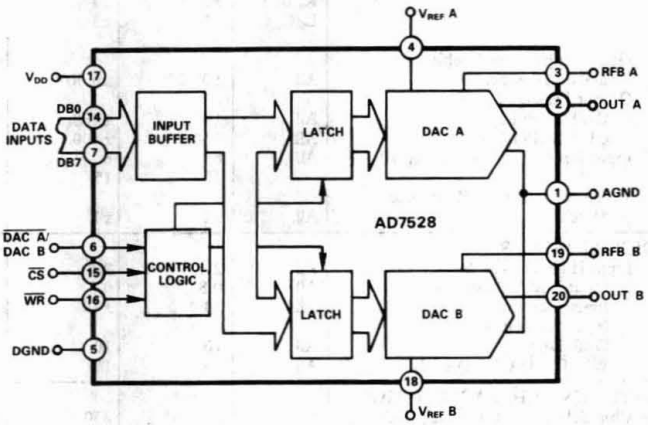
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7528

FEATURES
On-Chip Latches for Both DACs
+5 V to +15 V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS
Digital Control of:
Gain/Attenuation
Filter Parameters
Stereo Audio Circuits
X-Y Graphics

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-pin DIPs and in 20-terminal surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5 V to +15 V power supply, dissipating only 20 mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

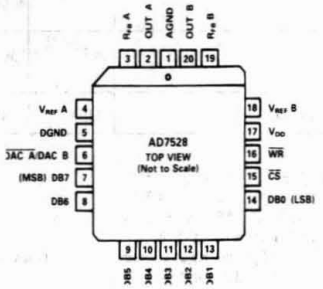
1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in either a small 20-pin DIP, SOIC, PLCC or LCCC.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7528JN	–40°C to +85°C	±1 LSB	±4 LSB	N-20
AD7528KN	–40°C to +85°C	±1/2 LSB	±2 LSB	N-20
AD7528LN	–40°C to +85°C	±1/2 LSB	±1 LSB	N-20
AD7528JP	–40°C to +85°C	±1 LSB	±4 LSB	P-20A
AD7528KP	–40°C to +85°C	±1/2 LSB	±2 LSB	P-20A
AD7528LP	–40°C to +85°C	±1/2 LSB	±1 LSB	P-20A
AD7528JR	–40°C to +85°C	±1 LSB	±4 LSB	R-20
AD7528KR	–40°C to +85°C	±1/2 LSB	±2 LSB	R-20
AD7528LR	–40°C to +85°C	±1/2 LSB	±1 LSB	R-20
AD7528AQ	–40°C to +85°C	±1 LSB	±4 LSB	Q-20
AD7528BQ	–40°C to +85°C	±1/2 LSB	±2 LSB	Q-20
AD7528CQ	–40°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7528SQ	–55°C to +125°C	±1 LSB	±4 LSB	Q-20
AD7528TQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-20
AD7528UQ	–55°C to +125°C	±1/2 LSB	±1 LSB	Q-20
AD7528SE	–55°C to +125°C	±1 LSB	±4 LSB	E-20A
AD7528TE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-20A
AD7528UE	–55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."
[2]Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

DIP, SOIC



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AD7528–SPECIFICATIONS (V_{REF} A = V_{REF} B = +10 V; OUT A = OUT B = 0 V unless otherwise noted)

Parameter	Version[1]	V_{DD} = +5 V		V_{DD} = +15 V		Units	Test Conditions/Comments
		T_A = +25°C	T_{MIN}, T_{MAX}	T_A = +25°C	T_{MIN}, T_{MAX}		
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±1/2	±1/2	±1/2	±1/2	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5
Gain Temperature Coefficient[4]							
ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF}A, V_{REF}B)	All	8	8	8	8	kΩ min	Input Resistance TC = –300 ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11 kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage, V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage, V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current, I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time, t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time, t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time, t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time, t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time, t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time, t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width, t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	All	100	500	100	500	μA max	All Digital Inputs 0 V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended PC Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5 V		V_{DD} = +15 V		Units	Test Conditions/Comments
		T_A = +25°C	T_{MIN}, T_{MAX}	T_A = +25°C	T_{MIN}, T_{MAX}		
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2 LSB. Out A/Out B Load = 100 Ω. $\overline{WR}$ = $\overline{CS}$ = 0 V. DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10 V OUT A, OUT B Load = 100 Ω C_{EXT} = 13 pF $\overline{WR}$ = $\overline{CS}$ = 0 V DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	160		440		nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT}A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT}B		50	50	50	50	pF max	
C_{OUT}A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT}B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	–70	–65	–70	–65	dB max	V_{REF} A, V_{REF} B = 20 V p-p Sine Wave @ 100 kHz
V_{REF} B to OUT B		–70	–65	–70	–65	dB max	
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF}A to OUT B	All	–77		–77		dB typ	V_{REF}A = 20 V p-p Sine Wave @ 100 kHz. V_{REF}B = 0 V See Figure 6.
V_{REF} B to OUT A		–77		–77		dB typ	V_{REF}A = 20 V p-p Sine Wave @ 100 kHz. V_{REF}A = 0 V See Figure 6
DIGITAL CROSSTALK	All	30		60		nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	–85		–85		dB typ	V_{IN} = 6 V rms @ 1 kHz

NOTES

[1]Temperature Ranges are J, K, L: –40°C to +85°C
A, B, C: –40°C to +85°C
S, T, U: –55°C to +125°C

[2]Specification applies to both DACs in AD7528.

[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1 nA.

[4]Guaranteed by design but not production tested.

[5]These characteristics are for design guidance only and are not subject to test.

[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

LC²MOS (8+4) Loading Dual 12-Bit DAC

AD7537

FEATURES
- Two 12-Bit DACs in One Package
- DAC Ladder Resistance Matching: 0.5%
- Space Saving Skinny DIP and Surface Mount Packages
- 4-Quadrant Multiplication
- Low Gain Error (1 LSB max Over Temperature)
- Byte Loading Structure
- Fast Interface Timing

APPLICATIONS
- Automatic Test Equipment
- Programmable Filters
- Audio Applications
- Synchro Applications
- Process Control

GENERAL DESCRIPTION

The AD7537 contains two 12-bit current output DACs on one monolithic chip. A separate reference input is provided for each DAC. The dual DAC saves valuable board space, and the monolithic construction ensures excellent thermal tracking. Both DACs are guaranteed 12-bit monotonic over the full temperature range.

The AD7537 has a 2-byte (8 LSBs, 4 MSBs) loading structure. It is designed for right-justified data format. The control signals for register loading are A0, A1, $\overline{CS}$, $\overline{WR}$ and $\overline{UPD}$. Data is loaded to the input registers when $\overline{CS}$ and $\overline{WR}$ are low. To transfer this data to the DAC registers, $\overline{UPD}$ must be taken low with $\overline{WR}$.

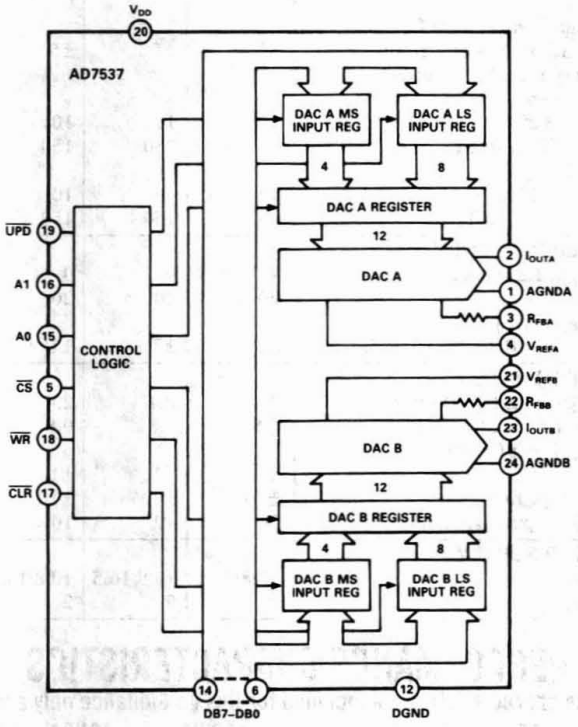
Added features on the AD7537 include an asynchronous $\overline{CLR}$ line which is very useful in calibration routines. When this is taken low, all registers are cleared. The double buffering of the data inputs allows simultaneous update of both DACs. Also, each DAC has a separate AGND line. This increases the device versatility; for instance one DAC may be operated with AGND biased while the other is connected in the standard configuration.

The AD7537 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC and 5 V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching:
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size:
   The AD7537 is packaged in small 24-pin 0.3" DIPs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance:
   The device operates on a +12 V to +15 V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7537JN	–40°C to +85°C	±1 LSB	±6 LSB	N-24
AD7537KN	–40°C to +85°C	±1/2 LSB	±3 LSB	N-24
AD7537LN	–40°C to +85°C	±1/2 LSB	±1 LSB	N-24
AD7537JP	–40°C to +85°C	±1 LSB	±6 LSB	P-28A
AD7537KP	–40°C to +85°C	±1/2 LSB	±3 LSB	P-28A
AD7537LP	–40°C to +85°C	±1/2 LSB	±1 LSB	P-28A
AD7537AQ	–40°C to +85°C	±1 LSB	±6 LSB	Q-24
AD7537BQ	–40°C to +85°C	±1/2 LSB	±3 LSB	Q-24
AD7537CQ	–40°C to +85°C	±1/2 LSB	±1 LSB	Q-24
AD7537SQ	–55°C to +125°C	±1 LSB	±6 LSB	Q-24
AD7537TQ	–55°C to +125°C	±1/2 LSB	±3 LSB	Q-24
AD7537UQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-24
AD7537SE	–55°C to +125°C	±1 LSB	±6 LSB	E-28A
AD7537TE	–55°C to +125°C	±1/2 LSB	±3 LSB	E-28A
AD7537UE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7537–SPECIFICATIONS

(V_{DD} = +12 V to +15 V, ±10%, V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = AGND = 0 V, I_{OUTB} = AGNDB = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Measured using R_{FBA}, R_{FBB}. Both DAC registers loaded with all 1s.
Gain Temperature Coefficient[2];								
ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1 ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14 kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB}								
Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12 V to +15 V; V_{REFA} = V_{REFB} = +10 V; I_{OUTA} = AGNDA = 0 V, I_{OUTB} = AGNDB = 0 V. Output Amplifiers are AD644 except where noted.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5		μs max	To 0.01% of full-scale range. I_{OUT} load = 100 Ω, C_{EXT} = 13 pF. DAC output measured from falling edge of $\overline{WR}$. Typical Value of Settling Time is 0.8 μs.
Digital-to-Analog Glitch Impulse	7		nV-s typ	Measured with V_{REFA} = V_{REFB} = 0 V. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	–70	–65	dB max	V_{REFA}, V_{REFB} = 20 V p-p 10 kHz sine wave.
V_{REFB} to I_{OUTB}	–70	–65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max – V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0s
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1s
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	–84		dB typ	V_{REFA} = 20 V p-p 10 kHz sine wave, V_{REFB} = 0 V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	–84		dB typ	V_{REFB} = 20 V p-p 10 kHz sine wave, V_{REFA} = 0 V. Both DACs loaded with all 1s.
Digital Crosstalk	7		nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF.
Output Noise Voltage Density (10 Hz–100 kHz)	25		nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10 Hz–100 kHz.
Total Harmonic Distortion	–82		dB typ	V_{IN} = 6 V rms, 1 kHz. Both DACs loaded with all 1s.

NOTES

[1]Temperature range as follows: J, K, L Versions: –40°C to +85°C; A, B, C Versions: –40°C to +85°C; S, T, U Versions: –55°C to +125°C

[2]Sample tested at +25°C to ensure compliance.

[3]Functional at V_{DD} = 5 V, with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

LC²MOS µP-Compatible 14-Bit DAC

AD7538

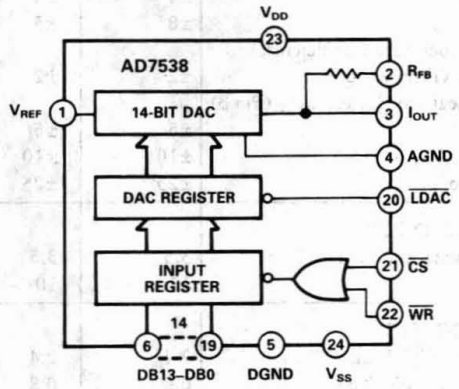
FEATURES

- All Grades 14-Bit Monotonic Over the Full Temperature Range
- Low Cost 14-Bit Upgrade for 12-Bit Systems
- 14-Bit Parallel Load with Double Buffered Inputs
- Small 24-Pin, 0.3" DIP and SOIC
- Low Output Leakage (<20 nA) Over the Full Temperature Range

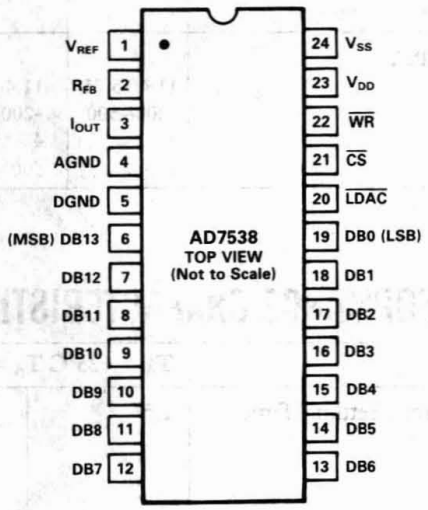
APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio
- Precision Servo Control
- Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
DIP, SOIC



GENERAL DESCRIPTION

The AD7538 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

The DAC is loaded by a single 14-bit wide word using standard Chip Select and Memory Write Logic. Double buffering, which is optional using $\overline{LDAC}$, allows simultaneous update in a system containing multiple AD7538s.

A novel low leakage configuration (U.S. Patent No. 4,590,456) enables the AD7538 to exhibit excellent output leakage current characteristics over the specified temperature range.

The AD7538 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7538 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Cost
   The AD7538, with its 14-bit dynamic range, affords a low cost solution for 12-bit system upgrades.
3. Small Package Size
   The AD7538 is packaged in a small 24-pin, 0.3" DIP and a 24-pin SOIC.
4. Low Output Leakage
   By tying V_{SS} (Pin 24) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
5. Wide Power Supply Tolerance
   The device operates on a +12 V to +15 V V_{DD}, with a ±5% tolerance on this nominal figure. All specifications are guaranteed over this range.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full-Scale Error	Package Option*
AD7538JN	0°C to +70°C	±2 LSB	±8 LSB	N-24
AD7538KN	0°C to +70°C	±1 LSB	±4 LSB	N-24
AD7538JR	0°C to +70°C	±2 LSB	±8 LSB	R-24
AD7538KR	0°C to +70°C	±1 LSB	±4 LSB	R-24
AD7538AQ	–25°C to +85°C	±2 LSB	±8 LSB	Q-24
AD7538BQ	–25°C to +85°C	±1 LSB	±4 LSB	Q-24
AD7538SQ	–55°C to +125°C	±2 LSB	±8 LSB	Q-24
AD7538TQ	–55°C to +125°C	±1 LSB	±4 LSB	Q-24

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

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AD7538–SPECIFICATIONS[1] (V_{DD} = +11.4 V to +15.75 V[2], V_{REF} = +10 V; V_{PIN3} = V_{PIN4} = 0 V, V_{SS} = –300 mV. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J, K Versions	A, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All Grades Guaranteed Monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Over Temperature.
Full-Scale Error						Measured Using Internal R_{FB} DAC
+25°C	±4	±4	±4	±4	LSB max	Registers Loaded with All 1s.
T_{MIN} to T_{MAX}	±8	±5	±10	±6	LSB max	
Gain Temperature Coefficient[3];						
ΔGain/ΔTemperature	±2	±2	±2	±2	ppm/°C typ	
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All Digital Inputs 0 V
T_{MIN} to T_{MAX}	±10	±10	±20	±20	nA max	V_{SS} = –300 mV
T_{MIN} to T_{MAX}	±25	±25	±150	±150	nA max	V_{SS} = 0 V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6 kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0 V or V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specification Guaranteed Over
V_{SS} Range	–200/–500	–200/–500	–200/–500	–200/–500	mV min/mV max	This Range
I_{DD}	4	4	4	4	mA max	All Digital Inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All Digital Inputs 0 V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4 V to +15.75 V, V_{REF} = +10 V, V_{PIN3} = V_{PIN4} = 0 V, V_{SS} = 0 V or –300 mV, Output Amplifier is AD711 except where noted.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5		μs max	To 0.003% of Full-Scale Range. I_{OUT} Load= 100 Ω, C_{EXT} = 13 pF. DAC Register Alternately Loaded with All 1s and All 0s. Typical Value of Settling Time Is 0.8 μs.
Digital to Analog Glitch Impulse	20		nV-sec typ	Measured with V_{REF} = 0 V. I_{OUT} Load = 100 Ω, C_{EXT} = 13 pF. DAC Register Alternately Loaded with All 1s and All 0s.
Multiplying Feedthrough Error	3	5	mV p-p typ	V_{REF} = ±10 V, 10 kHz Sine Wave DAC Register Loaded with All 0s.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC Register Loaded with All 1s
C_{OUT} (Pin 3)	130	130	pF max	DAC Register Loaded with All 0s
Output Noise Voltage Density (10 Hz–100 kHz)	15		$nV\sqrt{Hz}$ typ	Measured Between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: J, K Versions: 0°C to +70°C
A, B Versions: –25°C to +85°C
S, T Versions: –55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4 V to +15.75 V. At V_{DD} = 5 V, the device is fully functional with degraded specifications.

[3]Sample tested to ensure compliance.

Specifications subject to change without notice.

ANALOG DEVICES

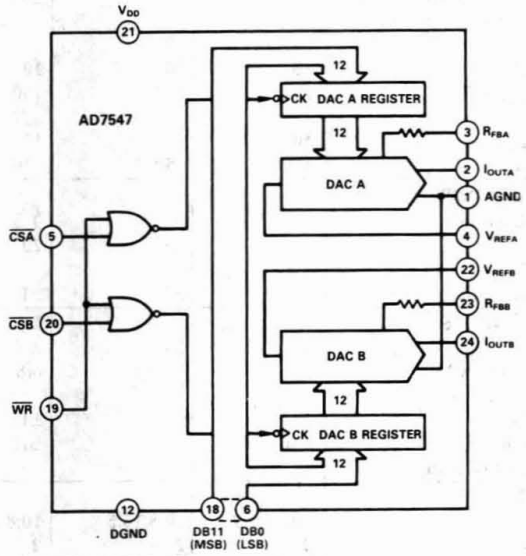
LC²MOS Parallel Loading Dual 12-Bit DAC

AD7547

FEATURES
Two 12-Bit DACs in One Package
DAC Ladder Resistance Matching: 0.5%
Space Saving Skinny DIP and Surface Mount Packages
4-Quadrant Multiplication
Low Gain Error (1 LSB max Over Temperature)
Fast Interface Timing

APPLICATIONS
Automatic Test Equipment
Programmable Filters
Audio Applications
Synchro Applications
Process Control

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7547 contains two 12-bit current output DACs on one monolithic chip. Also on-chip are the level shifters, data registers and control logic for easy microprocessor interfacing. There are 12 data inputs. $\overline{CSA}$, $\overline{CSB}$, $\overline{WR}$ control DAC selection and loading. Data is latched into the DAC registers on the rising edge of $\overline{WR}$. The device is speed compatible with most microprocessors and accepts TTL, 74HC and 5 V CMOS logic level inputs.

The D/A converters provide 4-quadrant multiplication capabilities with separate reference inputs and feedback resistors. Monolithic construction ensures that thermal and gain error tracking is excellent. 12-bit monotonicity is guaranteed for both DACs over the full temperature range.

The AD7547 is manufactured using the Linear Compatible CMOS (LC²MOS) process. This allows fast digital logic and precision linear circuitry to be fabricated on the same die.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. Many applications which are not practical using two discrete DACs are now possible. Typical matching: 0.5%.
2. Small Package Size
   The AD7547 is available in 0.3" wide 24-pin DIPs and SOICs and in 28-terminal surface mount packages.
3. Wide Power Supply Tolerance
   The device operates on a +12 V to +15 V V_{DD}, with ±10% tolerance on this nominal figure. All specifications are guaranteed over this range.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Gain Error	Package Option[3]
AD7547JN	–40°C to +85°C	±1 LSB	±6 LSB	N-24
AD7547KN	–40°C to +85°C	±1/2 LSB	±3 LSB	N-24
AD7547LN	–40°C to +85°C	±1/2 LSB	±1 LSB	N-24
AD7547JP	–40°C to +85°C	±1 LSB	±6 LSB	P-28A
AD7547KP	–40°C to +85°C	±1/2 LSB	±3 LSB	P-28A
AD7547LP	–40°C to +85°C	±1/2 LSB	±1 LSB	P-28A
AD7547JR	–40°C to +85°C	±1 LSB	±6 LSB	R-24
AD7547KR	–40°C to +85°C	±1/2 LSB	±3 LSB	R-24
AD7547LR	–40°C to +85°C	±1/2 LSB	±1 LSB	R-24
AD7547AQ	–40°C to +85°C	±1 LSB	±6 LSB	Q-24
AD7547BQ	–40°C to +85°C	±1/2 LSB	±3 LSB	Q-24
AD7547CQ	–40°C to +85°C	±1/2 LSB	±1 LSB	Q-24
AD7547SQ	–55°C to +125°C	±1 LSB	±6 LSB	Q-24
AD7547TQ	–55°C to +125°C	±1/2 LSB	±3 LSB	Q-24
AD7547UQ	–55°C to +125°C	±1/2 LSB	±2 LSB	Q-24
AD7547SE	–55°C to +125°C	±1 LSB	±6 LSB	E-28A
AD7547TE	–55°C to +125°C	±1/2 LSB	±3 LSB	E-28A
AD7547UE	–55°C to +125°C	±1/2 LSB	±2 LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship ceramic packages (D-24A) in lieu of cerdip packages (Q-24).
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheets.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

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AD7547–SPECIFICATIONS[1] (V_{DD} = +12 V to +15 V, ±10%, V_{REFA} = V_{REFB} = 10 V; I_{OUTA} = I_{OUTB} = AGND = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	L, C Versions	S Version	T Version	U Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1/2	±1	±1/2	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Gain Error	±6	±3	±1	±6	±3	±2	LSB max	Both DAC registers loaded with all 1s.
Gain Temperature Coefficient[2];								
ΔGain/ΔTemperature	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1 ppm/°C
Output Leakage Current								
I_{OUTA}								
+25°C	10	10	10	10	10	10	nA max	DAC A Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s.
I_{OUTB}								
+25°C	10	10	10	10	10	10	nA max	DAC B Register loaded
T_{MIN} to T_{MAX}	150	150	150	250	250	250	nA max	with all 0s.
REFERENCE INPUT								
Input Resistance	9	9	9	9	9	9	kΩ min	Typical Input Resistance = 14 kΩ
	20	20	20	20	20	20	kΩ max	
V_{REFA}, V_{REFB}								
Input Resistance Match	±3	±3	±1	±3	±3	±1	% max	Typically ±0.5%
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	10	10	10	10	10	10	pF max	
POWER SUPPLY[3]								
V_{DD}	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	2	2	2	2	2	2	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12 V to +15 V; V_{REFA} = V_{REFB} = +10 V, I_{OUTA} = I_{OUTB} = AGND = 0 V. Output Amplifiers are AD644 except where noted.)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5		μs max	To 0.01 % of full-scale range. I_{OUT} load = 100 Ω, C_{EXT} = 13 pF. DAC output measured from rising edge of $\overline{WR}$. Typical Value of Settling Time is 0.8 μs.
Digital-to-Analog Glitch Impulse	7		nV-s typ	Measured with V_{REFA} = V_{REFB} = 0 V. I_{OUTA}, I_{OUTB} load = 100 Ω, C_{EXT} = 13 pF. DAC registers alternately loaded with all 0s and all 1s.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	–70	–65	dB max	V_{REFA}, V_{REFB} = 20 V p-p, 10 kHz sine wave. DAC
V_{REFB} to I_{OUTB}	–70	–65	dB max	registers loaded with all 0s.
Power Supply Rejection				
$\Delta Gain/\Delta V_{DD}$	±0.01	±0.02	% per % max	ΔV_{DD} = V_{DD} max – V_{DD} min
Output Capacitance				
C_{OUTA}	70	70	pF max	DAC A, DAC B loaded with all 0s.
C_{OUTB}	70	70	pF max	
C_{OUTA}	140	140	pF max	DAC A, DAC B loaded with all 1s.
C_{OUTB}	140	140	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	–84		dB typ	V_{REFA} = 20 V p-p 10 kHz sine wave, V_{REFB} = 0 V. Both DACs loaded with all 1s.
V_{REFB} to I_{OUTA}	–84		dB typ	V_{REFB} = 20 V p-p 10 kHz sine wave, V_{REFA} = 0 V. Both DACs loaded with all 1s.
Digital Crosstalk	7		nV-s typ	Measured for a Code Transition of all 0s to all 1s. I_{OUTA}, I_{OUTB} Load = 100 Ω, C_{EXT} = 13 pF
Output Noise Voltage Density (10 Hz–100 kHz)	25		nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}. Frequency of measurement is 10 Hz–100 kHz.
Total Harmonic Distortion	–82		dB typ	V_{IN} = 6 V rms, 1 kHz. Both DACs loaded with all 1s.

NOTES

[1]Temperature range as follows: J, K, L Versions, –40°C to +85°C; A, B, C Versions, –40°C to +85°C; S, T, U Versions, –55°C to +125°C.

[2]Sample tested at +25°C to ensure compliance.

[3]Functional at V_{DD} = 5 V with degraded specifications.

[4]Pin 12 (DGND) on ceramic DIPs is connected to lid.

Specifications subject to change without notice.

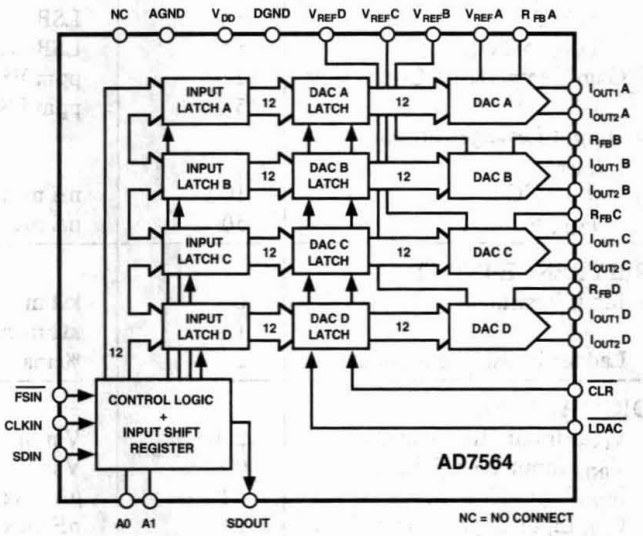
LC²MOS
+3.3 V/+5 V, Low Power, Quad 12-Bit DAC

AD7564

FEATURES
Four 12-Bit DACs in One Package
4-Quadrant Multiplication
Separate References
Single Supply Operation
Guaranteed Specifications with +3.3 V/+5 V Supply
Low Power
Versatile Serial Interface
Simultaneous Update Capability
Reset Function
28-Pin SOIC, SSOP and DIP Packages

APPLICATIONS
Process Control
Portable Instrumentation
General Purpose Test Equipment

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7564 contains four 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals. These DACs operate from a single +3.3 V to +5 V supply.

The AD7564 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. Two address pins A0 and A1 set up a device address, and this feature may be used to simplify device loading in a multi-DAC environment. Alternatively, A0 and A1 can be ignored and the serial out capability used to configure a daisy-chained system.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input, and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

The device is packaged in 28-pin SOIC, SSOP and DIP packages.

PRODUCT HIGHLIGHTS

1. The AD7564 contains four 12-bit current output DACs with separate V_{REF} inputs.
2. The AD7564 can be operated from a single +3.3 V to +5 V supply.
3. Simultaneous update capability and reset function are available.
4. The AD7564 features a fast, versatile serial interface compatible with modern 3 V and 5 V microprocessors and microcomputers.
5. Low power, 50 μW at 5 V and 33 μW at 3.3 V.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Nominal Supply Voltage	Package Option*
AD7564BN	–40°C to +85°C	±0.5	+5 V	N-28
AD7564BR	–40°C to +85°C	±0.5	+5 V	R-28
AD7564BRS	–40°C to +85°C	±0.5	+5 V	RS-28
AD7564AR-B	–40°C to +85°C	±1	+3.3 V to +5 V	R-28
AD7564ARS-B	–40°C to +85°C	±1	+3.3 V to +5 V	RS-28

*N = DIP; R = SOIC; RS = SSOP. For outline information see Package Information section.

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AD7564–SPECIFICATIONS

Normal Mode

(V_{DD} = +4.75 V to +5.25 V; $I_{OUT1}A$ to $I_{OUT1}D$ = $I_{OUT2}A$ = $I_{OUT2}D$ = AGND = 0 V; V_{REF} = +10 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	B Grade[1]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 2.44 mV when V_{REF} = 10 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	All Grades Guaranteed Monotonic Over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient[2]	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	
T_{MIN} to T_{MAX}	50	nA max	
REFERENCE INPUT			
Input Resistance	6	kΩ min	Typical Input Resistance = 9.5 kΩ
	13	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	µA max	
C_{IN}, Input Capacitance[2]	10	pF max	
DIGITAL OUTPUT (SDOUT)			
Output Low Voltage (V_{OL})	0.4	V max	Load Circuit as in Figure 2.
Output High Voltage (V_{OH})	4.0	V min	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	Part Functions from 3.3 V to 5.25 V
Power Supply Rejection[2]			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD}	10	µA max	V_{INH} = V_{DD}, V_{INL} = 0 V At Input Levels of 0.8 V and 2.4 V, I_{DD} is Typically 2 mA.

NOTES

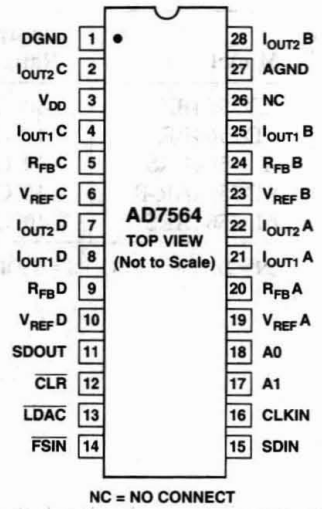
[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Not production tested. Guaranteed by characterization at initial product release.

Specifications subject to change without notice.

PIN CONFIGURATION

DIP, SOIC and SSOP Packages



NC = NO CONNECT

ANALOG DEVICES

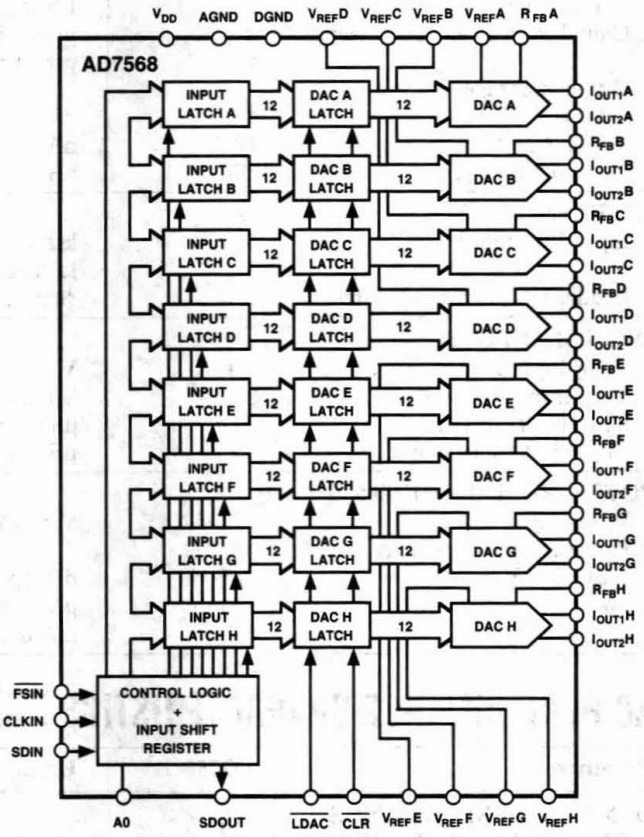
LC²MOS Octal 12-Bit DAC

AD7568

FEATURES
Eight 12-Bit DACs in One Package
4-Quadrant Multiplication
Separate References
Single +5 V Supply
Low Power: 1 mW
Versatile Serial Interface
Simultaneous Update Capability
Reset Function
44-Pin PQFP and PLCC

APPLICATIONS
Process Control
Automatic Test Equipment
General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7568 contains eight 12-bit DACs in one monolithic device. The DACs are standard current output with separate V_{REF}, I_{OUT1}, I_{OUT2} and R_{FB} terminals.

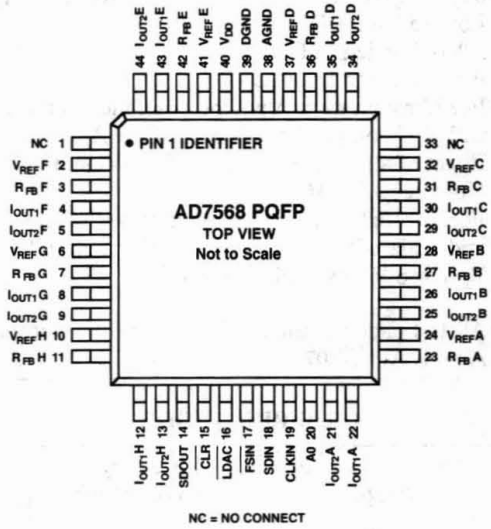
The AD7568 is a serial input device. Data is loaded using $\overline{FSIN}$, CLKIN and SDIN. One address pin, A0, sets up a device address, and this feature may be used to simplify device loading in a multi-DAC environment.

All DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and they can be cleared by asserting the asynchronous $\overline{CLR}$ input.

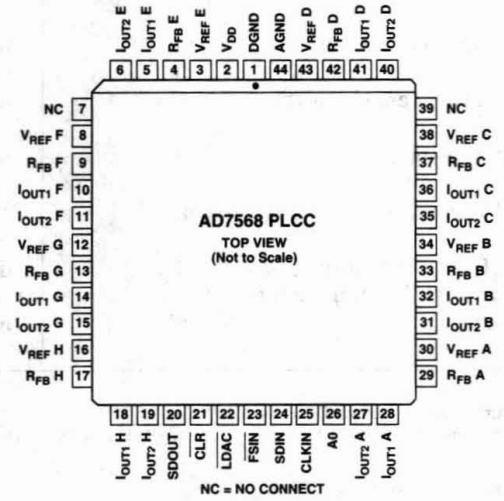
The AD7568 is housed in a space-saving 44-pin plastic quad flatpack and 44-lead PLCC.

PIN CONFIGURATIONS

Plastic Quad Flatpack



Plastic Leaded Chip Carrier



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AD7568–SPECIFICATIONS[1] (V_{DD} = +4.75 V to +5.25 V; I_{OUT1} = I_{OUT2} = 0 V; V_{REF} = +5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
ACCURACY			
Resolution	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 1.22 mV when V_{REF} = 5 V
Relative Accuracy	±0.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error			
+25°C	±4	LSBs max	
T_{MIN} to T_{MAX}	±5	LSBs max	
Gain Temperature Coefficient	2	ppm FSR/°C typ	
	5	ppm FSR/°C max	
Output Leakage Current			
I_{OUT1}			
@ +25°C	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	200	nA max	
REFERENCE INPUT			
Input Resistance	5	kΩ min	Typical Input Resistance = 7 kΩ
	9	kΩ max	
Ladder Resistance Mismatch	2	% max	Typically 0.6%
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{DD} Range	4.75/5.25	V min/V max	
Power Supply Sensitivity			
$\Delta Gain/\Delta V_{DD}$	–75	dB typ	
I_{DD}	300	μA max	V_{INH} = 4.0 V min, V_{INL} = 0.4 V max
	3.5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max

AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to test. DAC output op amp is AD843.)

Parameter	AD7568B[2]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	500	ns typ	To 0.01% of Full-Scale Range. DAC Latch Alternately Loaded with All 0s and All 1s.
Digital to Analog Glitch Impulse	40	nV–s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error	–66	dB max	V_{REF} = 20 V pk-pk, 10 kHz Sine Wave. DAC Latch Loaded with All 0s.
Output Capacitance	60	pF max	All 1s Loaded to DAC.
	30	pF max	All 0s Loaded to DAC.
Channel-to-Channel Isolation	–76	dB typ	Feedthrough from Any One Reference to the Others with 20 V pk-pk, 10 kHz Sine Wave Applied.
Digital Crosstalk	40	nV–s typ	Effect of all 0s to all 1s Code Transition on Nonselected DACs.
Digital Feedthrough	40	nV–s typ	Feedthrough to Any DAC Output with $\overline{FSIN}$ High and Square Wave Applied to SDIN and SCLK.
Total Harmonic Distortion	–83	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
Output Noise Spectral Density			
@ 1 kHz	20	nV/√Hz	All 1s Loaded to the DAC. V_{REF} = 0 V. Output Op Amp is AD OP07.

NOTES
[1]Temperature range as follows: B Version: –40°C to +85°C.
[2]All specifications also apply for V_{REF} = +10 V, except relative accuracy which degrades to ±1 LSB.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	Package Option*
AD7568BS	–40°C to +85°C	±0.5	S-44
AD7568BP	–40°C to +85°C	±0.5	P-44A

*S = Plastic Quad Flatpack (PQFP), P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

3.3 V to 5 V Quad 10-Bit DACs

AD7804/AD7805*

FEATURES

- Four 10-Bit DACs in One Package
- Serial and Parallel Loading Facilities Available
  - AD7804 Quad 10-Bit Serial Loading
  - AD7805 Quad 10-Bit Parallel Loading
- 3.3 V to 5 V Operation
- Power-Down Mode
- Power-On Reset
- Standby Mode (All DACs/Individual DACs)
- Low Power All CMOS Construction
- 10-Bit Resolution
- Double Buffered DAC Registers
- Dual External Reference Capability

APPLICATIONS

- Optical Disk Drives
- Instrumentation and Communication Systems
- Process Control and Voltage Setpoint Control
- Trim Potentiometer Replacement
- Automatic Calibration

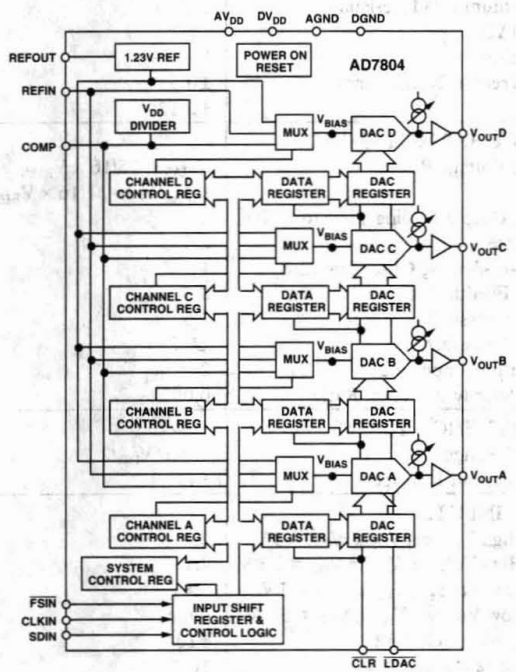
GENERAL DESCRIPTION

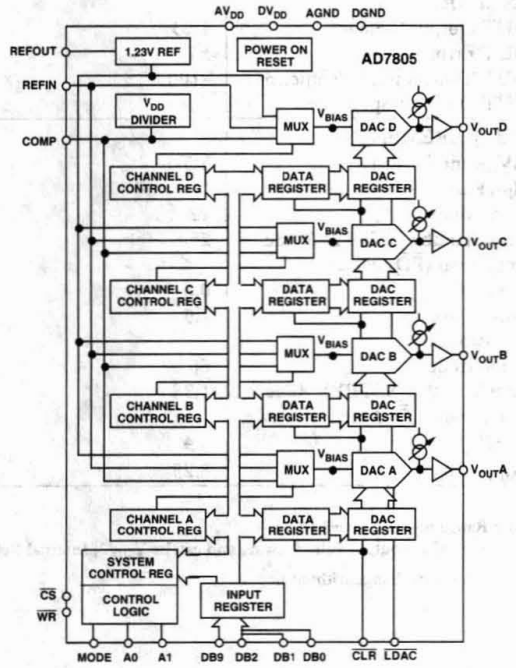
The AD7804 is a quad 10-bit digital-to-analog converter, with serial load capabilities, while the AD7805 is a quad 10-bit digital-to-analog converter with parallel load capabilities. This part operates from a +3.3 V to +5 V (±10%) power supply and incorporates an onboard reference. These DACs provide output signals in the form of $V_{BIAS} \pm V_{SWING}$. V_{SWING} is derived internally from V_{BIAS}. On-chip control registers include a system control register and channel control registers. The system control register has control over all DACs in the package. The channel control registers allow individual control of DACs. The complete transfer function of each individual DAC can be shifted around the V_{BIAS} point using an on-chip Sub DAC. All DACs contain double buffered data inputs, which allow all analog outputs to be simultaneously updated using the asynchronous $\overline{LDAC}$ input.

Control Features	Channels Controlled	Main DAC	Sub DAC
Hardware Clear	All	√	√
System Control			
Power Down*	All	√	√
System Standby**	All	√	√
System Clear	All	√	
Input Coding	All	√	√
Channel Control			
Channel Standby**	Selective	√	√
Channel Clear	Selective	√	
V_{BIAS}	Selective	√	√

*Powerdown function powers down all internal circuitry including the reference.
**Standby functions power down all circuitry except for the reference.

FUNCTIONAL BLOCK DIAGRAMS





*Patent pending.

AD7804/AD7805–SPECIFICATIONS (AV_{DD} and DV_{DD} = 3.3 V ± 10% to 5 V ± 10%; AGND = DGND = 0 V; Reference = Internal Reference; C_L = 100 pF; R_L = 2 kΩ to GND. Sub DAC at Midscale. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade[1]	C Grade[1]	Units	Comments
STATIC PERFORMANCE				
MAIN DAC				
Resolution	10	10	Bits	
Relative Accuracy	±3	±2	LSB max	Guaranteed Monotonic
Bias Offset Error	±35	±35	mV max	DAC Code = 0.5 Full Scale
Plus and Minus Full-Scale Error	±35	±35	mV max	
Minimum Load Resistance	2	2	kΩ min	
SUB DAC				
Resolution	8	8	Bits	
Differential Nonlinearity	±0.5	±0.5	LSB max	Refers to an LSB of the Main DAC
	±0.125	±0.125	LSB typ	
OUTPUT CHARACTERISTICS				
Output Voltage Range[2]	V_{BIAS} ± 15/16 × V_{BIAS}	V_{BIAS} ± 15/16 × V_{BIAS}	V	2s Complement Coding
	V_{BIAS}/16 to 31/16 × V_{BIAS}	V_{BIAS}/16 to 31/16 × V_{BIAS}	V	Offset Binary Coding
Voltage Output Settling Time to 10 Bits	4	4	µs max	Typically 1.5 µs
Slew Rate	2.5	2.5	V/µs typ	
Digital-to-Analog Glitch Impulse	1	1	nV-s typ	1 LSB Change Around the Major Carry
Digital Feedthrough	0.5	0.5	nV-s typ	
Digital Crosstalk	0.5	0.5	nV-s typ	
Analog Crosstalk	±0.2	±0.2	LSB typ	
DC Output Impedance	2	2	Ω typ	
Power Supply Rejection Ratio	0.002	0.002	%/% typ	ΔV_{DD} ± 10%
DAC REFERENCE INPUTS				
REF IN Range	1.0 to V_{DD}/2	1.0 to V_{DD}/2	V min to V max	
REF IN Input Leakage	±1	±1	µA max	Typically ±1 nA
DIGITAL INPUTS				
Input High Voltage, V_{IH} @ V_{DD} = 5 V	2.4	2.4	V min	
Input High Voltage, V_{IH} @ V_{DD} = 3.3 V	2.1	2.1	V min	
Input Low Voltage, V_{IL} @ V_{DD} = 5 V	0.8	0.8	V max	
Input Low Voltage, V_{IL} @ V_{DD} = 3.3 V	0.6	0.6	V max	
Input Leakage Current	±10	±10	µA max	
Input Capacitance	10	10	pF max	
Input Coding	2s Comp/Binary	2s Comp/Binary		
REFERENCE OUTPUT				
REF OUT Output Voltage	1.23	1.23	V nom	
REF OUT Error	±7	±7	% max	
REF OUT Temperature Coefficient	–100	–100	ppm/°C typ	
REF OUT Output Impedance	5	5	kΩ nom	
POWER REQUIREMENTS				
V_{DD} (AV_{DD} and DV_{DD})	3/5.5	3/5.5	V min to V max	
I_{DD} (AI_{DD} Plus DI_{DD})				Excluding Load Currents
Normal Mode	12	12	mA max	V_{IH} = V_{DD}, V_{IL} = DGND
System Standby ($\overline{SSTBY}$) Mode	250	250	µA	V_{IH} = V_{DD}, V_{IL} = DGND
Power Down ($\overline{PD}$) Mode				
@ +25°C	0.8	0.8	µA max	V_{IH} = V_{DD}, V_{IL} = DGND
T_{MIN}–T_{MAX}	1.5	1.5	µA max	
Power Dissipation				Excluding Power Dissipated in Load
Normal Mode	66	66	mW max	
System Standby ($\overline{SSTBY}$) Mode	1.38	1.38	mW max	
Power Down ($\overline{PD}$) Mode				
@ +25°C	4.4	4.4	µW max	
T_{MIN}–T_{MAX}	8.25	8.25	µW max	

NOTES

[1]Temperature Range is –40°C to +85°C.

[2]V_{BIAS} is the center of the output voltage swing and can be V_{DD}/2, Internal Reference or REFIN as determined by MX1 and MX0 in the channel control register.

Specifications subject to change without notice.

3.3 V to 5 V Octal 10-Bit DACs

AD7808/AD7809

FEATURES

- Four 10-Bit DACs in One Package
- Serial and Parallel Loading Facilities Available
  - AD7808 Octal 10-Bit Serial Loading
  - AD7809 Octal 10-Bit Parallel Loading
- 3.3 V to 5 V Operation
- Power-Down Mode
- Power-On Reset
- Standby Mode (All DACs/Individual DACs)
- Low Power All CMOS Construction
- 10-Bit Resolution
- Double Buffered DAC Registers
- Dual External Reference Capability

APPLICATIONS

- Optical Disk Drives
- Instrumentation and Communication Systems
- Process Control and Voltage Setpoint Control
- Trim Potentiometer Replacement
- Automatic Calibration

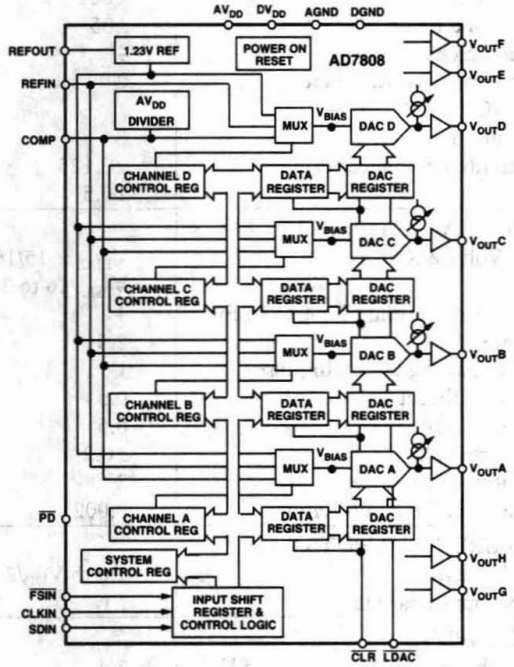
GENERAL DESCRIPTION

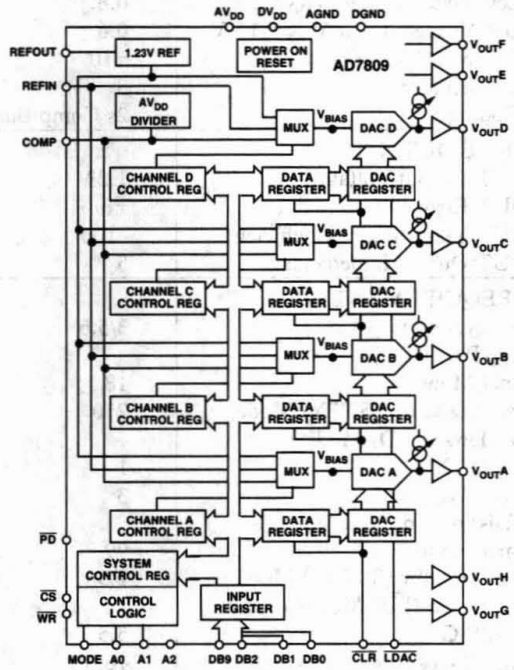
The AD7808 is an octal 10-bit digital-to-analog converter with serial load capabilities, while the AD7809 is an octal 10-bit digital-to-analog converter with parallel load capabilities. These parts operate from a +3.3 V to +5 V (±10%) power supply and incorporate an on-chip reference. These DACs provide output signals in the form of V_{BIAS} ±V_{SWING}. V_{SWING} is derived internally from V_{BIAS}. On-chip control registers include a system control register and channel control registers. The system control register has control over all DACs in the package. The channel control registers allow individual control of DACs. The complete transfer function of each individual DAC can be shifted around the V_{BIAS} point using an on-chip Sub DAC. All DACs contain double buffered data inputs, which allow all analog outputs to be simultaneously updated using the asynchronous $\overline{LDAC}$ input.

Control Features	Channels Controlled	Main DAC	Sub DAC
Hardware Clear	All	√	√
System Control			
Power Down*	All	√	√
System Standby**	All	√	√
System Clear	All	√	
Input Coding	All	√	√
Channel Control			
Channel Standby**	Selective	√	√
Channel Clear	Selective	√	
V_{BIAS}	Selective	√	√

*Power-down function powers down all internal circuitry including the reference.
**Standby functions power down all circuitry except for the reference.

FUNCTIONAL BLOCK DIAGRAMS





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AD7808/AD7809–SPECIFICATIONS

(AV_{DD} and DV_{DD} = 3.3 V ± 10% to 5 V ± 10%; AGND = DGND = 0 V; Reference = Internal Reference; C_L = 100 pF; R_L = 2 kΩ to GND. Sub DAC at Midscale. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Grade[1]	Units	Comments
STATIC PERFORMANCE			
MAIN DAC			
Resolution	10	Bits	
Relative Accuracy	±4	LSB max	
Gain Error	±3	% FSR max	
Bias Offset Error[2]	±60	mV max	DAC Code = 0.5 Full Scale
Zero-Scale Error	±35	mV max	DAC Code = 000H for Offset Binary
Monotonicity	9	Bits	and 200H for Twos Complement
Minimum Load Resistance	2	kΩ min	Coding
SUB DAC			
Resolution	8	Bits	
Differential Nonlinearity	±0.125	LSB typ	Refers to an LSB of the Main DAC
	±0.5	LSB max	
OUTPUT CHARACTERISTICS			
Output Voltage Range[3]	$V_{BIAS} \pm 15/16 \times V_{BIAS}$	V	2s Complement Coding
	$V_{BIAS}/16$ to $31/16 \times V_{BIAS}$	V	Offset Binary Coding
Voltage Output Settling Time to 10 Bits	4	µs max	Typically 1.5 µs
Slew Rate	2.5	V/µs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB Change Around the Major Carry
Digital Feedthrough	0.5	nV-s typ	
Digital Crosstalk	0.5	nV-s typ	
Analog Crosstalk	±0.2	LSB typ	
DC Output Impedance	2	Ω typ	
Power Supply Rejection Ratio	0.002	%/% typ	$\Delta V_{DD} \pm 10\%$
DAC REFERENCE INPUTS			
REF IN Range	1.0 to $V_{DD}/2$	V min to V max	
REF IN Input Leakage	±1	µA max	Typically ±1 nA
DIGITAL INPUTS			
Input High Voltage, V_{IH} @ V_{DD} = 5 V	2.4	V min	
Input High Voltage, V_{IH} @ V_{DD} = 3.3 V	2.1	V min	
Input Low Voltage, V_{IL} @ V_{DD} = 5 V	0.8	V max	
Input Low Voltage, V_{IL} @ V_{DD} = 3.3 V	0.6	V max	
Input Leakage Current	±10	µA max	
Input Capacitance	8	pF max	
Input Coding	2s Comp/Binary		
REFERENCE OUTPUT			
REF OUT Output Voltage	1.23	V nom	
REF OUT Error	±8	% max	
REF OUT Temperature Coefficient	–100	ppm/°C typ	
REF OUT Output Impedance	5	kΩ nom	
POWER REQUIREMENTS			
V_{DD} (AV_{DD} and DV_{DD})	3/5.5	V min to V max	
I_{DD} (AI_{DD} Plus DI_{DD})			Excluding Load Currents
Normal Mode	18	mA max	$V_{IH} = V_{DD}$, V_{IL} = DGND
System Standby ($\overline{SSTBY}$) Mode	250	µA max	$V_{IH} = V_{DD}$, V_{IL} = DGND
Power-Down ($\overline{PD}$) Mode			
@ +25°C	1	µA max	$V_{IH} = V_{DD}$, V_{IL} = DGND
T_{MIN}–T_{MAX}	3	µA max	
Power Dissipation			Excluding Power Dissipated in Load
Normal Mode	99	mW max	
System Standby ($\overline{SSTBY}$) Mode	1.38	mW max	
Power-Down ($\overline{PD}$) Mode			
@ +25°C	5.5	µW max	
T_{MIN}–T_{MAX}	16.5	µW max	

NOTES

[1]Temperature Range is –40°C to +85°C.

[2]Can be minimized using the Sub DAC.

[3]V_{BIAS} is the center of the output voltage swing and can be $V_{DD}/2$, Internal Reference or REFIN as determined by MX1 and MX0 in the channel control register.

Specifications subject to change without notice.

LC²MOS Quad 14-Bit DACs

AD7834/AD7835

FEATURES

Four 14-Bit DACs in One Package
AD7834—Serial Loading
AD7835—Parallel 8-/14-Bit Loading
Voltage Outputs
Power-On Reset Function
Max/Min Output Voltage Range of +/–8.192 V
Maximum Output Voltage Span of 14 V
Common Voltage Reference Inputs
User Assigned Device Addressing
Clear Function to User-Defined Voltage
Surface Mount Packages
AD7834—28-Pin SO, DIP and Cerdip
AD7835—44-Pin PQFP and PLCC

APPLICATIONS

Process Control
Automatic Test Equipment
General Purpose Instrumentation

GENERAL DESCRIPTION

The AD7834 and AD7835 contain four 14-bit DACs on one monolithic chip. The AD7834 and AD7835 have output voltages in the range of ±8.192 V with a maximum span of 14 V.

The AD7834 is a serial input device. Data is loaded in 16-bit format from the external serial bus, MSB first after two leading 0s, into one of the input latches via DIN, SCLK and $\overline{\text{FSYNC}}$. The AD7834 has five dedicated package address pins, PA0–PA4, that can be wired to AGND or V_{CC} to permit up to 32 AD7834s to be individually addressed in a multipackage application.

The AD7835 can accept either 14-bit parallel loading or double-byte loading, where right-justified data is loaded in one 8-bit and one 6-bit byte. Data is loaded from the external bus into one of the input latches under the control of the $\overline{\text{WR}}$, $\overline{\text{CS}}$, $\overline{\text{BYSHF}}$ and DAC channel address pins, A0–A2.

With either device, the $\overline{\text{LDAC}}$ signal can be used to update either all four DAC outputs simultaneously or individually, on reception of new data. In addition, for either device, the asynchronous $\overline{\text{CLR}}$ input can be used to set all signal outputs, $V_{OUT}1$–$V_{OUT}4$, to the user-defined voltage level on the Device Sense Ground pin, DSG. On power-on, before the power supplies have stabilized, internal circuitry holds the DAC output voltage levels to within ±2 V of the DSG potential. As the supplies stabilize, the DAC output levels move to the exact DSG potential (assuming $\overline{\text{CLR}}$ is exercised).

The AD7834 is available in 28-pin 0.3" SO and 0.6" DIP packages, and the AD7835 is available in a 44-pin PQFP package and a 44-pin PLCC package.

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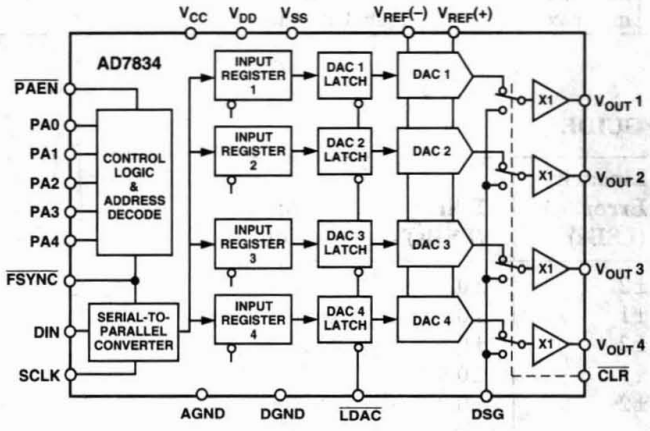
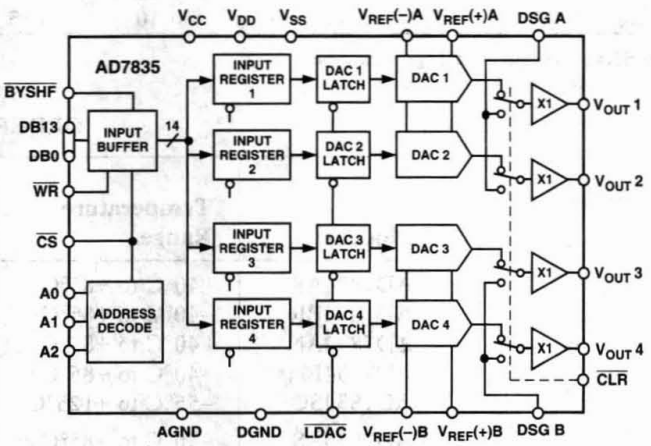
AD7834 FUNCTIONAL BLOCK DIAGRAM



AD7835 FUNCTIONAL BLOCK DIAGRAM



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AD7834/AD7835–SPECIFICATIONS (V_{CC} = +5 V ± 5%; V_{DD} = +15 V ± 5%; V_{SS} = –15 V ± 5%; AGND = DGND = 0 V; T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A	B	S	Units	Test Conditions/Comments
ACCURACY					
Resolution	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic Over Temperature
Full-Scale Error					$V_{REF}(+)$ = +7 V, $V_{REF}(-)$ = –7 V
T_{MIN} to T_{MAX}	±5	±5	±8	mV max	
Zero-Scale Error	±4	±4	±5	mV max	$V_{REF}(+)$ = +7 V, $V_{REF}(-)$ = –7 V
Gain Error	±0.5	±0.5	±0.5	mV typ	$V_{REF}(+)$ = +7 V, $V_{REF}(-)$ = –7 V
Gain Temperature Coefficient[2]	4	4	4	ppm FSR/°C typ	
	20	20	20	ppm FSR/°C max	
DC Crosstalk[2]	50	50	50	µV max	See Terminology. R_L = 10 kΩ
REFERENCE INPUTS					
DC Input Resistance	30	30	30	MΩ typ	
Input Current	±1	±1	±1	µA max	Per Input
$V_{REF}(+)$ Range	0/+8.192	+7/+8.192	0/+8.192	V min/max	
$V_{REF}(-)$ Range	–8.192/0	–8.192/0	–8.192/0	V min/max	
$[V_{REF}(+)–V_{REF}(-)]$	5/14	7/14	5/14	V min/max	For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed
DEVICE SENSE GROUND INPUTS					
Input Current	±2	±2	±2	µA max	Per Input. V_{DSG} = –2 V to +2 V
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	µA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
POWER REQUIREMENTS					
V_{CC}	5.0	5.0	5.0	V nom	±5% for Specified Performance
V_{DD}	15.0	15.0	15.0	V nom	±5% for Specified Performance
V_{SS}	–15.0	–15.0	–15.0	V nom	±5% for Specified Performance
Power Supply Sensitivity					
ΔFull Scale/ΔV_{DD}	110	110	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	100	100	dB typ	
I_{CC}	0.2	0.2	0.5	mA max	V_{INH} = V_{CC}, V_{INL} = DGND
	3	3	3	mA max	AD7834. V_{INH} = 2.4 V min, V_{INL} = 0.8 V max
	6	6	6	mA max	AD7835. V_{INH} = 2.4 V min, V_{INL} = 0.8 V max
I_{DD}	10	10	15	mA max	AD7834. Outputs Unloaded
	15	15	15	mA max	AD7835. Outputs Unloaded
I_{SS}	10	10	15	mA max	Outputs Unloaded

Specifications subject to change without notice

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	DNL (LSBs)	Package Option*
AD7834AR	–40°C to +85°C	±2	±0.9	R-28
AD7834BR	–40°C to +85°C	±1	±0.9	R-28
AD7834AN	–40°C to +85°C	±2	±0.9	N-28
AD7834BN	–40°C to +85°C	±1	±0.9	N-28
AD7834SQ	–55°C to +125°C	±2	±0.9	Q-28
AD7835AS	–40°C to +85°C	±2	±0.9	S-44
AD7835BS	–40°C to +85°C	±1	±0.9	S-44
AD7835AP	–40°C to +85°C	±2	±0.9	P-44A

*R = Small Outline IC (SOIC); N = Plastic DIP; Q = Cerdip; S = Plastic Quad Flatpack (PQFP); P = Plastic Leaded Chip Carrier (PLCC). For outline information see Package Information section.

ANALOG DEVICES

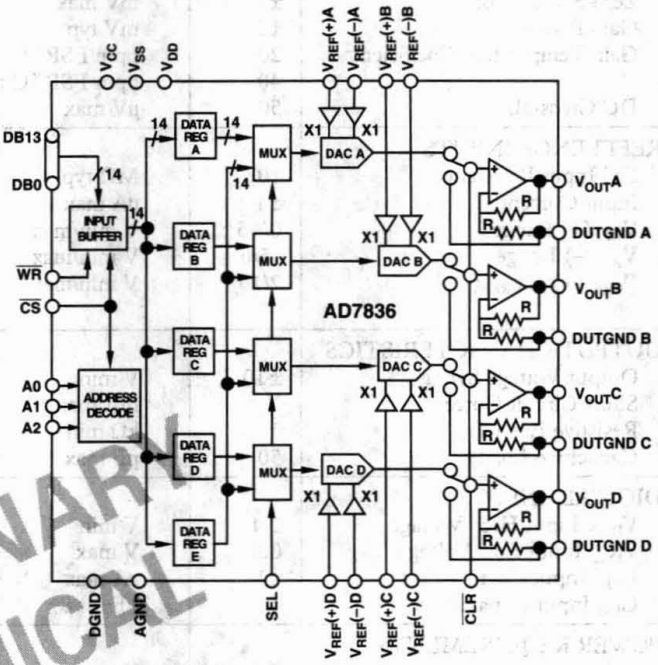
LC²MOS Quad 14-Bit DAC

AD7836

FEATURES
Four 14-Bit DACs in One Package
Voltage Outputs
Seperate Offset Adjust for Each Output
Reference Range of ±5 V
Maximum Output Voltage Range of ±10 V
Clear Function to User-Defined Code
44-Pin PQFP Package

APPLICATIONS
Process Control
Automatic Test Equipment
General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7836 contains four 14-bit DACs on one monolithic chip. It has output voltages with a full-scale range of ±10 V from reference voltages of ±5 V.

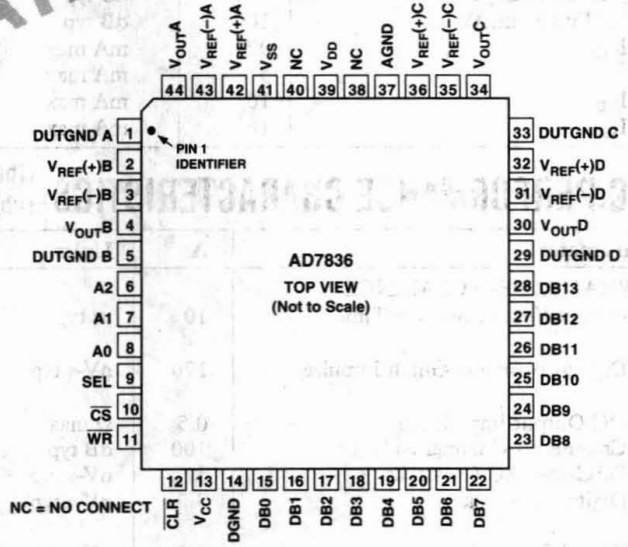
The AD7836 accepts 14-bit parallel loaded data from the external bus into one of the input latches under the control of the $\overline{WR}$, $\overline{CS}$ and DAC channel address pins, A0–A2.

The DAC outputs are updated individually, on reception of new data. In addition, the SEL input can be used to apply the user programmed value in DAC register E to all DACs, thus setting all DAC output voltages to the same level. The contents of the DAC data registers are not affected by the SEL input.

Each DAC output is buffered with a gain of two amplifier into which an external DAC offset voltage can be inserted via the DUTGNDx pins.

The AD7836 is available in a 44-pin PQFP package.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSBs)	DNL (LSBs)	Package Option*
AD7836AS	–40°C to +85°C	±2	±0.9	S-44

*S = Plastic Quad Flatpack (PQFP). For outline information see Package Information section.

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AD7836–SPECIFICATIONS

(V_{CC} = +5 V ± 5%; V_{DD} = +15 V ± 5%; V_{SS} = –15 V ± 5%; AGND = DGND = 0 V; T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A	Units	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy	±2	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed Monotonic Over Temperature
Full-Scale Error			$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V
+25°C	±5	mV max	
T_{MIN} to T_{MAX}	±5	mV max	
Zero-Scale Error	±4	mV max	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V
Gain Error	±2	mV typ	$V_{REF}(+)$ = +5 V, $V_{REF}(-)$ = –5 V
Gain Temperature Coefficient[2]	20	ppm FSR/°C typ	
	40	ppm FSR/°C max	
DC Crosstalk[2]	50	µV max	See Terminology. R_L = 10 kΩ
REFERENCE INPUTS			
DC Input Resistance	10	MΩ typ	
Input Current	±1	µA max	Per Input
$V_{REF}(+)$ Range	0/+5	V min/max	
$V_{REF}(-)$ Range	–5/0	V min/max	
$[V_{REF}(+) - V_{REF}(-)]$	2/10	V min/max	For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed
OUTPUT CHARACTERISTICS			
Output Voltage Swing	±10	V min	$(V_{REF}(-)+[V_{REF}(+)-V_{REF}(-)]\cdot D) - V_{DUTDGN}$
Short Circuit Current	X	mA max	
Resistive Load	5	kΩ min	To 0 V
Capacitive Load	50	pF max	To 0 V
DIGITAL INPUTS			
V_{INH}, Input High Voltage	2.4	V min	
V_{INL}, Input Low Voltage	0.8	V max	
I_{INH}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	10	pF max	
POWER REQUIREMENTS			
V_{CC}	5.0	V nom	±5% for Specified Performance
V_{DD}	15.0	V nom	±5% for Specified Performance
V_{SS}	–15.0	V nom	±5% for Specified Performance
Power Supply Sensitivity			
ΔFull Scale/ΔV_{DD}	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	dB typ	
I_{CC}	0.5	mA max	V_{INH} = V_{CC}, V_{INL} = DGND
	5	mA max	V_{INH} = 2.4 V min, V_{INL} = 0.8 V max
I_{DD}	16	mA max	Outputs Unloaded
I_{SS}	16	mA max	Outputs Unloaded

PRELIMINARY TECHNICAL DATA

AC PERFORMANCE CHARACTERISTICS

(These characteristics are included for Design Guidance and are not subject to production testing.)

Parameter	A	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	10	µs typ	Full-Scale Change to ±1/2 LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Digital-to-Analog Glitch Impulse	120	nV-s typ	Measured with $V_{REF}(+)$ = $V_{REF}(-)$ = 0 V. DAC Latch Alternately Loaded with All 0s and All 1s
DC Output Impedance	0.5	Ω max	See Terminology
Channel-to-Channel Isolation	100	dB typ	See Terminology; Applies to the AD7835 Only
DAC-to-DAC Crosstalk	3	nV-s typ	See Terminology
Digital Crosstalk	3	nV-s typ	Feedthrough to DAC Output Under Test Due to Change in Digital Input Code to Another Converter
Digital Feedthrough	0.2	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density			
@ 1 kHz	40	nV/$\sqrt{Hz}$ typ	All 1s Loaded to DAC. $V_{REF}(+)$ = $V_{REF}(-)$ = 0 V

NOTES

[1]Temperature range for A Version: –40°C to +85°C

[2]Guaranteed by design.

Specifications subject to change without notice.

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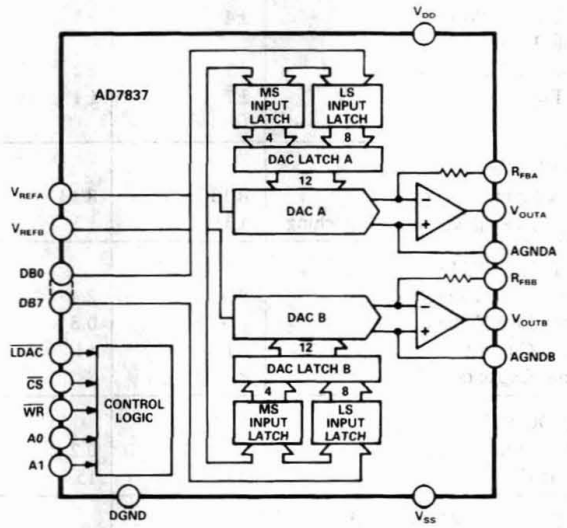
LC²MOS Complete, Dual 12-Bit MDACs

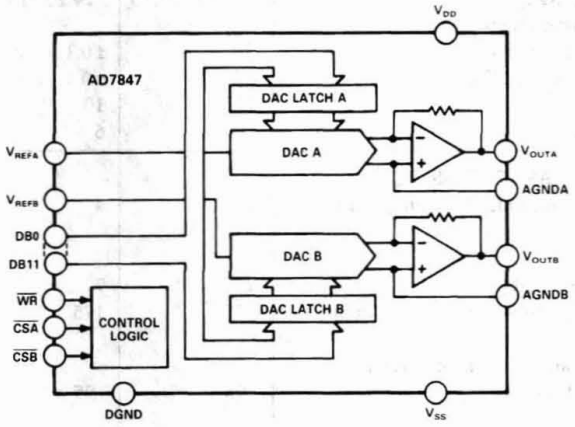
AD7837/AD7847

FEATURES
- Two 12-Bit MDACs with Output Amplifiers
- 4-Quadrant Multiplication
- Space-Saving 0.3", 24-Pin DIP and 24-Terminal SOIC Package
- Parallel Loading Structure: AD7847
- (8 + 4) Loading Structure: AD7837

APPLICATIONS
- Automatic Test Equipment
- Function Generation
- Waveform Reconstruction
- Programmable Power Supplies
- Synchro Applications

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7837/AD7847 is a complete, dual, 12-bit multiplying digital-to-analog converter with output amplifiers on a monolithic CMOS chip. No external user trims are required to achieve full specified performance.

Both parts are microprocessor compatible, with high speed data latches and interface logic. The AD7847 accepts 12-bit parallel data which is loaded into the respective DAC latch using the $\overline{WR}$ input and a separate Chip Select input for each DAC. The AD7837 has a double-buffered 8-bit bus interface structure with data loaded to the respective input latch in two write operations. An asynchronous $\overline{LDAC}$ signal on the AD7837 updates the DAC latches and analog outputs.

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy	Package Option[2]
AD7837AN	–40°C to +85°C	±1 LSB	N-24
AD7837BN	–40°C to +85°C	±1/2 LSB	N-24
AD7837AR	–40°C to +85°C	±1 LSB	R-24
AD7837BR	–40°C to +85°C	±1/2 LSB	R-24
AD7837AQ	–40°C to +85°C	±1 LSB	Q-24
AD7837BQ	–40°C to +85°C	±1/2 LSB	Q-24
AD7837SQ	–55°C to +125°C	±1 LSB	Q-24
AD7847AN	–40°C to +85°C	±1 LSB	N-24
AD7847BN	–40°C to +85°C	±1/2 LSB	N-24
AD7847AR	–40°C to +85°C	±1 LSB	R-24
AD7847BR	–40°C to +85°C	±1/2 LSB	R-24
AD7847AQ	–40°C to +85°C	±1 LSB	Q-24
AD7847BQ	–40°C to +85°C	±1/2 LSB	Q-24
AD7847SQ	–55°C to +125°C	±1 LSB	Q-24

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[2]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

The output amplifiers are capable of developing ±10 V across a 2 kΩ load. They are internally compensated with low input offset voltage due to laser trimming at wafer level.

The amplifier feedback resistors are internally connected to V_{OUT} on the AD7847.

The AD7837/AD7847 is fabricated in Linear Compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic.

A novel low leakage configuration (U.S. Patent No. 4,590,456) ensures low offset errors over the specified temperature range.

PRODUCT HIGHLIGHTS

1. The AD7837/AD7847 is a dual, 12-bit, voltage-out MDAC on a single chip. This single chip design offers considerable space saving and increased reliability over multichip designs.
2. The AD7837 and the AD7847 provide a fast versatile interface to 8-bit or 16-bit data bus structures.

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AD7837/AD7847–SPECIFICATIONS[1] (V_{DD} = +15 V ± 5%, V_{SS} = –15 V ± 5%, AGNDA = AGNDB = DGND = 0 V. V_{REFA} = V_{REFB} = +10 V, R_L = 2 kΩ, C_L = 100 pF [V_{OUT} connected to R_{FB} AD7837]. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version	B Version	S Version	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	12	12	12	Bits	
Relative Accuracy[2]	±1	±1/2	±1	LSB max	
Differential Nonlinearity[2]	±1	±1	±1	LSB max	Guaranteed Monotonic
Zero Code Offset Error[2]					
@ +25°C	±2	±2	±2	mV max	DAC Latch Loaded with All 0s
T_{MIN} to T_{MAX}	±4	±3	±5	mV max	Temperature Coefficient = ±5 µV/°C typ
Gain Error[2]					
@ +25°C	±5	±2	±5	LSB max	DAC Latch Loaded with All 1s
T_{MIN} to T_{MAX}	±7	±4	±7	LSB max	Temperature Coefficient = ±2 ppm of FSR/°C typ
REFERENCE INPUTS					
V_{REF} Input Resistance	8/13	8/13	8/13	kΩ min/max	Typical Input Resistance = 10 kΩ
V_{REFA}, V_{REFB} Resistance Matching	±3	±3	±3	% max	Typically ±0.5%
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	
Input Current	±1	±1	±1	µA max	Digital Inputs at 0 V and V_{DD}
Input Capacitance[3]	8	8	8	pF max	
ANALOG OUTPUTS					
DC Output Impedance	0.2	0.2	0.2	Ω typ	
Short Circuit Current	15	15	15	mA typ	V_{OUT} Connected to AGND
POWER REQUIREMENTS[4]					
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	V min/max	
V_{SS} Range	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	V min/max	
Power Supply Rejection					
$\Delta Gain/\Delta V_{DD}$	±0.1	±0.1	±0.1	% per % max	V_{DD} = 15 V ± 5%, V_{REF} = –10 V
$\Delta Gain/\Delta V_{SS}$	±0.1	±0.1	±0.1	% per % max	V_{SS} = –15 V ± 5%, V_{REF} = +10 V
I_{DD}	10	10	10	mA max	Output Unloaded. Typically 5 mA
I_{SS}	6	6	6	mA max	Output Unloaded. Typically 4 mA
AC CHARACTERISTICS[2, 3]					
Voltage Output Settling Time	4	4	4	µs typ	Settling Time to Within ±1/2 LSB of Final Value. DAC Latch Alternately Loaded with All 0s and All 1s
Slew Rate	7	7	7	V/µs typ	
Digital-to-Analog Glitch Impulse	175	175	175	nV secs typ	DAC Latch Alternately Loaded with 01 . . . 11 and 10 . . . 00
Channel-to-Channel Isolation					
V_{REFA} to V_{OUTB}	–95	–95	–95	dB typ	V_{REFA} = 20 V p-p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
V_{REFB} to V_{OUTA}	–95	–95	–95	dB typ	V_{REFB} = 20 V p-p, 10 kHz Sine Wave. DAC Latches Loaded with All 0s
Multiplying Feedthrough Error	–90	–90	–90	dB typ	V_{REF} = 20 V p-p, 10 kHz Sine Wave. DAC Latch Loaded with All 0s
Unity Gain Small Signal BW	600	600	600	kHz typ	V_{REF} = 100 mV p-p Sine Wave. DAC Latch Loaded with All 1s
Full Power BW	110	110	90	kHz typ	V_{REF} = 20 V p-p Sine Wave. DAC Latch Loaded with All 1s
Total Harmonic Distortion	–88	–88	–88	dB typ	V_{REF} = 6 V rms, 1 kHz. DAC Latch Loaded with All 1s
Digital Crosstalk	10	10	10	nV secs typ	Code Transition from All 0s to All 1s
Output Noise Voltage @ +25°C (0.1 Hz to 10 Hz)	2	2	2	µV rms typ	See Typical Performance Graphs Amplifier Noise and Johnson Noise of R_{FB}

NOTES

[1]Temperature ranges are as follows: A, B Versions, –40°C to +85°C; S Version, –55°C to +125°C.

[2]See Terminology.

[3]Sample tested @ +25°C to ensure compliance.

[4]The Devices are functional with V_{DD}/V_{SS} = ±12 V (See typical performance graphs.)

Specifications subject to change without notice.

LC²MOS Complete 14-Bit DAC

AD7840

FEATURES

Complete 14-Bit Voltage Output DAC
Parallel and Serial Interface Capability
80 dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors
e.g., ADSP-2100, TMS32010, TMS32020
45 ns min $\overline{WR}$ Pulse Width
Low Power – 70 mW typ.
Operates from ±5 V Supplies

GENERAL DESCRIPTION

The AD7840 is a fast, complete 14-bit voltage output D/A converter. It consists of a 14-bit DAC, 3 V buried Zener reference, DAC output amplifier and high speed control logic.

The part features double-buffered interface logic with a 14-bit input latch and 14-bit DAC latch. Data is loaded to the input latch in either of two modes, parallel or serial. This data is then transferred to the DAC latch under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 21 ns allows direct parallel interfacing to digital signal processors and high speed 16-bit microprocessors. In the serial mode, the maximum serial data clock rate can be as high as 6 MHz.

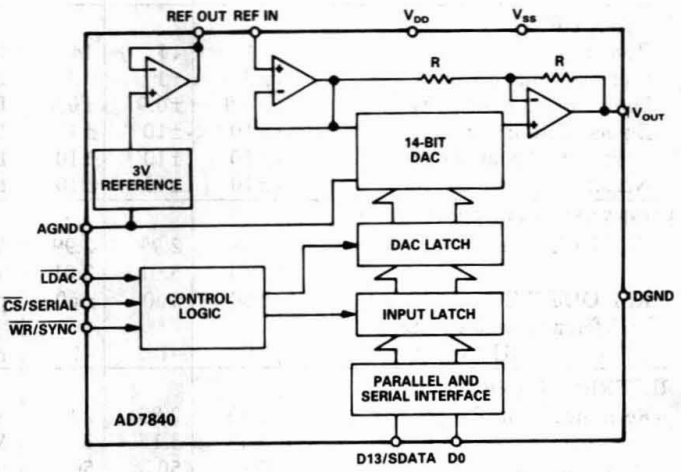
The analog output from the AD7840 provides a bipolar output range of ±3 V. The AD7840 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion as well as for traditional dc specifications. Full power output signals up to 20 kHz can be created.

The AD7840 is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin plastic and hermetic dual-in-line package (DIP) and is also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

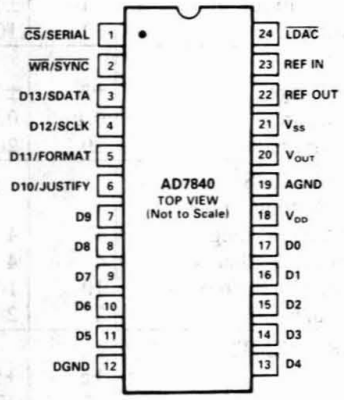
1. Complete 14-Bit D/A Function
   The AD7840 provides the complete function for creating ac signals and dc voltages to 14-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 14-bit D/A converter.
2. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7840 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Fast, Versatile Microprocessor Interface
   The AD7840 is capable of 14-bit parallel and serial interfacing. In the parallel mode, data setup times of 21 ns and write pulse widths of 45 ns make the AD7840 compatible with modern 16-bit microprocessors and digital signal processors. In the serial mode, the part features a high data transfer rate of 6 MHz.

FUNCTIONAL BLOCK DIAGRAM

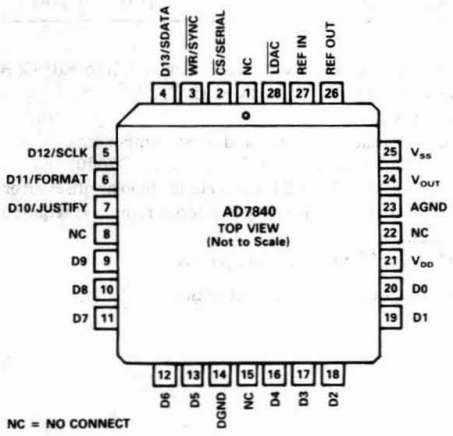


PIN CONFIGURATIONS

DIP/SSOP



PLCC



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AD7840–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, REF IN = +3 V, R_L = 2 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J, A[1]	K, B[1]	S[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]					
Signal to Noise Ratio[3] (SNR)	76	78	76	dB min	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically 82 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Total Harmonic Distortion (THD)	–78	–80	–78	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically –84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
Peak Harmonic or Spurious Noise	–78	–80	–78	dB max	V_{OUT} = 1 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically –84 dB at +25°C for 0 < V_{OUT} < 20 kHz[4]
DC ACCURACY					
Resolution	14	14	14	Bits	
Integral Nonlinearity	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	±10	LSB max	
Positive Full Scale Error[5]	±10	±10	±10	LSB max	
Negative Full Scale Error[5]	±10	±10	±10	LSB max	
REFERENCE OUTPUT[6]					
REF OUT @ +25°C	2.99 3.01	2.99 3.01	2.99 3.01	V min V max	
REF OUT TC	±60	±60	±60	ppm/°C max	
Reference Load Change (ΔREF OUT vs. ΔI)	–1	–1	–1	mV max	Reference Load Current Change (0–500 μA)
REFERENCE INPUT					
Reference Input Range	2.85 3.15	2.85 3.15	2.85 3.15	V min V max	3 V ± 5%
Input Current	50	50	50	μA max	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current ($\overline{CS}$ Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	pF max	
ANALOG OUTPUT					
Output Voltage Range	±3	±3	±3	V nom	
DC Output Impedance	0.1	0.1	0.1	Ω typ	
Short-Circuit Current	20	20	20	mA typ	
AC CHARACTERISTICS[7]					
Voltage Output Settling Time					Settling Time to within ±1/2 LSB of Final Value
Positive Full-Scale Change	4	4	4	μs max	Typically 2 μs
Negative Full-Scale Change	4	4	4	μs max	Typically 2.5 μs
Digital-to-Analog Glitch Impulse	10	10	10	nV secs typ	
Digital Feedthrough	2	2	2	nV secs typ	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	–5	–5	–5	V nom	±5% for Specified Performance
I_{DD}	14	14	15	mA max	Output Unloaded, SCLK = +5 V. Typically 10 mA
I_{SS}	6	6	7	mA max	Output Unloaded, SCLK = +5 V. Typically 4 mA
Power Dissipation	100	100	110	mW max	Typically 70 mW

NOTES

[1]Temperature ranges are as follows: J, K Versions, 0°C to +70°C; A, B Versions, –25°C to +85°C; S Version, –55°C to +125°C.

[2]V_{OUT} (pk-pk) = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Using external sample-and-hold (see Testing the AD7840).

[5]Measured with respect to REF IN and includes bipolar offset error.

[6]For capacitive loads greater than 50 pF, a series resistor is required (see Internal Reference section).

[7]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

ORDERING GUIDE

Model[1]	Temperature Range	SNR (dB)	Integral Nonlinearity (LSB)	Package Option[2]
AD7840JN	0°C to +70°C	78 min	±2 max	N-24
AD7840KN	0°C to +70°C	80 min	±1 max	N-24
AD7840JP	0°C to +70°C	78 min	±2 max	P-28A
AD7840KP	0°C to +70°C	80 min	±1 max	P-28A
AD7840AQ	–25°C to +85°C	78 min	±2 max	Q-24
AD7840ARS	–25°C to +85°C	78 min	±2 max	RS-24
AD7840BQ	–25°C to +85°C	80 min	±1 max	Q-24
AD7840SQ[3]	–55°C to +125°C	78 min	±2 max	Q-24

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.

[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

[3]This grade will be available to /883B processing only.

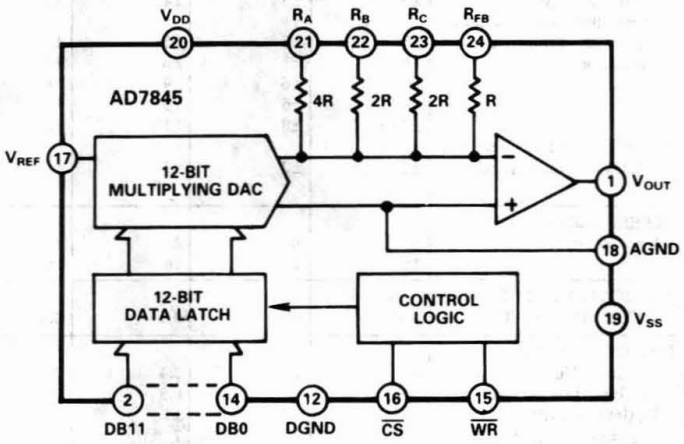
LC²MOS Complete 12-Bit Multiplying DAC

AD7845

FEATURES
- 12-Bit CMOS MDAC with Output Amplifier
- 4-Quadrant Multiplication
- Guaranteed Monotonic (T_{MIN} to T_{MAX})
- Space-Saving 0.3" DIPs and 24- or 28-Terminal Surface Mount Packages
- Application Resistors On Chip for Gain Ranging, etc.
- Low Power LC²MOS

APPLICATIONS
- Automatic Test Equipment
- Digital Attenuators
- Programmable Power Supplies
- Programmable Gain Amplifiers
- Digital-to-4–20 mA Converters

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7845 is the industry's first 4-quadrant multiplying D/A converter with an on-chip amplifier. It is fabricated on the LC²MOS process, which allows precision linear components and digital circuitry to be implemented on the same chip.

The 12 data inputs drive latches which are controlled by standard $\overline{CS}$ and $\overline{WR}$ signals, making microprocessor interfacing simple. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs can be tied to ground, making all latches transparent. All digital inputs are TTL and 5 V CMOS compatible.

The output amplifier can supply ±10 V into a 2 kΩ load. It is internally compensated, and its input offset voltage is low due to laser trimming at wafer level. For normal operation, R_{FB} is tied to V_{OUT}, but the user may alternatively choose R_A, R_B or R_C to scale the output voltage range.

PRODUCT HIGHLIGHTS

1. Voltage Output Multiplying DAC
   The AD7845 is the first DAC which has a full 4-quadrant multiplying capability and an output amplifier on chip. All specifications include amplifier performance.
2. Matched Application Resistors
   Three application resistors provide an easy facility for gain ranging, voltage offsetting, etc.
3. Space Saving
   The AD7845 saves space in two ways. The integration of the output amplifier on chip means that chip count is reduced. The part is housed in skinny 24-pin 0.3" DIP, 28-terminal LCC and PLCC and 24-terminal SOIC packages.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Package Option[3]
AD7845JN	0°C to +70°C	±1 LSB	N-24
AD7845KN	0°C to +70°C	±1/2 LSB	N-24
AD7845JP	0°C to +70°C	±1 LSB	P-28A
AD7845KP	0°C to +70°C	±1/2 LSB	P-28A
AD7845JR	0°C to +70°C	±1 LSB	R-24
AD7845KR	0°C to +70°C	±1/2 LSB	R-24
AD7845AQ	–25°C to +85°C	±1 LSB	Q-24
AD7845BQ	–25°C to +85°C	±1/2 LSB	Q-24
AD7845SQ/883B	–55°C to +125°C	±1 LSB	Q-24
AD7845TQ/883B	–55°C to +125°C	±1/2 LSB	Q-24
AD7845SE/883B	–55°C to +125°C	±1 LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7845–SPECIFICATIONS[1] (V_{DD} = +15 V, ± 5%, V_{SS} = –15 V, ± 5%, V_{REF} = +10 V, AGND = DGND = 0 V, V_{OUT} connected to R_{FB}. V_{OUT} load = 2 kΩ, 100 pF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J Version	K Version	A Version	B Version	S Version	T Version	Units	Test Conditions/Comments
ACCURACY								
Resolution	12	12	12	12	12	12	Bits	$1\ LSB = \frac{V_{REF}}{2^{12}} = 2.4\ mV$
Relative Accuracy								
at +25°C	±1	±1/2	±1	±1/2	±1	±1/2	LSB max	All Grades Are Guaranteed
T_{MIN} to T_{MAX}	±1	±3/4	±3/2	±1	±2	±1	LSB max	Monotonic over Temperature
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	DAC Register Loaded with All 0s.
Zero Code Offset Error								
at +25°C	±2	±1	±2	±1	±2	±1	mV max	
T_{MIN} to T_{MAX}	±4	±3	±4	±3	±5	±4	mV max	
Offset Temperature Coefficient;								
(ΔOffset/ΔTemperature)[2]	±5	±5	±5	±5	±5	±5	µV/°C typ	
Gain Error	±6	±3	±6	±3	±6	±3	LSB max	R_{FB}, V_{OUT} Connected
	±9	±6	±9	±6	±9	±6	LSB max	R_C, V_{OUT} Connected, V_{REF} = +5 V
	±9	±6	±9	±6	±9	±6	LSB max	R_B, V_{OUT} Connected, V_{REF} = +5 V
	±10	±8	±10	±8	±10	±8	LSB max	R_A, V_{OUT} Connected, V_{REF} = +2.5 V
Gain Temperature Coefficient;								
(ΔGain/ΔTemperature)[2]	±2	±2	±2	±2	±2	±2	ppm of FSR/°C typ	R_{FB}, V_{OUT} Connected
REFERENCE INPUT								
Input Resistance, Pin 17	8	8	8	8	8	8	kΩ min	Typical Input Resistance = 12 kΩ
	16	16	16	16	16	16	kΩ max	
APPLICATION RESISTOR								
RATIO MATCHING	0.5	0.5	0.5	0.5	0.5	0 5	% max	Matching Between R_A, R_B, R_C
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±1	±1	±1	±1	±1	±1	µA max	Digital Inputs at 0 V and V_{DD}
C_{IN} (Input Capacitance)[2]	7	7	7	7	7	7	pF max	
POWER SUPPLY[4]								
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V min/V max	
V_{SS} Range	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	–14.25/–15.75	V min/V max	
Power Supply Rejection								
$\Delta Gain/\Delta V_{DD}$	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{DD} = +15 V ± 5%, V_{REF} = –10 V
$\Delta Gain/\Delta V_{SS}$	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	V_{SS} = –15 V ± 5%.
I_{DD}	10	10	10	10	10	10	mA max	V_{OUT} Unloaded
I_{SS}	4	4	4	4	4	4	mA max	V_{OUT} Unloaded

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance and are not subject to test.

DYNAMIC PERFORMANCE								
Output Voltage Settling Time	5	5	5	5	5	5	µs max	To 0.01% of Full-Scale Range V_{OUT} Load = 2 kΩ, 100 pF. DAC Register Alternately Loaded with All 0s and All 1s. Typically 2.5 µs at 25°C.
Slew Rate	7	7	7	7	7	7	V/µs typ	V_{OUT} Load = 2 kΩ, 100 pF.
Digital-to-Analog Glitch Impulse	450	450	450	450	450	450	nV–s typ	Measured with V_{REF} = 0 V. DAC Register Alternately Loaded with All 0s and All 1s.
Multiplying Feedthrough Error[3]	5	5	5	5	5	5	mV p-p typ	V_{REF} = ± 10 V, 10 kHz Sine Wave DAC Register Loaded with All 0s.
Unity Gain Small Signal Bandwidth	600	600	600	600	600	600	kHz typ	V_{OUT}, R_{FB} Connected. DAC Loaded with All 1s V_{REF} = 100 mV p-p Sine Wave.
Full Power Bandwidth	250	250	250	250	250	250	kHz typ	V_{OUT}, R_{FB} Connected. DAC Loaded with All 1s. V_{REF} = 20 V p-p Sine Wave. R_L = 2 kΩ.
Total Harmonic Distortion	–90	–90	–90	–90	–90	–90	dB typ	V_{REF} = 6 V rms, 1 kHz Sine Wave.
OUTPUT CHARACTERISTICS[5]								
Open Loop Gain	85	85	85	85	85	85	dB min	V_{OUT}, R_{FB} Not Connected V_{OUT} = ± 10 V, R_L = 2 kΩ
Output Voltage Swing	±10	±10	±10	±10	±10	±10	V min	R_L = 2 kΩ, C_L = 100 pF
Output Resistance	0.2	0.2	0.2	0.2	0.2	0.2	Ω typ	R_{FB}, V_{OUT} Connected,
Short Circuit Current @ +25°C	15	15	15	15	15	15	mA typ	V_{OUT} Shorted to AGND
Output Noise Voltage								Includes Noise Due to Output
(0.1 Hz to 10 Hz) @ +25°C	2	2	2	2	2	2	µV rms typ	Amplifier and Johnson Noise
f = 10 Hz	250	250	250	250	250	250	$nV\sqrt{Hz}$ typ	of R_{FB}
f = 100 Hz	100	100	100	100	100	100	$nV\sqrt{Hz}$ typ	
f = 1 kHz	50	50	50	50	50	50	$nV\sqrt{Hz}$ typ	
f = 10 kHz	50	50	50	50	50	50	$nV\sqrt{Hz}$ typ	
f = 100 kHz	50	50	50	50	50	50	$nV\sqrt{Hz}$ typ	

NOTES

[1]Temperature ranges are as follows: J, K Versions: 0°C to +70°C; A, B Versions: –25°C to +85°C; T Version: –55°C to +125°C.

[2]Sample tested to ensure compliance.

[3]The metal lid on the ceramic D-24A package is connected to Pin 12 (DGND).

[4]The device is functional with a power supply of ± 12 V.

[5]Minimum specified load resistance is 2 kΩ.

Specifications subject to change without notice.

ANALOG DEVICES

LC²MOS 16-Bit Voltage Output DAC

AD7846

FEATURES

16-Bit Monotonicity over Temperature
±2 LSBs Integral Linearity Error
Microprocessor Compatible with Readback Capability
Unipolar or Bipolar Output
Multiplying Capability
Low Power (100 mW typical)

GENERAL DESCRIPTION

The AD7846 is a 16-bit DAC constructed with Analog Devices' LC²MOS process. It has V_{REF+} and V_{REF-} reference inputs and an on-chip output amplifier. These can be configured to give a unipooutput range (0 V to +5 V, 0 V to +10 V) or bipolar output ranges (±5 V, ±10 V).

The DAC uses a segmented architecture. The 4 MSBs in the DAC latch select one of the segments in a 16-resistor string. Both taps of the segment are buffered by amplifiers and fed to a 12-bit DAC, which provides a further 12 bits of resolution. This architecture ensures 16-bit monotonicity. Excellent integral linearity results from tight matching between the input offset voltages of the two buffer amplifiers.

In addition to the excellent accuracy specifications, the AD7846 also offers a comprehensive microprocessor interface. There are 16 data I/O pins, plus control lines ($\overline{CS}$, R/$\overline{W}$, $\overline{LDAC}$ and $\overline{CLR}$). R/$\overline{W}$ and $\overline{CS}$ allow writing to and reading from the I/O latch. This is the readback function which is useful in ATE applications. $\overline{LDAC}$ allows simultaneous updating of DACs in a multi-DAC system and the $\overline{CLR}$ line will reset the contents the DAC latch to 00 . . . 000 or 10 . . . 000 depending on the state of R/$\overline{W}$. This means that the DAC output can be reset to 0 V in both the unipolar and bipolar configurations.

The AD7846 is available in 28-pin plastic, ceramic, LCCC and PLCC packages.

PRODUCT HIGHLIGHTS

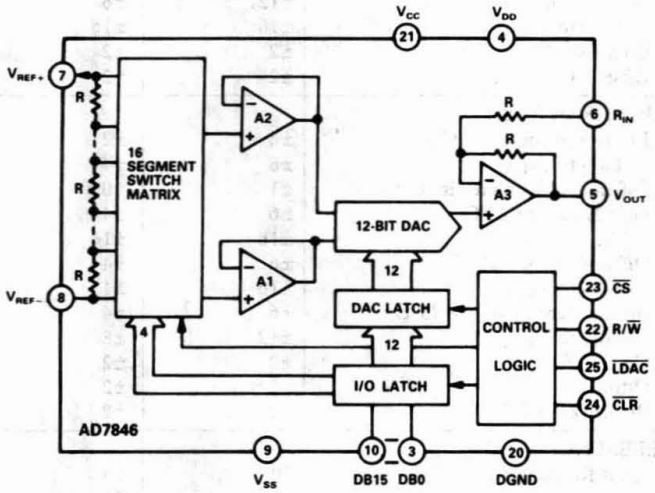
1. 16-Bit Monotonicity
   The guaranteed 16-bit monotonicity over temperature makes the AD7846 ideal for closed-loop applications.
2. Readback
   The ability to read back the DAC register contents minimizes software routines when the AD7846 is used in ATE systems.
3. Power Dissipation
   Power dissipation of 100 mW makes the AD7846 the lowest power, high accuracy DAC on the market.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Package Option*
AD7846JN	0°C to +70°C	±16 LSB	N-28A
AD7846KN	0°C to +70°C	±8 LSB	N-28A
AD7846JP	0°C to +70°C	±16 LSB	P-28A
AD7846KP	0°C to +70°C	±8 LSB	P-28A
AD7846AQ	–25°C to +85°C	±16 LSB	Q-28
AD7846BQ	–25°C to +85°C	±8 LSB	Q-28
AD7846SQ/883B	–55°C to +125°C	±16 LSB	Q-28
AD7846SE/883B	–55°C to +125°C	±16 LSB	E-28A

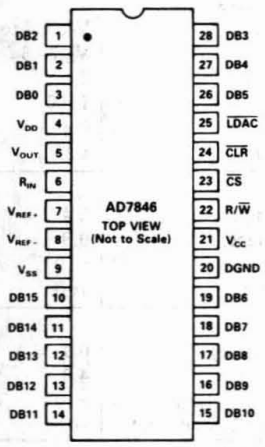
*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic DIP; Q = Cerdip. For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM

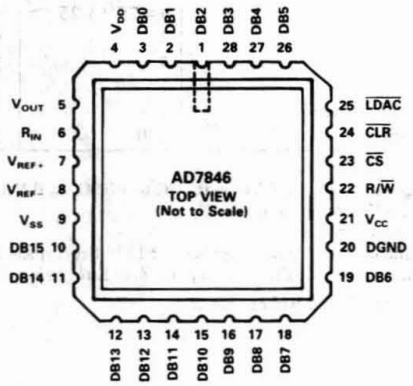


PIN CONFIGURATIONS

DIP



LCCC



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To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7846–SPECIFICATIONS[1]

(V_{DD} = +14.25 V to +15.75 V; V_{SS} = –14.25 V to –15.75 V; V_{CC} = +4.75 V to +5.25 V. V_{OUT} loaded with 2 kΩ,1000 pF to 0 V; V_{REF+} = +5 V; R_{IN} connected to 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	J, A Versions	K, B Versions	S Version[2]	Units	Test Conditions/Comments
RESOLUTION	16	16	16	Bits	
UNIPOLAR OUTPUT					V_{REF-} = 0 V, V_{OUT} = 0 V to +10 V
Relative Accuracy @ +25°C	±12	±4	±16	LSB typ	1 LSB = 153 μV
T_{MIN} to T_{MAX}	±16	±8	±16	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ +25°C	±12	±6	±12	LSB typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±16	±16	±24	LSB max	
Offset Error @ +25°C	±12	±6	±12	LSB typ	
T_{MIN} to T_{MAX}	±16	±16	±24	LSB max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-} = –5 V, V_{OUT} = –10 V to +10 V
Relative Accuracy @ +25°C	±6	±2	±6	LSB typ	1 LSB = 305 μV
T_{MIN} to T_{MAX}	±8	±4	±8	LSB max	
Differential Nonlinearity Error	±1	±0.5	±1	LSB max	All Grades Guaranteed Monotonic
Gain Error @ +25°C	±6	±4	±6	LSB typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±16	±16	±16	LSB max	
Offset Error @ +25°C	±6	±4	±6	LSB typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±16	±12	±16	LSB max	
Bipolar Zero Error @ +25°C	±6	±4	±6	LSB typ	
T_{MIN} to T_{MAX}	±12	±8	±16	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	20	20	20	kΩ min	Resistance from V_{REF+} to V_{REF-}
	40	40	40	kΩ max	Typically 30 kΩ
V_{REF+} Range	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	Volts	
V_{REF-} Range	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	V_{SS} + 6 to V_{DD} – 6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS} + 4 to V_{DD} – 3	V_{SS} + 4 to V_{DD} – 3	V_{SS} + 4 to V_{DD} – 3	V max	
Resistive Load	2	2	3	kΩ min	To 0 V
Capacitive Load	1000	1000	1000	pF max	To 0 V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	To 0 V or Any Power Supply
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	2.4	2.4	2.4	V min	
V_{INL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN} (Input Current)	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK} = 1.6 mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE} = 400 μA
Floating State Leakage Current	±10	±10	±10	μA max	DB0–DB15 = 0 to V_{CC}
Floating State Output Capacitance[3]	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+11.4/+15.75	+11.4/+15.75	+11.4/+15.75	V min/V max	
V_{SS}	–11.4/–15.75	–11.4/–15.75	–11.4/–15.75	V min/V max	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	V min/V max	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded
I_{CC}	1	1	1	mA max	
Power Supply Sensitivity[5]	1.5	1.5	2	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES

[1]Temperature ranges as follows: J, K Versions: 0°C to +70°C; A, B Versions: –25°C to +85°C; S Version: –55°C to +125°C.

[2]Minimum load for S Version is 3 kΩ.

[3]Sample tested to ensure compliance.

[4]The AD7846 is functional with power supplies of ±12 V. See Typical Performance Curves.

[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.

Specifications subject to change without notice.

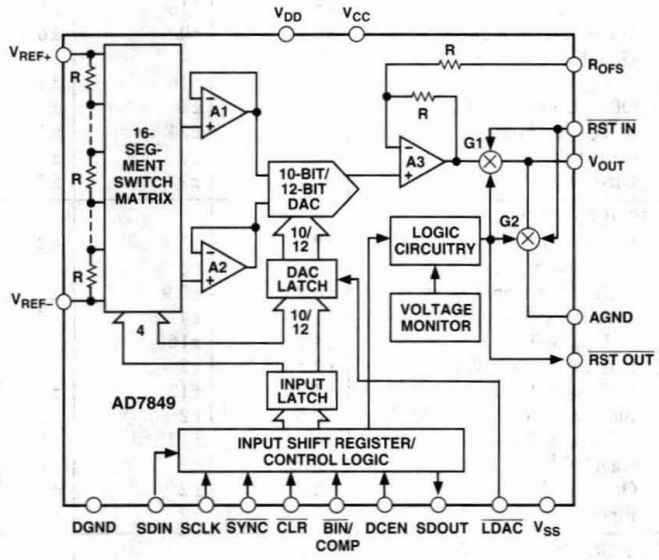
Serial Input, 14-Bit/16-Bit DAC

AD7849*

FEATURES
14-Bit/16-Bit Multiplying DAC
Guaranteed Monotonicity
Output Control on Power-Up and Power-Down
Internal or External Control
Versatile Serial Interface
DAC Clears to 0 V in Both Unipolar and Bipolar Output Ranges

APPLICATIONS
Industrial Process Control
PC Analog I/O Boards
Instrumentation

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7849 is a 14-bit/16-bit serial input multiplying DAC. The DAC architecture ensures excellent differential linearity performance, and monotonicity is guaranteed to 14 bits for the A grade and to 16 bits for all other grades over the specified temperature ranges.

During power-up and power-down sequences (when the supply voltages are changing), the V_{OUT} pin is clamped to 0 V via a low impedance path. To prevent the output of A3 being shorted to 0 V during this time, transmission gate G1 is also opened. These conditions are maintained until the power supplies stabilize and a valid word is written to the DAC register. At this time, G2 opens and G1 closes. Both transmission gates are also externally controllable via the Reset In ($\overline{\text{RST IN}}$) control input. For instance, if the $\overline{\text{RST IN}}$ input is driven from a battery supervisor chip, then on power-off or during a brown out, the $\overline{\text{RST IN}}$ input will be driven low to open G1 and close G2. The DAC must be reloaded, with $\overline{\text{RST IN}}$ high, to re-enable the output. Conversely, the on-chip voltage detector output ($\overline{\text{RST OUT}}$) is also available to the user to control other parts of the system.

The AD7849 has a versatile serial interface structure and can be controlled over three lines to facilitate opto-isolator applications.

SDOUT is the output of the on-chip shift register and can be used in a daisy-chain fashion to program devices in the multi-channel system. The DCEN (Daisy Chain Enable) input controls this function.

The $\overline{\text{BIN}}$/COMP pin sets the DAC coding; with $\overline{\text{BIN}}$/COMP set to 0, the coding is straight binary; and with it set to 1, the coding is 2s complement. This allows the user to reset the DAC to 0 V in both the unipolar and bipolar output ranges.

The part is available in a 20-pin DIP and 20-pin SOIC package.

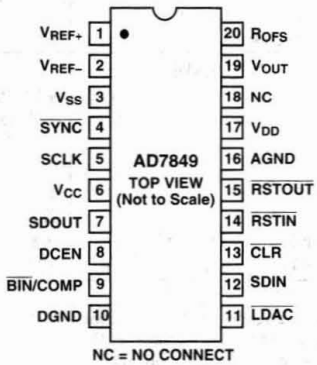
*Protected by U.S. Patent No. 5,319,371.

ORDERING GUIDE

Model	Temperature Range	Resolution (Bits)	Bipolar INL (LSBs)	Package Option*
AD7849AN	–40°C to +85°C	14	±3	N-20
AD7849BN	–40°C to +85°C	16	±8	N-20
AD7849CN	–40°C to +85°C	16	±4	N-20
AD7849AR	–40°C to +85°C	14	±3	R-20
AD7849BR	–40°C to +85°C	16	±8	R-20
AD7849CR	–40°C to +85°C	16	±4	R-20
AD7849TQ	–55°C to +125°C	16	±8	Q-20

*N = Plastic DIP; R = SOP (Small Outline Package); Q = Cerdip. For outline information see Package Information section.

PIN CONFIGURATION



NC = NO CONNECT

AD7849–SPECIFICATIONS[1]

(V_{DD} = +14.25 V to +15.75 V; V_{SS} = −14.25 V to −15.75 V; V_{CC} = 4.75 V to 5.25 V; V_{OUT} loaded with 2 kΩ,[2] 200 pF to 0 V; V_{REF+} = +5 V; R_{OFS} connected to 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A Versions	B, T Versions	C Versions	Units	Test Conditions/Comments
RESOLUTION	14	16	16	Bits	A Versions: 1 LSB = 2 (V_{REF+} − V_{REF-})/2^{14} B, C, T Versions: 1 LSB = 2 (V_{REF+} − V_{REF-})/2^{16}
UNIPOLAR OUTPUT					V_{REF-} = 0 V, V_{OUT} = 0 V to +10 V
Relative Accuracy @ +25°C	±4	±6	±4	LSBs typ	
T_{MIN} to T_{MAX}	±5	±16	±8	LSBs max	
Differential Nonlinearity	±0.25	±0.9	±0.5	LSBs max	All Grades Guaranteed Monotonic Over Temperature
Gain Error @ +25°C	±1	±4	±4	LSBs typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±4	±16	±16	LSBs max	
Offset Error @ +25°C	±1	±4	±4	LSBs typ	
T_{MIN} to T_{MAX}	±6	±24	±16	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
BIPOLAR OUTPUT					V_{REF-} = −5 V, V_{OUT} = −10 V to +10 V
Relative Accuracy @ +25°C	±2	±3	±2	LSBs typ	
T_{MIN} to T_{MAX}	±3	±8	±4	LSBs max	
Differential Nonlinearity	±0.25	±0.9	±0.5	LSBs max	All Grades Guaranteed Monotonic Over Temperature
Gain Error @ +25°C	±1	±4	±4	LSBs typ	V_{OUT} Load = 10 MΩ
T_{MIN} to T_{MAX}	±4	±16	±16	LSBs max	
Offset Error @ +25°C	±0.5	±2	±2	LSBs typ	
T_{MIN} to T_{MAX}	±3	±12	±8	LSBs max	
Bipolar Zero Error @ +25°C	±0.5	±2	±2	LSBs typ	
T_{MIN} to T_{MAX}	±4	±12	±8	LSBs max	
Gain TC[3]	±2	±2	±2	ppm FSR/°C typ	
Offset TC[3]	±2	±2	±2	ppm FSR/°C typ	
Bipolar Zero TC[3]	±2	±2	±2	ppm FSR/°C typ	
REFERENCE INPUT					
Input Resistance	25	25	25	kΩ min	Resistance from V_{REF+} to V_{REF-}
	43	43	43	kΩ max	Typically 34 kΩ
V_{REF+} Range	V_{SS} + 6 to V_{DD} − 6	V_{SS} + 6 to V_{DD} − 6	V_{SS} + 6 to V_{DD} − 6	Volts	
V_{REF-} Range	V_{SS} + 6 to V_{DD} − 6	V_{SS} + 6 to V_{DD} − 6	V_{SS} + 6 to V_{DD} − 6	Volts	
OUTPUT CHARACTERISTICS					
Output Voltage Swing	V_{SS} + 4 to V_{DD} − 4	V_{SS} + 4 to V_{DD} − 4	V_{SS} + 4 to V_{DD} − 4	V max	
Resistive Load	2	2	2	kΩ min	To 0 V
Capacitive Load	200	200	200	pF max	To 0 V
Output Resistance	0.3	0.3	0.3	Ω typ	
Short Circuit Current	±25	±25	±25	mA typ	Voltage Range: −10 V to +10 V
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	μA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
DIGITAL OUTPUTS					
V_{OL} (Output Low Voltage)	0.4	0.4	0.4	Volts max	I_{SINK} = 1.6 mA
V_{OH} (Output High Voltage)	4.0	4.0	4.0	Volts min	I_{SOURCE} = 400 μA
Floating State Leakage Current	±10	±10	±10	μA max	
Floating State Output Capacitance	10	10	10	pF max	
POWER REQUIREMENTS[4]					
V_{DD}	+14.25/15.75	+14.25/15.75	+14.25/15.75	V min/V max	
V_{SS}	−14.25/15.75	−14.25/15.75	−14.25/15.75	V min/V max	
V_{CC}	+4.75/+5.25	+4.75/+5.25	+4.75/+5.25	V min/V max	
I_{DD}	5	5	5	mA max	V_{OUT} Unloaded, V_{INH} = V_{DD} − 0.1 V, V_{INL} = 0.1 V
I_{SS}	5	5	5	mA max	V_{OUT} Unloaded, V_{INH} = V_{DD} − 0.1 V, V_{INL} = 0.1 V
I_{CC}	2.5	2.5	2.5	mA max	V_{INH} = V_{DD} − 0.1 V, V_{INL} = 0.1 V
Power Supply Sensitivity[5]	0.4	1.5	1.5	LSB/V max	
Power Dissipation	100	100	100	mW typ	V_{OUT} Unloaded

NOTES
[1]Temperature ranges: A, B, C Versions: −40°C to +85°C; T Version: −55°C to +125°C.
[2]Minimum load for T Version is 3 kΩ.
[3]Sample tested to ensure compliance.
[4]The AD7849 is functional with power supplies of ±12 V. See Typical Performance Curves.
[5]Sensitivity of Gain Error, Offset Error and Bipolar Zero Error to V_{DD}, V_{SS} variations.

Specifications subject to change without notice.

+3.3 V/+5 V Multiplying 12-Bit DACs

AD7943/AD7945/AD7948

FEATURES
12-Bit Multiplying DACs
Guaranteed Specifications with +3.3 V/+5 V Supply
0.5 LSBs INL and DNL
Low Power: 5 μW typ
Fast Interface
40 ns Strobe Pulse Width (AD7943)
40 ns Write Pulse Width (AD7945, AD7948)
Low Glitch: 60 nV-s with Amplifier Connected
Fast Settling: 600 ns to 0.01% with AD843

APPLICATIONS
Battery-Powered Instrumentation
Laptop Computers
Upgrades for All 754x Series DACs (5 V Designs)

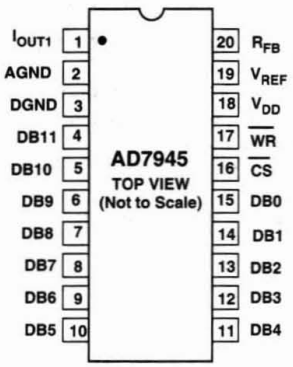
GENERAL DESCRIPTION

The AD7943, AD7945 and AD7948 are fast 12-bit multiplying DACs that operate from a single +5 V supply (Normal Mode) and a single +3.3 V to +5 V supply (Biased Mode). The AD7943 has a serial interface, the AD7945 has a 12-bit parallel interface, and the AD7948 has an 8-bit byte interface. They will replace the industry-standard AD7543, AD7545 and AD7548 in many applications, and they offer superior speed and power consumption performance.

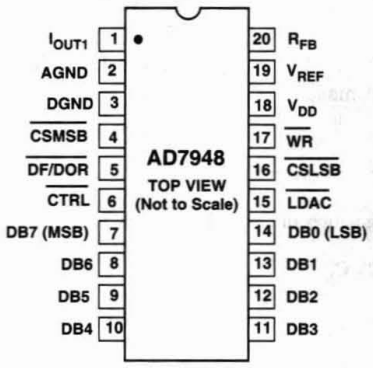
The AD7943 is available in 16-pin DIP, 16-pin SOP (Small Outline Package) and 20-pin SSOP (Shrink Small Outline Package).

PIN CONFIGURATIONS

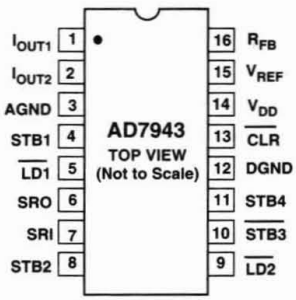
DIP/SOP/SSOP



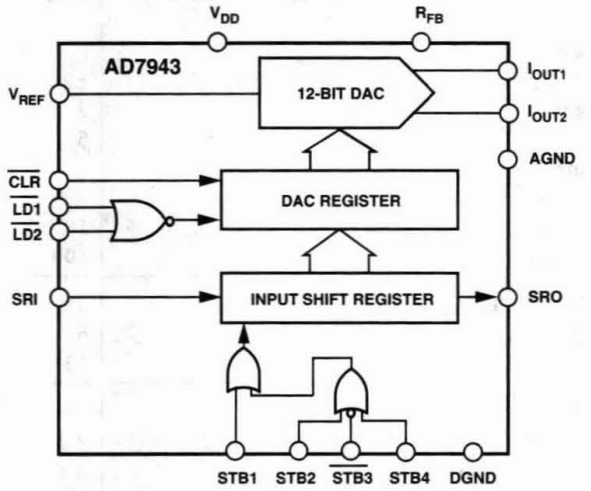
DIP/SOP/SSOP

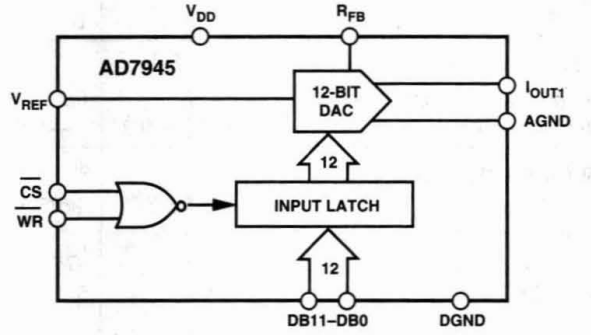


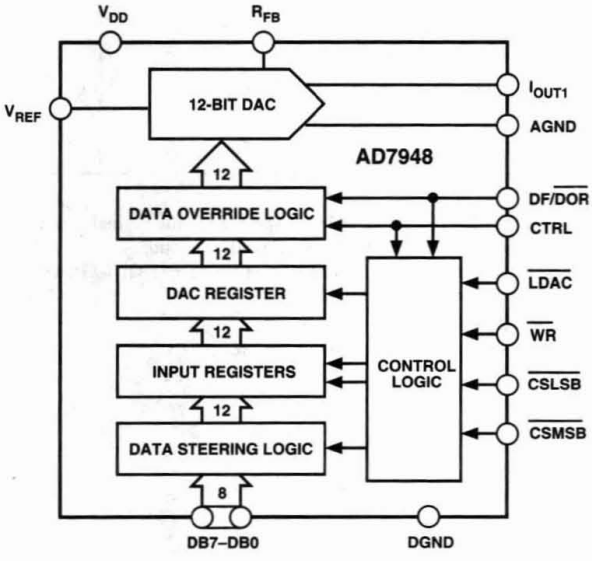
DIP/SOP



FUNCTIONAL BLOCK DIAGRAMS







The AD7945 is available in 20-pin DIP, 20-pin SOP and 20-pin SSOP.

The AD7948 is available in 20-pin DIP, 20-pin SOP and 20-pin SSOP.

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To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD7943/AD7945/AD7948–SPECIFICATIONS[1]

NORMAL MODE (AD7943: V_{DD} = +4.5 V to +5.5 V; V_{IOUT1} = V_{IOUT2} = AGND = 0 V; V_{REF} = +10 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. AD7945, AD7948: V_{DD} = +4.5 V to +5.5 V; V_{IOUT1} = AGND = 0 V; V_{REF} = +10 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	B Grades[2]	T Grade[2, 3]	Units	Test Conditions/Comments
ACCURACY				
Resolution	12	12	Bits	1 LSB = $V_{REF}/2^{12}$ = 2.44 mV when V_{REF} = 10 V
Relative Accuracy	±0.5	±0.5	LSB max	
Differential Nonlinearity	±0.5	±0.5	LSB max	All Grades Guaranteed Monotonic over Temperature
Gain Error				
T_{MIN} to T_{MAX}	±2	±2	LSB max	
Gain Temperature Coefficient[4]	2	2	ppm FSR/°C typ	
	5	5	ppm FSR/°C max	
Output Leakage Current				
I_{OUT1}				
@ +25°C	10	10	nA max	See Terminology Section
T_{MIN} to T_{MAX}	100	100	nA max	Typically 20 nA over Temperature
REFERENCE INPUT				
Input Resistance	6	6	kΩ min	Typical Input Resistance = 9 kΩ
	12	12	kΩ max	
DIGITAL INPUTS				
V_{INH}, Input High Voltage	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current	±1	±1	μA max	
C_{IN}, Input Capacitance[4]	10	10	pF max	
DIGITAL OUTPUT (AD7943 SRO)				For 1 CMOS Load
Output Low Voltage (V_{OL})	0.2	0.2	V max	
Output High Voltage (V_{OH})	V_{DD} – 0.2	V_{DD} – 0.2	V min	
POWER REQUIREMENTS				
V_{DD} Range	4.5/5.5	4.5/5.5	V min/V max	
Power Supply Sensitivity[4]				
$\Delta Gain/\Delta V_{DD}$	–75	–75	dB typ	
I_{DD} (AD7943)	5	5	μA max	V_{INH} = V_{DD} – 0.1 V min, V_{INL} = 0.1 V max. SRO Open Circuit. No STB Signal. Typically 1 μA. Typically 100 μA with a 1 MHz STB Frequency. At Input Levels of 0.8 V and 2.4 V, I_{DD} Is Typically 2.5 mA.
I_{DD} (AD7945, AD7948)	5	5	μA max	V_{INH} = V_{DD} – 0.1 V min, V_{INL} = 0.1 V max. Typically 1 μA. At Input Levels of 0.8 V and 2.4 V, I_{DD} Is Typically 2.5 mA.

NOTES

[1]The AD7943, AD7945 and AD7948 are specified in the normal current mode configuration and in the biased current mode for single-supply applications. Figures 15 and 16 are examples of normal mode operation.

[2]Temperature ranges as follows: B Grades: –40°C to +85°C; T Grade: –55°C to +125°C.

[3]The T Grade applies to the AD7945 only.

[4]Guaranteed by design.

Specifications subject to change without notice.

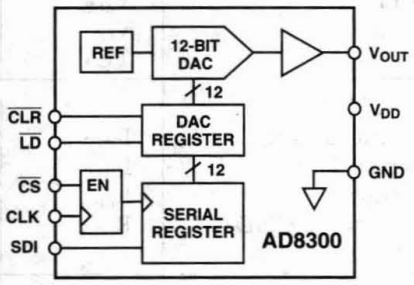
+3 Volt, Serial Input Complete 12-Bit DAC

AD8300

FEATURES
Complete 12-Bit DAC
No External Components
Single +3 Volt Operation
0.5 mV/Bit with 2.0475 V Full Scale
6 μs Output Voltage Settling Time
Low Power: 3.6 mW
Compact SO-8 1.5 mm Height Package

APPLICATIONS
Portable Communications
Digitally Controlled Calibration
Servo Controls
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD8300 is a complete 12-bit, voltage-output digital-to-analog converter designed to operate from a single +3 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in single-supply +3 volt systems. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V making this device ideal for battery operated applications.

The 2.0475 V full-scale voltage output is laser trimmed to maintain accuracy over the operating temperature range of the device. The binary input data format provides an easy-to-use one-half-millivolt-per-bit software programmability. The voltage outputs are capable of sourcing 5 mA.

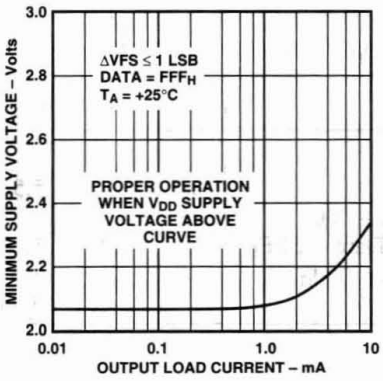


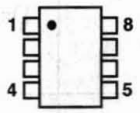
Figure 1. Minimum Supply Voltage vs. Load

A double buffered serial data interface offers high speed, three-wire, DSP and microcontroller compatible inputs using data in ($\overline{SDI}$), clock (CLK) and load strobe ($\overline{LD}$) pins. A chip select ($\overline{CS}$) pin simplifies connection of multiple DAC packages by enabling the clock input when active low. Additionally, a $\overline{CLR}$ input sets the output to zero scale at power on or upon user demand.

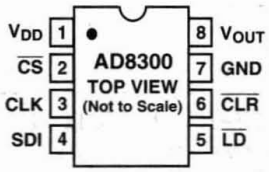
The AD8300 is specified over the extended industrial (–40°C to +85°C) temperature range. AD8300's are available in plastic DIP, and low profile 1.5 mm height SO-8 surface mount packages. See the AD8303 for a monolithic DUAL version.

PIN CONFIGURATIONS

SO-8



Plastic DIP



ORDERING GUIDE

Model	INL	Temp[1]	Package Description	Package Option[2]
AD8300AN	±2	XIND	8-Pin P-DIP	N-8
AD8300AR	±2	XIND	8-Lead SOIC	SO-8

NOTES
[1]XIND = –40°C to +85°C.
[2]For outline information see Package Information section.
The AD8300 contains 630 transistors. The die size measures 72 mil × 65 mil.

AD8300–SPECIFICATIONS

+3 V OPERATION (@ V_{DD} = +2.7 V to +3.6 V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	[Note 1]	12			Bits
Relative Accuracy	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[2]	DNL	Monotonic	–1	±1/2	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	mV
Full-Scale Voltage[3]	V_{FS}	Data = FFF_H	2.039	2.0475	2.056	Volts
Full-Scale Tempco	TCV_{FS}	[Notes 3, 4]		16		ppm/°C
ANALOG OUTPUT						
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB			5	mA
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB			2	mA
Load Regulation	L_{REG}	R_L = 200 Ω to ∞, Data = 800_H		1.5	5	LSB
Output Resistance to GND	R_{OUT}	Data = 000_H		30		Ω
Capacitive Load	C_L	No Oscillation[4]		500		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.6	V
Logic Input High Voltage	V_{IH}		2.1			V
Input Leakage Current	I_{IL}				10	μA
Input Capacitance	C_{IL}				10	pF
INTERFACE TIMING SPECIFICATIONS[4, 5]						
Clock Width High	t_{CH}		40			ns
Clock Width Low	t_{CL}		40			ns
Load Pulse Width	t_{LDW}		50			ns
Data Setup	t_{DS}		15			ns
Data Hold	t_{DH}		15			ns
Clear Pulse Width	t_{CLRW}		40			ns
Load Setup	t_{LD1}		15			ns
Load Hold	t_{LD2}		40			ns
Select	t_{CSS}		40			ns
Deselect	t_{CSH}		40			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time	t_S	To ±0.2% of Full Scale		7		μs
		To ±1 LSB of Final Value[6]		14		μs
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H		2.0		V/μs
DAC Glitch				15		nV/s
Digital Feedthrough				15		nV/s
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7		5.5	V
Positive Supply Current	I_{DD}	V_{DD} = 3 V, V_{IL} = 0 V, Data = 000_H		1.2	1.7	mA
Positive Supply Current	I_{DD}	V_{DD} = 3.6 V, V_{IH} = 2.3 V, Data = FFF_H		1.9	3.0	mA
Power Dissipation	P_{DISS}	V_{DD} = 3 V, V_{IL} = 0 V, Data = 000_H		3.6	5.1	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.001	0.005	%/%

NOTES

[1]1 LSB = 0.5 mV for 0 V to +2.0475 V output range.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

Obtain complete data sheet for remainder of specifications.

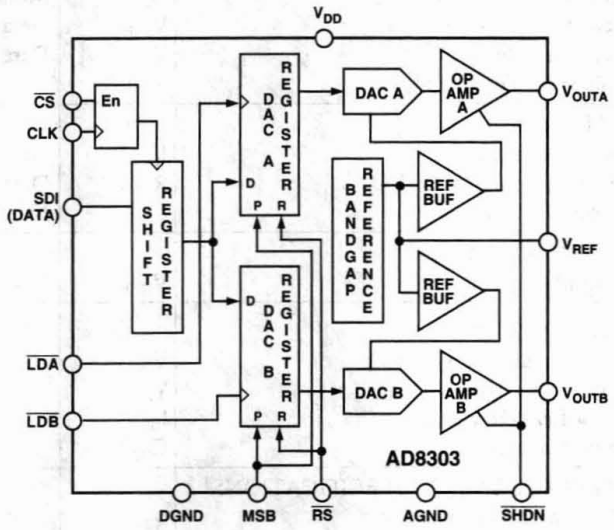
+3 V, Dual, Serial Input Complete 12-Bit DAC

AD8303

FEATURES
Complete Dual 12-Bit DAC
Pretrimmed Internal Voltage Reference
Single +3 V Operation
0.5 mV/Bit with 2.0475 V Full Scale
Low Power: 9.6 mW
3-Wire Serial SPI Compatible Interface
Power Shutdown I_{DD} < 1 μA
Compact SO-14, 1.75 mm Height Package

APPLICATIONS
Portable Communications
Digitally Controlled Calibration
Servo Controls
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD8303 is a complete (includes internal reference) dual, 12-bit, voltage output digital-to-analog converter designed to operate from a single +3 volt supply. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V making this device ideal for battery operated applications.

The 2.0475 V full-scale voltage output is laser-trimmed to maintain accuracy over the operating temperature range of the device. The binary input data format provides an easy-to-use one-half millivolt-per-bit software programmability. The voltage outputs are capable of sourcing 3 mA.

A double buffered serial data interface offers high speed, three-wire, DSP and SPI microcontroller compatible inputs using data in (SDI), clock (CLK) and load strobe ($\overline{LDA}$ + $\overline{LDB}$) pins. A chip-select ($\overline{CS}$) pin simplifies connection of multiple DAC packages by enabling the clock input when active low. Additionally, an $\overline{RS}$ input sets the output to zero scale or to 1/2 scale based on the level applied to the MSB pin. A power shutdown feature reduces power dissipation to less than 3 μW.

The AD8303 is specified over the extended industrial (–40°C to +85°C) temperature range. AD8303s are available in plastic DIP and low profile 1.75 mm height SO-14 surface mount packages. For single-channel DAC applications, see the AD8300.

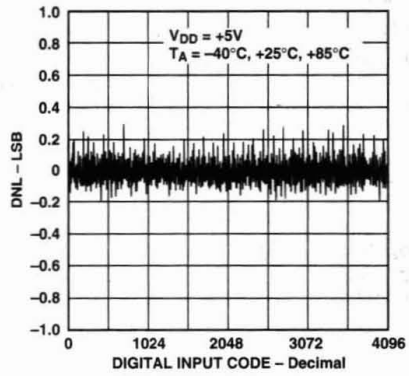


Figure 1. Differential Nonlinearity Error vs. Code

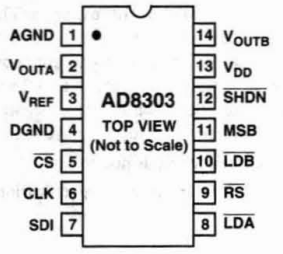
ORDERING GUIDE

Model	DNL	Temperature Range	Package Description	Package Option*
AD8303AN	±0.75	–40°C to +85°C	14-Pin P-DIP	N-14
AD8303AR	±0.75	–40°C to +85°C	14-Lead SOIC	R-14

*For outline information see Package Information section.

PIN CONFIGURATION

14-Pin P-DIP (N-14)
14-Lead SOIC (R-14)



AD8303–SPECIFICATIONS

+3 V OPERATION (@ V_{DD} = +2.7 V to +3.6 V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[1]	Max	Units
STATIC PERFORMANCE						
Resolution[2]	N		12			Bits
Relative Accuracy[2]	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[2]	DNL	Monotonic, T_A = +25°C	–3/4	±1/4	+3/4	LSB
Differential Nonlinearity[2]	DNL	Monotonic	–1	±1/2	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		1.25	+4.5	mV
Full-Scale Voltage[3]	V_{FS}	Data = FFF_H[2]	2.039	2.0475	2.056	Volts
Full-Scale Tempco[3, 4]	TCV_{FS}			16		ppm/°C
ANALOG OUTPUTS						
Output Current	I_{OUT}	Data = 800_H, ΔV_{OUT} < 3 mV			±3	mA
Output Resistance to GND	R_{OUT}	Data = 000_H		30		Ω
Capacitive Load[4]	C_L	No Oscillation[3]		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}	Load > 1 MΩ		1		V
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.6	V
Logic Input High Voltage	V_{IH}		2.1			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[4]	C_{IL}				10	pF
INTERFACE TIMING SPECIFICATIONS[4, 5]						
Clock Width High	t_{CH}		40			ns
Clock Width Low	t_{CL}		40			ns
Load Pulse Width	t_{LDW}		40			ns
Data Setup	t_{DS}		15			ns
Data Hold	t_{DH}		15			ns
Reset Pulse Width	t_{RS}		40			ns
Load Setup	t_{LD1}		15			ns
Load Hold	t_{LD2}		40			ns
Select	t_{CSS}		40			ns
Deselect	t_{CSH}		40			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time[6]	t_S	To ±0.1% of Full Scale		4		µs
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		14		µs
Shutdown Recovery Time	t_{DSR}	To ±0.1% of Full Scale		10		µs
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H		2.0		V/µs
DAC Glitch	Q			15		nV/s
Digital Feedthrough	Q			15		nV/s
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7		5.5	V
Shutdown Current	I_{DD_SD}	$\overline{SHDN}$ = 0, No Load, V_{IL} = 0 V, T_A = +25°C		0.02	1	µA
Supply Current[7]	I_{DD}	V_{DD} = 3 V, V_{IL} = 0 V, No Load		2	3.2	mA
Power Dissipation	P_{DISS}	V_{DD} = 3 V, V_{IL} = 0 V, No Load		6	9.6	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.001	0.004	%/%

NOTES

[1]Typical readings represent the average value of room temperature operation.

[2]1 LSB = 0.5 mV for 0 V to +2.0475 V output range. The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground.

[7]See Figure 6 for a plot of incremental supply current consumption as a function of the digital input voltage levels.

Specifications subject to change without notice.

Obtain complete data sheet for remainder of specification.

2-/4-Channel Digital Potentiometers

AD8402/AD8403

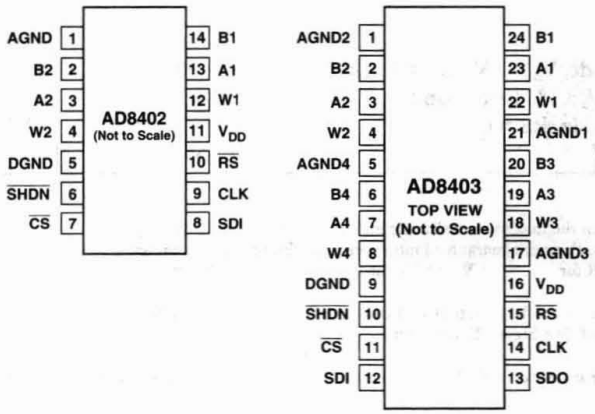
FEATURES
256 Position
Replaces 2 or 4 Potentiometers
10 kΩ, 50 kΩ, 100 kΩ
Power Shut Down—Less than 5 μA
3-Wire SPI Compatible Serial Data Input
10 MHz Update Data Loading Rate
+2.7 V to +5.5 V Single-Supply Operation
Midscale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Programmable Filters, Delays, Time Constants
Volume Control, Panning
Line Impedance Matching
Power Supply Adjustment

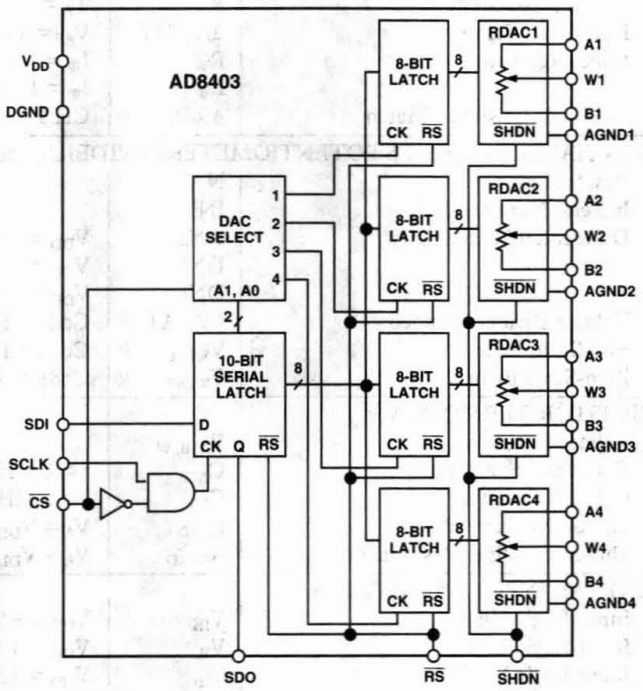
GENERAL DESCRIPTION

The AD8402/AD8403 provide a dual or quad channel, 256 position digitally controlled variable resistor (VR) device. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. The AD8402 contains two independent variable resistors in space saving SO-14 surface mount package. The AD8403 contains four independent variable resistors in 24-lead PDIP, SOIC and TSSOP packages. Each part contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the controlling serial input register. The resistance between the wiper and either endpoint of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. Each variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A to B terminal resistance of 10 kΩ, 50 kΩ or 100 kΩ has a ±1% channel-to-channel matching tolerance with a nominal temperature coefficient of 500 ppm/°C.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



The reset ($\overline{RS}$) pin forces the wiper to the midscale position by loading 80_H into the VR latch. The $\overline{SHDN}$ pin forces the resistor to an end-to-end open circuit condition on the A terminal and shorts the wiper to the B terminal, achieving a microwatt power shutdown state.

ORDERING GUIDE

Model	#CHs/ kΩ	Temperature Range	Package Description	Package Option*
AD8402AN10	X2/10	–40°C to +85°C	P-DIP-14	N-14
AD8402AR10	X2/10	–40°C to +85°C	SO-14	SO-14
AD8403AR10	X4/10	–40°C to +85°C	SOIC-24	SOL-24
AD8403AN10	X4/10	–40°C to +85°C	P-DIP-24	N-24
AD8403ARU10	X4/10	–40°C to +85°C	TSSOP-24	RU-24
AD8402AN50	X2/50	–40°C to +85°C	P-DIP-14	N-14
AD8402AR50	X2/50	–40°C to +85°C	SO-14	SO-14
AD8403AR50	X4/50	–40°C to +85°C	SOIC-24	SOL-24
AD8403AN50	X4/50	–40°C to +85°C	P-DIP-24	N-24
AD8402AN100	X2/100	–40°C to +85°C	P-DIP-14	N-14
AD8402AR100	X2/100	–40°C to +85°C	SO-14	SO-14
AD8403AR100	X4/100	–40°C to +85°C	SOIC-24	SOL-24
AD8403AN100	X4/100	–40°C to +85°C	P-DIP-24	N-24
AD8403ARU100	X4/100	–40°C to +85°C	TSSOP-24	RU-24

*The AD8402 and AD8403 contain 720 transistors. For outline information see Package Information section.

AD8402/AD8403–SPECIFICATIONS

10 kΩ VERSION

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3 V ± 10% or + 5 V ± 10%, V_A = +V_{DD}, V_B = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–2	±1/2	+2	LSB
Nominal Resistance[3]	R	T_A = +25°C, Model: AD840XYY10	8	10	12	kΩ
Resistance Tempco	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R V_{DD} = +5 V		50	100	Ω
	R_W	I_W = 1 V/R V_{DD} = +3 V		200		Ω
Nominal Resistance Match	$\Delta R/R_O$	CH 1 to 2, 3, or 4, V_{AB} = V_{DD}, T_A = +25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER Specifications apply to all VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		–2	±1/2	+2	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = +5 V	–1	±1/4	+1	LSB
	DNL	V_{DD} = +3 V T_A = +25°C	–1	±1/4	+1	LSB
	DNL	V_{DD} = +3 V T_A = –40°C, +85°C	–1.5	±1/2	+1.5	LSB
Voltage Divider Tempco	$\Delta V_W/\Delta T$	Code = 80_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–4	–2.8	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	+1.3	+2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		0		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = 80_H		75		pF
Capacitance[6] Wx	C_W	f = 1 MHz, Measured to GND, Code = 80_H		120		pF
Shutdown Current[7]	I_{A_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0		0.01	5	µA
Shutdown Wiper Resistance	R_{W_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = +5 V		100	200	Ω
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Output Logic High	V_{OH}	R_L = 1 kΩ to V_{DD}	V_{DD} – 0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = +5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V, V_{DD} = +5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)[8]	I_{DD}	V_{IH} = 2.4 V or 0.8 V, V_{DD} = +5.5 V		0.9	4	mA
Power Dissipation (CMOS)[9]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSS	V_{DD} = +5 V ± 10%		0.0002	0.001	%/%
	PSS	V_{DD} = +3 V ± 10%		0.006	0.03	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW_10K	R = 10 kΩ		600		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms + 2 V dc, V_B = 2 V dc, f = 1 kHz		0.003		%
V_W Settling Time	t_S	V_A = V_{DD}, V_B = 0 V, ±1% Error Band		25		µs
Resistor Noise Voltage	e_{NWB}	R_{WB} = 5 kΩ, f = 1 kHz, $\overline{RS}$ = 0		9		nV/√Hz
Crosstalk[11]	C_T	V_A = V_{DD}, V_B = 0 V		–65		dB

NOTES

[1] Typicals represent average readings at +25°C and V_{DD} = +5 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. See Figure 28 test circuit. I_W = 50 µA for V_{DD} = +3 V and I_W = 400 µA for V_{DD} = +5 V for the 10 kΩ versions. I_W = V_{DD}/R for V_{DD} = +3 V or +5 V for the 50 kΩ and 100 kΩ versions.

[3] V_{AB} = V_{DD}, Wiper (V_W) = No Connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL Specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions. See Figure 27 test circuit.

[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test. Resistor-terminal capacitance tests are measured with 2.5 V bias on the measured terminal. The remaining resistor terminals are left open circuit.

[7] Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.

[8] Worst case supply current consumed when input logic level at 2.4 V, standard characteristic of CMOS logic. See Figure 23 for a plot of I_{DD} versus logic voltage.

[9] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.

[10] All Dynamic Characteristics use V_{DD} = +5 V.

[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

Specifications subject to change without notice.

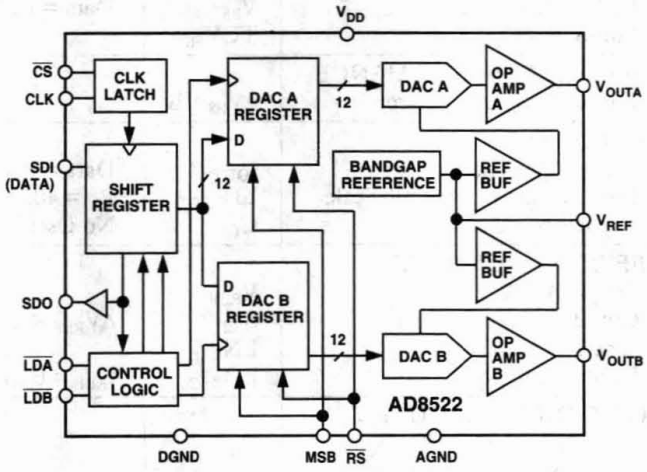
+5 Volt, Serial Input, Dual 12-Bit DAC

AD8522

FEATURES
Complete Dual 12-Bit DAC
No External Components
+5 V Single-Supply Operation ±10%
4.095 V Full Scale (1 mV/LSB)
Buffered Voltage Outputs
Low Power: 5 mW/DAC
Space Saving 1.5 mm Height SO-14 Package

APPLICATIONS
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
Computer Peripherals
Portable Instrumentation
Cellular Base Stations Voltage Adjustment

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD8522 is a complete dual 12-bit, single-supply, voltage output DAC in a 14-pin DIP, or SO-14 surface mount package. Fabricated in a CBCMOS process, features include a serial digital interface, onboard reference, and buffered voltage output. Ideal for +5 V-only systems, this monolithic device offers low cost and ease of use, and requires no external components to realize the full performance of the device.

The serial digital interface allows interfacing directly to numerous microcontroller ports, with a simple high speed, three-wire data, clock, and load strobe format. The 16-bit serial word contains the 12-bit data word and DAC select address, which is decoded internally or can be decoded externally using $\overline{LDA}$, $\overline{LDB}$ inputs. A serial data output allows the user to easily daisy-chain multiple devices in conjunction with a chip select input. A reset $\overline{RS}$ input sets the outputs to zero scale or midscale, as determined by the input MSB.

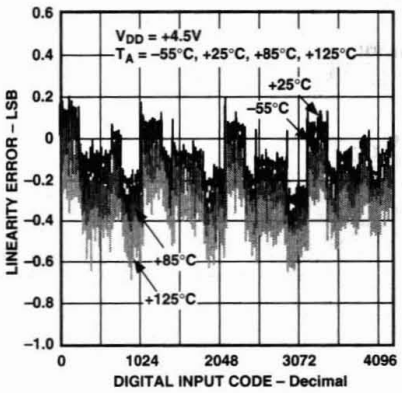


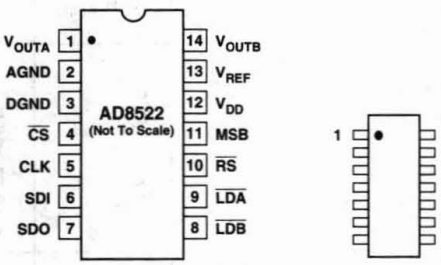
Figure 1. Linearity Error vs. Digital Code & Temperature

The output 4.095 V full scale is laser trimmed to maintain accuracy over the operating temperature range of the device, and gives the user an easy-to-use one-millivolt-per-bit resolution. A 2.5 V reference output is also available externally for other data acquisition circuitry, and for ratiometric applications. The output buffers are capable of driving ±5 mA.

The AD8522 is available in the 14-pin plastic DIP and low profile 1.5 mm SOIC-14 packages.

PIN CONFIGURATIONS

14-Pin Plastic DIP **14-Lead SO-14**



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8522AN	–40°C to +85°C	14-Pin P-DIP	N-14
AD8522AR	–40°C to +85°C	14-Lead SOIC	SO-14

*For outline information see Package Information section.
The AD8522 contains 1482 transistors.

AD8522–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5.0 V ± 10%, R_L = No Load, –40°C ≤ T_A ≤ +85°C, both DACs tested, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution[1]	N		12			Bits
Relative Accuracy	INL		-1.5	±0.5	+1.5	LSB
Differential Nonlinearity	DNL	Monotonic	-1	±0.5	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+0.5	+3	mV
Full-Scale Voltage[2]	V_{FS}	Data = FFF_H	4.079	4.095	4.111	Volts
Full-Scale Tempco[2, 3]	TCV_{FS}			±15		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching Error	$\Delta V_{FS}A/B$			±1		LSB
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H, $\Delta V_{OUT} \leq 3$ LSB			±5	mA
Load Regulation at Half-Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load[3]	C_L	No Oscillation		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current[4]	I_{REF}	ΔV_{REF} < 18 mV			5	mA
Line Rejection	LN_{REJ}			0.025	0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA, Data = 800_H		0.025	0.1	%/mA
LOGIC INPUTS & OUTPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance[3]	C_{IL}				10	pF
Logic Output Voltage Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic Output Voltage High	V_{OH}	I_{OH} = 400 µA	3.5			V
TIMING SPECIFICATIONS[3, 5]						
Clock Width High	t_{CH}		35			ns
Clock Width Low	t_{CL}		35			ns
Load Pulse Width	t_{LDW}		25			ns
Data Setup	t_{DS}		10			ns
Data Hold	t_{DH}		20			ns
Clear Pulse Width	t_{CLRW}		20			ns
Load Setup	t_{LD1}		10			ns
Load Hold	t_{LD2}		10			ns
Select	t_{CSS}		30			ns
Deselect	t_{CSH}		30			ns
Clock to SDO Propagation Delay	t_{PD}		20	45	80	ns
AC CHARACTERISTICS[3, 5]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Crosstalk	C_T	Signal Measured at DAC Output, While Changing Opposite $\overline{LDA}/B$		38		dB
DAC Glitch	Q	Half-Scale Transition		13		nV s
Digital Feedthrough	D_{FT}	Signal Measured at DAC Output, While Changing Data Without $\overline{LDA}/B$		2		nV s
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{DD} = 5.5 V, V_{IH} = 2.4 V or V_{IL} = 0.8 V		3	5	mA
		V_{DD} = 5 V, V_{IL} = 0 V		1	2	mA
Power Dissipation[7]	P_{DISS}	V_{DD} = 5 V, V_{IH} = 2.4 V or V_{IL} = 0.8 V		15	25	mW
		V_{DD} = 5 V, V_{IL} = 0 V		5	10	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]1 LSB = 1 mV for 0 V to +4.095 V output range.

[2]Includes internal voltage reference error.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Very little sink current is available at the V_{REF} pin. Use external buffer if setting up a virtual ground.

[5]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

[7]Power Dissipation is calculated $I_{DD} \times 5$ V.

Specifications subject to change without notice.

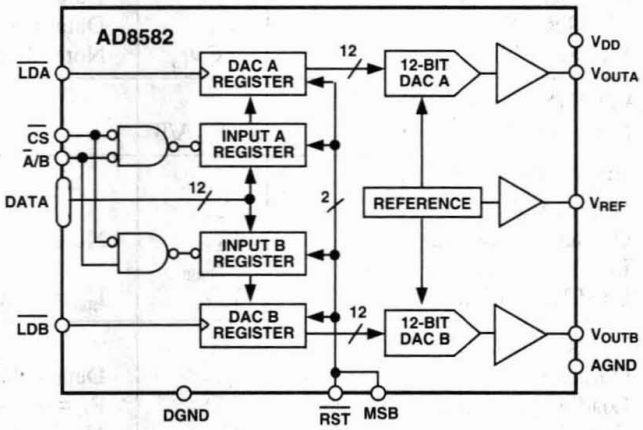
+5 Volt, Parallel Input Complete Dual 12-Bit DAC

AD8582

FEATURES
Complete Dual 12-Bit DAC
No External Components
Single +5 Volt Operation
1 mV/Bit with 4.095 V Full Scale
True Voltage Output, ±5 mA Drive
Very Low Power: 5 mW

APPLICATIONS
Digitally Controlled Calibration
Portable Equipment
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD8582 is a complete, parallel input, dual 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DACs, are a rail-to-rail amplifier, latch and reference. The reference (V_{REF}) is trimmed to 2.5 volts output, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The AD8582 is coded natural binary. The op amp output swings from 0 volt to +4.095 volts for a one-millivolt-per-bit resolution, and is capable of driving ±5 mA. Operation down to 4.3 V is possible with output load currents less than 1 mA.

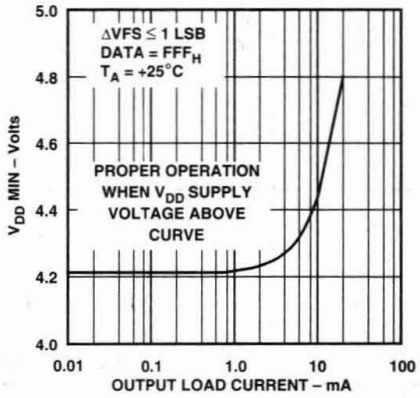


Figure 1. Minimum Supply Voltage vs. Load

The high speed parallel data interface connects to the fastest processors without wait states. The double-buffered input structure allows the user to load the input registers one at a time, then a single load strobe tied to both LDA + LDB inputs will update both DAC outputs simultaneously. LDA and LDB can also be activated independently to immediately update their respective DAC registers. An address input decodes DAC A or DAC B when the chip select $\overline{CS}$ input is strobed. An asynchronous reset input sets the output to zero scale. The MSB bit can be used to establish a preset to midscale when the reset input is strobed.

The AD8582 is available in the 24-pin plastic DIP and the surface mount SOIC-24. Each part is fully specified for operation over –40°C to +85°C, and the full +5 V ± 5% power supply range.

ORDERING INFORMATION[1]

Model	Temperature Range	Package Description	Package Option[2]
AD8582AN	–40°C to +85°C	24-Pin Plastic DIP	N-24
AD8582AR	–40°C to +85°C	24-Lead SOIC	SOL-24
AD8582CHIPS	+25°C	Die	

NOTES
[1]For die specifications contact your local Analog Devices sales office. The AD8582 contains 1270 transistors.
[2]For outline information see Package Information section.

AD8582–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 V ± 5%, R_L = No Load, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 1	12			Bits
Relative Accuracy	INL		–2	±3/4	+2	LSB
Differential Nonlinearity	DNL	Monotonic	–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+0.2	+3	mV
Full-Scale Voltage	V_{FS}	Data = FFF_H,[2]	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 2 and 3		±16		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching Error	$\Delta V_{FS}A/B$			±1		LSB
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 4			–5	mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 mA to 5 mA			0.1	%/mA
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H			±5	mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[3]		500		pF
DYNAMIC CHARACTERISTICS[3]						
Crosstalk	C_T			>64		dB
Voltage Output Settling Time[5]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough	F_T	Signal Measured at DAC Output, While Changing Data ($\overline{LDA}$ = $\overline{LDB}$ = "1")		35		nV s
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 3			10	pF
TIMING SPECIFICATIONS[3, 6]						
Chip Select Pulse Width	t_{CSW}		30			ns
DAC Select Setup	t_{AS}		30			ns
DAC Select Hold	t_{AH}		0			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Load Setup	t_{LS}		20			ns
Load Hold	t_{LH}		10			ns
Load Pulse Width	t_{LDW}		20			ns
Reset Pulse Width	t_{RSW}		30			ns
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		4	7	mA
		V_{IL} = 0 V, V_{DD} = +5 V		1	2	mA
Power Dissipation[7]	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		20	35	mW
		V_{IL} = 0 V, V_{DD} = +5 V		5	10	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]1 LSB = 1 mV for 0 V to +4.095 V output range.

[2]Includes internal voltage reference error.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Very little sink current is available at the V_{REF} pin. Use external buffer if setting up a virtual ground.

[5]Settling time is not guaranteed for the first six codes 0 through 5.

[6]All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[7]Power dissipation is a calculated value $I_{DD} \times 5$ V.

Specifications subject to change without notice.

ANALOG DEVICES

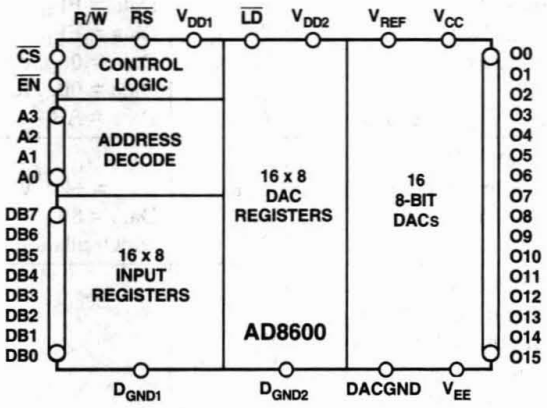
16-Channel, 8-Bit Multiplying DAC

AD8600*

FEATURES
16 Independently Addressable Voltage Outputs
Full-Scale Set by External Reference
2 μs Settling Time
Double Buffered 8-Bit Parallel Input
High Speed Data Load Rate
Data Readback
Operates from Single +5 V
Optional ±6 V Supply Extends Output Range

APPLICATIONS
Phased Array Ultrasound & Sonar
Power Level Setting
Receiver Gain Setting
Automatic Test Equipment
LCD Clock Level Setting

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The AD8600 contains 16 independent voltage output digital-to-analog converters that share a common external reference input voltage. Each DAC has its own DAC register and input register to allow double buffering. An 8-bit parallel data input, four address pins, a $\overline{CS}$ select, a $\overline{LD}$, $\overline{EN}$, R/$\overline{W}$, and $\overline{RS}$ provide the digital interface.

The AD8600 is constructed in a monolithic CBCMOS process which optimizes use of CMOS for logic and bipolar for speed and precision. The digital-to-analog converter design uses voltage mode operation ideally suited to single supply operation. The internal DAC voltage range is fixed at DACGND to V_{REF}. The voltage buffers provide an output voltage range that approaches ground and extends to 1.0 V below V_{CC}. Changes in reference voltage values and digital inputs will settle within ±1 LSB in 2 μs.

Data is preloaded into the input registers one at a time after the internal address decoder selects the input register. In the write mode (R/$\overline{W}$ low) data is latched into the input register during the positive edge of the $\overline{EN}$ pulse. Pulses as short as 40 ns can be used to load the data. After changes have been submitted to the input registers, the DAC registers are simultaneously updated by a common load $\overline{EN} \times \overline{LD}$ strobe. The new analog output voltages simultaneously appear on all 16 outputs.

***Patent pending.**

At system power up or during fault recovery the reset ($\overline{RS}$) pin forces all DAC registers into the zero state which places zero volts at all DAC outputs.

The AD8600 is offered in the PLCC-44 package. The device is designed and tested for operation over the extended industrial temperature range of –40°C to +85°C.

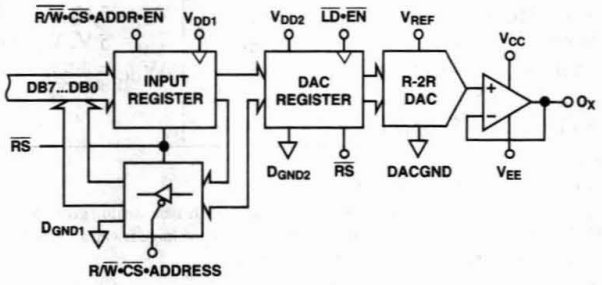


Figure 1. Equivalent DAC Channel

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD8600AP	–40°C to +85°C	44-Lead PLCC	P-44A

*For outline information see Package Information section.
The AD8600 contains 5782 transistors.

AD8600–SPECIFICATIONS

SINGLE SUPPLY (@ $V_{DD1} = V_{DD2} = V_{CC} = +5\ V \pm 5\%$, $V_{EE} = 0\ V$, $V_{REF} = +2.500\ V$, $-40°C \le T_A \le +85°C$, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE[1]						
Resolution	N		8			Bits
Relative Accuracy[2]	INL		–1	±1/2	+1	LSB
Differential Nonlinearity[2]	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Full-Scale Voltage	V_{FS}	Data = FF_H	2.480	2.490	2.500	V
Full-Scale Tempco	TCV_{FS}	Data = FF_H		±20		ppm/°C
Zero Scale Error	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0," T_A = +25°C			+3.5	LSB
	V_{ZSE}	Data = 00_H, $\overline{RS}$ = "0"			+5	LSB
Reference Input Resistance	R_{REF}	Data = AB_H	1.2	2		kΩ
ANALOG OUTPUT						
Output Voltage Range[2]	OVR_{SS}	V_{REF} = +2.5 V	0.000		2.500	V
Output Current	I_{OUT}	Data = 80_H		±2		mA
Capacitive Load	C_L	No Oscillation		50		pF
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Logic Input Current	I_{IL}				10	µA
Logic Input Capacitance[3]	C_{IL}				10	pF
LOGIC OUTPUTS						
Logic Out High Voltage	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Out Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
AC CHARACTERISTICS[3]						
Slew Rate	SR	For ΔV_{REF} or FS Code Change	4	7		V/µs
Voltage Output Settling Time[2]	t_{S1}	±1 LSB of Final Value, Full-Scale Data Change		2		µs
Voltage Output Settling Time[2]	t_{S2}	±1 LSB of Final Value, ΔV_{REF} = 1 V, Data = FF_H		2		µs
POWER SUPPLIES						
Positive Supply Current	I_{CC}	V_{IH} = 5 V, V_{IL} = 0 V, No Load		24	35	mA
Logic Supply Currents	$I_{DD1\&2}$	V_{IH} = 5 V, V_{IL} = 0 V, No Load			0.1	mA
Power Dissipation	P_{DISS}	V_{IH} = 5 V, V_{IL} = 0 V, No Load		120	175	mW
Power Supply Sensitivity	PSS	$\Delta V_{CC} = \pm 5\%$			0.007	%/%
Logic Power Supply Range	V_{DDR}		4.75		5.25	V
Positive Power Supply Range[3]	V_{CCR}		V_{DD}		7.0	V

NOTES

[1]When V_{REF} = 2.500 V, 1 LSB = 9.76 mV.

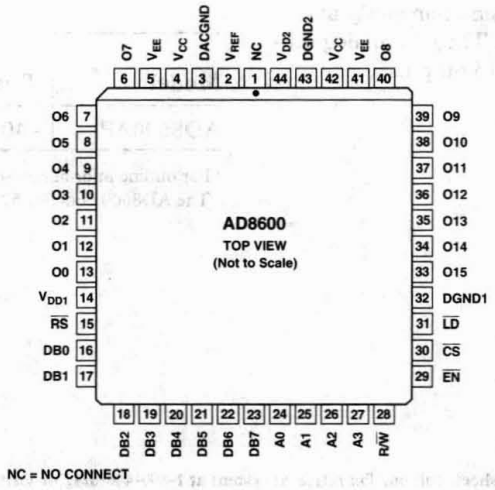
[2]Single supply operation does not include the final 2 LSBs near analog ground. If this performance is critical, use a negative supply (V_{EE}) pin of at least –0.7 V to –5.25 V. Note that for the INL measurement zero-scale voltage is extrapolated using codes 7_{10} to 80_{10}.

[3]Guaranteed by design not subject to production test.

Specifications subject to change without notice.

For remaining digital interface timing, and ±5 V operation specifications consult full data sheet.

PIN CONFIGURATION



NC = NO CONNECT

Octal 8-Bit TrimDACs with Power Shutdown

AD8801/AD8803

FEATURES

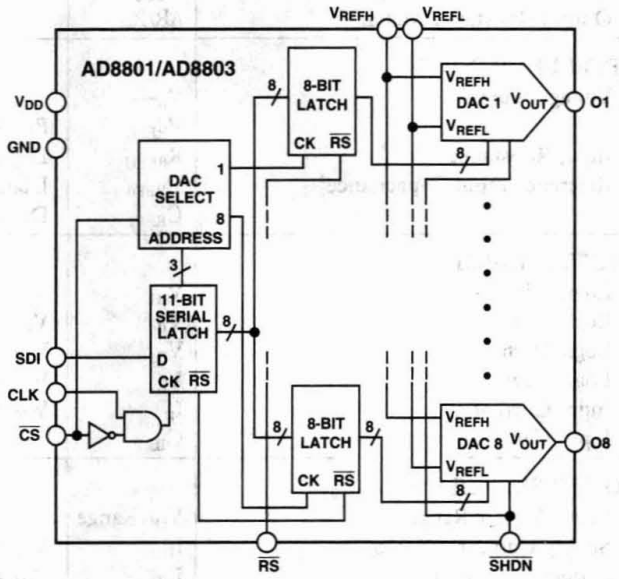
Low Cost
Replaces Eight Potentiometers
Eight Individually Programmable Outputs
Three-Wire Serial Input
Power Shutdown ≤ 25 μW Including I_{DD} and I_{REF}
Midscale Preset, AD8801
Separate V_{REFL} Range Setting, AD8803
+3 V to +5 V Single Supply Operation

APPLICATIONS

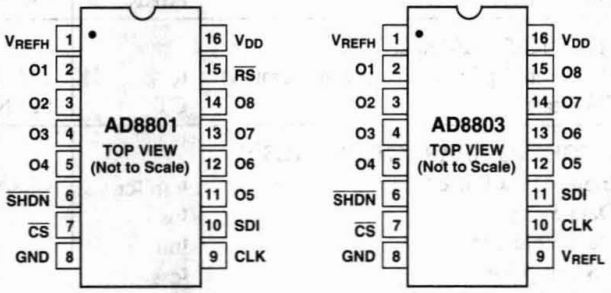
Automatic Adjustment
Trimmer Potentiometer Replacement
Video and Audio Equipment Gain and Offset Adjustment
Portable and Battery Operated Equipment

FUNCTIONAL BLOCK DIAGRAM

(DACs 2–7 Omitted for Clarity)



PIN CONFIGURATIONS



GENERAL DESCRIPTION

The AD8801/AD8803 provides eight digitally controlled dc voltage outputs. This potentiometer divider TrimDAC® allows replacement of the mechanical trimmer function in new designs. The AD8801/AD8803 is ideal for dc voltage adjustment applications.

Easily programmed by serial interfaced microcontroller ports, the AD8801 with its midscale preset is ideal for potentiometer replacement where adjustments start at a nominal value. Applications such as gain control of video amplifiers, voltage controlled frequencies and bandwidths in video equipment, geometric correction and automatic adjustment in CRT computer graphic displays are a few of the many applications ideally suited for these parts. The AD8803 provides independent control of both the top and bottom end of the potentiometer divider allowing a separate zero-scale voltage setting determined by the V_{REFL} pin. This is helpful for maximizing the resolution of devices with a limited allowable voltage control range.

Internally the AD8801/AD8803 contain eight voltage output digital-to-analog converters, sharing a common reference voltage input.

Each DAC has its own DAC register that holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register that is loaded from a standard three-wire serial input digital interface. Eleven data bits make up the data word clocked into the serial input register. This data word is decoded where the first 3 bits determine the address of the DAC register to be loaded with the last 8 bits of data. The AD8801/AD8803 consumes only 5 μA from 5 V power supplies. In addition, in shutdown mode reference input current consumption is also reduced to 5 μA while saving the DAC latch settings for use after return to normal operation.

The AD8801/AD8803 is available in 16-pin plastic DIP and the 1.5 mm height SO-16 surface mount packages.

ORDERING GUIDE

Model	FTN	Temperature	Package Description	Package Option*
AD8801AN	$\overline{RS}$	–40°C to +85°C	P-DIP-16	N-16
AD8801AR	$\overline{RS}$	–40°C to +85°C	SO-16	R-16A
AD8803AN	REFL	–40°C to +85°C	P-DIP-16	N-16
AD8803AR	REFL	–40°C to +85°C	SO-16	R-16A

*For outline information see Package Information section.

See the AD8802/AD8804 for a twelve channel version of this product.
TrimDAC is a registered trademark of Analog Devices, Inc.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD8801/AD8803–SPECIFICATIONS (V_{DD} = +3 V ± 10% or +5 V ± 10%, V_{REFH} = +V_{DD}, V_{REFL} = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
STATIC ACCURACY						
Specifications Apply to All DACs						
Resolution	N		8			Bits
Integral Nonlinearity Error	INL		–1.5	±1/2	+1.5	LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Full-Scale Error	G_{FSE}		–4	–2.8	+0.5	LSB
Zero-Code Error	V_{ZSE}		–0.5	±0.1	+0.5	LSB
DAC Output Resistance	R_{OUT}		3	5	8	kΩ
Output Resistance Match	$\Delta R/R_O$			1		%
REFERENCE INPUT						
Voltage Range[2]	V_{REFH}		0		V_{DD}	V
	V_{REFL}	Pin Available on AD8803 Only	0		V_{DD}	V
Input Resistance	R_{REFH}	Digital Inputs = 55_H, V_{REFH} = V_{DD}		2		kΩ
Reference Input Capacitance[3]	C_{REF0}	Digital Inputs All Zeros		25		pF
	C_{REF1}	Digital Inputs All Ones		25		pF
DIGITAL INPUTS						
Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V			±1	µA
Input Capacitance[3]	C_{IL}			5		pF
POWER SUPPLIES[4]						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	5	µA
Supply Current (TTL)	I_{DD}	V_{IH} = 2.4 V or V_{IL} = 0.8 V, V_{DD}= +5.5 V		1	4	mA
Shutdown Current	I_{REFH}	$\overline{SHDN}$ = 0		0.01	5	µA
Power Dissipation	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			27.5	µW
Power Supply Sensitivity	PSRR	V_{DD} = 5 V ± 10%, V_{REFH} = +4.5 V		0.001	0.002	%/%
Power Supply Sensitivity	PSRR	V_{DD} = 3 V ± 10%, V_{REFH} = +2.7 V		0.01		%/%
DYNAMIC PERFORMANCE[3]						
V_{OUT} Settling Time (Positive or Negative)	t_S	±1/2 LSB Error Band		0.6		µs
Crosstalk	CT	See Note 5, f = 100 kHz		50		dB
SWITCHING CHARACTERISTICS[3, 6]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	15			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		10			ns
Reset Pulse Width	t_{RS}		60			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		15			ns
$\overline{CS}$ Rise to Next Rising Clock	t_{CS1}		10			ns

NOTES

[1]Typical values represent average readings measured at +25°C.

[2]V_{REFH} can be any value between GND and V_{DD}, for the AD8803 V_{REFL} can be any value between GND and V_{DD}.

[3]Guaranteed by design and not subject to production test.

[4]Digital Input voltages V_{IN} = 0 V or V_{DD} for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from ($I_{DD} \times V_{DD}$).

[5]Measured at a V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.

[6]See timing diagram for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

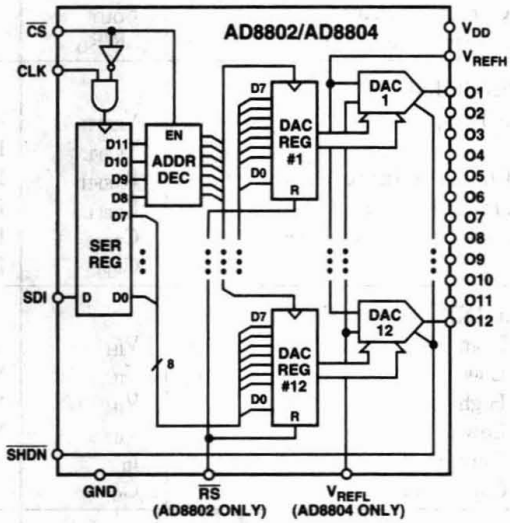
12 Channel, 8-Bit TrimDACs with Power Shutdown

AD8802/AD8804

FEATURES
Low Cost
Replaces 12 Potentiometers
Individually Programmable Outputs
3-Wire SPI Compatible Serial Input
Power Shutdown <55 μWatts Including I_{DD} & I_{REF}
Midscale Preset, AD8802
Separate V_{REFL} Range Setting, AD8804
+3 V to +5 V Single Supply Operation

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Video and Audio Equipment Gain and Offset Adjustment
Portable and Battery Operated Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 12-channel AD8802/AD8804 provides independent digitally-controllable voltage outputs in a compact 20-lead package. This potentiometer divider TrimDAC® allows replacement of the mechanical trimmer function in new designs. The AD8802/AD8804 is ideal for dc voltage adjustment applications.

Easily programmed by serial interfaced microcontroller ports, the AD8802 with its midscale preset is ideal for potentiometer replacement where adjustments start at a nominal value. Applications such as gain control of video amplifiers, voltage controlled frequencies and bandwidths in video equipment, geometric correction and automatic adjustment in CRT computer graphic displays are a few of the many applications ideally suited for these parts. The AD8804 provides independent control of both the top and bottom end of the potentiometer divider allowing a separate zero-scale voltage setting determined by the V_{REFL} pin. This is helpful for maximizing the resolution of devices with a limited allowable voltage control range.

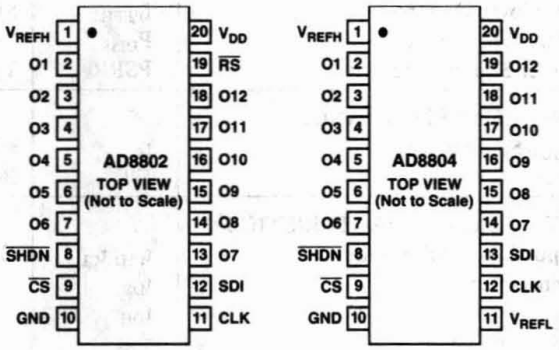
Internally the AD8802/AD8804 contains 12 voltage-output digital-to-analog converters, sharing a common reference-voltage input.

Each DAC has its own DAC latch that holds its output state. These DAC latches are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial input digital interface. The serial-data-input word is decoded where the first 4 bits determine the address of the DAC latches to be loaded with the last 8 bits of data. The AD8802/AD8804 consumes only 10 μA from 5 V power supplies. In addition, in shutdown mode reference input current consumption is also reduced to 10 μA while saving the DAC latch settings for use after return to normal operation.

The AD8802/AD8804 is available in the 20-pin plastic DIP, the SOIC-20 surface mount package, and the 1 mm thin TSSOP-20 package.

TrimDAC is a registered trademark of Analog Devices, Inc.

PIN CONFIGURATIONS



ORDERING GUIDE

Model	FTN	Temperature Range	Package Description	Package Option*
AD8802AN	$\overline{RS}$	−40°C/+85°C	P-DIP-20	N-20
AD8802AR	$\overline{RS}$	−40°C/+85°C	SOL-20	R-20
AD8802ARU	$\overline{RS}$	−40°C/+85°C	TSSOP-20	RU-20
AD8804AN	REFL	−40°C/+85°C	P-DIP-20	N-20
AD8804AR	REFL	−40°C/+85°C	SOL-20	R-20
AD8804ARU	REFL	−40°C/+85°C	TSSOP-20	RU-20

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD8802/AD8804–SPECIFICATIONS (V_{DD} = +3 V ± 10% or +5 V ± 10%, V_{REFH} = +V_{DD}, V_{REFL} = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
STATIC ACCURACY						
Specifications apply to all DACs						
Resolution	N		8			Bits
Differential Nonlinearity Error	DNL	Guaranteed Monotonic	–1	±1/4	+1	LSB
Integral Nonlinearity Error	INL		–1.5	±1/2	+1.5	LSB
Full-Scale Error	G_{FSE}		–1	1/2	+1	LSB
Zero Code Error	V_{ZSE}		–1	1/4	+1	LSB
DAC Output Resistance	R_{OUT}		3	5	8	kΩ
Output Resistance Match	$\Delta R/R_O$			1.5		%
REFERENCE INPUT						
Voltage Range[2]	V_{REFH}		0		V_{DD}	V
	V_{REFL}	Pin Available on AD8804 Only	0		V_{DD}	V
REFH Input Resistance	R_{REFH}	Digital Inputs = 55_H, V_{REFH} = V_{DD}		1.2		kΩ
REFL Input Resistance[3]	R_{REFL}	Digital Inputs = 55_H, V_{REFL} = V_{DD}		1.2		kΩ
Reference Input Capacitance[3]	C_{REF0}	Digital Inputs all Zeros		32		pF
	C_{REF1}	Digital Inputs all Ones		32		pF
DIGITAL INPUTS						
Logic High	V_{IH}	V_{DD} = +5 V	2.4			V
Logic Low	V_{IL}	V_{DD} = +5 V			0.8	V
Logic High	V_{IH}	V_{DD} = +3 V	2.1			V
Logic Low	V_{IL}	V_{DD} = +3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or +5 V			±1	μA
Input Capacitance[3]	C_{IL}			5		pF
POWER SUPPLIES[4]						
Power Supply Range	V_{DD} Range		2.7		5.5	V
Supply Current (CMOS)	I_{DD}	V_{IH} = V_{DD} or V_{IL} = 0 V		0.01	10	μA
Supply Current (TTL)	I_{DD}	V_{IH} = 2.4 V or V_{IL} = 0.8 V, V_{DD} = +5.5 V		1	4	mA
Shutdown Current	I_{REFH}	$\overline{SHDN}$ = 0		0.2	10	μA
Power Dissipation	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = 0 V, V_{DD} = +5.5 V			55	μW
Power Supply Sensitivity	PSRR	V_{DD} = +5 V ± 10%		0.001	0.002	%/%
DYNAMIC PERFORMANCE[3]						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band		0.6		μs
Crosstalk	CT	Between Adjacent Outputs[5]		50		dB
SWITCHING CHARACTERISTICS[3, 6]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	15			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		10			ns
Reset Pulse Width	t_{RS}		90			ns
CLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		20			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES

[1]Typicals represent average readings at +25°C.

[2]V_{REFH} can be any value between GND and V_{DD}, for the AD8804 V_{REFL} can be any value between GND and V_{DD}.

[3]Guaranteed by design and not subject to production test.

[4]Digital Input voltages V_{IN} = 0 V or V_{DD} for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from (I_{DD} × V_{DD}).

[5]Measured at a V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change (f = 100 kHz).

[6]See timing diagram for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

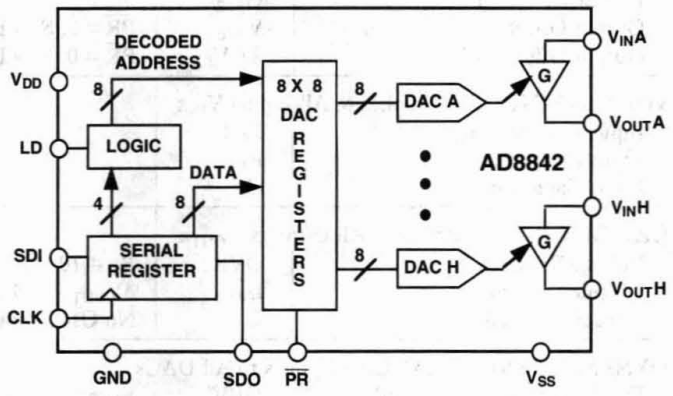
8-Bit Octal, 4-Quadrant Multiplying, CMOS TrimDAC

AD8842

FEATURES
Low Cost
Replaces 8 Potentiometers
50 kHz 4-Quadrant Multiplying Bandwidth
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 V Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS
Automatic Adjustment
Trimmer Replacement
Vertical Deflection Amplitude Adjustment
Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD8842 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC® capability allows replacement of the mechanical trimmer function in new designs. The AD8842 is ideal for ac or dc gain control of up to 50 kHz bandwidth signals. The four-quadrant multiplying capability is useful for signal inversion and modulation often found in video vertical deflection circuitry.

Internally the AD8842 contains eight voltage output digital-to-analog converters, each with separate voltage inputs. A new current conveyor amplifier design performs the four-quadrant multiplying function with a single amplifier at the output of the current steering digital-to-analog converter. This approach offers an improved constant input resistance performance versus previous voltage switched DACs used in TrimDAC circuits, eliminating the need for additional input buffer amplifiers.

Each DAC has its own DAC register that holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register that is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple DAC applications without additional external decoding logic.

TrimDAC is a registered trademark of Analog Devices, Inc.
The current conveyor amplifier is a patented circuit belonging to Analog Devices, Inc.

The AD8842 consumes only 95 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC8841. The AD8842 is pin compatible with the 1 MHz multiplying bandwidth DAC8840. The AD8842 is available in 24-pin plastic DIP and surface mount SOL-24 packages.

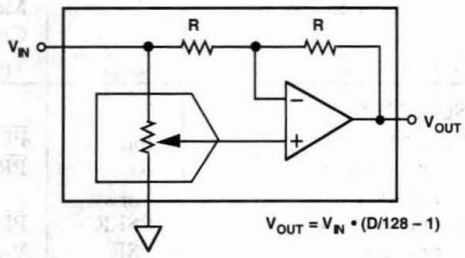


Figure 1. Functional Circuit of One 4-Quadrant Multiplying Channel

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option[2]
AD8842AN	XIND	24-Pin 300mil P-DIP	N-24
AD8842AR	XIND	24-Pin 300mil SOIC	SOL-24

NOTES
[1]XIND = –40°C to +85°C. The AD8842 contains 2452 transistors.
[2]For outline information see Package Information section.

AD8842–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = +5 V, V_{SS} = –5 V, All $V_{IN}x$ = +3 V, T_A = –40°C to +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY—All Specifications Apply for DACs A, B, C, D, E, F, G, H						
Resolution	N		8			Bits
Integral Nonlinearity Error	INL			±0.2	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic		±0.4	±1	LSB
Full-Scale Gain Error	G_{FSE}			2		LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		5	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		5		µV/°C
VOLTAGE INPUTS—Applies to All Inputs $V_{IN}x$						
Input Voltage Range[1]	IVR		±3	±4		V
Input Resistance	R_{IN}		12	19		kΩ
Input Capacitance	C_{IN}			9		pF
DAC OUTPUTS—Applies to All Outputs $V_{OUT}x$						
Voltage Range[1]	OVR	R_L = 10 kΩ	±3	±4		V
Output Current	I_{OUT}	ΔV_{OUT} < 1.5 LSB	±3			mA
Capacitive Load	C_L	No Oscillation		500		pF
DYNAMIC PERFORMANCE—Applies to All DACs						
Full Power Gain Bandwidth[1]	GBW	$V_{IN}x$ = ±3 V_P, R_L = 2 kΩ, C_L = 10 pF	10	50		kHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}x$ = +5.5 V	0.5	1.0		V/µs
Negative	SR–	$\Delta V_{OUT}x$ = –5.5 V	1.0	1.8		V/µs
Total Harmonic Distortion	THD	$V_{IN}x$ = 4 V p-p, D = FF_H, f = 1 kHz, f_{LPF} = 80 kHz, R_L = 1 kΩ		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz, V_{IN} = 0 V		78		nV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 00_H to FF_H		2.9		µs
		D = FF_H to 00_H		5.4		µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz		72		dB
Digital Feedthrough	Q	$V_{IN}x$ = 0 V, D = 0 to 255_{10}		5		nV-s
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		10	14	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		9	13	mA
Power Dissipation[2]	P_{DISS}			95	135	mW
Power Supply Rejection	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0001	0.01	%/%
Power Supply Range	PSR	V_{DD}, $\lvert V_{SS} \rvert$	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7		pF
Input Coding				Offset Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS[1]						
Input Clock Pulse Width	t_{CH}, t_{CL}		60			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				80	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTES

[1]Guaranteed by design, not subject to production test.

[2]Calculated limit = 5 V × (I_{DD} + I_{SS}).

Specifications subject to change without notice.

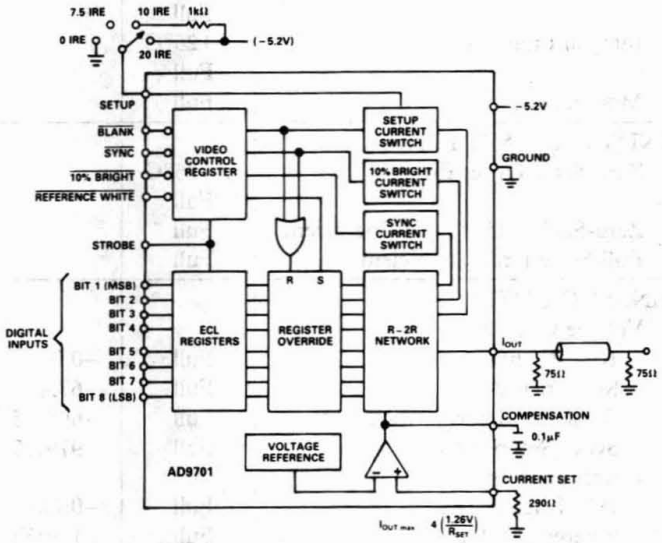
250 MSPS Video Digital-to-Analog Converter

AD9701

FEATURES
250 MSPS Update Rate
Low Glitch Impulse
Complete Composite Functions
Internal Voltage Reference
Single –5.2 V Supply

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

FUNCTIONAL BLOCK DIAGRAM



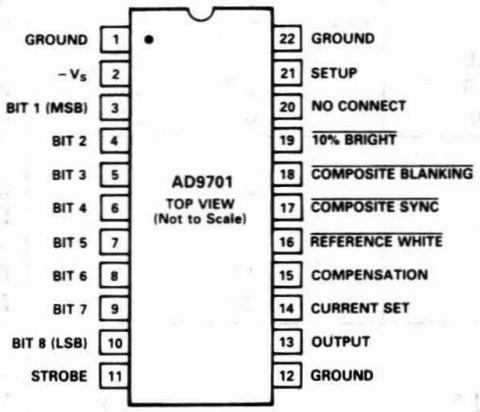
GENERAL DESCRIPTION

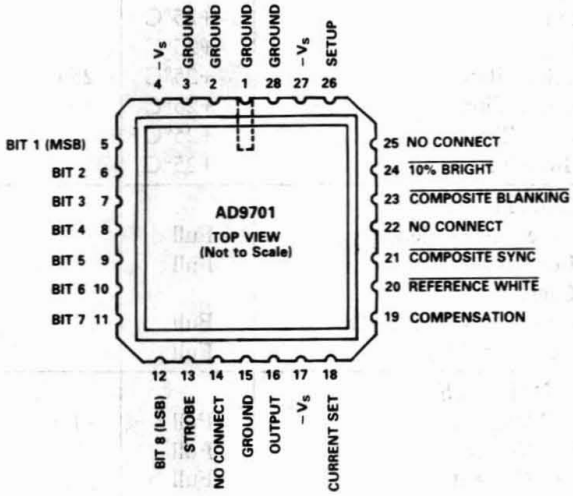
The AD9701 is a high-speed, 8-bit digital-to-analog converter with fully integrated composite video functions. High-speed ECL input registers provide synchronous operation of data and control functions up to 250 MSPS.

The AD9701 incorporates on-board control functions including horizontal sync, blanking, reference white level, and a 10% bright signal for highlighting. The setup level is also adjustable from 0 IRE units to 20 IRE units, through the control pin. An internal voltage reference allows the AD9701 to operate as a stand-alone video reconstruction DAC.

The AD9701 is available as an industrial temperature range device, –25°C to +85°C, and as an extended temperature range device, –55°C to +125°C. Both grades of the AD9701 are packaged in a 22-pin ceramic DIP, with the extended temperature device also available in a 28-pin LCC package.

PIN CONFIGURATIONS





ORDERING GUIDE

Device	Temperature Range	Description	Package Option*
AD9701BQ	–25°C to +85°C	22-Pin DIP, Industrial Temperature	Q-22
AD9701SE	–55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9701SQ	–55°C to +125°C	22-Pin DIP, Extended Temperature	Q-22

*E = Leadless Ceramic Chip Carrier; Q = Cerdip. For outline information see Package Information section.

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AD9701–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Supply Voltages = –5.2 V; R_L = 37.5 Ω; Setup = 0 V, unless otherwise noted)

Parameter	Temp	AD9701BQ Min	AD9701BQ Typ	AD9701BQ Max	AD9701SQ/SE Min	AD9701SQ/SE Typ	AD9701SQ/SE Max	Units
RESOLUTION		8			8			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Integral Linearity	+25°C		0.25	0.5		0.25	0.5	LSB
	Full			1.0			1.0	LSB
Monotonicity	Full		Guaranteed			Guaranteed		
INITIAL OFFSET ERROR								
Zero-Scale Offset Error	+25°C		0.05	0.9		0.05	0.9	mV
	Full			0.9			0.9	mV
Zero-Scale Offset Drift Coefficient	Full		2			2		µV/°C
Full-Scale Drift Coefficient	Full		50			50		µV/°C
ANALOG OUTPUT								
Voltage Output								
10% Bright	Full	–0.9	0		–0.9	0		mV
Reference White	Full	–67.45	–71	–74.55	–67.45	–71	–74.55	mV
Blanking (Setup = 0IRE)	Full	–698.55	–708.5	–718.45	–698.55	–708.5	–718.45	mV
Sync (Setup = 0IRE)	Full	–979.25	–993.5	–1007.75	–979.25	–993.5	–1007.75	mV
Current output								
10% Bright	Full	–0.024	0		–0.024	0		mA
Reference White	Full	–1.805	–1.9	–1.996	–1.805	–1.9	–1.995	mA
Blanking (Setup = 0IRE)	Full	–18.63	–18.9	–19.16	–18.63	–18.9	–19.16	mA
Sync (Setup = 0IRE)	Full	–26.11	–26.5	–26.87	–26.11	–26.5	–26.87	mA
Output Compliance Range	Full		–1.6; +0.1			–1.6; +0.1		V
Output Resistance	+25°C	640	800		640	800		Ω
DYNAMIC PERFORMANCE								
Update Rate	+25°C	225	250		225	250		MSPS
Output Propagation Delay	+25°C		5	6		5	6	ns
Output Settling Time								
Current	+25°C		8			8		ns
Voltage	+25°C		12			12		ns
Output Slew Rate	+25°C	255	300		255	300		V/µs
Output Rise Time	+25°C		1.7	2.0		1.7	2.0	ns
Output Fall Time	+25°C		1.7	2.0		1.7	2.0	ns
Glitch Impulse	+25°C		60	70		60	70	pV-s
SETUP CONTROL								
Setup Level (Grounded)	Full		0			0		IRE
Setup Level (Open)	Full		7.5			7.5		IRE
Setup Level								
(Tied to –5.2 V with 1 kΩ)	Full		10			10		IRE
Setup Level (–5.2 V)	Full		20			20		IRE
DIGITAL INTPUTS								
Logic "1" Voltage	Full	–1.1			–1.1			V
Logic "0" Voltage	Full			–1.5			–1.5	V
Logic "1" Current	Full			100			100	µA
Logic "0" Current	Full			15			15	µA
Input Capacitance	+25°C		4	5.5		4	5.5	pF
Data Setup Time	+25°C	0.1			0.1			ns
Data Hold Time	+25°C	1.4			1.4			ns
POWER SUPPLY								
Supply Current (–5.2 V)	+25°C		140	160		140	160	mA
	Full			160			160	mA
Nominal Power Dissipation	+25°C		728			728		mW
Power Supply Rejection Ratio	Full		3	6		3	6	mV/V

Specifications subject to change without notice.

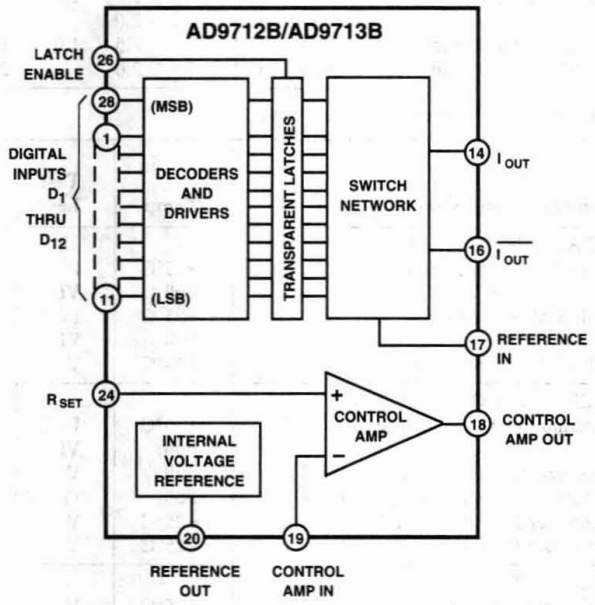
12-Bit, 100 MSPS D/A Converters

AD9712B/AD9713B

FEATURES
100 MSPS Update Rate
ECL/TTL Compatibility
SFDR @ 1 MHz: 70 dBc
Low Glitch Impulse: 28 pV-s
Fast Settling: 27 ns
Low Power: 725 mW
1/2 LSB DNL (B Grade)
40 MHz Multiplying Bandwidth

APPLICATIONS
ATE
Signal Reconstruction
Arbitrary Waveform Generators
Digital Synthesizers
Signal Generators

FUNCTIONAL BLOCK DIAGRAM



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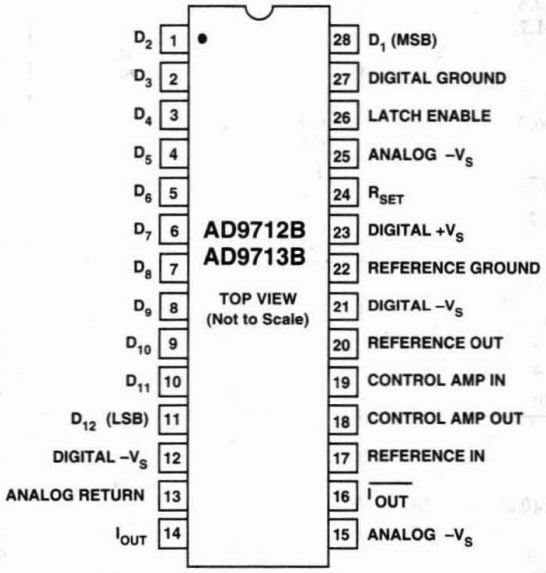
GENERAL DESCRIPTION

The AD9712B and AD9713B D/A converters are replacements for the AD9712 and AD9713 units which offer improved ac and dc performance. Like their predecessors, they are 12-bit, high speed digital-to-analog converters fabricated in an advanced oxide isolated bipolar process. The AD9712B is an ECL-compatible device featuring update rates of 100 MSPS minimum; the TTL-compatible AD9713B will update at 80 MSPS minimum.

Designed for direct digital synthesis, waveform reconstruction, and high resolution imaging applications, both devices feature low glitch impulse of 28 pV-s and fast settling times of 27 ns. Both units are characterized for dynamic performance and have excellent harmonic suppression.

The AD9712B and AD9713B are available in 28-pin plastic DIPs and PLCCs, with an operating temperature range of –25°C to +85°C. Both are also available for extended temperature ranges of –55°C to +125°C in cerdips and 28-pin LCC packages.

DIP/PLCC/LCC



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9712BAN	–25°C to +85°C	28-Pin P-DIP	N-28
AD9712BBN	–25°C to +85°C	28-Pin P-DIP	N-28
AD9712BAP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9712BBP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9712BSQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BSE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9712BTQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9712BTE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9713BAN	–25°C to +85°C	28-Pin P-DIP	N-28
AD9713BBN	–25°C to +85°C	28-Pin P-DIP	N-28
AD9713BAP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9713BBP	–25°C to +85°C	28-Pin PLCC	P-28A
AD9713BSQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BSE/883B	–55°C to +125°C	28-Pin LCC	E-28A
AD9713BTQ/883B	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9713BTE/883B	–55°C to +125°C	28-Pin LCC	E-28A

*For outline information see Package Information section.

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AD9712B/AD9713B–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

[$-V_S = -5.2$ V; $+V_S = +5$ V (AD9713B only); Reference Voltage = –1.2 V; $R_{SET} = 7.5$ kΩ; $V_{OUT} = 0$ V (virtual ground); unless otherwise noted]

Parameter (Conditions)	Temp	Test Level	AD9712B/AD9713B AN/AP Min	AN/AP Typ	AN/AP Max	AD9712B/AD9713B BN/BP Min	BN/BP Typ	BN/BP Max	AD9712B/AD9713B SE/SQ Min	SE/SQ Typ	SE/SQ Max	AD9712B/AD9713B TE/TQ Min	TE/TQ Typ	TE/TQ Max	Units
RESOLUTION				12			12			12			12		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I	–1.25	1.0	+1.25	–0.75	0.5	+0.75	–1.5	1.0	+1.5	–1.0	0.5	+1.0	LSB
	Full	VI	–2.0		2.0	–1.5		1.5	–2.0		2.0	–1.5		1.5	LSB
Integral Nonlinearity	+25°C	I	–1.5	1.0	1.5	–1.0	0.75	1.0	–1.75	1.5	1.75	–1.25	1.0	1.25	LSB
("Best Fit" Straight Line)	Full	VI	–2.0		2.0	–1.75		1.75	–2.0		2.0	–1.75		1.75	LSB

Specifications subject to change without notice.

Parameter (Conditions)	Temp	Test Level	AD9712B All Grades Min	AD9712B All Grades Typ	AD9712B All Grades Max	AD9713B All Grades Min	AD9713B All Grades Typ	AD9713B All Grades Max	Units
INITIAL OFFSET ERROR									
Zero-Scale Offset Error	+25°C	I		0.5	2.5		0.5	2.5	µA
	Full	VI			5.0			5.0	µA
Full-Scale Gain Error	+25°C	I		1.0	5		1.0	5	%
	Full	VI			8			8	%
Offset Drift Coefficient	+25°C	V		0.01			0.01		µA/°C
REFERENCE/CONTROL AMP									
Internal Reference Voltage	+25°C	I	–1.14	–1.18	–1.22	–1.14	–1.18	–1.22	V
	Full	VI	–1.12		–1.24	–1.12		–1.24	V
Internal Reference Voltage Drift	Full	V		50			50		ppm/°C
Internal Reference Output Current	Full	IV	–50		+500	–50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50		kΩ
Amplifier Bandwidth	+25°C	V		300			300		kHz
REFERENCE INPUT									
Reference Input Impedance	+25°C	V		3			3		kΩ
Reference Multiplying Bandwidth	+25°C	V		40			40		MHz
DYNAMIC PERFORMANCE									
Full-Scale Output Current	+25°C	V		20.48			20.48		mA
Output Compliance Range	+25°C	IV	–1.2		+2	–1.2		+2	V
Output Resistance	+25°C	IV	2.0	2.5	3.0	2.0	2.5	3.0	kΩ
Output Capacitance	+25°C	V		15			15		pF
Output Update Rate	+25°C	IV	100	110		80	100		MSPS
Output Settling Time (t_{ST})	+25°C	V		27			27		ns
Output Propagation Delay (t_{PD})	+25°C	V		6			7		ns
Glitch Impulse	+25°C	V		28			28		pV-s
Output Rise Time	+25°C	V		2			2		ns
Output Fall Time	+25°C	V		2			2		ns
DIGITAL INPUTS									
Logic "1" Voltage	Full	VI	–1.0	–0.8		2.0			V
Logic "0" Voltage	Full	VI		–1.7	–1.5			0.8	V
Logic "1" Current	Full	VI			20			20	µA
Logic "0" Current	Full	VI			10			600	µA
Input Capacitance	+25°C	V		3			3		pF
Input Setup Time (t_S)	+25°C	IV	0.5	–0.3		0.5	–0.3		ns
	Full	IV	0.8			0.8			ns
Input Hold Time (t_H)	+25°C	IV	1.8	1.2		1.8	1.2		ns
	Full	IV	2.0			2.0			ns
Latch Pulse Width (t_{LPW}) (LOW)	+25°C	IV	2.5	1.7		2.5	1.7		ns
(Transparent)	Full		2.8			2.8			ns
AC LINEARITY									
Spurious-Free Dynamic Range (SFDR)									
1.23 MHz; 10 MSPS; 2 MHz Span	+25°C	V		70			70		dB
5.055 MHz; 20 MSPS; 2 MHz Span	+25°C	V		72			72		dB
10.1 MHz; 50 MSPS; 2 MHz Span	+25°C	V		68			68		dB
16 MHz; 40 MSPS; 10 MHz Span	+25°C	V		68			68		dB
POWER SUPPLY									
Positive Supply Current (+5.0 V)	+25°C	I					6	12	mA
	Full	VI						14	mA
Negative Supply Current (–5.2 V)	+25°C	I		140	178		145	184	mA
	Full	VI			183			188	mA
Nominal Power Dissipation	+25°C	V		728			784		mW
Power Supply Rejection Radio (PSRR)	+25°C	I		30	100		30	100	µA/V

Specifications subject to change without notice.

10-Bit, 400 MSPS D/A Converters

AD9720/AD9721

FEATURES

400 MSPS (ECL)/100 MSPS (TTL) Update Rate
Low Glitch Impulse: 1.5 pV-s
Fast Settling: 4.5 ns to 1/2 LSB
Low Power: 1.1 W
On-Board Quadrature Logic for DDS Applications
Differential Clock (ECL)

APPLICATIONS

Direct Digital Synthesis
Arbitrary Waveform Synthesis
Waveform Reconstruction
High Speed Imaging

GENERAL DESCRIPTION

The AD9720 and AD9721 D/A converters are 10-bit, high speed digital-to-analog converters constructed in an oxide isolated bipolar process. The AD9720 is ECL compatible, and will update up to 400 MSPS; the AD9721 is TTL compatible and will update up to 100 MSPS.

Designed for direct digital synthesis (DDS), waveform reconstruction, and high resolution video applications, both devices feature low glitch impulse of 1.5 pV-s and fast settling times of 4.5 ns to l/2 LSB.

Both converters are characterized for dynamic performance, and have excellent harmonic suppression and spectral purity in waveform generation applications.

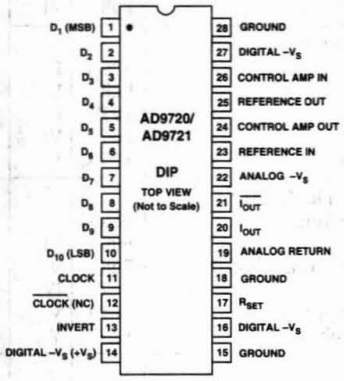
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9720BN	–25°C to +85°C	28-Pin Plastic DIP	N-28
AD9720BR	–25°C to +85°C	28-Pin SOIC	R-28
AD9720TE	–55°C to +125°C	28-Pin LCC	E-28A
AD9720TQ	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9721BN	–25°C to +85°C	28-Pin Plastic DIP	N-28
AD9721BR	–25°C to +85°C	28-Pin SOIC	R-28
AD9721TE	–55°C to +125°C	28-Pin LCC	E-28A
AD9721TQ	–55°C to +125°C	28-Pin Cerdip	Q-28

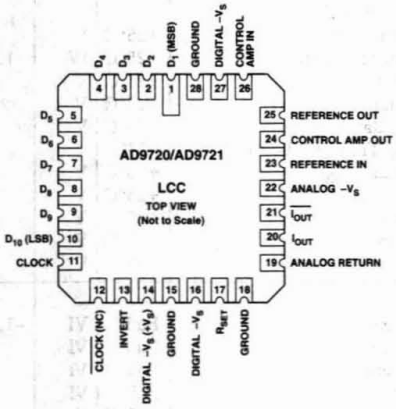
*For outline information see Package Information section.

PIN CONFIGURATIONS

DIP & SOIC Packages

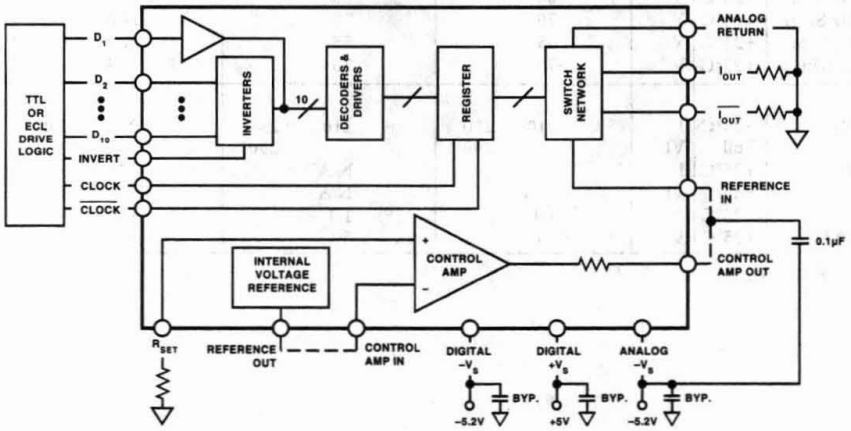


LCC Package



The units are available in 28-pin DIPs, LCCs and SOICs. Industrial temperature range devices are packaged in plastic for operation from –25°C to +25°C; extended temperature range devices for operation from –55°C to +125°C are in hermetic ceramic packages. Contact the factory for information about the availability of MIL-STD-883 devices.

FUNCTIONAL BLOCK DIAGRAM



AD9720/AD9721–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($-V_S = -5.2$ V; $+V_S = +5$ V (AD9721 only); Reference Voltage = –1.25 V; R_{SET} = 1,960 Ω, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9720BN/BR Min	AD9720BN/BR Typ	AD9720BN/BR Max	AD9720TE/TQ Min	AD9720TE/TQ Typ	AD9720TE/TQ Max	AD9721BN/BR Min	AD9721BN/BR Typ	AD9721BN/BR Max	AD9721TE/TQ Min	AD9721TE/TQ Typ	AD9721TE/TQ Max	Units
RESOLUTION				10			10			10			10		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.25	0 75		0.6	1.0		0.25	0.75		0.6	1.0	LSB
	Full	VI			1.0			1.5			1.0			1.5	LSB
Integral Nonlinearity	+25°C	I		0.5	1.0		0.7	1.5		0.5	1.0		0.7	1.5	LSB
("Best Fit" Straight Line)	Full	VI			1.5			2.0			1.5			2.0	LSB
INITIAL OFFSET ERROR															
Zero-Scale Offset Error	+25°C	I		16	60		16	60		16	60		16	60	µA
	Full	VI		20	75		20	75		20	75		20	75	µA
Full-Scale Gain Error	+25°C	I		2	15		2	15		2	15		2	15	%
	Full	VI			15			15			15			15	%
Offset Drift Coefficient	+25°C	V		0.04			0.04			0.04			0.04		µA/°C
REFERENCE/CONTROL AMP															
Internal Reference Voltage	+25°C	I	–1.15	–1.25	–1.35	–1.15	–1.25	–1.35	–1.15	–1.25	–1.35	–1.15	–1.25	–1.35	V
	Full	VI	–1.15		–1.35	–1.15		–1.35	–1.15		–1.35	–1.15		–1.35	V
Internal Reference Voltage Drift	Full	V		100			100			100			100		µV/°C
Internal Reference Output Current	Full	IV	–50		+500	–50		+500	–50		+500	–50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50			50			50		kΩ
Amplifier Bandwidth	+25°C	V		1			1			1			1		MHz
REFERENCE INPUT															
Reference Input Impedance	+25°C	V		4.6			4.6			4.6			4.6		kΩ
Reference Multiplying Bandwidth	+25°C	V		75			75			75			75		MHz
OUTPUT PERFORMANCE															
Full-Scale Output Current	+25°C	V		20.48			20.48			20.48			20.48		mA
Output Compliance Range	+25°C	IV	–1.5		+3	–1.5		+3	–1.5		+3	–1.5		+3	V
Output Resistance	+25°C	V		210			210			210			210		Ω
Output Capacitance	+25°C	V		6			6			6			6		pF
Output Update Rate	+25°C	V		400			400			100			100		MSPS
Voltage Settling Time (1/2 LSB)	+25°C	V		4.5			4.5			4.5			4.5		ns
Propagation Delay (t_{PD})	+25°C	V		4.0			4.0			4.5			4.5		ns
Glitch Impulse	+25°C	V		1.5			1.5			1.5			1.5		pV-s
Output Slew Rate	+25°C	V		1,000			1,000			1,000			1,000		V/µs
Output Rise Time	+25°C	V		675			675			675			675		ps
Output Fall Time	+25°C	V		470			470			470			470		ps
DIGITAL INPUTS															
Logic "1" Voltage	Full	VI	–1.0			–0.9			2.0			2.0			V
Logic "0" Voltage	Full	VI			–1.5			–1.6			0.8			0.8	V
Logic "1" Current	Full	VI			50			50			400			400	µA
Logic "0" Current	Full	VI			2			2			700			700	µA
Input Capacitance	+25°C	V		3			3			3			3		pF
Input Setup Time (t_S)	+25°C	IV	1.0	0.4		1.0	0.4		1.0	0.5		1.0	0.5		ns
	Full	IV	1.2			1.2			1.2			1.2			ns
Input Hold Time (t_H)	+25°C	IV	1.6	1.2		1.6	1.2		2.0	1.25		2.0	1.25		ns
	Full	IV	2.8			2.8			2.3			2.3			ns
Clock Pulse Width (Low)	+25°C	IV	1.1	0.85		1.1	0.85		1.0	0.85		1.0	0.85		ns
Clock Pulse Width (High)	+25°C	IV	1.4	0.85		1.4	0.85		1.1	0.85		1.1	0.85		ns
DYNAMIC PERFORMANCE															
Spurious-Free Dynamic Range (SFDR)															
2.02 MHz; 100 MSPS; 2 MHz Span	+25°C	V		75			75			75			75		dBc
25.01 MHz; 100 MSPS; 2 MHz Span	+25°C	V		66			66			66			66		dBc
10.02 MHz; 250 MSPS; 5 MHz Span	+25°C	V		70			70			N/A			N/A		dBc
62.54 MHz; 250 MSPS; 5 MHz Span	+25°C	V		55			55			N/A			N/A		dBc
70 MHz; 220 MSPS; 10 MHz Span	+25°C	V		70			70			N/A			N/A		dBc
POWER SUPPLY															
Negative Supply Current (–5.2 V)	+25°C	I		210	280		210	280		218	290		218	290	mA
	Full	VI			290			290			300			300	mA
Positive Supply Current (+5.0 V)	+25°C	I		N/A			N/A			14	30		14	30	mA
	Full	VI		N/A			N/A				30			30	mA
Nominal Power Dissipation	+25°C	V		1.1			1.1			1.2			1.2		W
Power Supply Rejection Ratio (PSRR)	+25°C	V		50			50			50			50		µA/V

Specifications subject to change without notice.

ANALOG DEVICES

Ultrahigh Speed IC D/A Converter

AD9768

FEATURES
5 ns Settling Time
100 MSPS Update Rate
20 mA Output Current
ECL-Compatible
40 MHz Multiplying Mode

APPLICATIONS
Raster Scan & Vector Graphic Displays
High Speed Waveform Generation
Digital VCOs
Ultrafast Digital Attenuators

GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100 MSPS. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40 MHz.

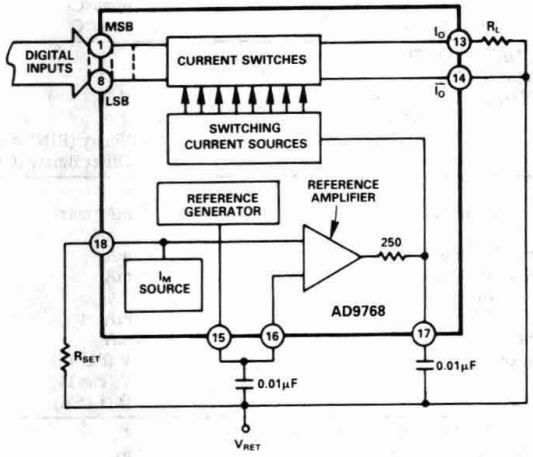
An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20 mA, which corresponds to a 1 volt drop across a 50 Ω load, or ±1 volt across 100 Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26$ V) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

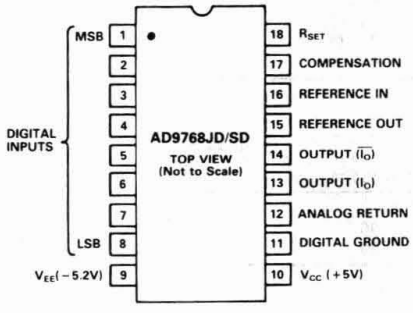
FUNCTIONAL BLOCK DIAGRAM



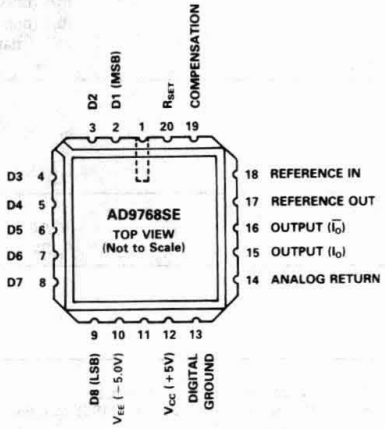
The reference voltage source is a modified bandgap type and is nominally –1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, Pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from Pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900 pF, although a 0.01 μF ceramic chip capacitor is recommended.

The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

AD9768JD/SD PIN CONNECTIONS



AD9768SE PIN CONNECTIONS



AD9768–SPECIFICATIONS (typical @ +25°C under following conditions unless otherwise noted; nominal digital input levels; nominal power supplies; R_L = 50 Ω; R_{SET} = 220 Ω; V_{RET} = 0 V)

Parameter	Unit	AD9768SJD/SD/SE
RESOLUTION (FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	µA	78
ACCURACY[1]		
Differential Nonlinearity	± % FS	0.2
Integral Nonlinearity	± % FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	µA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	1.5
Reference Voltage (–1.26 V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "1" =	V	–0.9
"0" =	V	–1.7
Coding	Binary (BIN) = Unipolar Out Offset Binary (OBN) = Bipolar Out	
OUTPUT		
Current (Unipolar) FS	mA (max)	2 to 20 (30)
I_{OUT} (@ Pin 13)		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
I_{OUT} (@ Pin 14)		
All Digital "1" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V (Pin 13)	–0.7 to +3.0
	V (Pin 14)	–1.1 to +3.0
Impedance	Ω (±15%)	750
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/µs	400
Update Rate	MSPS	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	–1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to –1.1 (–2)
Current-Multiplying Mode	mA (max)	0 to –5 (–7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	–0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8: –0.1 V_M Input = 0 mA I_{OUT}; –1.1 V_M Input = 0 mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: –0.1 V_M Input = 1 mA I_{OUT}; –1.1 V_M Input = 20 mA I_{OUT}	
Large Signal Bandwidth (–3 dB Point)	kHz	250
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range (at Pins 17 & 18)	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8: 1 mA I_M Input = 0 mA I_{OUT}; 5 mA I_M Input = 0 mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: 1 mA I_M Input = 4 mA I_{OUT}; 5 mA I_M Input = 20 mA I_{OUT}	
Large Signal Bandwidth (–3 dB Point)	MHz	40
POWER REQUIREMENTS		
–5.2 V ±0.25	mA (max)	66 (70)
+5.0 V ±0.25	mA (max)	14 (15)
Power Dissipation	mW (max)	410 (430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating		
AD9768JD	°C	0 to +70
AD9768SD/SE	°C	–55 to +125
Storage	°C	–55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θ_{JA} (Free Air)	°C/W	90
Junction to Case, θ_{JA}	°C/W	20
PACKAGE OPTION[8]		
Ceramic (D-18)	AD9768JD AD9768SD	
LCC (E-20A)	AD9768SE	

NOTES
[1]Relative to FS, including linearity (within voltage compliance limits).
[2]Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3]Applies when operating AD9768 as standard D/A.
[4]Based on R_L = 50 ohms; R_{SET} = 220 ohms; V_{RET} = 0 V.
[5]1% change in either power supply voltage causes 0.07% change in analog output.
[6]Case temperature.
[7]Maximum junction temperature 125°C.
[8]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

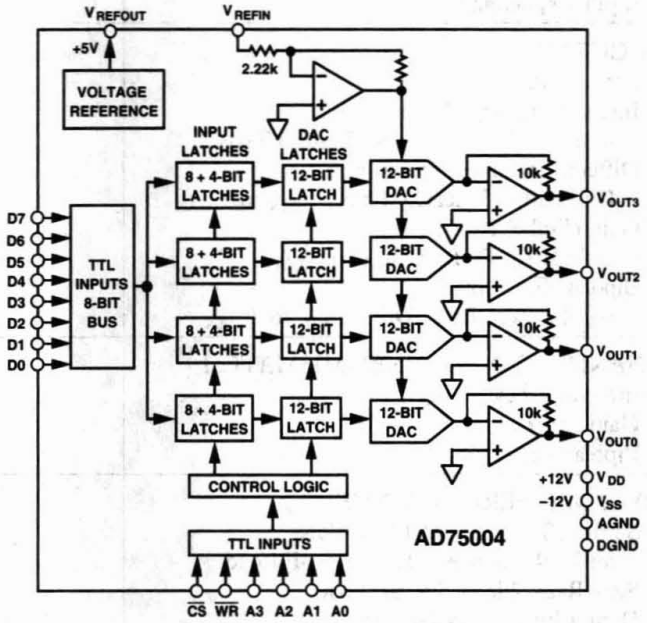
Specifications subject to change without notice.

Quad 12-Bit D/A Converter

AD75004

FEATURES
4 Complete 12-Bit D/A Functions
Double-Buffered Latches
Simultaneous Update of All DACs Possible
±5 V Output Range
High Stability Bandgap Reference
Monolithic BiMOS Construction
Guaranteed Monotonic over Temperature
3/4 LSB Linearity Guaranteed over Temperature
4 μs max Settling Time to 0.01%
Operates with ±12 V Supplies
Low Power: 720 mW max Including Reference
TTL/5 V CMOS Compatible Logic Inputs
8-Bit Microprocessor Interface
24-Pin PDIP or 28-Lead PLCC Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD75004 contains four complete, voltage output, 12-bit digital-to-analog converters, a high stability bandgap reference, and double-buffered input latches on a single chip. The converters use 12 precision high speed bipolar current steering switches and laser-trimmed thin-film resistor networks to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latches. The design of the input latches allows direct interface to 8-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 50 ns, allowing use with fast microprocessors.

The functional completeness and high performance of the AD75004 results from a combination of advanced switch design, the BiMOS II fabrication process, and proven laser trimming technology. BiMOS II is an epitaxial BiCMOS process optimized for analog and converter functions. The AD75004 is trimmed at the wafer level and is specified to ±1/2 LSB maximum linearity error at 25°C and ±3/4 LSB over the full operating temperature range. The on-chip output amplifiers provide an output range of ±5 V, with 1 LSB equal to 2.44 mV.

The bandgap reference on the chip has low noise, long term stability and temperature drift characteristics comparable to discrete reference diodes. The absolute value of the reference is laser trimmed to +5.00 V with 0.6% maximum error. Its temperature coefficient is also laser trimmed.

Typical full-scale gain TC is 15 ppm/°C. With guaranteed monotonicity over the full temperature range, the AD75004 is well suited for wide temperature range performance.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD75004KN	0°C to +70°C	N-24A
AD75004KP	0°C to +70°C	P-28A

*N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

AD75004–SPECIFICATIONS (T_A = +25°C, ±12.0 V power supplies unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
DIGITAL INPUTS (D0–D7, A0–A3, $\overline{CS}$, $\overline{WR}$)					
Logic Levels (TTL Compatible)					
Input Voltage, Logic "1"	V_{IH}	**2.0**		**5.5**	V
Input Voltage, Logic "0"	V_{IL}	**0**		**0.8**	V
Input Current, V_{IH} = 5.5 V	I_{IH}			**10**	μA
Input Current, V_{IL} = 0.8 V	I_{IL}			**10**	μA
Input Capacitance	C_{IN}			10	pF
ACCURACY					
Resolution				12	Bits
Integral Linearity Error			±1/4	**±1/2**	LSB
Integral Linearity Error, T_{MIN} to T_{MAX}			±1/2	±3/4	LSB
Differential Linearity Error			±1/2	**±3/4**	LSB
Differential Linearity Error, T_{MIN} to T_{MAX}			Guaranteed Monotonic		
Gain (Full-Scale) Error[1]			±2	**±10**	LSB
Gain Error Drift, T_{MIN} to T_{MAX}[1]			±15	±30	ppm/°C
Bipolar Zero Error[1]			±1	**±2**	LSB
Bipolar Zero Error Drift, T_{MIN} to T_{MAX}[1]			±3	±7	ppm/°C
CHANNEL-TO-CHANNEL MISMATCH					
Integral Linearity Error			±1/2	**±1**	LSB
Gain Error[1]			±1	**±4**	LSB
Bipolar Zero Error[1]			±1	**±2**	LSB
DYNAMIC PERFORMANCE					
Settling Time to ±0.01% of FSR for FSR Change, 2 kΩ ‖ 500 pF Load			2	4	μs
Slew Rate, 2 kΩ ‖ 500 pF Load		5			V/μs
Digital Input Crosstalk (Static)[2]				–50	dB
ANALOG OUTPUTS					
Full-Scale Range (FSR)	V_{OUT}		±5		V
Output Current	I_{OUT}	±5			mA
Short Circuit Limit Current				**±40**	mA
VOLTAGE REFERENCE					
Reference Output Voltage	V_{REFOUT}	**4.97**	5.00	**5.03**	V
Temperature Coefficient			±15	±25	ppm/°C
Reference Output Currents[3]		3.0	5.0		mA
Reference Input Voltage	V_{REFIN}	4.5	5.0	5.5	V
Reference Input Current @ 5.0 V	I_{REFIN}			3.0	mA
POWER SUPPLY GAIN SENSITIVITY					
$\Delta Gain/\Delta V_{DD}$, V_{DD} = +10.8 to +13.2 V dc[1]			±15	**±25**	ppm of FSR/%
$\Delta Gain/\Delta V_{SS}$, V_{SS} = –10.8 to –13.2 V dc[1]			±15	**±25**	ppm of FSR/%
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{SS}	**±10.8**	±12	**±13.2**	V
Supply Currents	I_{DD}, I_{SS}		±25	**±30**	mA
TEMPERATURE RANGE					
Specification	T_{MIN}, T_{MAX}	0		+70	°C
Storage		–65		+150	°C

NOTES

[1]Gain and bipolar zero errors are measured using internal voltage reference and include its errors.

[2]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2 kΩ ‖ 500 pF load by means of varying the digital input code.

[3]The internal voltage reference is intended to drive on-chip only; buffer it if using it externally.

[4]All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

CMOS
80 MHz, 10-Bit Video DAC

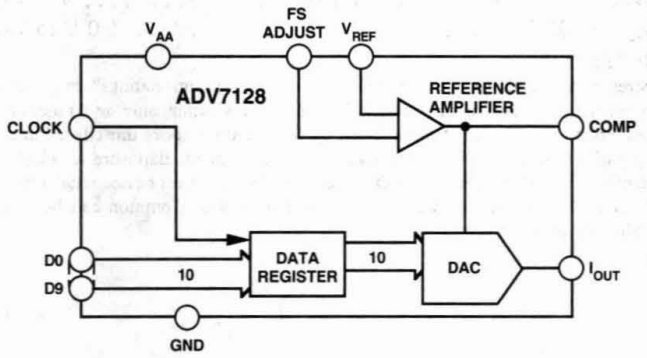
ADV7128

FEATURES
80 MHz Pipelined Operation
10-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
28-Pin SOIC Package

APPLICATIONS
High Definition Television (HDTV)
High Resolution Color Graphics
Digital Radio Modulation
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Direct Digital Synthesis (DDS) & I/O Modulation
Wireless LAN
Wireless Local Loop

SPEED GRADES
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The ADV7128 (ADV®) is a video speed, digital-to-analog converter on a single monolithic chip. It consists of a high speed, 10-bit, video D/A converters; a standard TTL input interface; and a high impedance, analog output, current source.

The ADV7128 has a 10-bit pixel input port. A single +5 V power supply, an external 1.23 V reference and pixel clock input are and all that are required to make the part operational.

The ADV7128 is capable of generating video output signals which are compatible with RS-343A, RS-170 and most proposed production system HDTV video standards, including SMPTE 240M.

The ADV7128 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The ADV7128 is available in a 28-lead small outline IC (SOIC).

ADV is a registered trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Guaranteed monotonic to 10 bits. Ten bits of resolution allows for implementation of linearization functions such as gamma correction and contrast enhancement.
3. Compatible with a wide variety of high resolution color graphics systems including RS-343A/RS-170 and the proposed SMPTE 240M standard for HDTV.
4. Combined with a numerically controlled oscillator (AD9955), it forms a complete frequency synthesizer (DDS).
5. Using the part's reduced power output DAC modes, it is ideal for power and cost sensitive communications type applications.

ORDERING GUIDE

Model	Speed	Accuracy DNL	Accuracy INL	Temperature Range	Package Option*
ADV7128KR80	80 MHz	±1	±1	0°C to +70°C	R-28
ADV7128KR50	50 MHz	±1	±1	0°C to +70°C	R-28
ADV7128KR30	30 MHz	±1	±1	0°C to +70°C	R-28

*R = SOIC. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ABSOLUTE MAXIMUM RATINGS[1]

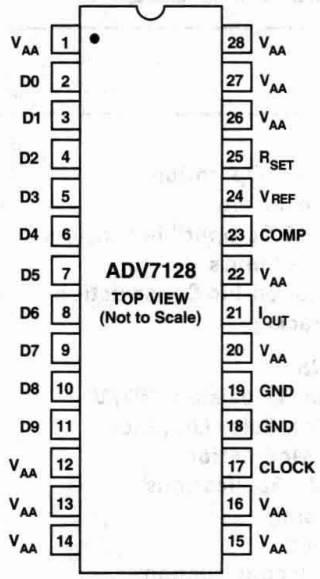
V_{AA} to GND ..... +7 V
Voltage on Any Digital Pin ..... GND –0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Vapor Phase Soldering (2 minutes) ..... +220°C
I_{OUT} to GND[2] ..... 0 V to V_{AA}

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7128 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R9, G0–G9, B0–B9, $\overline{SYNC}$ and $\overline{BLANK}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
D0–D9	Data inputs (TTL compatible). Data is latched on the rising edge of CLOCK. D0 is the least significant data bit. Unused data inputs should be connected to either the regular PCB power or ground plane.
I_{OUT}	Current output. This high impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable.
R_{SET}	Full-scale adjust control. A resistor (R_{SET}) connected between this pin and GND, controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on I_{OUT} is given by: I_{OUT} (mA) = 7,969 × V_{REF}(V)/R_{SET}(Ω)
COMP	Compensation pin. This is a compensation pin for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between COMP and V_{AA}.
V_{REF}	Voltage reference input. An external 1.23 V voltage reference must be connected to this pin. The use of an external resistor divider network is not recommended. A 0.1 µF decoupling ceramic capacitor should be connected between V_{REF} and V_{AA}.
V_{AA}	Analog power supply (5 V ± 5%). All V_{AA} pins on the ADV7128 must be connected.
GND	Ground. All GND pins must be connected.

ANALOG DEVICES

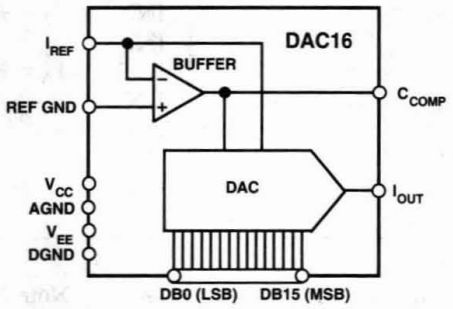
16-Bit High Speed Current-Output DAC

DAC16

FEATURES
±1 LSB Differential Linearity (max)
Guaranteed Monotonic Over Temperature Range
±2 LSB Integral Linearity (max)
500 ns Settling Time
5 mA Full-Scale Output
TTL/CMOS Compatible
Low Power: 190 mW (typ)
Available in Die Form

APPLICATIONS
Communications
ATE
Data Acquisition Systems
High Resolution Displays

FUNCTIONAL BLOCK DIAGRAM



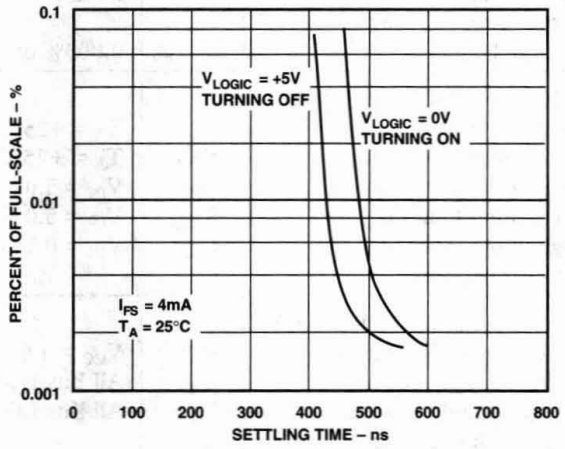


Figure 1. DAC16 Settling Time Accuracy vs. Percent of Full Scale

GENERAL DESCRIPTION

The DAC16 is a 16-bit high speed current-output digital-to-analog converter with a settling time of 500 ns. A unique combination of low distortion, high signal-to-noise ratio, and high speed make the DAC16 ideally suited to performing waveform synthesis and modulation in communications, instrumentation, and ATE systems. Input reference current is buffered, with full-scale output current of 5 mA. The 16-bit parallel digital input bus is TTL/CMOS compatible. Operating from +5 V and –15 V supplies, the DAC16 consumes 190 mW (typ) and is available in a 24-pin epoxy DIP, epoxy surface-mount small outline (SOL), ceramic side brazed DIP, 28-pin leadless ceramic chip carrier (LCC) packages, and in die form.

ORDERING GUIDE

Model	Grade DNL (max)	Temperature Range	Package Description	Package Option[1]
DAC16EP	±1	–40°C to +85°C	24-Pin PDIP	N-24
DAC16ES	±1	–40°C to +85°C	24-Pin SOL	R-24
DAC16FP	±2	–40°C to +85°C	24-Pin PDIP	N-24
DAC16FS	±2	–40°C to +85°C	24-Pin SOL	R-24
DAC16BWB[2]	±2	–55°C to +125°C	24-Pin Ceramic DIP	D-24A
DAC16BTC[2]	±2	–55°C to +125°C	28-Pin LCC	E-28A
DAC16GBC	±1	+25°C	Die	

NOTES
[1]For outline information see Package Information section.
[2]Consult factory for availability.

DAC16–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{CC} = +5.0 V, V_{EE} = –15.0 V, I_{REF} = 0.5 mA, C_{COMP} = 47 µF, –40°C ≤ T_A ≤ +85°C unless otherwise noted. See Note 1 for supply variations.)

Parameter		Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL	T_A = +25°C	–2	±1.2	+2	LSB
Integral Linearity "E"	INL		–4	±1.6	+4	LSB
Differential Linearity "E"	DNL	T_A = +25°C	–1	±0.5	+1	LSB
Differential Linearity "E"	DNL		–1	±0.7	+1.5	LSB
Integral Linearity "F"	INL	T_A = +25°C	–4	±1.4	+4	LSB
Integral Linearity "F"	INL		–6	±2	+6	LSB
Differential Linearity "F"	DNL	T_A = +25°C	–1	±0.5	+1.5	LSB
Differential Linearity "F"	DNL		–1.5	±0.6	+2	LSB
Zero Scale Error	ZSE				1	LSB
Zero Scale Drift	TC_{ZSE}			0.025		ppm/°C
Gain Error	GE				±0.225	% FS
Gain Drift	TC_{GE}			5		ppm/°C
REFERENCE[2]						
Reference Input Current	I_{REF}	Note 2	350		625	µA
OUTPUT CHARACTERISTICS						
Output Current	I_{OUT}	Note 2	2.8		5.0	mA
Output Capacitance	C_{OUT}			10		pF
Settling Time	t_S	0.003% of Full Scale		500		ns
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Input Current	I_{INH}	V_{IN} = 5.0 V, DB0–DB10			7.5	µA
Logic Input Current	I_{INH}	V_{IN} = 5.0 V, DB11–DB15			100	µA
Logic Input Current	I_{INL}	V_{IN} = 0 V, DB0–DB15			1	µA
Input Capacitance	C_{IN}			8		pF
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	V_{CC} = 4.5 V to 5.5 V, V_{EE} = –13 V to –17 V			20	ppm/V
Positive Supply Current	I_{CC}	All Bits HIGH		15	22	mA
Positive Supply Current	I_{CC}	All Bits LOW		6	7.5	mA
Negative Supply Current	I_{EE}			7.5	10	mA
Power Dissipation	P_{DISS}			188	260	mW

NOTES
[1]All supplies can be varied ±5% and operation is guaranteed. Device is tested with nominal supplies.
[2]Operation is guaranteed over this reference range, but linearity is neither tested not guaranteed (see Figures 7 and 8).
Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{CC} = +5.0 V, V_{EE} = –15.0 V, I_{REF} = 0.5 mA, C_{COMP} = 47 µF, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	DAC16G Limit	Units
Integral Nonlinearity	INL		±3	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Zero Scale Error	ZSE		±1	LSB max
Gain Error	GE		±0.12	% FS max
Logic Input High Voltage	V_{INH}		2.4	V min
Logic Input Low Voltage	V_{INL}		0.8	V max
Logic Input Current	I_{IN}		75	µA max
Positive Supply Current	I_{CC}		20	mA max
Negative Supply Current	I_{EE}		10	mA max
Power Dissipation	P_{DISS}		250	mW max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ANALOG DEVICES

12-Bit High Speed Multiplying D/A Converter

DAC312

FEATURES
Differential Nonlinearity: ±1/2 LSB
Nonlinearity: 0.05%
Fast Settling Time: 250 ns
High Compliance: –5 V to +10 V
Differential Outputs: 0 to 4 mA
Guaranteed Monotonicity: 12 Bits
Low Full-Scale Tempco: 10 ppm/°C
Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS
Low Power Consumption: 225 mW
Industry Standard AM6012 Pinout
Available In Die Form

GENERAL DESCRIPTION

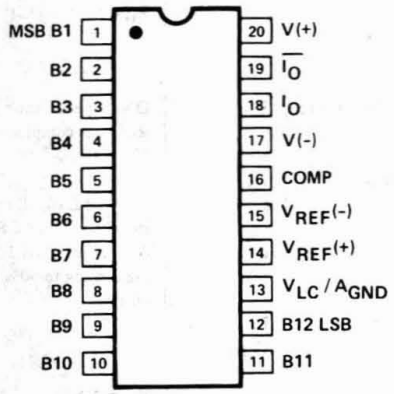
The DAC312 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

The DAC312 combines a 9-bit master D/A converter with a 3-bit (MSBs) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to ±1/2 LSB from the ideal), monotonicity to 12-bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of 1/2 LSB (0.012%) would be required.

The 250 ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

PIN CONNECTIONS

20-Pin Hermetic DIP (R-Suffix),
20-Pin Plastic DIP (P-Suffix),
20-Pin SOL (S-Suffix)

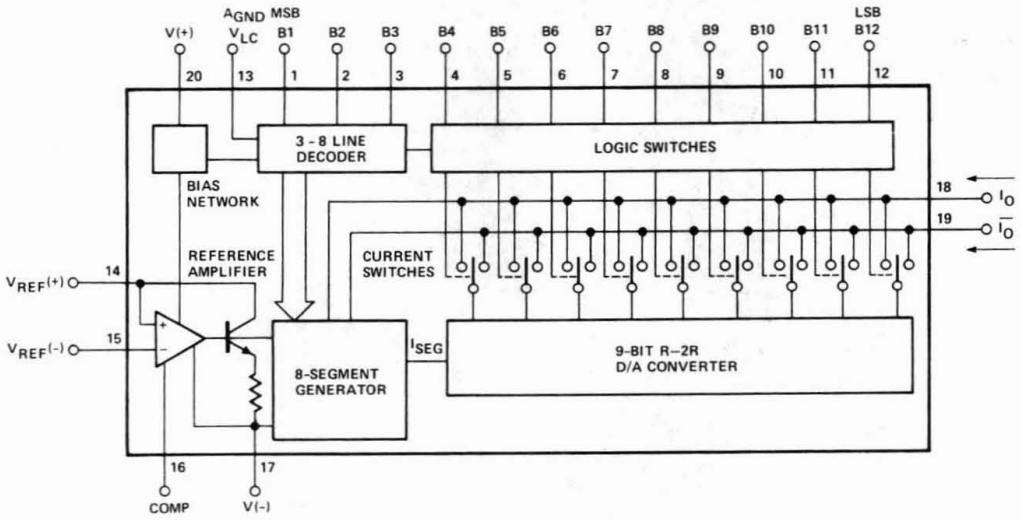


ORDERING GUIDE

Model	DNL	Temperature Range	Package Description	Package* Option
DAC312ER	±1/2	0°C to +70°C	Cerdip-20	Q-20
DAC312FR	±1	–40°C to +85°C	Cerdip-20	Q-20
DAC312BR/883	±1	–55°C to +125°C	Cerdip-20	Q-20
DAC312HP	±1	–40°C to +85°C	Plastic DIP-20	N-20
DAC312HS	±1	–40°C to +85°C	SOL-20	R-20

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

DAC312–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ $V_S = \pm 15$ V, $I_{REF} = 1.0$ mA, $0°C \le T_A \le +70°C$ for DAC312E and $-40°C \le T_A \le +85°C$ for DAC312F, DAC312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT}.)

Parameter	Symbol	Conditions	DAC312E			DAC312F			DAC312H			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution			12			12			12			Bits
Monotonicity			12			12			12			Bits
Differential Nonlinearity	DNL	Deviation from ideal			±0.0125			±0.0250			±0.0250	%FS
		step size[2]			±0.5			±1			±1	LSB
Nonlinearity	INL	Deviation from ideal straight line[1]			±0.05			±0.05			±0.05	%FS
Full-Scale Current	I_{FS}	$V_{REF} = 10$ V										
		$R_{14} = R_{15} = 10\ k\Omega$[2]	3.967	3.999	4.031	3.935	3.999	4.063	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}			±5	±20		±10	±40		±80		ppm/°C
				±0.005	±0.002		±0.001	±0.004		±0.008		%FS/°C
Output Voltage Compliance	V_{OC}	DNL Specification guaranteed over compliance range	−5		+10	−5		+10	−5		+10	V
Full-Scale Symmetry	I_{FSS}	$\lvert I_{FS}\rvert - \lvert I_{FS}\rvert$		±0.4	±1		±0.4	±2		±0.4	±2	µA
Zero-Scale Current	I_{ZS}				0.10			0.10			0.10	µA
Settling Time	t_S	To ±1/2 LSB, all bits switched ON or OFF[1]		250	500		250	500		250	500	ns
Propagation Delay–All Bits	t_{PLH}	All bits switched 50% point		25	50		25	50		25	50	ns
	t_{PHL}	logic swing to 50% point output[1]		25	50		25	50		25	50	ns
Output Resistance	R_O			>10			>10			>10		MΩ
Output Capacitance	C_{OUT}			20			20			20		pF
Logic Input												
Levels "0"	V_{IL}	V_{LC} = GND			0.8			0.8			0.8	V
Levels "1"	V_{IH}	V_{LC} = GND	2			2			2			V
Logic Input Current	I_{IN}	$V_{IN} = -5$ to +18 V			40			40			40	µA
Logic Input Swing	V_{IS}		−5		+18	−5		+18	−5		+18	V
Reference Bias Current	I_{15}		0	−0.5	−2	0	−0.5	−2	0	−0.5	−2	µA
Reference Input												
Slew Rate	dI/dt	$R_{14(eq)} = 800\ \Omega$, $C_C = 0$ pF[1]	4	8		4	8		4	8		mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	V+ = +13.5 V to +16.5 V, V− = −15 V		±0.0005	±0.001		±0.0005	±0.001		±0.0005	±0.001	%FS/%ΔV
	$PSSI_{FS-}$	V− = −13.5 V to −16.5 V, V+ = +15 V		±0.00025	±0.001		±0.00025	±0.001		±0.00025	±0.001	%FS/%ΔV
Power Supply Range	V+	$V_{OUT} = 0$ V	4.5		18	4.5		18	4.5		18	V
	V−	$V_{OUT} = 0$ V	−18		−10.8	−18		−10.8	−18		−10.8	V
Power Supply Current	I+	V+ = +5 V, V− = −15 V		3.3	7		3.3	7		3.3	7	mA
	I−	V+ = +15 V, V− = −15 V		−13.9	−18		−13.9	−18		−13 9	−18	mA
	I+	V+ = +5 V, V− = −15 V		3 9	7		3 9	7		3 9	7	mA
	I−	V+ = +15 V, V− = −15 V		−13.9	−18		−13.9	−18		−13.9	−18	mA
Power Dissipation	P_d	V+ = +5 V, V− = −15 V		225	305		225	305		225	305	mW
		V+ = +15 V, V− = −15 V		267	375		267	375		267	375	mW

NOTES
[1]Guaranteed by design.
[2]T_A= 25°C for DAC312H grade only.

Specifications subject to change without notice.

12-Bit Serial Input Multiplying CMOS D/A Converter

DAC8043

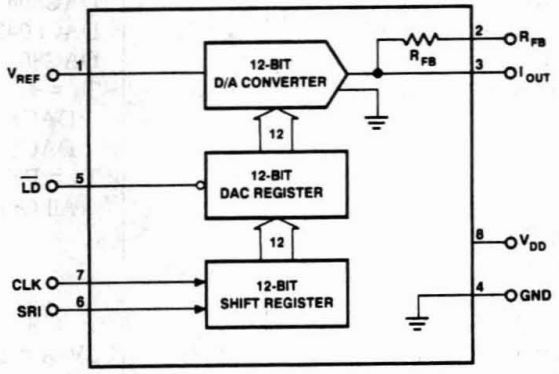
FEATURES

- 12-Bit Accuracy in an 8-Pin Mini-DIP
- Fast Serial Data Input
- Double Data Buffers
- Low ±1/2 LSB Max INL and DNL
- Max Gain Error: ±1 LSB
- Low 5 ppm/°C Max Tempco
- ESD Resistant
- Low Cost
- Available in Die Form

APPLICATIONS

- Autocalibration Systems
- Process Control and Industrial Automation
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Filters

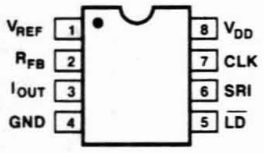
FUNCTIONAL BLOCK DIAGRAM



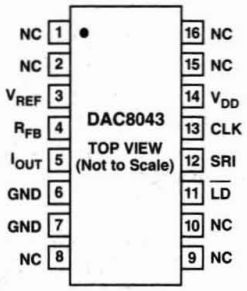
6

PIN CONNECTIONS

8-Pin Epoxy DIP
(P-Suffix)
8-Pin Cerdip
(Z-Suffix)



16-Lead Wide-Body SOL
(S-Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The DAC8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-pin mini-DIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC8043 is ideal for applications where PC board space is at a premium. Also, improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043's fast interface timing may reduce timing design considerations while minimizing microprocessor wait states. For applications requiring an asynchronous CLEAR function or more versatile microprocessor interface logic, refer to the PM7543.

Operating from a single +5 V power supply, the DAC8043 is the ideal low power, small size, high performance solution to many application problems. It is available in plastic and cerdip packages that are compatible with auto-insertion equipment.

DAC8043–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5 V; V_{REF} = +10 V; I_{OUT} = GND = 0 V; T_A = Full Temperature Range specified under Absolute Maximum Ratings unless otherwise noted)

Parameter	Symbol	Conditions	DAC8043 Min	DAC8043 Typ	DAC8043 Max	Units
STATIC ACCURACY						
Resolution	N		12			Bits
Nonlinearity	INL	DAC8043A/E/G			±1/2	LSB
(Note 1)		DAC8043F			1	LSB
Differential Nonlinearity	DNL	DAC8043A/E			±1/2	LSB
(Note 2)		DAC8043F/G			±1	LSB
Gain Error	G_{FSE}	T_A = +25°C				
(Note 3)		DAC8043A/E			1	LSB
		DAC8043F/G			2	LSB
		T_A = Full Temperature Range				
		All Grades			2	LSB
Gain Tempco						
(Δ Gain/Δ Temp)	TC_{GFS}				±5	ppm/°C
(Note 5)						
Power Supply						
Rejection Ratio	PSRR	ΔV_{DD} = ±5%		±0.0006	±0.002	%/%
(Δ Gain/Δ V_{DD})						
Output Leakage Current	I_{LKG}	T_A = +25°C			±5	nA
(Note 4)		T_A = Full Temperature Range				
		DAC8043A			±100	nA
		DAC8043E/F/G			±25	nA
Zero Scale Error	I_{ZSE}	T_A = +25°C			0.03	LSB
(Notes 7, 12)		T_A = Full Temperature Range				
		DAC8043A			0.61	LSB
		DAC8043E/F/G			0.15	LSB
Input Resistance						
(Note 8)	R_{IN}		7	11	15	kΩ
AC PERFORMANCE						
Output Current						
Settling Time	t_S	T_A = +25°C		0.25	1	µs
(Notes 5, 6)						

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... +17 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
Digital Input Voltage Range ..... –0.3 V to V_{DD}
Output Voltage (Pin 3) ..... –0.3 V to V_{DD}
Operating Temperature Range
AZ Versions ..... –55°C to +125°C
EZ/FZ/FP Versions ..... –40°C to +85°C
GP Version ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W

*θ_{JA} is specified for worst case mounting conditions, i. e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages.

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2).
2. The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ORDERING GUIDE

Model	Relative Accuracy	Temperature Range	Package Option*
DAC8043AZ	±1/2 LSB	–55°C to +125°C	8-Pin Cerdip
DAC8043AZ/883	±1/2 LSB	–55°C to +125°C	8-Pin Cerdip
DAC8043EZ	±1/2 LSB	–40°C to +125°C	8-Pin Cerdip
DAC8043FS	±1 LSB	–40°C to +85°C	16-Lead (Wide) SOL
DAC8043FZ	±1 LSB	–40°C to +85°C	8-Pin Cerdip
DAC8043FP	±1 LSB	–40°C to +85°C	8-Pin Epoxy DIP
DAC8043GP	±1/2 LSB	0°C to +70°C	8-Pin Epoxy DIP
DAC8043HP	±1 LSB	0°C to +70°C	8-Pin Epoxy DIP

*For outline information see Package Information section.

ANALOG DEVICES

12-Bit Serial Daisy-Chain CMOS D/A Converter

DAC8143

FEATURES

Fast, Flexible, Microprocessor Interfacing in Serially Controlled Systems
Buffered Digital Output-Pin for Daisy-Chaining Multiple DACs
Minimizes Address-Decoding in Multiple DAC Systems—Three Wire Interface for Any Number of DACs
- One Data Line
- One CLK Line
- One Load Line

Improved Resistance to ESD
–40°C to +85°C for the Extended Industrial Temperature Range
Available in Die Form

APPLICATIONS

Multiple-Channel Data Acquisition Systems
Process Control and Industrial Automation
Test Equipment
Remote Microprocessor-Controlled Systems

GENERAL INFORMATION

The DAC8143 is a 12-bit serial-input daisy-chain CMOS D/A converter, which features serial data input and buffered serial data output. It was designed for multiple serial DAC systems, where serially daisy-chaining one DAC after another is greatly simplified.

The DAC8143 also minimizes address decoding lines enabling simpler logic interfacing. It allows 3-wire interface for any number of DACs: one data line, one CLK line, and one load line.

Serial data in the input register (MSB first) is sequentially clocked out to the SRO pin as the new data word (MSB first) is simultaneously clocked in from the SRI pin. The strobe inputs are used to clock in/out data on the rising or falling (user selected) strobe edges (STB_1, STB_2, $\overline{STB_3}$, STB_4).

When the shift register's data has been updated, the new data word is transferred to the DAC register with use of $\overline{LD_1}$ and $\overline{LD_2}$ inputs.

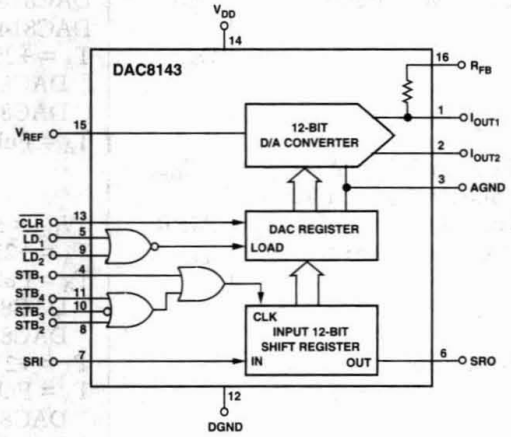
Separate LOAD control inputs allow simultaneous output updating of multiple DACs. An asynchronous CLEAR input resets the DAC register without altering data in the input register.

Improved linearity and gain error performance permits reduced circuit parts count through the elimination of trimming components. Also, fast interface timing reduces timing design consideration while minimizing microprocessor wait states.

The DAC8143 is available in standard cerdip and plastic packages that are compatible with auto-insertion equipment.

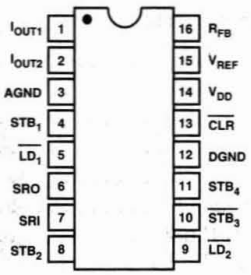
Cerdip and plastic packages devices come in the extended industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

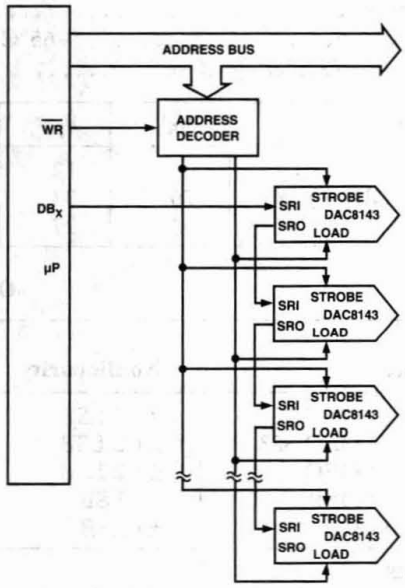


PIN CONNECTIONS

16-Pin Epoxy DIP (P-Suffix), 16-Pin Cerdip (Q-Suffix)
16-Pin SOL (S-Suffix)



MULTIPLE DAC8143s WITH 3-WIRE INTERFACE



DAC8143–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} +5 V; V_{REF} = +10 V; V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0 V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		12			Bits
Nonlinearity	INL	DAC8143A/E			±1/2	
		DAC8143F			±1	LSB
Differential Nonlinearity	DNL	DAC8143A/E			±1/2	
		DAC8143F			±1	LSB
Gain Error	G_{FSE}	T_A = +25°C				
		DAC8143A/E			±1	
		DAC8143F			±2	LSB
		T_A = Full Temperature Range (All Grades)			±2	
Gain Tempco (ΔGain/ΔTemp)	TC_{GFS}				±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%		±0.0006	±0.002	%/%
Output Leakage Current	I_{LKG}	T_A = +25°C			±5	
		T_A = Full Temperature Range				
		DAC8143A			±100	nA
		DAC8143E/F			±25	
Zero Scale Error	I_{ZSE}	T_A = +25°C		±0.002	±0.03	
		T_A = Full Temperature Range				
		DAC8143A		±0.05	±0.61	LSB
		DAC8143E/F		±0.01	±0.15	
Input Resistance	R_{IN}	V_{REF} Pin	7	11	15	kΩ

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... +17 V
V_{REF} to DGND ..... ±25 V
V_{RFB} to DGND ..... ±25 V
AGND to DGND ..... V_{DD} + 0.3 V
DGND to AGND ..... V_{DD} + 0.3 V
Digital Input Voltage Range ..... –0.3 V to V_{DD}
Output Voltage (Pin 1, Pin 2) ..... –0.3 V to V_{DD}
Operating Temperature Range
AQ Version ..... –55°C to +125°C
EQ/FP/FS Versions ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions. i.e., θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package

CAUTION

1. Do not apply voltage higher than V_{DD} or less than DGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ORDERING INFORMATION[1]

Model	Nonlinearity	Gain Error	Temperature Range	Package Description
DAC8143AQ	±1/2 LSB	±1 LSB	–55°C to +125°C	16-Pin Cerdip
DAC8143AQ/883[2]	±1/2 LSB	±1 LSB	–55°C to +125°C	16-Pin Cerdip
DAC8143EQ	±1/2 LSB	±1 LSB	–40°C to +85°C	16-Pin Cerdip
DAC8143FP	±1 LSB	±2 LSB	–40°C to +85°C	16-Pin Plastic DIP
DAC8143FS[3]	±1 LSB	±2 LSB	–40°C to +85°C	16-Lead SOL

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in Cerdip and plastic DIP. For outline information see Package Information section.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

Dual 12-Bit Double-Buffered Multiplying CMOS D/A Converter

DAC8222

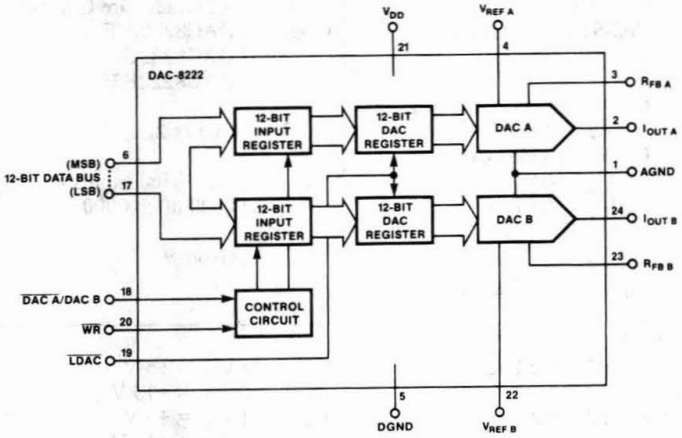
FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- Double-Buffered Digital Inputs
- 12-Bit Endpoint Linearity (±1/2 LSB) Over Temperature
- +5 V to +15 V Single Supply Operation
- DACs Matched to 1% Max
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL Package
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Robotics/Process Control/Automation
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

FUNCTIONAL DIAGRAM



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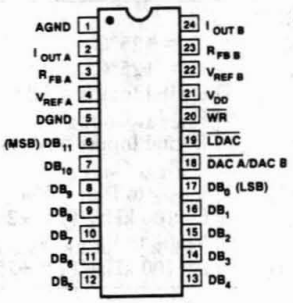
GENERAL DESCRIPTION

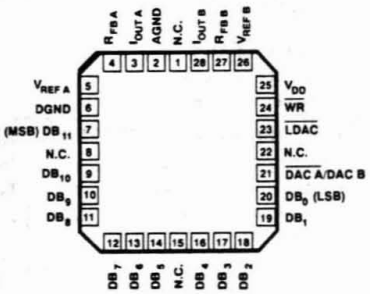
The DAC8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See PMI's DAC8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC8222 to be packaged in a narrow 24-pin 0.3" DIP and save PCB space.

PIN CONNECTIONS

24-Pin 0.3" Cerdip (W Suffix)
24-Pin Epoxy DIP (P Suffix)
24-Pin SOL (S Suffix)



28-Contact LCC (TC Suffix)



NC = NO CONNECT

ORDERING GUIDE

Model	INL (LSB)	GFSE (LSB)	Temperature Range	Package Description	Package Option[1]
DAC8222EW	±1/2	±1	–40°C to +85°C	Cerdip-24	Q-24
DAC8222GP	±1/2	±2	0°C to +70°C	P-DIP-24	N-24
DAC8222BTC/883[2]	±1	±4	–55°C to +125°C	LCC-28	E-28
DAC8222FW	±1	±4	–40°C to +85°C	Cerdip-24	Q-24
DAC8222FP	±1	±4	–40°C to +85°C	P-DIP-24	N-24
DAC8222FS	±1	±4	–40°C to +85°C	P-DIP-24	N-24

NOTES
[1]For outline information see Package Information section.
[2]Consult factory for DAC8222/883 MIL-STD data sheet.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

DAC8222–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V or +15 V, $V_{REF\,A}$ = $V_{REF\,B}$ = +10 V, $V_{OUT\,A}$ = $V_{OUT\,B}$ = 0 V; AGND = DGND = 0 V; T_A = Full Temperature Range Specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
STATIC ACCURACY							
Resolution	N			12			Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC8222A/E/G			±1/2	LSB
			DAC8222F/H			±1	LSB
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic				±1	LSB
Full-Scale Gain Error[1]	G_{FSE}	DAC8222A/E				±1	LSB
		DAC8222G				±2	LSB
		DAC8222F/H				±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)			±2	±5	ppm/°C
Output Leakage Current $I_{OUT\,A}$ (Pin 2), $I_{OUT\,B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C		±5	±10	nA
			T_A = Full Temp. Range			±50	nA
Input Resistance ($V_{REF\,A}$, $V_{REF\,B}$)	R_{REF}	(Note 9)		8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$				±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5 V		2.4			V
		V_{DD} = +15 V		13.5			V
Digital Input Low	V_{INL}	V_{DD} = +5 V				0.8	V
		V_{DD} = +15 V				1.5	V
Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}	T_A = +25°C		±0.001	±1	μA
		and V_{INL} or V_{INH}	T_A = Full Temp. Range			±10	μA
Input Capacitance[2]	C_{IN}	DB0–DB11				10	pF
		$\overline{WR}$, $\overline{LDAC}$, $\overline{DAC\ A/DAC\ B}$				15	pF
POWER SUPPLY							
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}				2	mA
		All Digital Inputs 0 V or V_{DD}			10	100	μA
DC Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%				0.002	%/%
AC PERFORMANCE CHARACTERISTICS[2]							
Propagation Delay[4, 5]	t_{PD}	T_A = +25°C				350	ns
Current Settling Time[5, 6]	t_S	T_A = +25°C				1	μs
Output Capacitance	C_O	Digital Inputs = All 0s				90	pF
		$C_{OUT\,A}$, $C_{OUT\,B}$				90	pF
		Digital Inputs = All 1s				120	pF
		$C_{OUT\,A}$, $C_{OUT\,B}$				120	pF
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = 20 V p-p;				–70	dB
		f = 100 kHz; T_A = +25°C				–70	dB
		$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = 20 V p-p;				–70	dB
	FT_B	f = 100 kHz; T_A = +25°C				–70	dB

SWITCHING CHARACTERISTICS[2, 3]		V_{DD} = +5 V			V_{DD} = +15 V	
		+25°C	–40°C to +85°C[8]	–55°C to +125°C	All Temps[10]	
DAC Select to Write Set-Up Time	t_{AS}	150	180	210	60	ns min
DAC Select to Write Hold Time	t_{AH}	0	0	0	0	ns min
LDAC to Write Set-Up Time	t_{LS}	80	100	120	60	ns min
LDAC to Write Hold Time	t_{LH}	20	20	20	20	ns min
Data Valid to Write Set-Up Time	t_{DS}	220	240	260	100	ns min
Data Valid to Write Hold Time	t_{DH}	0	0	0	10	ns min
Write Pulse Width	t_{WR}	130	160	170	90	ns min
LDAC Pulse Width	t_{LWD}	100	120	130	60	ns min

NOTES

[1]Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.

[2]Guaranteed and not tested.

[3]See timing diagram.

[4]From 50% of digital input to 90% of final analog output current. $V_{REF\,A}$ = $V_{REF\,B}$ = +10 V; OUT A, OUT B load = 100 Ω, C_{EXT} = 13 pF.

[5]$\overline{WR}$, $\overline{LDAC}$ = 0 V; DB0–DB11 = 0 V to V_{DD} or V_{DD} to 0 V.

[6]Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.

[7]Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.

[8]These limits apply for the commercial and industrial grade products.

[9]Absolute temperature coefficient is approximately +50 ppm/°C.

[10]These limits also apply as typical values for V_{DD} = +12 V with +5 V CMOS logic levels and T_A = +25°C.

Specifications subject to change without notice.

Dual 12-Bit (8-Bit Byte) Double Buffered CMOS D/A Converter

DAC8248

FEATURES

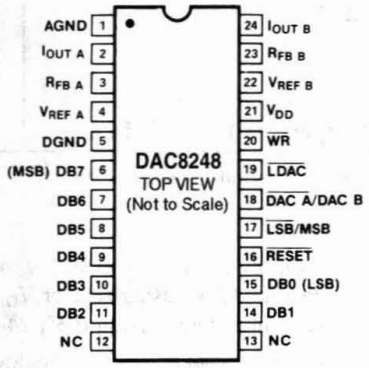
- Two Matched 12-Bit DACs on One Chip
- 12-Bit Resolution with an 8-Bit Data Bus
- Direct Interface with 8-Bit Microprocessors
- Double-Buffered Digital Inputs
- $\overline{\text{RESET}}$ to Zero Pin
- 12-Bit Endpont Linearity (±1/2 LSB) Over Temperature
- +5 V to +15 V Single Supply Operation
- Latch-Up Resistant
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL Package
- Available in Die Form

APPLICATIONS

- Multichannel Microprocessor-Controlled Systems
- Robotics/Process Control/Automation
- Automatic Test Equipment
- Programmable Attenuator, Power Supplies, Window Comparators
- Instrumentation Equipment
- Battery Operated Equipment

PIN CONNECTIONS

24-Pin 0.3" Cerdip (W Suffix), 24-Pin Epoxy DIP (P Suffix), 24-Pin SOL (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

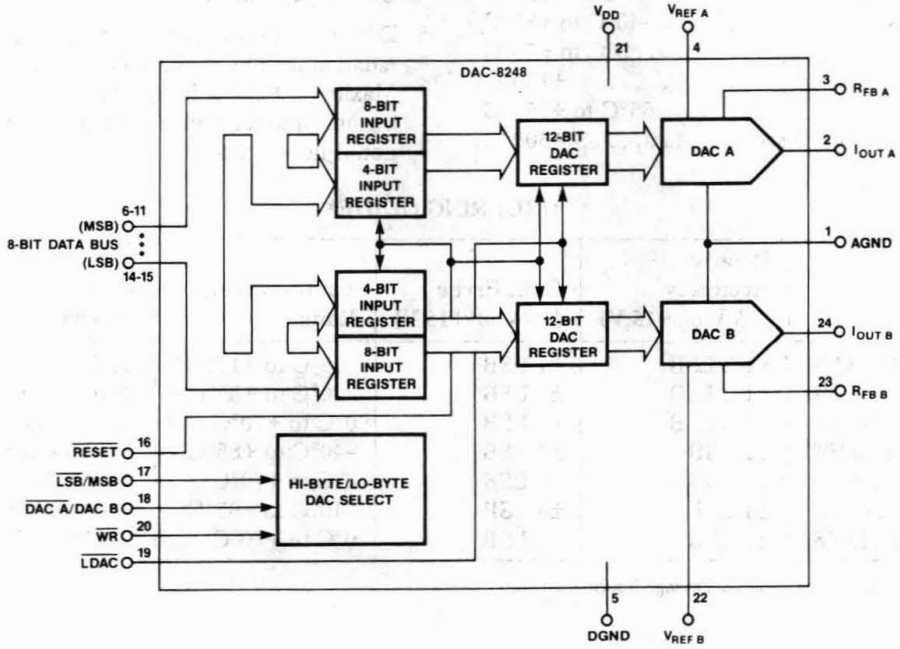
The DAC8248 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has an 8-bit wide input data port that interfaces directly with 8-bit microprocessors. It loads a 12-bit word in two bytes using a single control; it can accept either a least significant byte or most significant byte first. For designs with a 12-bit or 16-bit wide data path, choose the DAC8222 or DAC8221.

The DAC8248's double-buffered digital inputs allow both DAC's analog output to be updated simultaneously. This is particularly useful in multiple DAC systems where a common $\overline{\text{LDAC}}$ signal updates all DACs at the same time. A single $\overline{\text{RESET}}$ pin resets both outputs to zero.

The DAC8248's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC consists of two thin-film R-2R resistor ladder networks, two 12-bit, two 8-bit, and two 4-bit data registers, and control logic circuitry. Separate reference input and feedback resistors are provided for each DAC. The DAC8248

(continued on next page)

FUNCTIONAL BLOCK DIAGRAM



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DAC8248–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5 V or +15 V; $V_{REF\,A}$ = $V_{REF\,B}$ = +10 V; V_{OUTA} = $V_{OUT\,B}$ = 0 V; AGND = DGND = 0 V; T_A = Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.)

Parameter	Symbol	Conditions	DAC8248 Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		12			Bits
Relative Accuracy	INL	DAC8248A/E/G			±1/2	LSB
		DAC8248F/H			±1	LSB
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic			±1	LSB
Full Scale Gain Error[1]	G_{FSE}	DAC8248A/E			±1	LSB
		DAC8248G			±2	LSB
		DAC8248F/H			±4	LSB
Gain Temperature Coefficient (ΔGain/ΔTemperature)	TCG_{FS}	(Notes 2, 6)		±2	±5	ppm/°C

Specifications subject to change without notice.

(continued)

operates on a single supply from +5 V to +15 V, and it dissipates less than 0.5 mW at +5 V (using zero or V_{DD} logic levels). The device is packaged in a space-saving 0.3", 24-pin DIP.

The DAC8248 is manufactured with PMI's highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND ..... 0 V, +17 V
V_{DD} to DGND ..... 0 V, +17 V
AGND to DGND ..... –0.3 V, V_{DD} +0.3 V
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} +0.3 V
$I_{OUT\,A}$, $I_{OUT\,B}$ to AGND ..... –0.3 V, V_{DD} +0.3 V
$V_{REF\,A}$, $V_{REF\,B}$ to AGND ..... ±25 V
$V_{RFB\,A}$, $V_{RFB\,B}$ to AGND ..... ±25 V
Operating Temperature Range
AW Version ..... –55°C to +125°C
EW, FW, FP Versions ..... –40°C to +85°C
GP, HP, HS Versions ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
24-Pin Hermetic DIP (W)	69	10	°C/W
24-Pin Plastic DIP (P)	62	32	°C/W
24-Pin SOL (S)	72	24	°C/W

NOTE
[1]θ_{JA} specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods. This is a stress rating only and functional operation at or above this specification is not implied.

ORDERING GUIDE*

Model	Relative Accuracy (+5 V or +15 V)	Gain Error (+5 V or +15 V)	Temperature Range	Package Description
DAC8248AW	±1/2 LSB	±1 LSB	–55°C to +125°C	24-Pin Cerdip
DAC8248EW	±1/2 LSB	±1 LSB	–40°C to +85°C	24-Pin Cerdip
DAC8248GP	±1/2 LSB	±2 LSB	0°C to +70°C	24-Pin Plastic DIP
DAC8248FW	±1 LSB	±4 LSB	–40°C to +85°C	24-Pin Cerdip
DAC8248HP	±1 LSB	±4 LSB	0°C to +70°C	24-Pin Plastic DIP
DAC8248FP	±1 LSB	±4 LSB	–40°C to +85°C	24-Pin Plastic DIP
DAC8248HS	±1 LSB	±4 LSB	0°C to +70°C	24-Pin SOL

*For outline information see Package Information section.

Quad 8-Bit Multiplying CMOS D/A Converter with Memory

DAC8408

FEATURES

- Four DACs in a 28 Pin, 0.6 Inch Wide DIP or 28 Pin JEDEC Plastic Chip Carrier
- ±1/4 LSB Endpoint Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (with Memory)
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single-Supply Operation (+5 V)
- Low Power Consumption
- Latch-Up Resistant
- Available In Die Form

APPLICATIONS

- Voltage Set Points in Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multichannel Microprocessor-Controlled Systems
- Digitally Controlled Op Amp Offset Adjustment
- Process Control
- Digital Attenuators

GENERAL DESCRIPTION

The DAC8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and on-board data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines $\overline{DS1}$, $\overline{DS2}$, and A/$\overline{B}$ determine which DAC will accept data. Data loading is similar to that of a RAMs write cycle. Data can be read back onto the same data bus with control line R/$\overline{W}$. The DAC8408 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The DAC8408 operates on a single +5 volt supply and dissipates less than 20 mW. The DAC8408 is manufactured using PMI's highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ORDERING INFORMATION[1]

Model	INL	DNL	Temperature Range	Package Description
DAC8408GP	±1/4 LSB	±1/2 LSB	0°C to +70°C	28-Pin Plastic DIP
DAC8408ET	±1/4 LSB	±1/2 LSB	–40°C to +85°C	28-Pin Cerdip
DAC8408AT[2]	±1/4 LSB	±1/2 LSB	–55°C to +125°C	28-Pin Cerdip
DAC8408FT	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Pin Cerdip
DAC8408BT[2]	±1/2 LSB	±1 LSB	–55°C to +125°C	28-Pin Cerdip
DAC8408FPC[3]	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Contact PLCC
DAC8408FS	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Pin SOL
DAC8408FP	±1/2 LSB	±1 LSB	–40°C to +85°C	28-Pin Plastic DIP

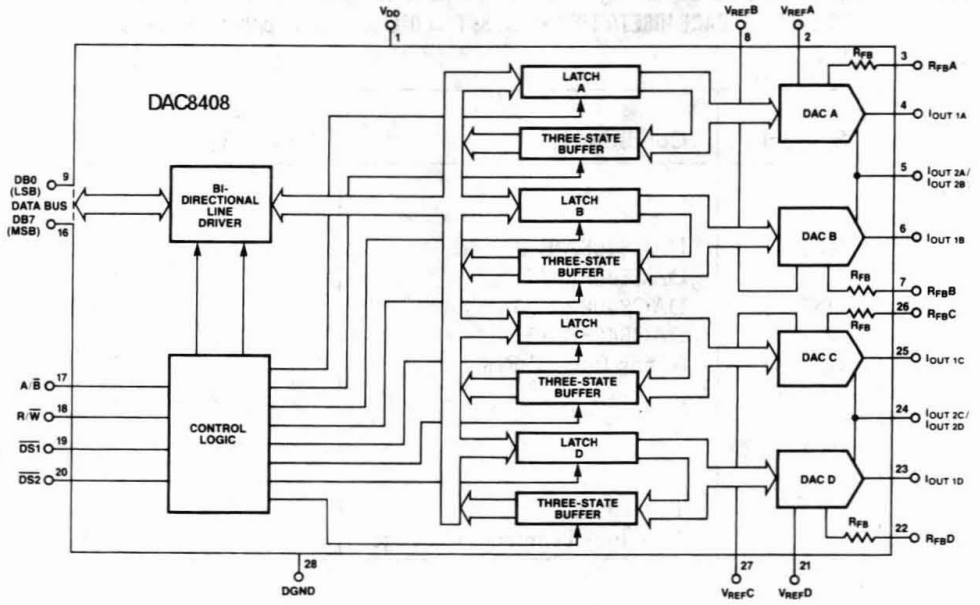
NOTES

[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages. For outline information see Package Information section.

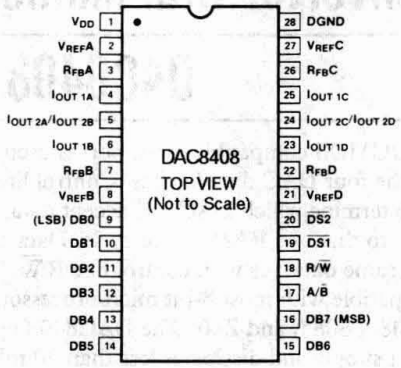
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL BLOCK DIAGRAM



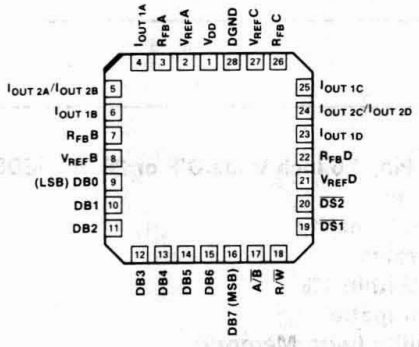
PIN CONNECTIONS



28-PIN HERMETIC DIP (T Suffix)

28-PIN EPOXY DIP (P Suffix)

28-PIN SOL (S Suffix)



28-PIN PLASTIC LEADED CHIP CARRIER (PC Suffix)

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to $I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ . . . . . 0 V, +7 V
V_{DD} to DGND . . . . . 0 V, +7 V
$I_{OUT\ 1A}$, $I_{OUT\ 1B}$,
$I_{OUT\ 1C}$, $I_{OUT\ 1D}$ to DGND . . . . . −0.3 V to V_{DD} +0.3 V
$R_{FB}A$, $R_{FB}B$, $R_{FB}C$, $R_{FB}D$ to I_{OUT} . . . . . ±25 V
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$,
$I_{OUT\ 2C}$, $I_{OUT\ 2D}$ to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
DB0 through DB7 to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
Control Logic
Input Voltage to DGND . . . . . −0.3 V + V_{DD} + 0.3 V
$V_{REF}A$, $V_{REF}B$, $V_{REF}C$, $V_{REF}D$ to
$I_{OUT\ 2A}$, $I_{OUT\ 2B}$, $I_{OUT\ 2C}$, $I_{OUT\ 2D}$ . . . . . ±25 V
Operating Temperature Range
Commercial Grade (GP) . . . . . 0°C to +70°C
Industrial Grade (ET, FT, FP, FPC, FS) . −40°C to +85°C
Military Grade (AT, BT) . . . . . −55°C to +125°C
Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
28-Pin Hermetic DIP (T)	55	10	°C/W
28-Pin Plastic DIP (P)	53	27	°C/W
28-Pin SOL (S)	68	23	°C/W
28-Contact PLCC (PC)	66	29	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION

1. Do not apply voltages higher than V_{DD} +0.3 V or less than −0.3 V potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high energy electrostatic fields. Keep in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V; V_{REF} = ±10 V; V_{OUT}A, B, C, D = 0 V; T_A = −55°C to +125°C apply for DAC8408AT/BT, T_A = −40°C to +85°C apply for DAC8408ET/FT/FP/FPC/FS; T_A = 0°C to +70°C apply for DAC8408GP, unless otherwise noted. Specifications apply for DAC A, B, C, & D.)

Parameter	Symbol	Conditions	DAC8408 Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		8			Bits
Nonlinearity	INL	DAC8408A/E/G			±1/4	LSB
		DAC8408B/F/H			±1/2	
Differential Nonlinearity	DNL	DAC8408A/E/G			±1/2	LSB
		DAC8408B/F/H			±1	
Gain Error	G_{FSE}	(Using Internal R_{FB})			±1	LSB
Gain Tempco	TC_{GFS}			±2	±40	ppm/°C
Power Supply Rejection (ΔV_{DD} = ±10%)	PSR				0.001	%FSR/%
$I_{OUT\ 1A, B, C, D}$ Leakage Current	I_{LKG}	T_A =+25°C			±30	nA
		T_A = Full Temperature Range			±100	

Specifications subject to change without notice.

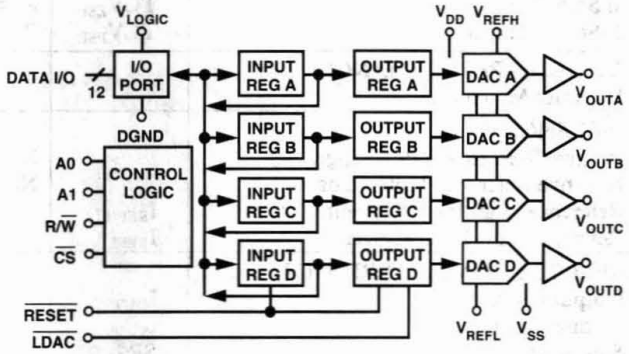
Quad, 12-Bit DACs Voltage Output with Readback

DAC8412/DAC8413

FEATURES
- +5 to ±15 Volt Operation
- Unipolar or Bipolar Operation
- True Voltage Output
- Double-Buffered Inputs
- Reset to Min or Center Scale
- Fast Bus Access Time
- Readback

APPLICATIONS
- Automatic Test Equipment
- Digitally Controlled Calibration
- Servo Controls
- Process Control Equipment

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

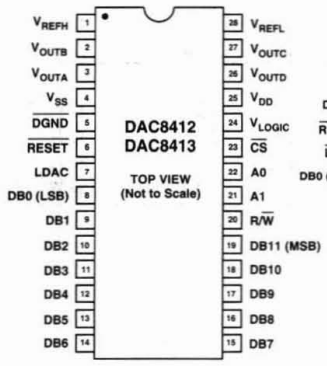
The DAC8412 and DAC8413 are quad, 12-bit voltage output DACs with readback capability. Built using a complementary BiCMOS process, these monolithic DACs offer the user very high package density.

Output voltage swing is set by the two reference inputs V_{REFH} and V_{REFL}. By setting the V_{REFL} input to 0 volts and V_{REFH} to a positive voltage, the DAC will provide a unipolar positive output range. A similar configuration with V_{REFH} at 0 volts and V_{REFL} at a negative voltage will provide a unipolar negative output range. Bipolar outputs are configured by connecting both V_{REFH} and V_{REFL} to nonzero voltages. This method of setting output voltage range has advantages over other bipolar offsetting methods because it is not dependent on internal and external resistors with different temperature coefficients.

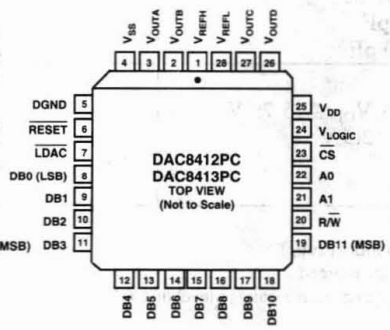
Digital controls allow the user to load or read back data from any DAC, load any DAC and transfer data to all DACs at one time.

An active low $\overline{RESET}$ loads all DAC output registers to midscale for the DAC8412 and zero scale for the DAC8413.

DIP



PLCC



The DAC8412/DAC8413 are available in 28-pin plastic DIP, cerdip, PLCC and LCC packages. They can be operated from a wide variety of supply and reference voltages with supplies ranging from single +5 volt to ±15 volts, and references from +2.5 to ±10 volts. Power dissipation is less than 330 mW with ±15 volt supplies and only 60 mW with a +5 volt supply.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8412/DAC8413/883 data sheet which specifies operation over the –55°C to +125°C temperature range. All 883 parts are also available on Standard Military Drawings 5962-91-76401MXA through -76404M3A.

ORDERING INFORMATION[1]

INL (LSB)	Military[2] Temperature –55°C to +125°C	Extended Industrial[2] Temperature –40°C to +85°C	Package	Package Option[3]
±1		DAC8412FPC	PLCC	P-28A
±1.5	DAC8412BTC/883		LCC	E-28A
±0.5		DAC8412ET	Cerdip	Q-28
±0.75	DAC8412AT/883		Cerdip	Q-28
±1		DAC8412FT	Cerdip	Q-28
±1.5	DAC8412BT/883		Cerdip	Q-28
±0.5		DAC8412EP	Plastic	N-28
±1		DAC8412FP	Plastic	N-28
±1		DAC8412GBC	Dice	
±1		DAC8413FPC	PLCC	P-28A
±1.5	DAC8413BTC/883		LCC	E-28A
±0.5		DAC8413ET	Cerdip	Q-28
±0.75	DAC8413AT/883		Cerdip	Q-28
±1		DAC8413FT	Cerdip	Q-28
±1.5	DAC8413BT/883		Cerdip	Q-28
±0.5		DAC8413EP	Plastic	N-28
±1		DAC8413FP	Plastic	N-28
±1		DAC8413GBC	Dice	

NOTES
[1]Burn-in is available on extended industrial temperature range parts in cerdip.
[2]A complete /883 data sheet is available. For availability and burn-in information, contact your local sales office.
[3]For outline information see Package Information section.

DAC8412/DAC8413–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +15.0 V, V_{SS} = –15.0 V, V_{LOGIC} = +5.0 V, V_{REFH} = +10.0 V, V_{REFL} = –10.0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted. See Note 1 for supply variations.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Integral Linearity "E"	INL			0.25	±0.5	LSB
Integral Linearity "F"	INL				±1	LSB
Differential Linearity	DNL	Monotonic Over Temperature	–1			LSB
Min Scale Error	V_{ZSE}	R_L = 2 kΩ			±2	LSB
Full-Scale Error	V_{FSE}	R_L = 2 kΩ			±2	LSB
Min Scale Tempco	TCV_{ZSE}	R_L = 2 kΩ		15		ppm/°C
Full-Scale Tempco	TCV_{FSE}	R_L = 2 kΩ		20		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range		Note 2	V_{REFL} + 2.5		V_{DD} – 2.5	V
Negative Reference Input Range		Note 2	–10		V_{REFH} – 2.5	V
Reference High Input Current	I_{REFH}		–2.75	+1.5	+2.75	mA
Reference Low Input Current	I_{REFL}		0	+2	+2.75	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		–5		+5	mA
Settling Time	t_S	to 0.01%		6		µs
Slew Rate	SR	10% to 90%		2.2		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}	T_A = +25°C	2.4			V
Logic Input Low Voltage	V_{INL}	T_A = +25°C			0.8	V
Logic Output High Voltage	V_{OH}	I_{OH} = +0.4 mA	2.4			V
Logic Output Low Voltage	V_{OL}	I_{OL} = –1.6 mA			0.4	V
Logic Input Current	I_{IN}				1	µA
Input Capacitance	C_{IN}			8		pF
Crosstalk				>72		dB
Large Signal Bandwidth		–3 dB, V_{REFH} = 0 to +10 V p-p		160		kHz
LOGIC TIMING CHARACTERISTICS		Note 3				
WRITE						
Chip Select Write Pulse Width	t_{WCS}		80	40		ns
Write Setup	t_{WS}	t_{WCS} = 80 ns	0			ns
Write Hold	t_{WH}	t_{WCS} = 80 ns	0			ns
Address Setup	t_{AS}		0			ns
Address Hold	t_{AH}		0			ns
Load Setup	t_{LS}		70	30		ns
Load Hold	t_{LH}		30	10		ns
Write Data Setup	t_{WDS}	t_{WCS} = 80 ns	20			ns
Write Data Hold	t_{WDH}	t_{WCS} = 80 ns	0			ns
Load Pulse Width	t_{LWD}		170	130		ns
Reset Pulse Width	t_{RESET}		140	100		ns
READ						
Chip Select Read Pulse Width	t_{RCS}		130	100		ns
Read Data Hold	t_{RDH}	t_{RCS} = 130 ns	0			ns
Read Data Setup	t_{RDS}	t_{RCS} = 130 ns	0			ns
Data to Hi Z	t_{DZ}	C_L = 10 pF		150		ns
Chip Select to Data	t_{CSD}	C_L = 100 pF		120	160	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	14.25 V ≤ V_{DD} ≤ 15.75 V			150	ppm/V
Positive Supply Current	I_{DD}	V_{REFH} = +2.5 V		8.5	12	mA
Negative Supply Current	I_{SS}		–10	–6.5		mA
Power Dissipation	P_{DISS}				330	mW

NOTES

[1]All supplies can be varied ±5%, and operation is guaranteed. Device is tested with nominal supplies.

[2]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[3]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

Quad 12-Bit Serial Voltage Output DAC

DAC8420

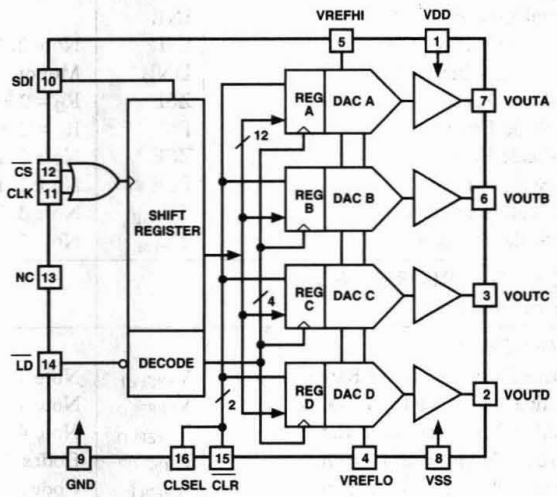
FEATURES

Guaranteed Monotonic Over Temperature
Excellent Matching Between DACs
Unipolar or Bipolar Operation
Buffered Voltage Outputs
High Speed Serial Digital Interface
Reset to Zero- or Center-Scale
Wide Supply Range, +5 V-Only to ±15 V
Low Power Consumption (35 mW max)
Available in 16-Pin DIP and SOL Packages

APPLICATIONS

Software Controlled Calibration
Servo Controls
Process Control and Automation
ATE

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

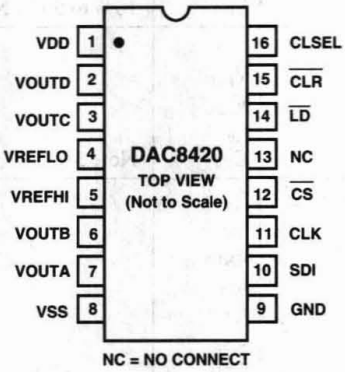
The DAC8420 is a quad, 12-bit voltage-output DAC with serial digital interface, in a 16-pin package. Utilizing BiCMOS technology, this monolithic device features unusually high circuit density and low power consumption. The simple, easy-to-use serial digital input and fully buffered analog voltage outputs require no external components to achieve specified performance.

The three-wire serial digital input is easily interfaced to microprocessors running at 10 MHz rates, with minimal additional circuitry. Each DAC is addressed individually by a 16-bit serial word consisting of a 12-bit data word and an address header. The user-programmable reset control $\overline{CLR}$ forces all four DAC outputs to either zero or midscale, asynchronously overriding the current DAC register values. The output voltage range, determined by the inputs VREFHI and VREFLO, is set by the user for positive or negative unipolar or bipolar signal swings within the supplies allowing considerable design flexibility.

The DAC8420 is available in 16-pin epoxy DIP, cerdip, and wide-body SOL (small-outline surface mount) packages. Operation is specified with supplies ranging from +5 V-only to ±15 V, with references of +2.5 V to ±10 V respectively. Power dissipation when operating from ±15 V supplies is less than 255 mW (max), and only 35 mW (max) with a +5 V supply.

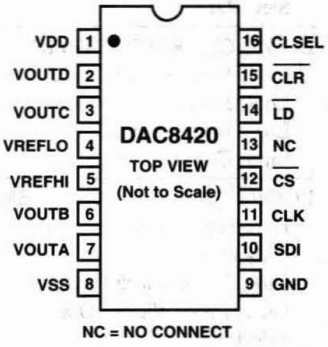
For applications requiring product meeting MIL-STD-883, contact your local sales office for the DAC8420/883 data sheet, which specifies operation over the –55°C to +125°C temperature range.

DIP



NC = NO CONNECT

SOL



NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	INL (±LSB)	Package Description	Package Option[2]
DAC8420EP	–40°C to +85°C	0.5	Plastic DIP	N-16
DAC8420EQ	–40°C to +85°C	0.5	Cerdip	Q-16
DAC8420ES	–40°C to +85°C	0.5	SOIC	SOL-16
DAC8420FP	–40°C to +85°C	1.0	Plastic DIP	N-16
DAC8420FQ	–40°C to +85°C	1.0	Cerdip	Q-16
DAC8420FS	–40°C to +85°C	1.0	SOIC	SOL-16
DAC8420GBC	–40°C to +85°C	1.0	Dice[3]	

NOTES
[1]A complete /883 data sheet is available. For availability and burn-in information, contact your local sales office.
[2]PMI division letter designator. For outline information see Package Information section.
[3]Dice tested at +25°C only.

DAC8420–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (at V_{DD} = +5.0 V ± 5%, V_{SS} = 0.0 V, V_{VREFHI} = +2.5 V, V_{VREFLO} = 0.0 V, and V_{SS} = –5.0 V ± 5%, V_{VREFLO} = –2.5 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted. See Note 1 for supply variations.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC ACCURACY						
Integral Linearity "E"	INL			±1/4	±1	LSB
Integral Linearity "E"	INL	Note 2, V_{SS} = 0 V		±1/2	±3	LSB
Integral Linearity "F"	INL			±3/4	±2	LSB
Integral Linearity "F"	INL	Note 2, V_{SS} = 0 V		±1	±4	LSB
Differential Linearity	DNL	Monotonic Over Temperature		±1/4	±1	LSB
Min-Scale Error	ZSE	R_L = 2 kΩ, V_{SS} = –5 V			±4	LSB
Full-Scale Error	FSE	R_L = 2 kΩ, V_{SS} = –5 V			±4	LSB
Min-Scale Error	ZSE	Note 2, R_L = 2 kΩ, V_{SS} = 0 V			±8	LSB
Full-Scale Error	FSE	Note 2, R_L = 2 kΩ, V_{SS} = 0 V			±8	LSB
Min-Scale Tempco	TC_{ZSE}	Note 3, R_L = 2 kΩ, V_{SS} = –5 V		±10		ppm/°C
Full-Scale Tempco	TC_{FSE}	Note 3, R_L = 2 kΩ, V_{SS} = –5 V		±10		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching				±1		LSB
REFERENCE						
Positive Reference Input Range	V_{VREFHI}	Note 4	V_{VREFLO} + 2.5		V_{DD} – 2.5	V
Negative Reference Input Range	V_{VREFLO}	Note 4	V_{SS}		V_{VREFHI} – 2.5	V
Negative Reference Input Range	V_{VREFLO}	Note 4, V_{SS} = 0 V	0		V_{VREFHI} – 2.5	V
Reference High Input Current	I_{VREFHI}	Codes 000_H, 555_H	–0.75	±0.25	+0.75	mA
Reference Low Input Current	I_{VREFLO}	Codes 000_H, 555_H, V_{SS} = –5 V	–1.0	–0.6		mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}	V_{SS} = –5 V	–1.25		+1.25	mA
Settling Time	t_S	to 0.01%, Note 5		8		µs
Slew Rate	SR	10% to 90%, Note 5		1.5		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}				10	µA
Input Capacitance	C_{IN}	Note 3		13		pF
LOGIC TIMING CHARACTERISTICS[3, 6]						
Data Setup Time	t_{DS}		25			ns
Data Hold	t_{DH}		55			ns
Clock Pulse Width HIGH	t_{CH}		90			ns
Clock Pulse Width LOW	t_{CL}		120			ns
Select Time	t_{CSS}		90			ns
Deselect Delay	t_{CSH}		5			ns
Load Disable Time	t_{LD1}		130			ns
Load Delay	t_{LD2}		35			ns
Load Pulse Width	t_{LDW}		80			ns
Clear Pulse Width	t_{CLRW}		150			ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSRR			0.002	0.01	%/%
Positive Supply Current	I_{DD}			4	7	mA
Negative Supply Current	I_{SS}		–6	–3		mA
Power Dissipation	P_{DISS}	V_{SS} = 0 V		20	35	mW

NOTES

[1]All supplies can be varied ±5% and operation is guaranteed. Device is tested with V_{DD} = +4.75 V.

[2]For single-supply operation (V_{VREFLO} = 0 V, V_{SS} = 0 V), due to internal offset errors INL and DNL are measured beginning at code 003_H.

[3]Guaranteed but not tested.

[4]Operation is guaranteed over this reference range, but linearity is neither tested nor guaranteed.

[5]V_{OUT} swing between +2.5 V and –2.5 V with V_{DD} = 5.0 V.

[6]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[7]Typical values indicate performance measured at +25°C.

Specifications subject to change without notice.

Quad 8-Bit Voltage Out CMOS DAC Complete with Internal 10 V Reference

DAC8426

FEATURES

No Adjustments Required, Total Error ±1 LSB Max Over Temperature
Four Voltage-Output DACs on a Single Chip
Internal 10 V Bandgap Reference
Operates from Single +15 V Supply
Fast 50 ns Data Load Time, All Temperatures
Pin-for-Pin Replacement for PM-7226 and AD7226, Eliminates External Reference

APPLICATIONS

Process Controls
Multichannel Microprocessor Controlled:
System Calibration
Op Amp Offset and Gain Adjust
Level and Threshold Setting

GENERAL DESCRIPTION

The DAC8426 is a complete quad voltage output D/A converter with internal reference. This product fits directly into any existing 7226 socket where the user currently has a 10 V external reference. The external reference is no longer necessary. The internal reference of the DAC8426 is laser-trimmed to ±0.4% offering a 25 ppm/°C temperature coefficient and 5 mA of external load driving capability.

The DAC8426 contains four 8-bit voltage-output CMOS D/A converters on a single chip. A 10 V output bandgap reference sets the output full-scale voltage. The circuit also includes four input latches and interface control logic.

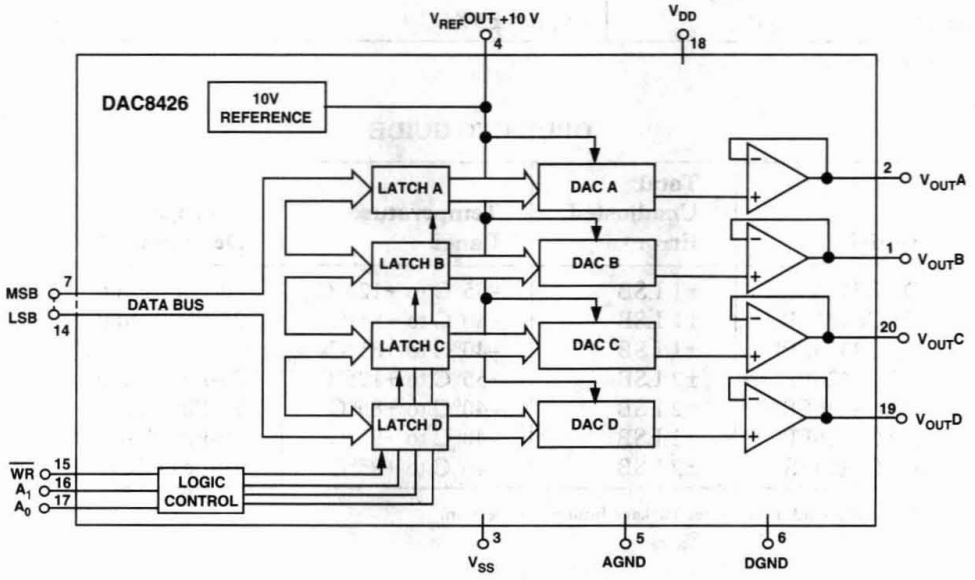
One of the four latches, selected by the address inputs, is loaded from the 8-bit data bus input when the write strobe is active low. All digital inputs are TTL/CMOS (5 V) compatible. The on-board amplifiers can drive up to 10 mA from either a single or dual supply. The on-board reference that is always connected to the internal DACs has 5 mA available to drive external devices.

Its compact size, low power, and economical cost-per-channel, make the DAC8426 attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. System reliability is also increased due to reduced parts count.

PMI's advanced oxide-based, silicon-gate, CMOS process allows the DAC8426's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

6

SIMPLIFIED SCHEMATIC



DAC8426–SPECIFICATIONS (V_{DD} = +15 V ± 10%, AGND = DGND = 0 V, V_{SS} = 0 V, T_A = –55°C to +125°C applies for DAC8426AR/BR, T_A = –40°C to +85°C applies for DAC8426ER/EP/FR/FP/FS, unless otherwise noted.)

Parameter	Symbol	Conditions		DAC8426 Min	Typ	Max	Units
STATIC PERFORMANCE							
Resolution	N			8			Bits
Total Unadjusted Error[1]	TUE	Includes Reference	A, E			±1	LSB
			B, F			±2	LSB
Relative Accuracy	INL		A, E			±1/2	LSB
			B, F			±1	LSB
Differential Nonlinearity[2]	DNL					±1	LSB
Full-Scale Temperature Coefficient	TCG_{FS}	Includes Reference			25		ppm/°C
Zero Scale Error	V_{ZSE}					20	mV
Zero Scale Error Temperature Coefficient	TCV_{ZS}	Dual Supply	V_{SS} = –5 V		10		µV/°C
REFERENCE OUTPUT							
Output Voltage	$V_{REF}OUT$	No Load	A, E	9.96		10.04	V
			B, F	9.92		10.08	V
Temperature Coefficient	$TCV_{REF}OUT$				20		ppm/°C
Load Regulation	LD_{REG}	ΔI_L = 5 mA			0.02	0.1	%/mA
Line Regulation	LN_{REG}	ΔV_{DD} ±10%			0.008	0.04	%/V
Output Noise[3]	e_n rms	f = 0.1 Hz to 10 Hz			3	10	µV p-p
Output Current	$I_{REF}OUT$	$\Delta V_{REF}OUT$ < 40 mV		5	7		mA
DIGITAL INPUTS							
Logic Input "0"	V_{INL}					0.8	V
Logic Input "1"	V_{INH}			2.4			V
Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}			0.1	10	µA
Input Capacitance[3]	C_{IN}				4	8	pF
POWER SUPPLIES							
Positive Supply Current[4]	I_{DD}				6	14	mA
Negative Supply Current[4]	I_{SS}	Dual Supply	V_{SS} = –5 V		4	10	mA
Power Dissipation[5]	P_{DISS}				90	210	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%			0.0002	0.01	%/%

Specifications subject to change without notice.

ORDERING GUIDE

Model	Total Unadjusted Error	Temperature Range	Package Description*
DAC8426AR	±1 LSB	–55°C to +125°C	20-Pin Cerdip
DAC8426ER	±1 LSB	–40°C to +85°C	20-Pin Cerdip
DAC8426EP	±1 LSB	–40°C to +85°C	20-Pin Plastic DIP
DAC8426BR	±2 LSB	–55°C to +125°C	20-Pin Cerdip
DAC8426FR	±2 LSB	–40°C to +85°C	20-Pin Cerdip
DAC8426FP	±2 LSB	–40°C to +85°C	20-Pin Plastic DIP
DAC8426FS	±2 LSB	–40°C to +85°C	20-Lead SOL

*For outline information see Package Information section.

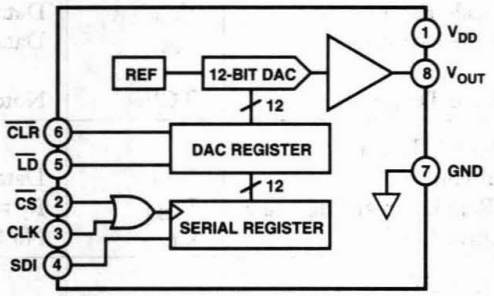
+5 V, Serial Input Complete 12-Bit DAC

DAC8512

FEATURES
Space Saving SO-8 or Mini-DIP Packages
Complete, Voltage Output with Internal Reference
1 mV/Bit with 4.095 V Full Scale
Single +5 Volt Operation
No External Components
3-Wire Serial Data Interface, 20 MHz Data Loading Rate
Low Power: 2.5 mW

APPLICATIONS
Portable Instrumentation
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The DAC8512 is a complete serial input, 12-bit, voltage output digital-to-analog converter designed to operate from a single +5 V supply. It contains the DAC, input shift register and latches, reference and a rail-to-rail output amplifier. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease of use in +5 V only systems.

Coding for the DAC8512 is natural binary with the MSB loaded first. The output op amp can swing to either rail and is set to a range of 0 V to +4.095 V—for a one-millivolt-per-bit resolution. It is capable of sinking and sourcing 5 mA. An on-chip reference is laser trimmed to provide an accurate full-scale output voltage of 4.095 V.

Serial interface is high speed, three-wire, DSP compatible with data in (SDI), clock (CLK) and load strobe (LD). There is also a chip-select pin for connecting multiple DACs.

A CLR input sets the output to zero scale at power on or upon user demand.

The DAC8512 is specified over the extended industrial (–40°C to +85°C) temperature range. DAC8512s are available in plastic DIPs and SO-8 surface mount packages.

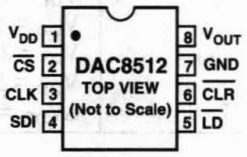
ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Description	Package Option*
DAC8512EP	±1	–40°C to +85°C	8-Pin P-DIP	N-8
DAC8512FP	±2	–40°C to +85°C	8-Pin P-DIP	N-8
DAC8512FS	±2	–40°C to +85°C	8-Lead SOIC	SO-8
DAC8512GBC	±2	+25°C	Dice	

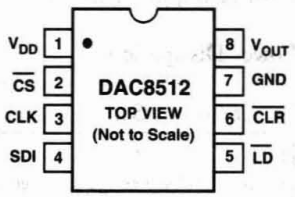
*For outline information see Package Information section.

PIN CONFIGURATIONS

SO-8



P-DIP-8



DAC8512–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 V ± 5%, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ	Max	Units
STATIC PERFORMANCE							
Resolution	N	Note 2		12			Bits
Relative Accuracy	INL		E Grade	–1	±1/4	+1	LSB
			F Grade	–2	±3/4	+2	LSB
Differential Nonlinearity	DNL	No Missing Codes		–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H			+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data = FFF_H[3]	E Grade	4.087	4.095	4.103	V
			F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4			16		ppm/°C
ANALOG OUTPUT							
Output Current	I_{OUT}	Data = 800_H		±5	±7		mA
Load Regulation at Full Scale	L_{REG}	R_L = 402 Ω to ∞, Data = 800_H			1	3	LSB
Capacitive Load	C_L	No Oscillation[4]			500		pF
LOGIC INPUTS							
Logic Input Low Voltage	V_{IL}					0.8	V
Logic Input High Voltage	V_{IH}			2.4			V
Input Leakage Current	I_{IL}					10	µA
Input Capacitance	C_{IL}					10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]							
Clock Width High	t_{CH}			30	10		ns
Clock Width Low	t_{CL}			30	10		ns
Load Pulse Width	t_{LDW}			20			ns
Data Setup	t_{DS}			15	10		ns
Data Hold	t_{DH}			15	5		ns
Clear Pulse Width	t_{CLRW}			30	20		ns
Load Setup	t_{LD1}			15			ns
Load Hold	t_{LD2}			10			ns
Select	t_{CSS}			30			ns
Deselect	t_{CSH}			20			ns
AC CHARACTERISTICS[4]							
Voltage Output Settling Time	t_S	To ±1 LSB of Final Value[5]			16		µs
DAC Glitch					15		nV s
Digital Feedthrough					15		nV s
SUPPLY CHARACTERISTICS							
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load			1.5	2.5	mA
		V_{DD} = 5 V, V_{IL} = 0 V, No Load			0.5	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V, No Load			7.5	12.5	mW
		V_{DD} = 5 V, V_{IL} = 0 V, No Load			2.5	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%			0.002	0.004	%/%

NOTES

[1]All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB = 1 mV for 0 V to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

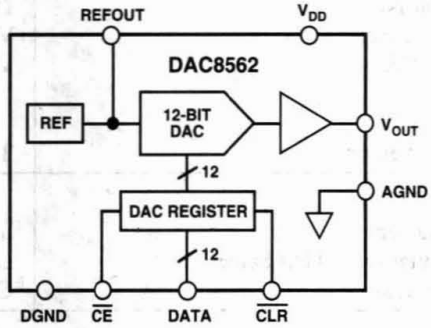
+5 Volt, Parallel Input Complete 12-Bit DAC

DAC8562

FEATURES
Complete 12-Bit DAC
No External Components
Single +5 Volt Operation
1 mV/Bit with 4.095 V Full Scale
True Voltage Output, ±5 mA Drive
Very Low Power –3 mW

APPLICATIONS
Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



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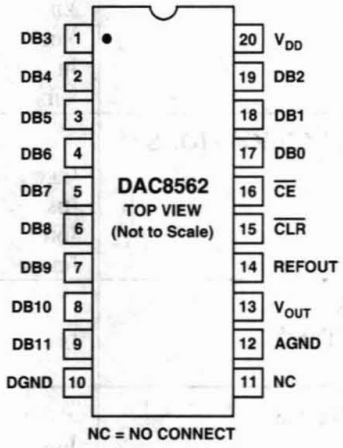
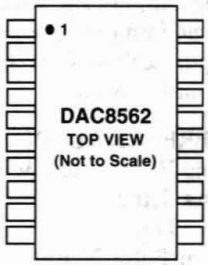
PIN CONFIGURATIONS

20-Pin P-DIP (N-20)



NC = NO CONNECT

SOL-20 (R-20)



GENERAL DESCRIPTION

The DAC8562 is a complete, parallel input, 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DAC, is a rail-to-rail amplifier, latch and reference. The reference (REFOUT) is trimmed to 2.5 volts, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The DAC8562 is coded straight binary. The op amp output swings from 0 to +4.095 volts for a one millivolt per bit resolution, and is capable of driving ±5 mA. Built using low temperature-coefficient silicon-chrome thin-film resistors, excellent linearity error over temperature has been achieved as shown below in the linearity error versus digital input code plot.

Digital interface is parallel and high speed to interface to the fastest processors without wait states. The interface is very simple requiring only a single $\overline{CE}$ signal. An asynchronous $\overline{CLR}$ input sets the output to zero scale.

The DAC8562 is available in two different 20-pin packages, plastic DIP and SOL-20. Each part is fully specified for operation over –40°C to +85°C, and the full +5 V ± 5% power supply range.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8562/883 data sheet which specifies operation over the –55°C to +125°C temperature range.

ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Option*
DAC8562EP	±1/2	–40°C to +85°C	N-20
DAC8562FP	±1	–40°C to +85°C	N-20
DAC8562FS	±1	–40°C to +85°C	R-20
DAC8562GBC	±1	+25°C	Dice

*For outline information see Package Information section.

DAC8562–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 V ± 5%, R_S = No Load, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 2	12			Bits
Relative Accuracy	INL	E Grade	–1/2	±1/4	+1/2	LSB
		F Grade	–1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+1/2	+3	LSB
Full-Scale Voltage	V_{FS}	Data - FFF_H[3]				
		E Grade	4.087	4.095	4.103	V
		F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 3, 4		±16		ppm/°C
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H	±5	±7		mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[4]		500		pF
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 5	5	7		mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 to 5 mA			0.1	%/mA
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 4			10	pF
INTERFACE TIMING SPECIFICATIONS[1, 4]						
Chip Enable Pulse Width	t_{CEW}		30			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Clear Pulse Width	t_{CLRW}		20			ns
AC CHARACTERISTICS[4]						
Voltage Output Settling Time[6]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough				35		nV sec
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		3	6	mA
		V_{IL} = 0 V, V_{DD} = +5 V		0.6	1	mA
Power Dissipation	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		15	30	mW
		V_{IL} = 0 V, V_{DD} = +5V		3	5	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]1 LSB = 1 mV for 0 to +4.095 V output range.

[3]Includes internal voltage reference error.

[4]These parameters are guaranteed by design and not subject to production testing.

[5]Very little sink current is available at the REFOUT pin. Use external buffer if setting up a virtual ground.

[6]The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

Octal 8-Bit CMOS D/A Converter

DAC8800

FEATURES

- ±1/2 LSB Total Unadjusted Error
- 2 µs Settling Time
- Serial Data Input
- ±Full-Scale Output Set by $V_{REF}H$ and $V_{REF}L$
- Unipolar and Bipolar Operation
- TTL Input Compatible
- 20-Pin DIP or SOL Package
- Low Cost

APPLICATIONS

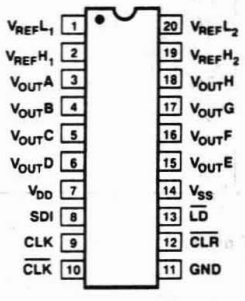
- Voltage Setpoint Control
- Digital Offset & Gain Adjustment
- Microprocessor Controlled Calibration
- General Purpose Trimming Adjustments

GENERAL DESCRIPTION

The DAC8800 TrimDAC® is designed to be a general purpose digitally controlled voltage adjustment device. The output voltage range can be independently set for each set of four D/A converters. In addition, both unipolar and bipolar output voltage ranges are easy to establish by external reference input high and low terminals. The digitally-programmed output voltages are ideal for op amp trimming, voltage-controlled amplifier gain setting and any general purpose trimming tasks.

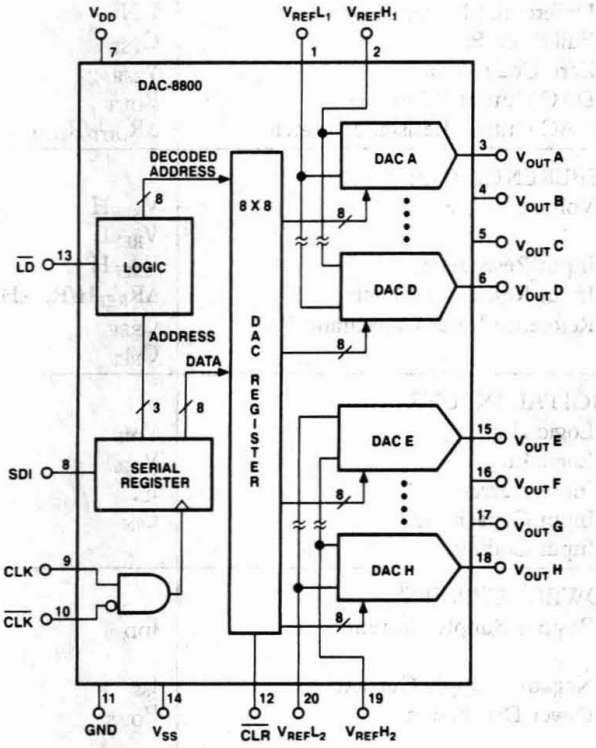
A three-wire serial digital interface loads the contents of eight internal DAC registers which establish the output voltage levels. An asynchronous Clear (CLR) input places all DACs in a zero code output condition, very handy for system power-up. An internal regulator provides TTL input compatibility over a wide range of V_{DD} supply voltages. Single supply operation is available by connecting V_{SS} to GND.

PIN CONNECTIONS



TrimDAC is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION[1]

Model	Temperature Range	Package Description[2]
DAC8800BR[3]	–55°C to +125°C	Q-20 Cerdip
DAC8800FR	–40°C to +85°C	Q-20 Cerdip
DAC8800FP	–40°C to +85°C	N-20 Plastic DIP
DAC8800FS	–40°C to +85°C	R-20 SOL

NOTES

[1]Burn in is available on commercial and industrial temperature range parts in Cerdip and plastic DIP packages.

[2]For outline information see Package Information section.

[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

DAC8800–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1]

Single Supply; V_{DD} = +12 V, V_{SS} = 0 V, $V_{REF}H$ = +5 V, $V_{REF}L$ = 0 V; or Dual Supply; V_{DD} = +12 V, V_{SS} = –5 V, $V_{REF}H$ = +2.5 V, $V_{REF}L$ = –2.5 V; F Grade; –40°C ≤ T_A ≤ +85°C; B Grade; –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY (All specifications apply for DACs A, B, C, D, E, F, G, H)						
Resolution	N		8			Bits
Total Unadjusted Error[2]	TUE				±1/2	LSB
Differential Nonlinearity[3]	DNL				±1	LSB
Full Scale Error	G_{FSE}				±1/2	LSB
Zero Code Error	V_{ZSE}				±1/2	LSB
DAC Output Resistance	R_{OUT}		8	12	16	kΩ
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$			0.5		%
REFERENCE INPUT						
Voltage Range[5]	$V_{REF}H$	Pins 2 & 19	$V_{REF}L$		(V_{DD} – 4)	V
	$V_{REF}L$	Pins 1 & 20	V_{SS}		$V_{REF}H$	V
Input Resistance	$V_{REF}H$	Digital Inputs = 55_H	2	3		kΩ
Input Resistance Match	$\Delta R_{REF}H/R_{REF}H$	Digital Inputs = 55_H		0.5		%
Reference Input Capacitance[4]	C_{REF}	Digital Inputs All Zeros		50	75	pF
	C_{REF}	Digital Inputs All Ones		75	100	pF
DIGITAL INPUTS						
Logic High	V_{INH}		2.4			V
Logic Low	V_{INL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0 V or +5 V			±1	μA
Input Capacitance[4]	C_{IN}			4	8	pF
Input Coding				Binary		
POWER SUPPLIES[6]						
Positive Supply Current	I_{DD}	Dual Supply–TTL		1	2	mA
		Dual Supply–CMOS		0.2	0.4	mA
Negative Supply Current	I_{SS}	Dual Supply		0.01	0.2	mA
Power Dissipation	P_{DISS}	Single Supply Operation		12	24	mW
		Dual Supply Operation		12	25	mW
DC Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%		0.001	0.01	%/%
DYNAMIC PERFORMANCE[4]						
V_{OUT} Settling Time	t_S	±1/2 LSB Error Band		0.8	2	μs
Channel-to-Channel Crosstalk[7]	CT	Measured Between Adjacent DAC Outputs		80		nVs
SWITCHING CHARACTERISTICS[4, 8]						
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock Level High or Low	60			ns
Data Setup Time	t_{DS}		30			ns
Data Hold Time	t_{DH}		30			ns
DAC Register Load Pulse Width	t_{LD}		50			ns
Clear Pulse Width	t_{CLR}		50			ns
Clock Edge to Load Time	t_{CKLD}		50			ns
Edge Time	t_{LDCK}		50			ns

NOTES

[1]Testing performed in SINGLE SUPPLY mode, except I_{DD}, I_{SS}, and PSRR which are tested in DUAL SUPPLY mode.

[2]Includes Full Scale Error, Relative Accuracy, and Zero Code Error.

[3]All devices guaranteed monotonic over the full operating temperature range.

[4]Guaranteed by design and not subject to production test.

[5]V_{DD} – 4 volts is the maximum reference voltage for the above specifications. Also $V_{REF}H \geq V_{REF}L$

[6]Digital lnput voltages $V_{IN} = V_{INL}$ or V_{INH} for TTL condition; V_{IN} = 0 V or +5 V for CMOS condition. DAC outputs unloaded. P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).

[7]Measured at V_{OUT} pin where an adjacent V_{OUT} pin is making a full-scale voltage change.

[8]See timing diagram for location of measured values.

Specifications subject to change without notice.

8-Bit, Octal, 4-Quadrant Multiplying, CMOS TrimDAC

DAC8840

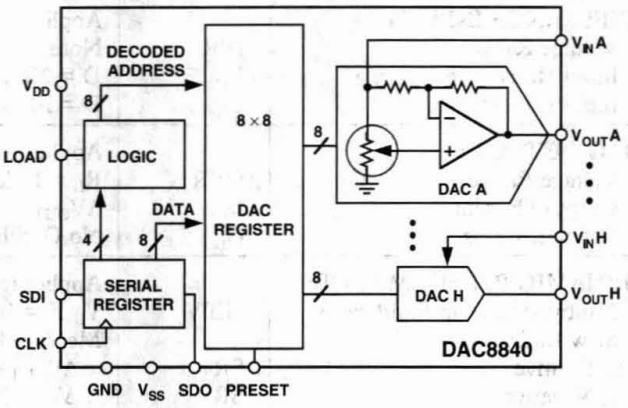
FEATURES

Replaces 8 Potentiometers
1 MHz 4-Quadrant Multiplying Bandwidth
No Signal Inversion
Low Zero Output Error
Eight Individual Channels
3-Wire Serial Input
500 kHz Update Data Loading Rate
±3 Volt Output Swing
Midscale Preset, Zero Volts Out

APPLICATIONS

Automatic Adjustment
Trimmer Replacement
Dynamic Level Adjustment
Special Waveform Generation and Modulation

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The DAC8840 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC® capability allows replacement of the mechanical trimmer function in new designs. The DAC8840 is ideal for ac or dc gain control of up to 1 MHz bandwidth signals. The 4-quadrant multiplying capability is useful for signal inversion and modulation often found in video convergence circuitry.

Internally the DAC8840 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

The DAC8840 consumes only 190 mW from ±5 V power supplies. For single 5 V supply applications consult the DAC8841.

The DAC8840 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages.

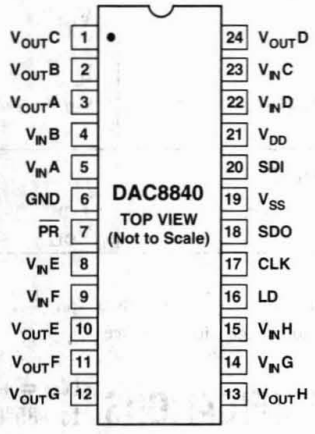
TrimDAC is a registered trademark of Analog Devices, Inc.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
DAC8840FP	–40°C to +85°C	Plastic DIP	N-24
DAC8840FW	–40°C to +85°C	Cerdip	Q-24
DAC8840FS	–40°C to +85°C	SOL-24	R-24
DAC8840GBC	25°C	DICE	

*For outline information see Package Information section.

PIN CONFIGURATION



DAC8840–SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = –5 V, All $V_{IN}X$ = +3 V, T_A = –40°C to +85°C apply for DAC8840F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL			±1/4	±1	LSB
Differential Nonlinearity	DNL	All Devices Monotonic			±1	LSB
Output Offset	V_{BZE}	$\overline{PR}$ = 0, Sets D = 80_H		3	25	mV
Output Offset Drift	TCV_{BZ}	$\overline{PR}$ = 0, Sets D = 80_H		10		µV/°C
REFERENCE INPUTS		Applies to All Inputs $V_{IN}X$				
Voltage Range	IVR	Note 1	±3			V
Input Resistance	R_{IN}	D = $2B_H$, Code Dependent	3	6		kΩ
Input Capacitance	C_{IN}	D = FF_H, Code Dependent		19	30	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	±3			V
Output Current	I_{OUT}	ΔV_{OUT} < 1 LSB	±5	±10		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p-p	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
Positive	SR+	$\Delta V_{OUT}X$ = +6 V	1.3	4.0		V/µs
Negative	SR–	$\Delta V_{OUT}X$ = –6 V	1.3	2.5		V/µs
Total Harmonic Distortion	THD	$V_{IN}X$ = 4 V p-p, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_N	f = 1 kHz		0.17		µV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, D = 0 to FF_H		3.5	6	µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	80		dB
Digital Feedthrough	Q	$V_{IN}X$ = 0 V, D = 0 to 255_{10}		6		nVs
POWER SUPPLIES						
Power Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Negative Supply Current	I_{SS}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			190	260	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V, ΔV_{DD} = ±5%		0.0002	0.01	%/%
Power Supply Range	PSR	V_{DD}, |V_{SS}|	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}			7	10	pF
Input Coding			Offset Binary			
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V

NOTE
[1]Maximum input voltage is always 2 V less than V_{DD}.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{DD} = +5 V, V_{SS} = –5 V, All $V_{IN}X$ = +3 V, T_A = –40°C to +85°C apply for DAC8840F, unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Clock Pulse Width	t_{CH}, t_{CL}	80		ns
Data Setup Time	t_{DS}	40		ns
Data Hold Time	t_{DH}	20		ns
CLK to SDO Propagation Delay	t_{PD}		120	ns
DAC Register Load Pulse Width	t_{LD}	70		ns
Preset Pulse Width	t_{PR}	50		ns
Clock Edge to Load Time	t_{CKLD}	30		ns
Load Edge to Next Clock Edge	t_{LDCK}	60		ns

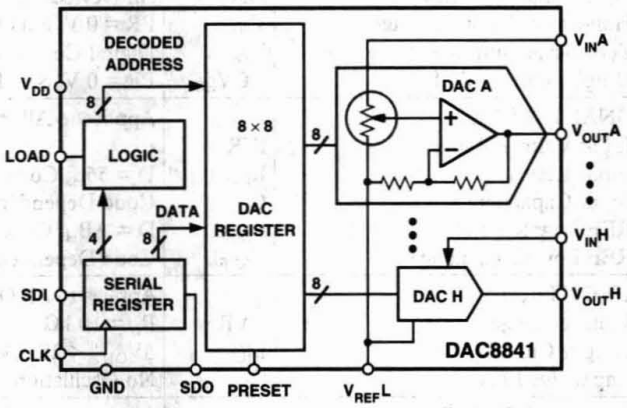
8-Bit Octal, 2-Quadrant Multiplying, CMOS TrimDAC

DAC8841

FEATURES
- Replaces 8 Potentiometers
- Operates From Single +5 V Supply
- 1 MHz 2-Quadrant Multiplying Bandwidth
- No Signal Inversion
- Eight Individual Channels
- 3-Wire Serial Input
- 500 kHz Update Data Loading Rate
- +3 Volt Output Swing
- Midscale Preset
- Low 95 mW Power Dissipation

APPLICATIONS
- Trimmer Replacement
- Dynamic Level Adjustment
- Special Waveform Generation and Modulation
- Programmable Gain Amplifiers

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

The DAC8841 provides eight general purpose digitally controlled voltage adjustment devices. The TrimDAC™ capability replaces the mechanical trimmer function in new designs. It is ideal for ac or dc gain control of up to 1 MHz bandwidth signals.

Internally the DAC8841 contains eight voltage output CMOS digital-to-analog converters, each with separate reference inputs. Each DAC has its own DAC register which holds its output state. These DAC registers are updated from an internal serial-to-parallel shift register which is loaded from a standard 3-wire serial input digital interface. Twelve data bits make up the data word clocked into the serial input register. This data word is decoded where the first 4 bits determine the address of the DAC register to be loaded with the last 8 bits of data. A serial data output pin at the opposite end of the serial register allows simple daisy-chaining in multiple DAC applications without additional external decoding logic.

The DAC8841 consumes only 95 mW from a +5 V power supply. For dual polarity applications see the DAC8840 which provides full 4-quadrant-multiplying ±3 V signal capability while operating from ±5 V power supplies.

The DAC8841 is available in 24-pin plastic DIP, cerdip, and SOIC-24 packages.

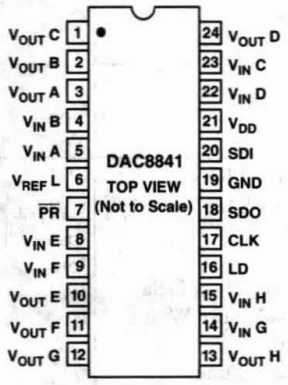
TrimDAC is a trademark of Analog Devices, Inc.

ORDERING GUIDE

Model	Temperature Range	Package Option*
DAC8841FP	–40°C to +85°C	Plastic DIP
DAC8841FW	–40°C to +85°C	Cerdip
DAC8841FS	–40°C to +85°C	SOIC
DAC8841GBC	–25°C	Dice

*For outline information see Package Information section.

PIN CONFIGURATION



DAC8841–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5 V, All $V_{IN}X$ = +1.5 V, $V_{REF}L$ = 0 V, T_A = –40°C to +85°C apply for DAC8841F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY		All Specifications Apply for DACs A, B, C, D, E, F, G, H				
Resolution	N		8			Bits
Integral Nonlinearity	INL	Note 1		±1/2	±1.5	LSB
Differential Nonlinearity	DNL	All Devices Monotonic, Note 1			±1	LSB
Half-Scale Output Voltage	V_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H	1.475	1.500	1.525	V
Zero-Scale Output Voltage	V_{ZS}	Digital Code = 00_H		20	100	mV
Output Voltage Drift	TCV_{HS}	$\overline{PR}$ = 0 V, Sets D = 80_H		10		µV/°C
SIGNAL INPUTS		Applies to All Inputs $V_{IN}X$ or $V_{REF}L$				
Input Voltage Range	IVR		0		1.5	V
Input Resistance	R_{IN}	D = 55_H; Code Dependent	4	10		kΩ
Input Capacitance	C_{IN}	Code Dependent		19	30	pF
REF Low Resistance	$R_{REF}L$	D = AB_H; Code Dependent	0.3	0.75		kΩ
REF Low Capacitance	$C_{REF}L$	Code Dependent		190	250	pF
DAC OUTPUTS		Applies to All Outputs $V_{OUT}X$				
Voltage Range	OVR	R_L = 10 kΩ	0		3	V
Output Current	I_{OUT}	ΔV_{OUT} < 25 mV, $V_{IN}X$ = 1.375 V, $\overline{PR}$ = 0 V	±5	7		mA
Capacitive Load	C_L	No Oscillation			200	pF
DYNAMIC PERFORMANCE		Applies to All DACs				
Multiplying Gain Bandwidth	GBW	$V_{IN}X$ = 100 mV p-p + 1.0 V dc	1	2.5		MHz
Slew Rate		Measured 10% to 90%				
	+SR	$\Delta V_{OUT}X$ = +3 V	1.3	4.0		V/µs
	–SR	$\Delta V_{OUT}X$ = –3 V	1.3	2.5		V/µs
Total Harmonic Distortion	THD	$V_{IN}X$ = 1 V p-p + 1.0 V dc, D = FF_H, f = 1 kHz, f_{LP} = 80 kHz		0.01		%
Spot Noise Voltage	e_n	f = 1 kHz		0.17		µV/√Hz
Output Settling Time	t_S	±1 LSB Error Band, 8_{10} to 255_{10}		3.5	6	µs
Channel-to-Channel Crosstalk	C_T	Measured Between Adjacent Channels, f = 100 kHz	60	70		dB
Digital Feedthrough	Q	$V_{REF}L$ = +1.5 V, D = 0 to FF_H		6		nVs
POWER SUPPLIES						
Positive Supply Current	I_{DD}	$\overline{PR}$ = 0 V		19	26	mA
Power Dissipation	P_{DISS}			95	130	mW
DC Power Supply Rejection Ratio	PSRR	$\overline{PR}$ = 0 V			0.01	%/%
Power Supply Range	PSR	V_{DD}	4.75	5.00	5.25	V
DIGITAL INPUTS						
Logic High	V_{IH}		2.4			V
Logic Low	V_{IL}				0.8	V
Input Current	I_L				±10	µA
Input Capacitance	C_{IL}				8	pF
Input Coding				Binary		
DIGITAL OUTPUT						
Logic High	V_{OH}	I_{OH} = –0.4 mA	3.5			V
Logic Low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
TIMING SPECIFICATIONS						
Input Clock Pulse Width	t_{CH}, t_{CL}		80			ns
Data Setup Time	t_{DS}		40			ns
Data Hold Time	t_{DH}		20			ns
CLK to SDO Propagation Delay	t_{PD}				120	ns
DAC Register Load Pulse Width	t_{LD}		70			ns
Preset Pulse Width	t_{PR}		50			ns
Clock Edge to Load Time	t_{CKLD}		30			ns
Load Edge to Next Clock Edge	t_{LDCK}		60			ns

NOTE

[1]INL and DNL tests do not include operation at codes 0 through 7 due to zero-scale output voltage. For bias voltages above 100 mV on $V_{REF}L$, INL and DNL are maintained over all codes.

Specifications subject to change without notice.

Instrumentation Amplifiers
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Instrumentation Amplifiers–Selection Guides

Resistor Programmable

Model	Gain Range 1 RTO Error at +25°C = G × RTI + RTO mV	10 mV	100 mV	1000 mV	–3 dB BW A_V = 1–1000 MHz	V_{NOISE} RTI 1 to 10 Hz µV p-p	V_{OS} RTI +25°C µV	V_{OS} RTI µV/°C	# Pins	Page No.	Comments	Fax-code
SSM2017	501.00	512.00	620	1700	4–0.2	NS	1200	NS	8/16	16–9	Ultralow Distortion Audio Preamp	1782
AMP01F/G	6.1	7	16	106	0.57–0.026	13	100	1	18/20/28	7–23		1607
AMP01E/A	3.05	3.5	8	53	0.57–0.026	13	50	0.30	18/20/28	7–23		1607
AMP02F	8.2	10	28	208	1.2–0.2	10	200	4	8/16	7–25		1608
AMP02E	4.1	5	14	104	1.2–0.2	10	100	2	8/16	7–25		1608
AMP04F	3.3	6	33	303	0.7–ns	7	300	6	8	7–27	True Single Supply, Zero In/Out	1610
AMP04E	1.65	3	16.5	152	0.7–ns	7	150	6	8	7–27		1610
AD620A	0.53	1.65	12.9	125.4	0.8–0.012	6	125	1.0	8	7–7		1197
AD620B	0.25	0.7	5.2	50.2	0.8–0.012	6	50	0.6	8	7–7		1197
AD622A	1.75	4	15	250	0.8–0.012	6	125	2	8	7–11		1986
AD625J/A	5.2	7	25	205	0.6–0.025	4	200	2	16/20	7–15	Gain to 10,000	1200
AD625K/B	3.05	3.5	8	53	0.6–0.025	4	50	1	16/20	7–15		1200
AD625C	2.025	2.25	4.5	27	0.6–0.025	4	25	0.25	16/20	7–15		1200

Software Programmable

AD526A	1.5	12	NA	NA	4–0.35	9	1.5	20	16	7–5	Program Gain 1, 2, 4, 8	1144
AD526B	0.7	5.6	NA	NA	4–0.35	9	0.7	10	16	7–5		1144
AD526C	0.5	4	NA	NA	4–0.35	9	0.5	10	16	7–5		1144

Pin Programmable

AD524A	5.25	7.5	30	255	1–0.025	15	250.00	2	16/20	7–3	Program Gain 1, 10, 100, 1000	1142
AD524B	3.1	4	13	103	1–0.025	15	100.00	0.75/2	16/20	7–3		1142
AD524C	2.05	2.5	7	52	1–0.025	15	50.00	0.50	16/20	7–3		1142
AD621A	NA	2.5	25	NA	0.4–0.15	6	250	15	8	7–9	Program Gain 10, 100	1198
AD621B	NA	1.25	12.5	NA	0.4–0.15	6	125	7	8	7–9	Program Gain 10, 100	1198
AD624A	5.2	7	25	205	1 > 0.025	10	200	2	16	7–13	Pin Program Gains 1, 100, 500, 1000	1199
AD624B	3.075	3.75	10.5	78	1 > 0.025	10	75	0.5	16	7–13		1199
AD624C	2.025	2.25	4.5	27	1 > 0.025	10	25	0.25	16	7–13		1199
Single Supply, Sensor Interface, with RFI Input Atten.,												
AD626		20	200		0.1	2	200	NA	8	7–17	Pin Program Gains, 10, 100	1201
AD22050	1	20			0.02	2	1	15	8	7–19	Fixed A_V = 20, or Adj. 1 > 160, +3 V > 36	1883
AD22057	1	20			0.02	2	1	15	8	7–21	Fixed A_V = 20, or Adj. 1 > 160	1914

ANALOG DEVICES

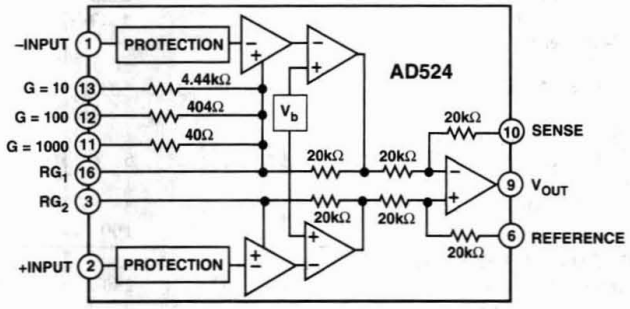
Precision Instrumentation Amplifier

AD524

FEATURES

Low Noise: 0.3 μV p-p 0.1 Hz to 10 Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120 dB (G = 1000)
Low Offset Voltage: 50 μV
Low Offset Voltage Drift: 0.5 μV/°C
Gain Bandwidth Product: 25 MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On–Power Off
No External Components Required
Internally Compensated
MIL-STD-883B and Chips Available
16-Pin Ceramic DIP and SOIC Packages and 20-Terminal Leadless Chip Carriers Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Standard Military Drawing Also Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD524 has an output offset voltage drift of less than 25 mV/°C, input offset voltage drift of less than 0.5 mV/°C, CMR above 90 dB at unity gain (120 dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25 MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5 V/ms and settles in 15 ms to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.

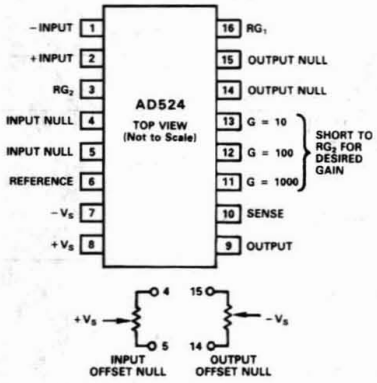
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD524AD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524AE	–40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524AR-16	–40°C to +85°C	16-Pin Gull-Wing SOIC	R-16
AD524AR-16-REEL	–40°C to +85°C	Tape & Reel Packaging	
AD524AR-16-REEL7	–40°C to +85°C	Tape & Reel Packaging	
AD524BD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524BE	–40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524CD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524SD	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SD/883B	–55°C to +125°C	16-Pin Ceramic DIP	D-16
5962-8853901EA[2]	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SE/883B	–55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD524SCHIPS	–55°C to +125°C	Die	

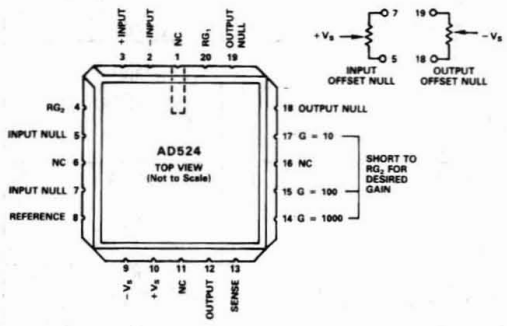
[1]For outline information see Package Information section.
[2]Refer to official DESC drawing for tested specifications.

CONNECTION DIAGRAMS

Ceramic (D) and SOIC (R) Packages



Leadless Chip Carrier (E) Package



To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD524—SPECIFICATIONS (@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C unless otherwise noted)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation	$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			
Gain Range (Pin Programmable)	1 to 1000			1 to 1000			1 to 1000			1 to 1000			
Gain Error													
G = 1			**±0.05**			**±0.03**			**±0.02**			**±0.05**	%
G = 10			**±0.25**			**±0.15**			**±0.1**			**±0.25**	%
G = 100			**±0.5**			**±0.35**			**±0.25**			**±0.5**	%
G = 1000			**±2.0**			**±1.0**			**±0.5**			**±2.0**	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10,100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			**250**			**100**			**50**			**100**	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	mV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to Input vs. Supply													
G = 1	**70**			**75**			**80**			**75**			dB
G = 1000	**100**			**110**			**115**			**110**			dB
INPUT CURRENT													
Input Bias Current			**±50**			**±25**			**±15**			**±50**	nA
Input Offset Current			**±35**			**±15**			**±10**			**±35**	nA
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_{DL})	±10			±10			±10			±10			V
Max Common-Mode Linear (V_{CM})	$12\text{ V}-\left(\frac{G}{2}\times V_D\right)$			$12\text{ V}-\left(\frac{G}{2}\times V_D\right)$			$12\text{ V}-\left(\frac{G}{2}\times V_D\right)$			$12\text{ V}-\left(\frac{G}{2}\times V_D\right)$			V
Common-Mode Rejection dc to 60 Hz with 1 kΩ Source Imbalance													
G = 1	**70**			**75**			**80**			**70**			dB
G = 1000	**110**			**115**			**120**			**110**			dB
OUTPUT RATING													
V_{OUT}, R_L = 2 kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal – 3 dB													
G = 1		1			1			1			1		MHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step													
G = 1 to 100		15			15			15			15		µs
NOISE													
Voltage Noise, 1 kHz													
R.T.I.		7			7			7			7		$nV/\sqrt{Hz}$
R.T.O.		**90**			**90**			**90**			**90**		$nV\sqrt{Hz}$
R.T.I., 0.1 Hz to 10 Hz													
G = 1		15			15			15			15		µV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		µV p-p
Current Noise													
0.1 Hz to 10 Hz		**60**			**60**			**60**			**60**		pA p-p
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ±20%
I_{IN}		15			15			15			15		µA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ±20%
I_{IN}		15			15			15			15		µA
Voltage Range	±10			±10			10			10			V
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA

Specifications subject to change without notice.

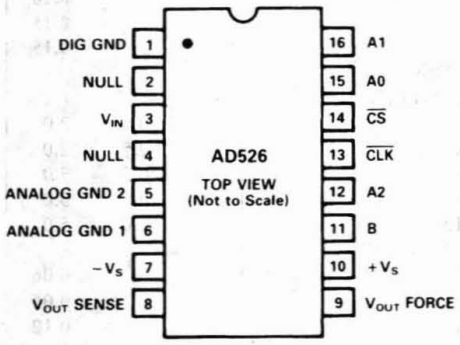
Software Programmable Gain Amplifier

AD526

FEATURES

Digitally Programmable Binary Gains from 1 to 16
Two-Chip Cascade Mode Achieves Binary Gain from 1 to 256
Gain Error:
0.01% max, Gain = 1, 2, 4 (C Grade)
0.02% max, Gain = 8, 16 (C Grade)
0.5 ppm/°C Drift Over Temperature
Fast Settling Time
10 V Signal Change:
0.01% in 4.5 μs (Gain = 16)
Gain Change:
0.01% in 5.6 μs (Gain = 16)
Low Nonlinearity: ±0.005% FSR max (J Grade)
Excellent DC Accuracy:
Offset Voltage: 0.5 mV max (C Grade)
Offset Voltage Drift: 3 μV/°C (C Grade)
TTL Compatible Digital Inputs

PIN CONFIGURATION



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PRODUCT DESCRIPTION

The AD526 is a single-ended, monolithic software programmable gain amplifier (SPGA) that provides gains of 1, 2, 4, 8 and 16. It is complete, including amplifier, resistor network and TTL-compatible latched inputs, and requires no external components.

Low gain error and low nonlinearity make the AD526 ideal for precision instrumentation applications requiring programmable gain. The small signal bandwidth is 350 kHz at a gain of 16. In addition, the AD526 provides excellent dc precision. The FET-input stage results in a low bias current of 50 pA. A guaranteed maximum input offset voltage of 0.5 mV max (C grade) and low gain error (0.01%, G = 1, 2, 4, C grade) are accomplished using Analog Devices' laser trimming technology.

To provide flexibility to the system designer, the AD526 can be operated in either latched or transparent mode. The force/sense configuration preserves accuracy when the output is connected to remote or low impedance loads.

The AD526 is offered in one commercial (0°C to +70°C) grade, J, and three industrial grades, A, B and C, which are specified from –40°C to +85°C. The S grade is specified from –55°C to +125°C. The military version is available processed to MIL-STD-883B, Rev C. The J grade is supplied in a 16-pin plastic DIP, and the other grades are offered in a 16-pin hermetic side-brazed ceramic DIP.

APPLICATION HIGHLIGHTS

1. **Dynamic Range Extension for ADC Systems:**
   A single AD526 in conjunction with a 12-bit ADC can provide 96 dB of dynamic range for ADC systems.
2. **Gain Ranging Pre-Amps:**
   The AD526 offers complete digital gain control with precise gains in binary steps from 1 to 16. Additional gains of 32, 64, 128 and 256 are possible by cascading two AD526s.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD526JN	Commercial	16-Pin Plastic DIP	N-16
AD526AD	Industrial	16-Pin Cerdip	D-16
AD526BD	Industrial	16-Pin Cerdip	D-16
AD526CD	Industrial	16-Pin Cerdip	D-16
AD526SD/883B	Military	16-Pin Cerdip	D-16
5962-9089401MEA[2]			

NOTES
[1]For outline information see Package Information section.
[2]Refer to official DESC drawing for tested specifications.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD526—SPECIFICATIONS (@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C unless otherwise noted)

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
GAIN													
Gain Range													
(Digitally Programmable)		1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16		
Gain Error													
G = 1			**0.05**			**0.02**			**0.01**			**0.01**	%
G = 2			**0.05**			**0.03**			**0.02**			**0.01**	%
G = 4			**0.10**			**0.03**			**0.02**			**0.01**	%
G = 8			**0.15**			**0.07**			**0.04**			**0.02**	%
G = 16			**0.15**			**0.07**			**0.04**			**0.02**	%
Gain Error Drift													
Over Temperature													
G = 1		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 2		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 4		0.5	3.0		0.5	3.0		0.5	3.0		0.5	3.0	ppm/°C
G = 8		0.5	5.0		0.5	5.0		0.5	5.0		0.5	5.0	ppm/°C
G = 16		1.0	5.0		1.0	5.0		1.0	5.0		1.0	5.0	ppm/°C
Gain Error (T_{MIN} to T_{MAX})													
G = 1			0.06			**0.03**			**0.02**			**0.015**	%
G = 2			0.06			**0.04**			**0.03**			**0.015**	%
G = 4			0.12			**0.04**			**0.03**			**0.015**	%
G = 8 to 16			0.17			**0.08**			**0.05**			**0.03**	%
Nonlinearity													
G = 1			**0.005**			**0.005**			**0.005**			**0.0035**	% FSR
G = 2 to 16			0.001			0.001			0.001			0.001	% FSR
Nonlinearity (T_{MIN} to T_{MAX})													
G = 1			0.01			**0.01**			**0.01**			**0.007**	% FSR
G = 2 to 16			0.001			0.001			0.001			0.001	% FSR
VOLTAGE OFFSET, ALL GAINS													
Input Offset Voltage		0.4	**1.5**		0.25	**0.7**		0.25	**0.5**		0.25	**0.5**	mV
INPUT BIAS CURRENT													
Over Input Voltage Range ±10 V		50	**150**		50	**150**		50	**150**		50	**150**	pA
OUTPUT													
Voltage	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Current (V_{OUT} = ±10 V)	**±5**	±10		**±5**	±10		**±5**	±10		**±5**	±10		mA
Load Capacitance													
(For Stable Operation)		700			700			700			700		pF
NOISE, ALL GAINS													
Voltage Noise, RTI													
0.1 Hz to 10 Hz		3			3			3			3		µV p-p
DYNAMIC RESPONSE													
–3 dB Bandwidth (Small Signal)													
G = 1		4.0			4.0			4.0			4.0		MHz
G = 2		2.0			2.0			2.0			2.0		MHz
G = 4		1.5			1.5			1.5			1.5		MHz
G = 8		0.65			0.65			0.65			0.65		MHz
G = 16		0.35			0.35			0.35			0.35		MHz
TEMPERATURE RANGE													
Specified Performance	0		+70	–40		+85	–40/–55		+85/+125	–40		+85	°C
POWER SUPPLY													
Operating Range	**±4.5**		**±16.5**	**±4.5**		**±16.5**	**±4.5**		**±16.5**	**±4.5**		**±16.5**	V
Positive Supply Current		10	**14**		10	**14**		10	**14**		10	**14**	mA
Negative Supply Current		10	**13**		10	**13**		10	**13**		10	**13**	mA

Specifications subject to change without notice.

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES
EASY TO USE
Gain Set with One External Resistor (Gain Range 1 to 1000)
Wide Power Supply Range (±2.3 V to ±18 V)
Higher Performance than Three Op Amp IA Designs
Available in 8-Pin DIP and SOIC Packaging
Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("A GRADE")
125 μV max, Input Offset Voltage (50 μV max "B" Grade)
1 μV/°C max, Input Offset Drift
2.0 nA max, Input Bias Current
93 dB min Common-Mode Rejection Ratio (G = 10)

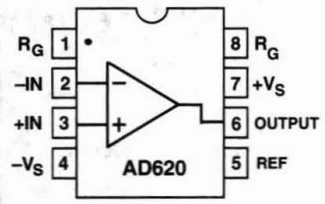
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
120 kHz Bandwidth (G = 100)
15 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
ECG and Medical Instrumentation
Transducer Interface
Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



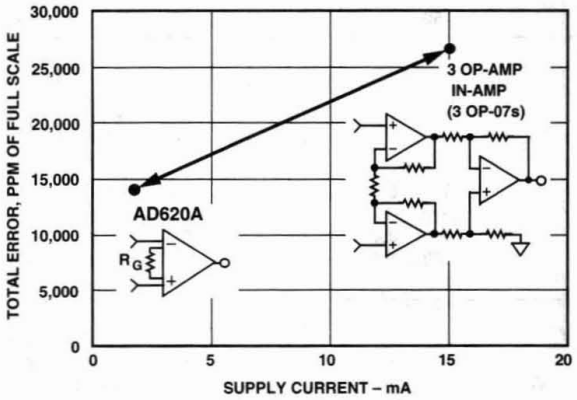
TOP VIEW

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier which requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-pin SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in amp per channel.



Three Op Amp IA Designs vs. AD620

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD620AN	–40°C to +85°C	N-8
AD620BN	–40°C to +85°C	N-8
AD620AR	–40°C to +85°C	R-8
AD620BR	–40°C to +85°C	R-8
AD620A Chips	–40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

AD620—SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10, 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = –10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature	Gain <1000[2]			–50			–50			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100, 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
INPUT											
Input Impedance Differential, Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Common-Mode Rejection Ratio dc to 60 Hz with I kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10, 1000		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ, V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	*Total RTI Noise* = $\sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$–V_S$ + 1.6		$+V_S$ –1.6	V_S + 1.6		$+V_S$ – 1.6	$–V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA

Specifications subject to change without notice.

Low Drift, Low Power Instrumentation Amplifier

AD621

FEATURES
EASY TO USE
Pin-Strappable Gains of 10 & 100
All Errors Specified for Total System Performance
Higher Performance than Discrete In-Amp Designs
Available in 8-Pin DIP and SOIC
Low Power, 1.3 mA max Supply Current
Wide Power Supply Range (±2.3 V to ±18 V)

EXCELLENT DC PERFORMANCE
0.15% max, Total Gain Error
±5 ppm/°C, Total Gain Drift
125 μV max, Total Offset Voltage
1.0 μV/°C max, Offset Voltage Drift

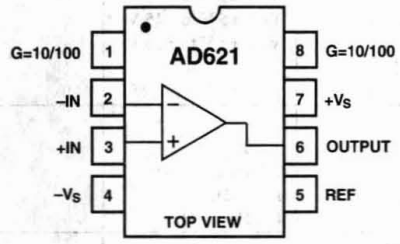
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
800 kHz Bandwidth (G = 10), 200 kHz (G = 100)
12 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
Transducer Interface & Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

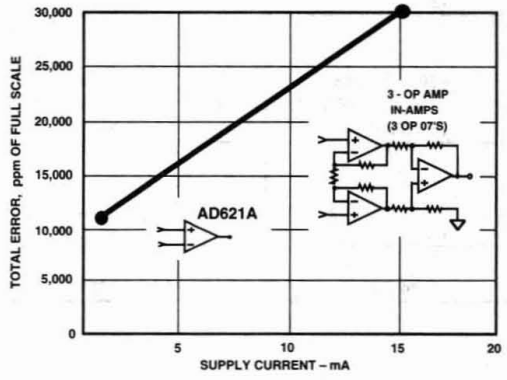
CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD621 is an easy to use, low cost, low power, high accuracy instrumentation amplifier which is ideally suited for a wide range of applications. Its unique combination of high performance, small size and low power, outperforms discrete in amp implementations. High functionality, low gain errors and low gain drift errors are achieved by the use of internal gain setting resistors. Fixed gains of 10 and 100 can be easily set via external pin strapping. The AD621 is fully specified as a total system, therefore, simplifying the design process.



Three Op Amp IA Designs vs. AD621

For portable or remote applications, where power dissipation, size and weight are critical, the AD621 features a very low supply current of 1.3 mA max and is packaged in a compact 8-pin SOIC, 8-pin plastic DIP or 8-pin cerdip. The AD621 also excels in applications requiring high total accuracy, such as precision data acquisition systems used in weigh scales and transducer interface circuits. Low maximum error specifications including nonlinearity of 10 ppm, gain drift of 5 ppm/°C, 50 μV offset voltage and 0.6 μV/°C offset drift ("B" grade), make possible total system performance at a lower cost than has been previously achieved with discrete designs or with other monolithic instrumentation amplifiers.

When operating from high source impedances, as in ECG and blood pressure monitors, the AD621 features the ideal combination of low noise and low input bias currents. Voltage noise is specified as 9 nV/√Hz at 1 kHz and 0.28 μV p-p from 0.1 Hz to 10 Hz. Input current noise is also extremely low at 0.1 pA/√Hz. The AD621 outperforms FET input devices with an input bias current specification of 1.5 nA max over the full industrial temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD621AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD621BN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD621AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621BR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621SQ/883B[2]	–55°C to +125°C	8-Pin Cerdip	Q-8
AD621ACHIPS	–40°C to +85°C	Die	

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.
[2]See Analog Devices' military data sheet for 883B specifications.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD621–SPECIFICATIONS

Gain = 100 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity,											
V_{OUT} = –10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			–1	±5		–1	±5		–1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±5 V to ±15 V		35	125		25	50		35	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			215			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Offset Referred to the											
Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	110	140		120	140		110	140		dB
TOTAL NOISE											
Voltage Noise (RTI)	1 kHz		9	13		9	13		9	13	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz–10 Hz		10			10			10		pA p-p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.3		$+V_S$ – 1.4	V
Common-Mode Rejection											
Ratio DC to 60 Hz with											
1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal,											
–3 dB Bandwidth			200			200			200		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN} +, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$–V_S$ + 1.6		$+V_S$ – 1.6	$–V_S$ + 1.6		$+V_S$ – 1.6	$–V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

NOTES

[1]See Analog Devices military data sheet for 883B tested specifications.

[2]This is defined as the supply range over which PSRR is defined.

[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost Instrumentation Amplifier

AD622

FEATURES

Easy to Use
Low Cost Solution
Higher Performance than Two or Three Op Amp Design
Unity Gain with No External Resistor
Optional Gains with One External Resistor (Gain Range 2 to 1000)
Wide Power Supply Range (±2.6 V to ±15 V)
Available in 8-Lead PDIP and SOIC
Low Power, 1.5 mA max Supply Current

GOOD DC PERFORMANCE

0.15% Gain Accuracy (G = 1)
250 μV max Input Offset Voltage
2.0 μV/°C max Input Offset Drift
5 nA max Input Bias Current
66 dB min Common-Mode Rejection Ratio (G = 1)

NOISE

12 nV/√Hz @ 1 kHz Input Voltage Noise
0.60 μV p-p Noise (0.1 Hz to 10 Hz, G = 10)

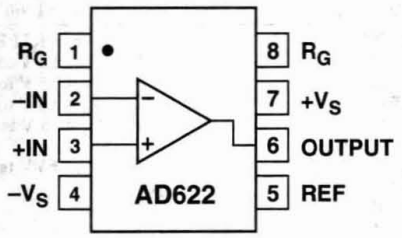
EXCELLENT AC CHARACTERISTICS

800 kHz Bandwidth (G = 10)
10 μs Settling Time to 0.1% @ G = 1–100
1.2 V/μs Slew Rate

APPLICATIONS

Transducer Interface
Low Cost Thermocouple Amplifier
Industrial Process Controls
Difference Amplifier
Low Cost Data Acquisition

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD622 is a low cost, moderately accurate instrumentation amplifier that requires only one external resistor to set any gain between 2 and 1,000. Or for a gain of 1, no external resistor is required. The AD622 is a complete difference or subtracter amplifier "system" while providing superior linearity and common-mode rejection by incorporating precision laser trimmed resistors.

The AD622 replaces low cost, discrete, two or three op amp instrumentation amplifier designs and offers good common-mode rejection, superior linearity, temperature stability, reliability, and board area consumption. The low cost of the AD622 eliminates the need to design discrete instrumentation amplifiers to meet stringent cost targets. While providing a lower cost solution, it also provides performance and space improvements.

ORDERING GUIDE

Model*	Temperature Range	Package Option
AD622AN	–40°C to +85°C	N-8
AD622AR	–40°C to +85°C	SO-8

*N = Plastic DIP, R = SOIC. For outline information see Package Information section.

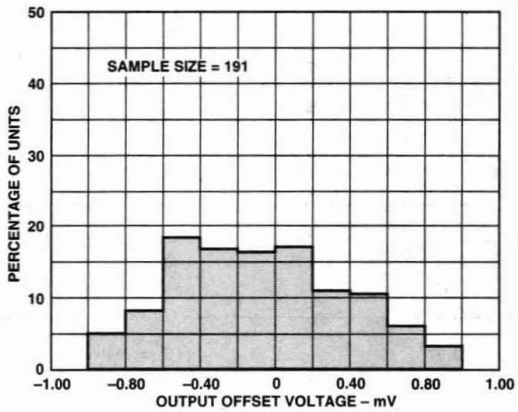


Figure 1. Typical Distribution of Output Offset Voltage

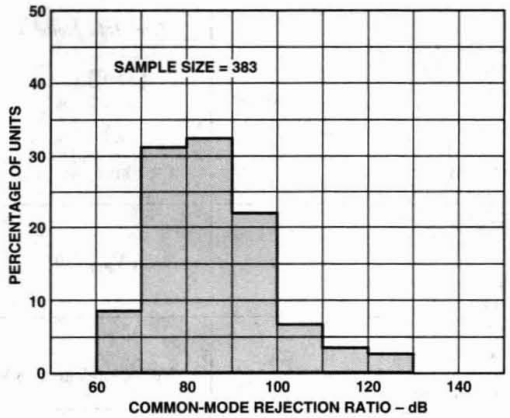


Figure 2. Typical Distribution of Common-Mode Rejection

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AD622—SPECIFICATIONS (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise noted)

Model	Conditions	Min	Typ	Max	Units
GAIN	G = 1 + (50.5 k/R_G)				
Gain Range		1		1000	
Gain Error[1]	V_{OUT} = ±10 V				
G = 1			0.05	0.15	%
G = 10			0.2	0.50	%
G = 100			0.2	0.50	%
G = 1000			0.2	0.50	%
Nonlinearity,	V_{OUT} = ±10 V				
G = 1–1000	R_L = 10 kΩ		10		ppm
G = 1–100	R_L = 2 kΩ		10		ppm
Gain vs. Temperature	Gain <1000[1]			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)				
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		60	250	µV
Average TC	V_S = ±5 V to ±15 V			2.0	µV/°C
Output Offset, V_{OSO}	V_S = ±5 V to ±15 V		600	1500	µV
Average TC	V_S = ±5 V to ±15 V			15	µV/°C
Offset Referred to the					
Input vs. Supply (PSR)	V_S = ±5 V to ±15 V				
G = 1		80	100		dB
G = 10		95	120		dB
G = 100		110	140		dB
G = 1000		110	140		dB
INPUT CURRENT					
Input Bias Current			2.0	5.0	nA
Average TC			3.0		pA/°C
Input Offset Current			0.7	2.5	nA
Average TC			2.0		pA/°C
INPUT					
Input Impedance					
Differential			10‖2		GΩ‖pF
Common-Mode			10‖2		GΩ‖pF
Input Voltage Range[2]	V_S = ±2.6 V to ±5 V	$-V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$-V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$-V_S$ + 2.1		$+V_S$ – 1.4	V
Common-Mode Rejection					
Ratio DC to 60 Hz with					
1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V				
G = 1		66	78		dB
G = 10		86	98		dB
G = 100		103	118		dB
G = 1000		103	118		dB
OUTPUT					
Output Swing	R_L = 10 kΩ,				
	V_S = ±2.6 V to ±5 V	$-V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$-V_S$ + 1.4		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$-V_S$ + 1.6		$+V_S$ – 1.5	V
Short Current Circuit			±18		mA
DYNAMIC RESPONSE					
Small Signal –3 dB Bandwidth					
G = 1			1000		kHz
G = 10			800		kHz
G = 100			120		kHz
G = 1000			12		kHz
Slew Rate			1.2		V/µs
Settling Time to 0.1%	10 V Step				
G = 1–100			10		µs
NOISE					
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$				
Input, Voltage Noise, e_{ni}			12		nV/√Hz
Output, Voltage Noise, e_{no}			72		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 1			4.0		µV p-p
G = 10			0.6		µV p-p
G = 100–1000			0.3		µV p-p
Current Noise	f = 1 kHz		100		fA/√Hz
0.1 Hz to 10 Hz			10		pA p-p
REFERENCE INPUT					
R_{IN}			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0015		
POWER SUPPLY					
Operating Range[3]		±2.6		±18	V
Quiescent Current	V_S = ±2.6 V to ±18 V		0.9	1.3	mA
Over Temperature			1.1	1.5	mA
TEMPERATURE RANGE					
For Specified Performance			–40 to +85		°C

NOTES

[1]Does not include effects of external resistor R_G.

[2]One input grounded. G = 1.

[3]This is defined as the same supply range that is used to specify PSR.

Specifications subject to change without notice.

ANALOG DEVICES

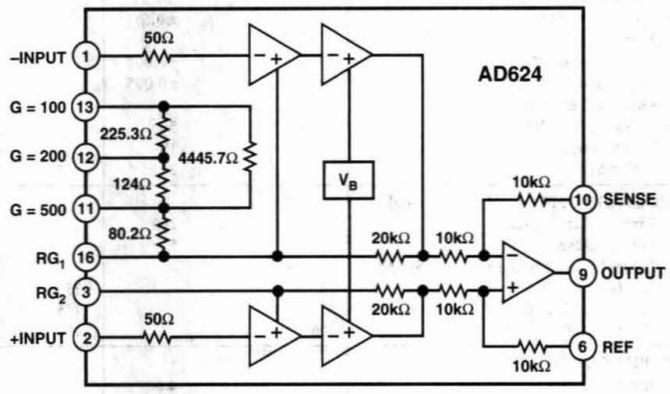
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2 μV p-p 0.1 Hz to 10 Hz
Low Gain TC: 5 ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130 dB min (G = 500 to 1000)
Low Input Offset Voltage: 25 μV max
Low Input Offset Voltage Drift: 0.25 μV/°C max
Gain Bandwidth Product: 25 MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD624 is a high precision, low noise, instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25 μV/°C, output offset voltage drift of less than 10 μV/°C, CMRR above 80 dB at unity gain (130 dB at G = 500) and a maximum nonlinearity of 0.001% at G = 1. In addition to these outstanding dc specifications, the AD624 exhibits superior ac performance as well. A 25 MHz gain bandwidth product, 5 V/μs slew rate and 15 μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pretrimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

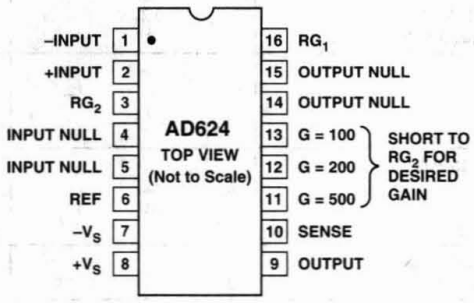
1. The AD624 offers outstanding noise performance. Input noise is typically less than 4 nV/$\sqrt{\text{Hz}}$ at 1 kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pretrimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD624AD	–25°C to +85°C	16-Pin Ceramic DIP	D-16
AD624BD	–25°C to +85°C	16-Pin Ceramic DIP	D-16
AD624CD	–25°C to +85°C	16-Pin Ceramic DIP	D-16
AD624SD	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD624SD/883B	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD624SCHIPS	–55°C to +125°C	Die	

*For outline information see Package Information section.

CONNECTION DIAGRAM



FOR GAINS OF 1000 SHORT RG_1 TO PIN 12 AND PINS 11 AND 13 TO RG_2

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AD624—SPECIFICATIONS (@ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C, unless otherwise noted)

Model	AD624A			AD624B			AD624C			AD624S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN													
Gain Equation (External Resistor Gain Programming)	$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40,000}{R_G}+1\right]\pm 20\%$			
Gain Range (Pin Programmable)	1 to 1000			1 to 1000			1 to 1000			1 to 1000			
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 100			±0.25			±0.15			±0.1			±0.25	%
G = 200, 500			±0.5			±0.35			±0.25			±0.5	%
Nonlinearity													
G = 1, 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1, 100, 200			5			5			5			5	ppm/°C
G = 100, 200			10			10			10			10	ppm/°C
G = 500			25			15			15			15	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			200			75			25			75	µV
Output Offset Voltage			5			3			2			3	mV
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 100, 200	95			105			110			105			dB
G = 500	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
Input Offset Current			±35			±15			±10			±35	nA
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_{DL})	±10			±10			±10			±10			V
Max Common-Mode Linear (V_{CM})	$12\ V-\left(\frac{G}{2}\times V_D\right)$			$12\ V-\left(\frac{G}{2}\times V_D\right)$			$12\ V-\left(\frac{G}{2}\times V_D\right)$			$12\ V-\left(\frac{G}{2}\times V_D\right)$			V
Common-Mode Rejection dc to 60 Hz with 1 kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 100, 200	100			105			110			100			dB
G = 500	110			120			130			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2 kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal –3 dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step													
G = 1 to 200		15			15			15			15		µs
G = 500		35			35			35			35		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1 kHz													
R.T.I.		4			4			4			4		nV/√Hz
R.T.O.		75			75			75			75		nV/√Hz
R.T.I., 0.1 Hz to 10 Hz													
G = 1		10			10			10			10		µV p-p
G = 100		0.3			0.3			0.3			0.3		µV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2		µV p-p
Current Noise, 0.1 Hz to 10 Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		µA
Voltage Range	±10			±10			±10			±10			V
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		µA
Voltage Range	±10			±10			±10			±10			V
TEMPERATURE RANGE													
Specified Performance	–25		+85	–25		+85	–25		+85	–55		+125	°C
POWER SUPPLY													
Power Supply Range	±6	±15	±18	±6	±15	±18	±6	±15	±18	±6	±15	±18	V
Quiescent Current		3.5	5		3.5	5		3.5	5		3.5	5	mA

Specifications subject to change without notice.

ANALOG DEVICES

Programmable Gain Instrumentation Amplifier

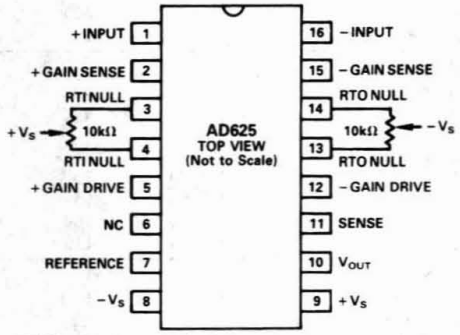
AD625

FEATURES

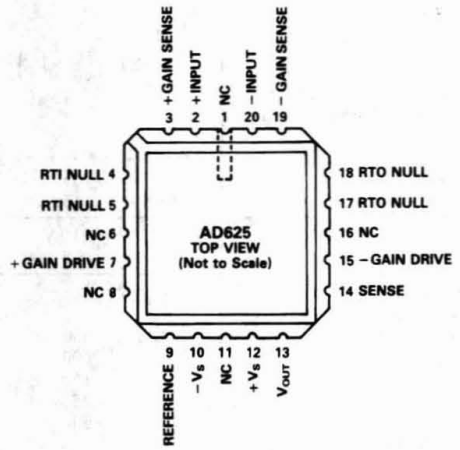
User Programmed Gains of 1 to 10,000
Low Gain Error: 0.02% max
Low Gain TC: 5 ppm/°C max
Low Nonlinearity: 0.001% max
Low Offset Voltage: 25 μV
Low Noise 4 nV/√Hz (at 1 kHz) RTI
Gain Bandwidth Product: 25 MHz
16-Pin Ceramic or Plastic DIP Package, 20-Pin LCC Package
Standard Military Drawing Available
MIL-Standard Parts Available
Low Cost

CONNECTION DIAGRAMS

Ceramic DIP (D) and Plastic DIP (N) Packages



Leadless Chip Carrier (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier specifically designed to fulfill two major areas of application: 1) Circuits requiring nonstandard gains (i.e., gains not easily achievable with devices such as the AD524 and AD624). 2) Circuits requiring a low cost, precision software programmable gain amplifier.

For low noise, high CMRR, and low drift the AD625JN is the most cost effective instrumentation amplifier solution available. An additional three resistors allow the user to set any gain from 1 to 10,000. The error contribution of the AD625JN is less than 0.05% gain error and under 5 ppm/°C gain TC; performance limitations are primarily determined by the external resistors. Common-mode rejection is independent of the feedback resistor matching.

The AD625 based SPGA will deliver 12-bit precision, and can be programmed for any set of gains between 1 and 10,000, with completely user selected gain steps.

PRODUCT HIGHLIGHTS

1. The AD625 affords up to 16-bit precision for user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A 12-bit software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The gain accuracy and gain temperature coefficient of the amplifier circuit are primarily dependent on the user selected external resistors.
4. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
5. The proprietary design of the AD625 provides input voltage noise of 4 nV/√Hz at 1 kHz.
6. External resistor matching is not required to maintain high common-mode rejection.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD625AD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625BD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625CD	–40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625SD	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD625SD/883B	–55°C to +125°C	16-Pin Ceramic DIP	D-16
AD625SE/883B	–55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD625JN	–40°C to +85°C	16-Pin Plastic DIP	N-16
AD625JK	–40°C to +85°C	16-Pin Plastic DIP	N-16
AD625ACHIPS	–40°C to +85°C	Die	
AD625SCHIPS	–55°C to +125°C	Die	
5962-8771901EA	Standard Military Drawing Available		

*For outline information see Package Information section.

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AD625—SPECIFICATIONS (typical @ V_S = ±15 V, R_L = 2 kΩ and T_A = +25°C, unless otherwise noted)

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
GAIN										
Gain Equation		$\frac{2\,R_F}{R_G}+1$			$\frac{2\,R_F}{R_G}+1$			$\frac{2\,R_F}{R_G}+1$		
Gain Range	1		10,000	1		10,000	1		10,000	
Gain Error		±.035	**±0.05**		±0.02	**±0.03**		±0.01	**±0.02**	%
Nonlinearity, Gain = 1-256			±0.005			±0.002			±0.001	%
Gain>256			±0.01			±0.008			±0.005	%
Gain vs. Temp. Gain<1000			5			5			5	ppm/°C
GAIN SENSE INPUT										
Gain Sense Current		300	**500**		150	**250**		50	**100**	nA
Gain Sense Offset Current		150	**500**		75	**250**		50	**100**	nA
VOLTAGE OFFSET (May be Nulled)										
Input Offset Voltage		50	**200**		25	**50**		10	**25**	µV
Output Offset Voltage		4	**5**		2	**3**		1	**2**	mV
Offset Referred to the Input vs. Supply										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	85	95		90	100		95	105		dB
G = 100	95	100		105	110		110	120		dB
G = 1000	**100**	110		**110**	120		**115**	140		dB
INPUT CURRENT										
Input Bias Current		±30	**±50**		±20	**±25**		±10	**±15**	nA
Input Offset Current		±2	**±35**		±1	**±15**		±1	**±5**	nA
INPUT										
Input Impedance										
Differential Resistance		1			1			1		GΩ
Differential Capacitance		4			4			4		pF
Input Voltage Range										
Differ. Input Linear (V_{DL})[2]	±10			±10			±10			V
Common-Mode Linear (V_{CM})		$12\,V-\left(\frac{G}{2}\times V_D\right)$			$12\,V-\left(\frac{G}{2}\times V_D\right)$			$12\,V-\left(\frac{G}{2}\times V_D\right)$		
Common-Mode Rejection Ratio dc to 60 Hz with 1 kΩ Source Imbalance										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	90	95		90	105		100	115		dB
G = 100	100	105		105	115		110	125		dB
G = 1000	**110**	115		**110**	125		**120**	140		dB
OUTPUT RATING		±10 V @ 5 mA			±10 V @ 5 mA			±10 V @ 5 mA		
DYNAMIC RESPONSE										
Small Signal –3 dB										
G = 1 (R_F = 20 kΩ)		650			650			650		kHz
G = 10		400			400			400		kHz
G = 100		150			150			150		kHz
G = 1000		25			25			25		kHz
Slew Rate		5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20 V Step										
G = 1 to 200		15			15			15		µs
G = 500		35			35			35		µs
G = 1000		75			75			75		µs
NOISE										
Voltage Noise, 1 kHz										
R.T.I.		4			4			4		nV/√Hz
R.T.O.		75			75			75		nV/√Hz
R.T.I., 0.1 Hz to 10 Hz										
G = 1		10			10			10		µV p-p
G = 10		1.0			1.0			1.0		µV p-p
G = 100		0.3			0.3			0.3		µV p-p
G = 1000		0.2			0.2			0.2		µV p-p
Current Noise										
0.1 Hz to 10 Hz		60			60			60		pA p-p
SENSE INPUT										
R_{IN}		10			10			10		kΩ
I_{IN}		30			30			30		µA
Voltage Range	±10			±10			±10			V
REFERENCE INPUT										
R_{IN}		20			20			20		kΩ
I_{IN}		30			30			30		µA
Voltage Range	±10			±10			±10			V
POWER SUPPLY										
Power Supply Range		±6 to ±18			±6 to ±18			±6 to ±18		V
Quiescent Current		3.5	5		3.5	5		3.5	5	mA

Specifications subject to change without notice.

Low Cost, Single Supply Differential Amplifier

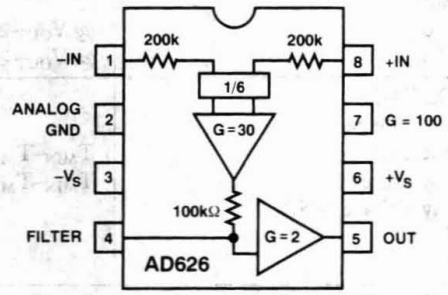
AD626

FEATURES
- Pin Selectable Gains of 10 and 100
- True Single Supply Operation
  - Single Supply Range of +2.4 V to +10 V
  - Dual Supply Range of ±1.2 V to ±6 V
  - Wide Output Voltage Range of 30 mV to 4.7 V
- Optional Low-Pass Filtering
- Excellent DC Performance
  - Low Input Offset Voltage: 500 μV max
  - Large Common-Mode Range: 0 V to +54 V
  - Low Power: 1.2 mW (V_S = +5 V)
  - Good CMR of 90 dB typ
- AC Performance
  - Fast Settling Time: 24 μs (0.01%)
- Includes Input Protection
  - Series Resistive Inputs (R_{IN} = 200 kΩ)
  - RFI Filters Included
  - Allows 50 V Continuous Overload

APPLICATIONS
- Current Sensing
- Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N) and SOIC (R) Packages



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD626AN	–40°C to +85°C	N-8
AD626AR	–40°C to +85°C	R-8
AD626BN	–40°C to +85°C	N-8

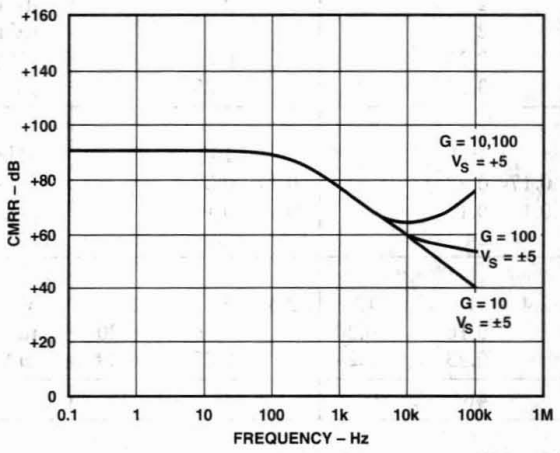
*N = Plastic DIP; R = Small Outline IC. For outline information see Package Information section.

7

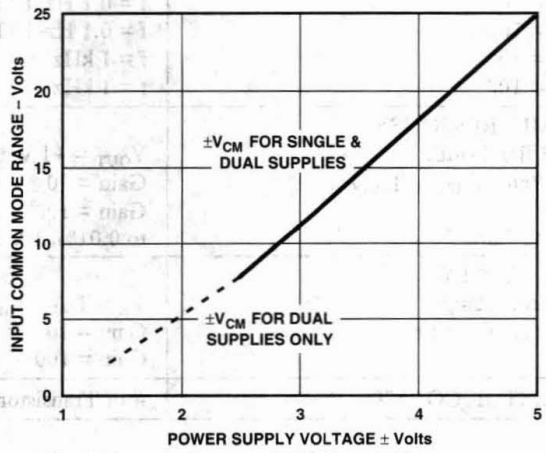
PRODUCT DESCRIPTION

The AD626 is a low cost, true single supply differential amplifier designed for amplifying and low-pass filtering small differential voltages from sources having a large common-mode voltage. It can operate from either a single supply of +2.4 V to +10 V, or dual supplies of ±1.2 V to ±6 V. The input common-mode range of this amplifier is equal to 6 ($+V_S$ – 1 V) which provides a +24 V CMR while operating from a +5 V supply. Furthermore, the AD626 features a CMR of 90 dB typ.

The amplifier's inputs are protected against continuous overload of up to 50 V, and RFI filters are included in the attenuator network. The amplifier provides a preset gain of 10, but gains between 10 to 100 can be easily configured with an external resistor. Furthermore, a gain of 100 is available by connecting the G = 100 pin to analog ground. The AD626 also offers low-pass filter capability by connecting a capacitor between the filter pin and analog ground.



Common-Mode Rejection vs. Frequency



Input Common-Mode Range vs. Supply

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD626–SPECIFICATIONS

SINGLE SUPPLY (@ $+V_S$ = +5 V and T_A = +25°C)

Model / Parameter	Condition	AD626A Min	AD626A Typ	AD626A Max	AD626B Min	AD626B Typ	AD626B Max	Units
GAIN								
Gain Accuracy	Total Error							
Gain = 10	@ $V_{OUT} \geq 100$ mV dc		0.04	1.0		0.2	0.6	%
Gain = 100	@ $V_{OUT} \geq 100$ mV dc		0.1	1.0		0.5	0.6	%
Over Temperature, $T_A = T_{MIN}$–T_{MAX}	G = 10			50			30	ppm/°C
	G = 100			150			120	ppm/°C
Gain Linearity								
Gain = 10	@ $V_{OUT} \geq 100$ mV dc		0.014	0.016		0.014	0.016	%
Gain = 100	@ $V_{OUT} \geq 100$ mV dc		0.014	0.02		0.014	0.02	%
OFFSET VOLTAGE								
Input Offset Voltage			1.9	2.5		1.9	2.5	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			2.9			2.9	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			6			6	µV/°C
vs. Supply Voltage (PSR)								
+PSR		74	80		74	80		dB
–PSR		64	66		64	66		dB
COMMON-MODE REJECTION	R_L = 10 kΩ							
+CMR Gain = 10, 100	f = 100 Hz, V_{CM} = +24 V	66	90		80	90		dB
±CMR Gain = 10, 100	f = 10 kHz, V_{CM} = 6 V	55	64		55	64		dB
–CMR Gain = 10, 100[1]	f = 100 Hz, V_{CM} = –2 V	60	85		73	85		dB
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	CMR > 85 dB		+24			+24		V
–CMV Gain = 10	CMR > 85 dB		–2			–2		V
INPUT								
Input Resistance								
Differential			200			200		kΩ
Common Mode			100			100		kΩ
Input Voltage Range (Common Mode)			6 (V_S – 1)			6 (V_S – 1)		V
OUTPUT								
Output Voltage Swing	R_L = 10 kΩ							
Positive	Gain = 10	4.7	4.90		4.7	4.90		V
	Gain = 100	4.7	4.90		4.7	4.90		V
Negative	Gain = 10	0.03			0.03			V
	Gain = 100	0.03			0.03			V
Short Circuit Current								
$+I_{SC}$			12			12		mA
NOISE								
Voltage Noise RTI								
Gain = 10	f = 0.1 Hz–10 Hz		2			2		µV p-p
Gain = 100	f = 0.1 Hz–10 Hz		2			2		µV p-p
Gain = 10	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
Gain = 100	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
DYNAMIC RESPONSE								
–3 dB Bandwidth	V_{OUT} = +1 V dc		100			100		kHz
Slew Rate, T_{MIN} to T_{MAX}	Gain = 10	0.17	0.22		0.17	0.22		V/µs
	Gain = 100	0.1	0.17		0.1	0.17		V/µs
Settling Time	to 0.01%, 1 V Step		24			22		µs
POWER SUPPLY								
Operating Range	$T_A = T_{MIN}$–T_{MAX}	2.4	5	12	2.4	5	10	V
Quiescent Current	Gain = 10		0.16	0.20		0.16	0.20	mA
	Gain = 100		0.23	0.29		0.23	0.29	mA
TRANSISTOR COUNT	# of Transistors		46			46		

NOTES

[1]At temperatures above +25°C, –CMV degrades at the rate of 12 mV/°C; i.e., @ +25°C CMV = –2 V, @ +85°C CMV = –1.28 V.

Specifications subject to change without notice.

Single-Supply Sensor Interface Amplifier

AD22050*

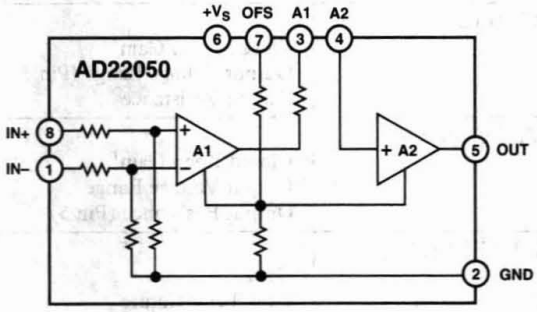
FEATURES

Gain of ×20. Alterable from ×1 to ×160
Input CMR from Below Ground to 6× (V_S – 1 V)
Output Span 20 mV to (V_S – 0.2) V
1-, 2-, 3-Pole Low-Pass Filtering Available
Accurate Midscale Offset Capability
Differential Input Resistance 400 kΩ
Drives 1 kΩ Load to +4 V Using V_S = +5 V
Supply Voltage: +3.0 V to +36 V
Transient Spike Protection & RFI Filters Included
Peak Input Voltage (40 ms): 60 V
Reversed Supply Protection: –34 V
Operating Temperature Range: –40°C to +125°C

APPLICATIONS

Current Sensing
Motor Control
Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD22050 is a single-supply difference amplifier for amplifying and low-pass filtering small differential voltages (typically 100 mV FS at a gain of 40) from sources having a large common-mode voltage.

Supply voltages of between +3.0 V and +36 V can be used. The input common-mode range extends from below ground to +24 V using a +5 V supply with excellent rejection of this common-mode voltage. This is achieved by the use of a special resistive attenuator at the input, laser trimmed to a very high differential balance.

Provisions are included for optional low-pass filtering and gain adjustment. An accurate midscale offset feature allows bipolar signals to be amplified.

***Patents pending.**

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD22050N	–40°C to +125°C	N-8
AD22050R	–40°C to +125°C	R-8
AD22050R-Reel[2]	–40°C to +125°C	R-8

NOTES
[1]N = Plastic DIP; R = Plastic SOIC. For outline information see Package Information section.
[2]Tape and reel quantities must be in increments of 1,000 pieces each.

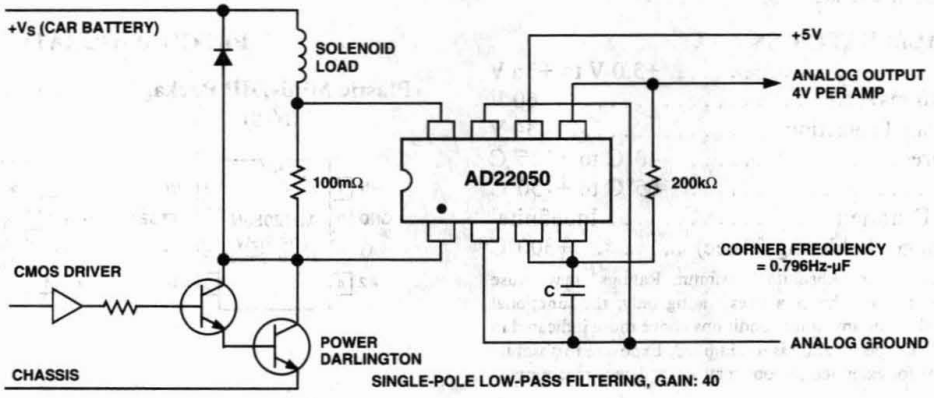


Figure 1. Typical Application Circuit for a Current Sensor Interface

AD22050–SPECIFICATIONS (T_A = +25°C, V_S = +5 V, and V_{CM} = 0 unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
INPUTS (Pins 1 and 8)						
+CMR	Positive Common-Mode Range	$T_A = T_{MIN}$ to T_{MAX}			+24	V
–CMR	Negative Common-Mode Range	$T_A = T_{MIN}$ to +85°C	–1.0			V
$CMRR_{LF}$	Common-Mode Rejection Ratio	f ≤ 10 Hz	**80**	90		dB
$CMRR_{HF}$	Common-Mode Rejection Ratio	f = 10 kHz	**60**	75		dB
R_{INCM}	Common-Mode Input Resistances	Pin 1 or Pin 8 to Pin 2	200	250	300	kΩ
R_{MATCH}	Matching of Resistances			±0.5		%
R_{INDIFF}	Differential Input Resistance	Pin 1 to Pin 8	350	450		kΩ
PREAMPLIFIER						
G_{CL}	Closed-Loop Gain[1]		9.7	10.0	10.3	
V_O	Output Voltage Range (Pin 3)		+0.01		+4.8	V
R_O	Output Resistance[2]		**97**	100	**103**	kΩ
OUTPUT BUFFER						
G_{CL}	Closed-Loop Gain[1]	$R_{LOAD} \geq 10$ kΩ	**1.94**	2.0	**2.06**	
V_O	Output Voltage Range	$T_A = T_{MIN}$ to T_{MAX}	**+0.02**		**+4.8**	V
R_O	Output Resistance (Pin 5)	V_O > 0.1 V dc		0.2		Ω
OVERALL SYSTEM						
G	Gain[1]	$V_O \geq 0.1$ V dc	**19.9**	20.0	**20.1**	
	Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	19.8		20.2	
V_{OS}	Initial Offset Voltage[3]		**–1**	0.03	**1**	mV
	Over Temperature	$T_A = T_{MIN}$ to T_{MAX}	–3		3	mV
OFS	Midscale Offset (Pin 7) Scaling[4]		**0.49**	0.50	**0.51**	
	Input Resistance	Pin 7 to Pin 2	2.5		3.0	kΩ
Iosc	Short-Circuit Output Current	$T_A = T_{MIN}$ to T_{MAX}	7	11	25	mA
$BW_{-3\ dB}$	–3 dB Bandwidth	V_O = +1 V dc	20	30		kHz
SR	Slew Rate			0.2		V/µs
N_{SD}	Noise Spectral Density[3]	f = 100 Hz to 10 kHz		0.2		µV/√Hz
POWER SUPPLY						
V_S	Operating Range	$T_A = T_{MIN}$ to T_{MAX}	3.0	5	36	V
I_S	Quiescent Supply Current[5]	T_A = +25°C, V_S = +5 V		200	**500**	µA
TEMPERATURE RANGE						
T_{OP}	Operating Temperature Range		–40		+125	°C
PACKAGE	Plastic Mini-DIP (N-8)			AD22050N		
	Plastic SOIC (R-8)			AD22050R		

NOTES

[1]Specified for default mode, i.e., with no external components. The overall gain is trimmed to 1% while the individual gains of A1 and A2 may be subject to a maximum ±3% tolerance. Note that the actual gain in a particular application can be modified by the use of external resistor networks.

[2]The actual output resistance of A1 is only a few ohms, but access to this output, via Pin 3, is always through the resistor R12 (see Figure 2) which is 100 kΩ, trimmed to ±3%.

[3]Referred to the input (Pins 1 and 8).

[4]The midscale offset scaling factor determines the fraction of voltage applied to Pin 7 which appears at the output. For example, with Pin 7 tied to Pin 6 and V_S = +5 V, the output will be offset to +2.5 V ±5 mV. The designer should be aware that the impedance at Pin 7, OFS, is 4 kΩ. Care should be taken so that the steady-state voltage at this pin does not cause the package to dissipate too much power. We recommend that the continuous V_S stay below +20 V when it is connected to the OFS pin.

[5]With V_{DM} = 0 V. Differential mode signals are referred to as V_{DM}, while V_{CM} refers to common-mode voltages—see the section *Product Description* and Figure 3.

All min and max specifications are guaranteed, although only those marked in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

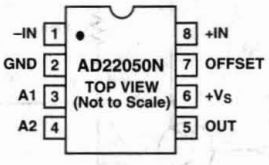
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... +3.0 V to +36 V
Peak Input Voltage (40 ms) ..... 60 V
Reversed Supply Voltage Protection ..... –34 V
Operating Temperature ..... –40°C to +125°C
Storage Temperature ..... –65°C to +150°C
Output Short Circuit Duration ..... Indefinite
Lead Temperature Range (Soldering 60 sec) ..... +300°C

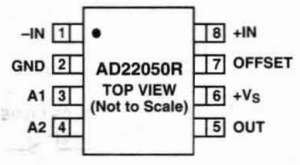
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS

Plastic Mini-DIP Package (N-8)



Plastic SOIC Package (R-8)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD22050 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ANALOG DEVICES

Single-Supply Sensor Interface Amplifier

AD22057*

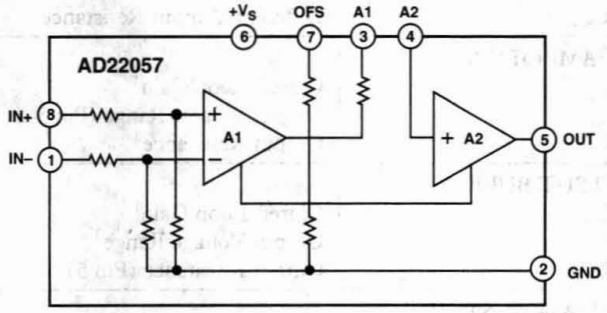
FEATURES

Gain of ×20, Alterable from ×1 to ×160
Input Offset Voltage Over Temperature ±2 mV
Low Long-Term Drift of Gain and Offset Voltage
Input CMR from Ground to 6× (V_S – 1 V)
Output Span 20 mV to (V_S – 0.25) V
1, 2, 3 Pole Low-Pass Filtering Available
Accurate Midscale Offset Capability
Differential Input Resistance 400 kΩ
Drives 1 kΩ Load to +4 V Using V_S = +5 V
Supply Voltage: +3 V to +36 V
Transient Spike Protection and RFI Filters Included
Peak Input Voltage
Reversed Supply Protection: –34 V
Operating Temperature Range: –40°C to +125°C

APPLICATIONS

Current Sensing
Motor Control
Interface for Accelerometers, Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD22057 is a single-supply difference amplifier for the amplification and low-pass filtering of small differential voltages from sources having a large common-mode voltage.

Supply voltages from +3 V to +36 V can be used. The input common-mode range extends from below ground to 24 V using a +5 V supply with excellent rejection of this common-mode voltage.

This range is achieved by the use of a special resistive attenuator at the input, laser trimmed to a very high differential balance. Low initial offset voltage and offset voltage drift are specified, and long-term stability of gain and offset voltage is also provided.

Provisions are included for optional low-pass filtering and gain adjustment. An accurate midscale offset feature allows bipolar signals to be amplified.

***Protected by U.S. Patent No. 5,043,675.**

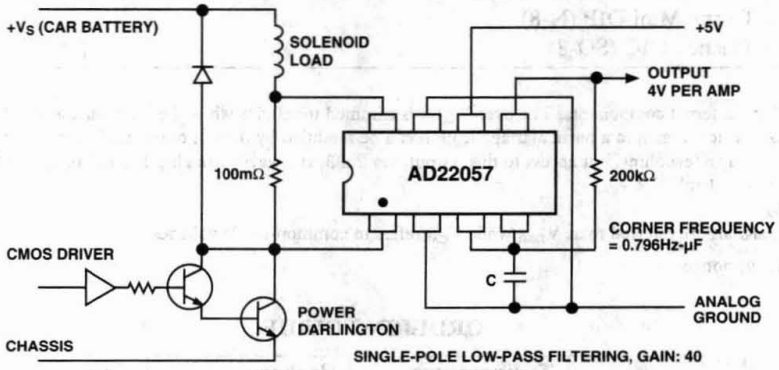


Figure 1. Typical Application Circuit for a Current Sensor Interface

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD22057–SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, V_{CM} = 0, R_L = 10 kΩ unless otherwise noted)

Parameter	Comments	Test Conditions	Min	Typ	Max	Units
INPUTS (PINS 1 AND 8)						
+CMR	Positive Common-Mode Range				+24	V
CMR	Negative Common-Mode Range	$T_A = T_{MIN}$ to +85°C	–1.0			V
$CMRR_{LF}$	Common-Mode Rejection Ratio	f ≤ 10 Hz	80	90		dB
$CMRR_{HF}$	Common-Mode Rejection Ratio	f = 1 kHz	80	90		dB
R_{INCM}	Common-Mode Input Resistance	Pin 1 or Pin 8 to Pin 2	180	240	300	kΩ
R_{MATCH}	Matching of Resistances			0.5		%
R_{INDIFF}	Differential Input Resistance	Pin 1 to Pin 8	280	400		kΩ
PREAMPLIFIER						
G_{CL}	Closed-Loop Gain[1]		9.7	10.0	10.3	V/V
V_O	Output Voltage Range (Pin 3)		+0.01		+4.8	V
R_O	Output Resistance[2]		97	100	103	kΩ
OUTPUT BUFFER						
G_{CL}	Closed-Loop Gain[1]	$R_{LOAD} \geq 10$ kΩ	1.94	2.0	2.06	V/V
V_O	Output Voltage Range[3]		+0.02		+4.8	V
R_O	Output Resistance (Pin 5)	$V_O \geq 0.1$ V dc, $I_O < 1$ mA		2.0		Ω
OVERALL SYSTEM						
G	Gain[1]	$V_O \geq 0.1$ V dc	19.9	20.0	20.1	V/V
	Gain Drift	$T_A = T_{MIN}$ to T_{MAX}	–62.5		+62.5	ppm/°C
V_{OS}	Input Offset Voltage[4]		–1	0.03	1	mV
	Offset Drift	$T_A = T_{MIN}$ to T_{MAX}	–12.5		+12.5	µV/°C
OFS	Midscale Offset (Pin 7) Scaling		0.49	0.50	0.51	V/V
	Input Resistance	Pin 7 to Pin 2	2.5	3.0		kΩ
I_{OSC}	Short-Circuit Output Current		7	11	25	mA
		$T_A = T_{MIN}$ to T_{MAX}	5		27	mA
$BW_{-3\ dB}$	–3 dB Bandwidth	V_O = +1 V dc		30		kHz
SR	Slew Rate			0.2		V/µs
N_{SD}	Noise Spectral Density[4]	f = 100 Hz to 10 kHz		0.2		µV/√Hz
PSR		V_S = 5 V, V_O = 1 V to 4.2 V				
		V_S = 24 V, V_O = 1 V to 22 V				
		$T_A = T_{MIN}$ to T_{MAX}				
Offset					20.0	µV/V
Gain					0.05	%/V
POWER SUPPLY						
V_S	Operating Range	$T_A = T_{MIN}$ to T_{MAX}	3	5	36	V
I_S	Quiescent Supply Range[5]	T_A = +25°C, V_S = +5 V		200	500	µA
TEMPERATURE RANGE						
T_{OP}	Operating Temperature Range		–40		+105	°C
PACKAGE	Plastic Mini-DIP (N-8) Plastic SOIC (SO-8)			AD22057N AD22057R		

PRELIMINARY TECHNICAL DATA

NOTES

[1]Specified for default mode i.e., with no external components. The overall gain is trimmed to ±0.5% while the individual gains of A1 and A2 may be subject to a maximum ±3% tolerance. Note that the actual gain in a particular application can be modified by the use of external resistor networks.

[2]The actual output resistance of A1 is only a few ohms, but access to this output, via Pin 3, is always through a 100 kΩ resistor, which is trimmed to ±3%.

[3]For $V_{CM} \leq 20$ V. For $V_{CM} > 20$ V, $V_{OL} \simeq 1$ mV/V × V_{CM}.

[4]Referred to the input (Pins 1 and 8).

[5]With V_{DM} = 0 V. Differential mode signals are referred to as V_{DM}, while V_{CM} refers to common-mode voltages.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD22057N	–40°C to +105°C	Plastic Mini-DIP	N-8
AD22057R	–40°C to +105°C	Plastic SOIC	SO-8

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Noise, Precision Instrumentation Amplifier

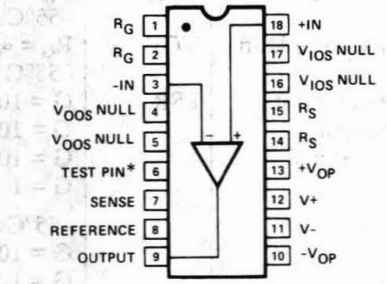
AMP01

FEATURES

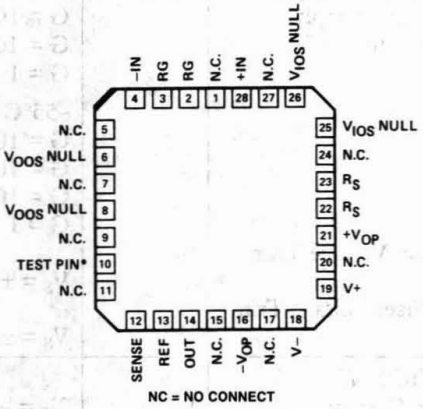
Low Offset Voltage: 50 μV max
Very Low Offset Voltage Drift: 0.3 μV/°C max
Low Noise: 0.12 μV p-p (0.1 Hz to 10 Hz)
Excellent Output Drive: ±10 V at ±50 mA
Capacitive Load Stability: to 1 μF
Gain Range: 0.1 to 10,000
Excellent Linearity: 16-Bit at G = 1000
High CMR: 125 dB min (G = 1000)
Low Bias Current: 4 nA max
May be Configured as a Precision Op Amp
Output-Stage Thermal Shutdown
Available in Die Form

PIN CONFIGURATIONS

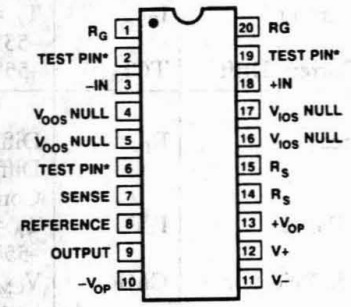
18-Pin Hermetic DIP (X Suffix)



AMP01 BTC/883
28-Lead LCC (TC Suffix)



20-Pin SOL (S Suffix)



GENERAL DESCRIPTION

The AMP01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high current output stage. The output remains stable with high capacitance loads (1 μF), a unique ability for an instrumentation amplifier. Consequently, the AMP01 can amplify low level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (20 μV) which generally eliminates the external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically 0.15 μV/°C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10 nA over the military temperature range. High common-mode rejection of 130 dB, 16-bit linearity at a gain of 1000, and 50 mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb dc specifications. The AMP01 slews at 4.5 V/μs into capacitive loads of up to 15 nF, settles in 50 μs to 0.01% at a gain of 1000, and boasts a healthy 26 MHz gain-bandwidth product. These features make the AMP01 ideal for high speed data-acquisition systems.

Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain-temperature-coefficient of 10 ppm/°C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50 Ω, 500 Ω, and 2 kΩ. Loaded with 500 Ω, the output delivers ±13.0 V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP01 can also be configured as a high performance operational amplifier. In many applications, the AMP01 can be used in place of op amp/power-buffer combinations.

ORDERING GUIDE*

Model	Temperature Range	Package Description
AMP01AX	–55°C to +125°C	18-Pin Cerdip
AMP01BX	–55°C to +125°C	18-Pin Cerdip
AMP01BTC/883	–55°C to +125°C	28-Lead LCC
AMP01EX	–25°C to +85°C	18-Pin Cerdip
AMP01FX	–25°C to +85°C	18-Pin Cerdip
AMP01GS	0°C to +70°C	20-Pin SOL

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AMP01–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, R_S = 10 kΩ, R_L = 2 kΩ, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	AMP01A Min	AMP01A Typ	AMP01A Max	AMP01B Min	AMP01B Typ	AMP01B Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = +25°C		20	50		40	100	µV
		−55°C ≤ T_A ≤ +125°C		40	80		60	150	µV
Input Offset Voltage Drift	TCV_{IOS}	−55°C ≤ T_A ≤ +125°C		0.15	0.3		0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	T_A = +25°C		1	3		2	6	mV
		−55°C ≤ T_A ≤ +125°C		3	6		6	10	mV
Output Offset Voltage Drift	TCV_{OOS}	R_G = ∞							
		−55°C ≤ T_A ≤ +125°C		20	50		50	120	µV/°C
Offset Referred to Input vs. Positive Supply V+ = +5 V to +15 V	PSR	G = 1000	120	130		110	120		dB
		G = 100	110	130		100	120		dB
		G = 10	95	110		90	100		dB
		G = 1	75	90		70	80		dB
		−55°C ≤ T_A ≤ +125°C							
		G = 1000	120	130		110	120		dB
		G = 100	110	130		100	120		dB
		G = 10	95	110		90	100		dB
		G = 1	75	90		70	80		dB
Offset Referred to Input vs. Negative Supply V− = −5 V to −15 V	PSR	G = 1000	105	125		105	115		dB
		G = 100	90	105		90	95		dB
		G = 10	70	85		70	75		dB
		G = 1	50	65		50	60		dB
		−55°C ≤ T_A ≤ +125°C							
		G = 1000	105	125		105	115		dB
		G = 100	90	105		90	95		dB
		G = 10	70	85		70	75		dB
		G = 1	50	85		50	60		dB
Input Offset Voltage Trim Range		V_S = ±4.5 V to ±18 V		±6			±6		mV
Output Offset Voltage Trim Range		V_S = ±4.5 V to ±18 V		±100			±100		mV
INPUT CURRENT									
Input Bias Current	I_B	T_A = +25°C		1	4		2	6	nA
		−55°C ≤ T_A ≤ +125°C		4	10		6	15	nA
Input Bias Current Drift	TCI_B	−55°C ≤ T_A ≤ +125°C		40			50		pA/°C
Input Offset Current	I_{OS}	T_A = +25°C		0.2	1.0		0.5	2.0	nA
		−55°C ≤ T_A ≤ +125°C		0.5	3.0		1.0	6.0	nA
Input Offset Current Drift	TCI_{OS}	−55°C ≤ T_A ≤ +125°C		3			5		pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000		1			1		GΩ
		Differential, G ≤ 100		10			10		GΩ
		Common Mode, G = 1000		20			20		GΩ
Input Voltage Range	IVR	T_A = +25°C	±10.5			±10.5			V
		−55°C ≤ T_A ≤ +125°C	±10.0			±10.0			V
Common-Mode Rejection	CMR	V_{CM} = ±10 V, 1 kΩ Source Imbalance							
		G = 1000	125	130		115	125		dB
		G = 100	120	130		110	125		dB
		G = 10	100	120		95	110		dB
		G = 1	85	100		75	90		dB
		−55°C ≤ T_A ≤ +125°C							
		G = 1000	120	125		110	120		dB
		G = 100	115	125		105	120		dB
		G = 10	95	115		90	105		dB
		G = 1	80	95		75	90		dB

NOTES

For grade E and F specifications, request complete data sheet.

Specifications subject to change without notice.

High Accuracy 8-Pin Instrumentation Amplifier

AMP02

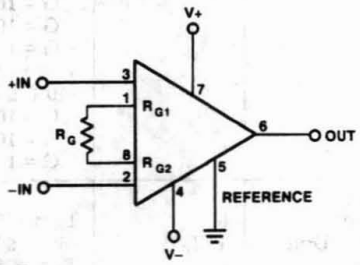
FEATURES

Low Offset Voltage: 100 μV max
Low Drift: 2 μV/°C max
Wide Gain Range 1 to 10,000
High Common-Mode Rejection: 115 dB min
High Bandwidth (G = 1000): 200 kHz typ
Gain Equation Accuracy: 0.5% max
Single Resistor Gain Set
Input Overvoltage Protection
Low Cost
Available In Die Form

APPLICATIONS

Differential Amplifier
Strain Gauge Amplifier
Thermocouple Amplifier
RTD Amplifier
Programmable Gain Instrumentation Amplifier
Medical Instrumentation
Data Acquisition Systems

BASIC CIRCUIT CONNECTIONS

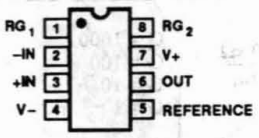


$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{50k\Omega}{R_G}\right) + 1$$

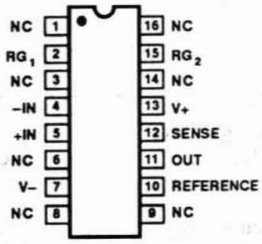
FOR SOL CONNECT SENSE TO OUTPUT

PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix) and Cerdip (Z Suffix)



16-Pin SOL (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The AMP02 is the first precision instrumentation amplifier available in an 8-pin package. Gain of the AMP02 is set by a single external resistor, and can range from 1 to 10,000. No gain set resistor is required for unity gain. The AMP02 includes an input protection network that allows the inputs to be taken 60 V beyond either supply rail without damaging the device.

Laser trimming reduces the input offset voltage to under 100 μV. Output offset voltage is below 4 mV and gain accuracy is better than 0.5% for gain of 1000. PMI's proprietary thin-film resistor process keeps the gain temperature coefficient under 50 ppm/°C.

Due to the AMP02's design, its bandwidth remains very high over a wide range of gain. Slew rate is over 4 V/μs making the AMP02 ideal for fast data acquisition systems.

A reference pin is provided to allow the output to be referenced to an external dc level. This pin may be used for offset correction or level shifting as required. In the 8-pin package, sense is internally connected to the output.

For an instrumentation amplifier with the highest precision, consult the AMP01 data sheet. For the highest input impedance and speed, consult the AMP05 data sheet.

ORDERING GUIDE

Model	V_{IOS} max @ T_A = +25°C	V_{OOS} max @ T_A = +25°C	Temperature Range	Package Description*
AMP02EP	100 μV	4 mV	–40°C to +85°C	8-Pin Plastic DIP
AMP02FP	200 μV	8 mV	–40°C to +85°C	8-Pin Plastic DIP
AMP02AZ/883C	200 μV	10 mV	–55°C to +125°C	8-Pin Cerdip
AMP02FS	200 μV	8 mV	–40°C to +85°C	16-Pin SOIC
AMP02GBC				Die
AMP02FS-REEL	200 μV	8 mV	–40°C to +85°C	16-Pin SOIC

*For outline information see Package Information section.

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AMP02–SPECIFICATIONS (@ V_S = ±15 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	AMP02E Min	AMP02E Typ	AMP02E Max	AMP02F Min	AMP02F Typ	AMP02F Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	T_A = +25°C		20	100		40	200	µV
		–40°C ≤ T_A ≤ +85°C		50	200		100	350	µV
Input Offset Voltage Drift	TCV_{IOS}	–40°C ≤ T_A ≤ +85°C		0.5	2		1	4	µV/°C
Output Offset Voltage	V_{OOS}	T_A = +25°C		1	4		2	8	mV
		–40°C ≤ T_A ≤ +85°C		4	10		9	20	mV
Output Offset Voltage Drift	TCV_{OOS}	–40°C ≤ T_A ≤ +85°C		50	100		100	200	µV/°C
Power Supply Rejection	PSR	V_S = ±4.8 V to ±18 V							
		G = 100, 1000	115	125		110	115		dB
		G = 10	100	110		95	100		dB
		G = 1	80	90		75	80		dB
		V_S = ±4.8 V to ±18 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 1000, 100	110	120		105	110		dB
		G = 10	95	110		90	95		dB
		G = 1	75	90		70	75		dB
INPUT CURRENT									
Input Bias Current	I_B	T_A = +25°C		2	10		4	20	nA
Input Bias Current Drift	TCI_B	–40°C ≤ T_A ≤ +85°C		150			250		pA/°C
Input Offset Current	I_{OS}	T_A = +25°C		1.2	5		2	10	nA
Input Offset Current Drift	TCI_{OS}	–40°C ≤ T_A ≤ +85°C		9			15		pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G ≤ 1000		10			10		GΩ
		Common-Mode, G = 1000		16.5			16.5		GΩ
Input Voltage Range	IVR	T_A = +25°C (Note 1)	±11			±11			V
Common-Mode Rejection	CMR	V_{CM} = ±11 V							
		G = 1000, 100	115	120		110	115		dB
		G = 10	100	115		95	110		dB
		G = 1	80	95		75	90		dB
		V_{CM} = ±11 V							
		–40°C ≤ T_A ≤ +85°C							
		G = 100, 1000	110	120		105	115		dB
		G = 10	95	110		90	105		dB
		G = 1	75	90		70	85		dB
GAIN									
Gain Equation Accuracy	$G = \frac{50\ k\Omega}{R_G} + 1$	G = 1000			0.50			0.70	%
		G = 100			0.30			0.50	%
		G = 10			0.25			0.40	%
		G = 1			0.02			0.05	%
Gain Range	G		1		10k	1		10k	V/V
Nonlinearity		G = 1 to 1000		0.006			0.006		%
Temperature Coefficient	G_{TC}	1 ≤ G ≤ 1000 (Notes 2, 3)		20	50		20	50	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	R_L = 1 kΩ	±12	±13		±12	±13		V
Positive Current Limit		Output-to-Ground Short		22			22		mA
Negative Current Limit		Output-to-Ground Short		32			32		mA
NOISE									
Voltage Density, RTI	e_n	f_O = 1 kHz							
		G = 1000		9			9		nV/√Hz
		G = 100		10			10		nV/√Hz
		G = 10		18			18		nV/√Hz
		G = 1		120			120		nV/√Hz
Noise Current Density, RTI	i_n	f_O = 1 kHz, G = 1000		0.4			0.4		pA/√Hz
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz							
		G = 1000		0.4			0.4		µV p-p
		G = 100		0.5			0.5		µV p-p
		G = 10		1.2			1.2		µV p-p
		G = 1		10			10		µV p-p
DYNAMIC RESPONSE									
Small-Signal Bandwidth (–3 dB)	BW	G = 1		1200			1200		kHz
		G = 10		300			300		kHz
		G = 100, 1000		200			200		kHz
Slew Rate	SR	G = 10, R_L = 1 kΩ	4	6		4	6		V/µs
Settling Time	t_S	To 0.01% ±10 V Step		10			10		µs
		G = 1 to 1000							
POWER SUPPLY									
Supply Voltage Range	V_S		±4.5		±18	±4.5		±18	V
Supply Current	I_{SY}			5	6		5	6	mA

NOTES

[1]Input voltage range guaranteed by common-mode rejection test.

[2]Guaranteed by design.

[3]Gain tempco does not include the effects of external component drift.

Specifications subject to change without notice.

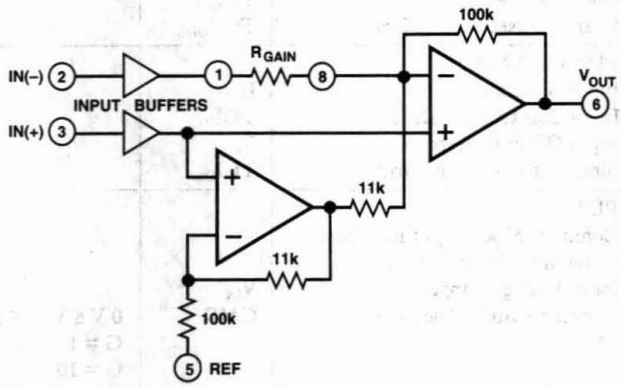
Precision Single Supply Instrumentation Amplifier

AMP04*

FEATURES
- Single Supply Operation
- Low Supply Current: 700 μA max
- Wide Gain Range: 1 to 1000
- Low Offset Voltage: 150 μV max
- Zero-In/Zero-Out
- Single-Resistor Gain Set
- 8-Pin Mini-DIP and SO Packages

APPLICATIONS
- Strain Gages
- Thermocouples
- RTDs
- Battery Powered Equipment
- Medical Instrumentation
- Data Acquisition Systems
- PC Based Instruments
- Portable Instrumentation

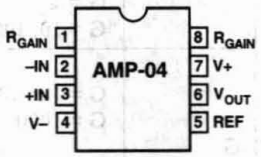
FUNCTIONAL BLOCK DIAGRAM



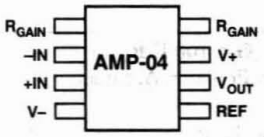
7

PIN CONNECTIONS

8-Lead Epoxy DIP (P Suffix)



8-Lead Narrow-Body SO (S Suffix)



GENERAL DESCRIPTION

The AMP04 is a single-supply instrumentation amplifier designed to work over a +5 volt to ±15 volt supply range. It offers an excellent combination of accuracy, low power consumption, wide input voltage range, and excellent gain performance.

Gain is set by a single external resistor and can be from 1 to 1000. Input common-mode voltage range allows the AMP04 to handle signals with full accuracy from ground to within 1 volt of the positive supply. And the output can swing to within 1 volt of the positive supply. Gain bandwidth is over 700 kHz. In addition to being easy to use, the AMP04 draws only 700 μA of supply current.

For high resolution data acquisition systems, laser trimming of low drift thin-film resistors limits the input offset voltage to under 150 μV, and allows the AMP04 to offer gain nonlinearity of 0.005% and a gain tempco of 30 ppm/°C.

*Protected by U.S. Patent No. 5,075,633.

A proprietary input structure limits input offset currents to less than 5 nA with drift of only 8 pA/°C, allowing direct connection of the AMP04 to high impedance transducers and other signal sources.

The AMP04 is specified over the extended industrial (–40°C to +85°C) temperature range. AMP04s are available in plastic and ceramic DIP plus SO-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

ORDERING GUIDE

Model	Temperature Range	V_{OS} @ +5 V T_A = +25°C	Package Description	Package Option*
AMP04EP	XIND	150 μV	Plastic DIP	N-8
AMPES	XIND	150 μV	SOIC	SO-8
AMP04FP	XIND	300 μV	Plastic DIP	N-8
AMP04FS	XIND	300 μV	SOIC	SO-8
AMP04FS-REEL	XIND	300 μV	SOIC	SO-8
AMP04FS-REEL7	XIND	300 μV	SOIC	SO-8
AMP04GBC	+25°C	300 μV		

*For outline information see Package Information section.

AMP04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +5 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	AMP04E Min	AMP04E Typ	AMP04E Max	AMP04F Min	AMP04F Typ	AMP04F Max	Units
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}			30	150			300	µV
Input Offset Voltage Drift	TCV_{IOS}				3			6	µV/°C
Output Offset Voltage	V_{OOS}			0.5	1.5			3	mV
Output Offset Voltage Drift	TCV_{OOS}				30			50	µV/°C
INPUT CURRENT									
Input Bias Current	I_B			22	30			40	nA
Input Bias Current Drift	TCI_B			65			65		pA/°C
Input Offset Current	I_{OS}			1	5			10	nA
Input Offset Current Drift	TCI_{OS}			8			8		pA/°C
INPUT									
Common-Mode Input Resistance				4			4		GΩ
Differential Input Resistance				4			4		GΩ
Input Voltage Range	V_{IN}		0		3.0	0		3.0	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.0 V							
		G = 1	60	80		55			dB
		G = 10	80	100		75			dB
		G = 100, 1000	90	105		80			dB
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 2.5 V −40°C ≤ T_A ≤ +85°C							
		G = 1	55			50			dB
		G = 10	75			70			dB
		G = 100, 1000	85			75			dB
Power Supply Rejection	PSRR	4.0 V ≤ V_S ≤ 12 V −40°C ≤ T_A ≤ +85°C							
		G = 1	95			85			dB
		G = 10, 100, 1000	105			95			dB
GAIN (G = 100 K/R_{GAIN})									
Gain Equation Accuracy		G = 1 to 100		0.2	0.5			0.75	%
		G = 1000		0.4			0.75		%
Gain Range	G		1		1000	1		1000	V/V
Nonlinearity		G = 1, R_L = 5 kΩ		0.005					%
		G = 10, R_L = 5 kΩ		0.015					%
		G = 100, R_L = 5 kΩ		0.025					%
Gain Temperature Coefficient	ΔG/ΔT			30			50		ppm/°C
OUTPUT									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	4.0	4.2		4.0			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ							
		−40°C ≤ T_A ≤ +85°C			2.0			2.5	mV
Output Current Limit		Sink		30			30		mA
		Source		15			15		mA
NOISE									
Noise Voltage Density, RTI	e_N	f = 1 kHz, G = 1		270			270		nV/√Hz
		f = 1 kHz, G = 10		45			45		nV/√Hz
		f = 100 Hz, G = 100		30			30		nV/√Hz
		f = 100 Hz, G = 1000		25			25		nV/√Hz
Noise Current Density, RTI	i_N	f = 100 Hz, G = 100		4			4		pA/√Hz
Input Noise Voltage	e_N p-p	0.1 to 10 Hz, G = 1		7			7		µV p-p
		0.1 to 10 Hz, G = 10		1.5			1.5		µV p-p
		0.1 to 10 Hz, G = 100		0.7			0.7		µV p-p
DYNAMIC RESPONSE									
Small Signal Bandwidth	BW	G = 1, −3 dB		300			300		kHz
POWER SUPPLY									
Supply Current	I_{SY}			550	700			700	µA
		−40°C ≤ T_A ≤ +85°C			850			850	µA

Specifications subject to change without notice.

Isolation Amplifiers
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Isolation Amplifiers–Selection Guide

Model	# Ports	Power Supply Volts	Power Supply mA	CMV @ 60 Hz V rms min	@ A_V = 1 @ 60 Hz dB min	Bandwidth A_V = 1 kHz	Linearity ±% max	Output Offset RTI +25°C ±mV max	TC ±µV max	Output Amplifier Yes	Output Amplifier No	# Pins	Page No.	Comments	Fax-code
A_V = 1 to 10															
AD215A	2	±15	40/18	750–1.5K	120	100	0.025	±80 ±2/A_V	±50 ±10/A_V	X		See D/S	8–9	Wide Bandwith, THD –80 dB, 1 kHz	1981
A_V = 1 to 100															
AD203S	2	+15	20	1500	106	10	0.025	±5 ±25/A_V	±6 ±100/A_V	X		See D/S	*		1084
AD102J	2	+15	5	500	100	1.5	0.05	±15 ±15/A_V	±10 ±10/A_V		X	See D/S	8–3		1819
AD202J	2	+15	5	750–1.5K	105	2	0.05	±15(5) ±15(5)/A_V	±10 ±10/A_V		X	See D/S	8–5	±5 ±5/A_V	1081
AD104J	2			500	100	4	0.05	±15(5) ±15(5)/A_V	±10 ±10/A_V		X	See D/S	8–3	Powered via ext Clk +15 V @ 25 kHz	1819
AD204J	2			750–1.5K	110	5	0.05	±15(5) ±15(5)/A_V	±10 ±10/A_V		X	See D/S	8–5	Powered via ext Clk +15 V @ 25 kHz	1081
AD210J	3	+15	50	1K–2K	120	20	0.025	±15 ±45/A_V	±10 ±50/A_V	X		See D/S	8–7		1089
A_V = 1 to 1000															
AD208A	2			750–1.5K	100	4	0.015–0.03	0.250 ±15/A_V	1 ±1.5 ±20/A_V		X	See D/S	*	Powered via ext Clk +15 V @ 25 kHz	1086
Note: AD246JY Clock Driver for AD104, AD204 or AD208													*	Specs & Pinout Given on Page 3 of AD202/AD204 Data Sheet	1081

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

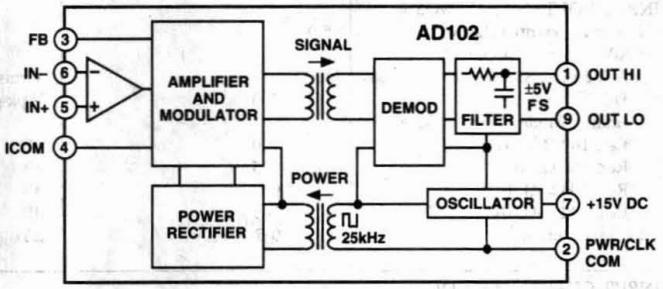
General Purpose Input Isolation Amplifiers

AD102/AD104

FEATURES
Integral Isolated Power Supply
500 V rms CMV Isolation Rating (100% Tested)
High Accuracy: ±0.05% Max Nonlinearity
Small SIP Style Footprint
Lowest Priced Isolation Amplifiers

APPLICATIONS
Single/Multichannel Data Acquisition Systems
Process Control Input Signal Isolation
Motor Control
Utility Power Monitoring
General Input Protection Circuits
Ground Loop Interruption

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD102 and AD104 are general purpose, two-port, isolation amplifiers suitable for use where input signal isolation is desired. Each offers a functionally complete, compact isolation solution rated at 500 V rms common mode, based upon the proven and reliable transformer-coupled, galvanic isolation technique used in all AD200 series isolation amplifier products.

Each model is offered in a minimum footprint package requiring no external components to operate. Though similar to the AD202 and AD204, the AD102 and AD104 models are intended as lower cost solutions where the performance of the AD202 or AD204 is not demanded.

Both the AD102 and AD104 can be used in applications where input-to-input and/or input-to-system isolation is desired. The AD102 is best suited for single input uses as it requires only +15 V dc power to operate. It may also be appropriate for multichannel applications when input-to-input isolation is not required such as where a single input multiplexer selects a specific channel prior to isolation.

For applications where input to input isolation is required, the AD104 may be a more desirable choice. It offers the lowest cost per channel especially when powered from a common clock source, the cost of which may be amortized over many channels.

The clock necessary for AD104 operation is a 25 kHz, 15 V p-p square wave applied to the clock input pin. Most standard oscillator components like a CD4047 or TL555 may be used, or a designer may choose the AD246 clock driver developed for the AD204 product.

ORDERING GUIDE*

Model	Package	Max CMV	Nonlinearity
AD102JY	SIP Style	500 V rms	0.05%
AD104JY	SIP Style	500 V rms	0.05%

*For outline information see Package Information section.

PIN DESIGNATIONS

Pin	Function
1	OUT HI
2	PWR/CLK COM
3	FB
4	ICOM
5	IN+
6	IN–
7	+15 V DC (AD102)
8	CLOCK INPUT (AD104)
9	OUT LO

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AD102/AD104–SPECIFICATIONS (@ T_A = +25°C and power supply of +15 V ± 5% unless otherwise noted)

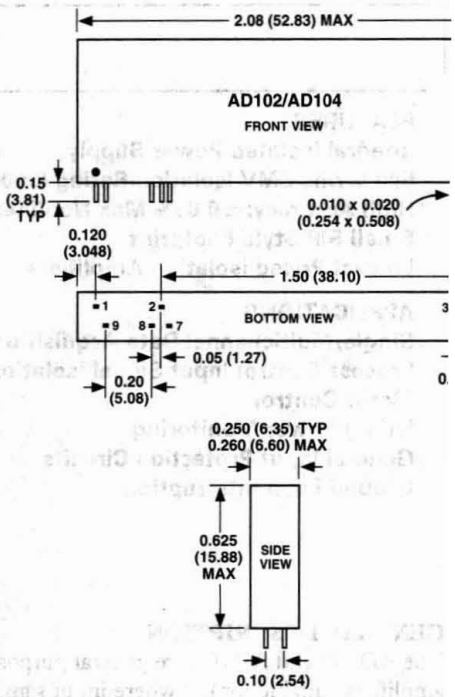
Parameter	Min	Typ	Max	Unit	Notes
ACCURACY					
Gain Range	1		100	V/V	
Unity Gain Error		±0.5	±5.0	%	
vs. Temperature		±45		ppm/°C	±100 ppm/°C max
vs. Time		±50		ppm	Per √1,000 Hours
vs. Supply Voltage, AD102[1]		±0.01		%/V	
vs. Supply Voltage, AD104[1]		±0.001		%/V	
Nonlinearity[2]			±0.05	%	
INPUT VOLTAGE RATINGS					
Linear Differential Range	±5.0			V	Between IN+ and IN–
CMV, Input to Output[2]					
AC, 60 Hz, Sinusoidal Waveform	500			V rms	100% Tested
DC		700		V pk-pk	
Common-Mode Rejection (CMR)					
$R_S \leq 100\ \Omega$, AD102[1]		100		dB	
$R_S \leq 100\ \Omega$, AD104[1]		105		dB	
$R_S \leq 1\ k\Omega$, AD102[1]		95		dB	
$R_S \leq 1\ k\Omega$, AD104[1]		105		dB	
Leakage Current		0.5		µA	2 µA max, In to Out, 240 V rms @ 60 Hz
INPUT CHARACTERISTICS					
Input Offset Voltage, Initial			(±15 ±15/G)	mV	+25°C
vs. Temperature		(±10 ±10/G)		µV/°C	0°C to +70°C
Input Bias Current, Initial		±100		pA	+25°C
vs. Temperature		±20		nA	0°C to +70°C
Input Difference Current, Initial		±10		pA	+25°C
vs. Temperature		±2		nA	0°C to +70°C
Input Voltage Noise					
0.1 Hz to 100 Hz		4		µV pk-pk	
f > 200 Hz		50		nV/√Hz	
Differential Input Impedance		10^{12}		Ω	
Common-Mode Input Impedance		2G‖5.5		Ω‖pF	
FREQUENCY RESPONSE					
Bandwidth, Full Power (–3 dB)					
AD102[1]		1.5		kHz	$V_{IN} \leq \pm 5$ V, G = 1–50 V/V
AD104[1]		4.0		kHz	$V_{IN} \leq \pm 5$ V, G = 1–50 V/V
Settling Time		1.0		ms	Time to ±10 mV from 10 V Step Input
RATED OUTPUT					
Output Voltage Range					
Between OUT HI and OUT LO	±5.0			V	
Between OUT HI or LO to PWR/ CLK COM		±6.5		V	
Output Resistance					
AD102[1]		8		kΩ	
AD104[1]		4		kΩ	
Output Ripple					
100 kHz Bandwidth		10		mV pk-pk	
5 kHz Bandwidth		0.5		mV rms	
POWER SUPPLY (AD102 ONLY)[1]					
Supply Voltage					
Rated Performance	+14.25	+15	+15.75	V dc	
Operational Performance	+13.5	+15	+16.5	V dc	
Supply Current		5		mA	
CLOCK OSCILLATOR (AD104 ONLY)[1]					
Source Voltage Amplitude	14.25	15	15.75	V p-p	±7.5 V Amplitude Within ±15 V Range
Square Wave Frequency		25		kHz	±5 kHz
Duty Cycle		50		% Hi vs. Low	±2%
TEMPERATURE RANGE					
Rated Performance	0		+70	°C	
Operating	–40		+85	°C	
Storage	–40		+85	°C	
PACKAGE DIMENSIONS					
SIP Style Package (Y)	2.08 × 0.260 × 0.625 in. (max)			Not Including Pin Length	

NOTES
[1]Specification(s) apply to one model only, either AD102 or AD104, as indicated.
[2]Nonlinearity is specified as a % deviation from a best fit straight line.
[3]All units 100% tested by "Partial Discharge" method @ 750 V rms for 5 sec, 150 pc maximum allowable discharge.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
PIN 7 IS ONLY PRESENT ON AD102
PIN 8 IS ONLY PRESENT ON AD104

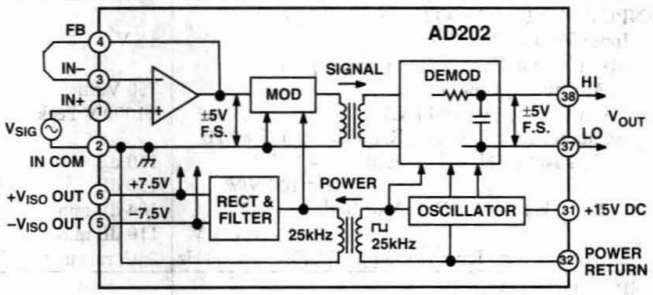
Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
- Small Size: 4 Channels/Inch
- Low Power: 35 mW (AD204)
- High Accuracy: ±0.025% max Nonlinearity (K Grade)
- High CMR: 130 dB (Gain = 100 V/V)
- Wide Bandwidth: 5 kHz Full-Power (AD204)
- High CMV Isolation: ±2000 V pk Continuous (K Grade) (Signal and Power)
- Isolated Power Outputs
- Uncommitted Input Amplifier

APPLICATIONS
- Multichannel Data Acquisition
- Current Shunt Measurements
- Motor Controls
- Process Signal Isolation
- High Voltage Instrumentation Amplifier

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD202 and AD204 are general purpose, two-port, transformer-coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a +15 V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver.

The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op amp on the input stage. They feature a bipolar ±5 V output range, an adjustable gain range of from 1 to 100 V/V, ±0.025% max nonlinearity (K grade), 130 dB of CMR and the AD204 consumes a low 35 mW of power.

ORDERING GUIDE

Model	Package Option	Max Common-Mode Voltage (Peak)	Max Linearity
AD202JY	SIP	1000 V	±0.05%
AD202KY	SIP	2000 V	±0.025%
AD202JN	DIP	1000 V	±0.05%
AD202KN	DIP	2000 V	±0.025%
AD204JY	SIP	1000 V	±0.05%
AD204KY	SIP	2000 V	±0.025%
AD204JN	DIP	1000 V	±0.05%
AD204KN	DIP	2000 V	±0.025%

PIN DESIGNATIONS

AD202/AD204 SIP Package

Pin	Function
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	–INPUT
4	INPUT FEEDBACK
5	$-V_{ISO}$ OUTPUT
6	$+V_{ISO}$ OUTPUT
31	+15 V POWER IN (AD202 ONLY)
32	CLOCK/POWER COMMON
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

AD202/AD204 DIP Package

Pin	Function
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	–INPUT
18	OUTPUT LO
19	OUTPUT HI
20	+15 V POWER IN (AD202 ONLY)
21	CLOCK INPUT (AD204 ONLY)
22	CLOCK/POWER COMMON
36	$+V_{ISO}$ OUTPUT
37	$-V_{ISO}$ OUTPUT
38	INPUT FEEDBACK

8

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AD202/AD204–SPECIFICATIONS (typical @ +25°C & V_S = +15 V unless otherwise noted)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1 V/V–100 V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20 ppm/°C typ (±45 ppm/°C max)	*	*	*
vs. Time	±50 ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1 V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	±5 V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60 Hz, Continuous	750 V rms	1500 V rms	750 V rms	1500 V rms
Continuous (AC and DC)	±1000 V Peak	±2000 V Peak	±1000 V Peak	±2000 V Peak
Isolation-Mode Rejection Ratio (IMRR) @ 60 Hz				
$R_S \leq 100\ \Omega$ (HI & LO Inputs) G = 1 V/V	110 dB	110 dB	105 dB	105 dB
G = 100 V/V	130 dB	*	*	*
$R_S \leq 1\ k\Omega$ (Input HI, LO, or Both) G = 1 V/V	104 dB min	104 dB min	100 dB min	100 dB min
G = 100 V/V	110 dB min	*	*	*
Leakage Current Input to Output @ 240 V rms, 60 Hz	2 µA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1 V/V)	$10^{12}\ \Omega$	*	*	*
Common Mode	2 GΩ‖4.5 pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	±30 pA	*	*	*
vs. Temperature (0°C to +70°C)	±10 nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±5 pA	*	*	*
vs. Temperature (0°C to +70°C)	±2 nA	*	*	*
INPUT NOISE				
Voltage, 0.1 Hz to 100 Hz	4 µV p-p	*	*	*
f > 200 Hz	50 nV/√Hz	*	*	*
FREQUENCY RESPONSE				
Bandwidth ($V_O \leq 10$ V p-p, G = 1 V–50 V/V)	5 kHz	5 kHz	2 kHz	2 kHz
Settling Time, to ±10 mV (10 V Step)	1 ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ +25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ±5/G)mV max	(±15 ±15/G)mV max	(±5 ±5/G)mV max
vs. Temperature (0°C to +70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)$ mV/°C	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5 V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5 V	*	*	*
Output Resistance	3 kΩ	3 kΩ	7 kΩ	7 kΩ
Output Ripple, 100 kHz Bandwidth	10 mV pk-pk	*	*	*
5 kHz Bandwidth	0.5 mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5 V	*	*	*
Accuracy	±10%	*	*	*
Current	2 mA (Either Output)[3]	2 mA (Either Output)[3]	400 µA Total	400 µA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100 mV pk-pk	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15 V pk-pk Nominal	15 V pk-pk Nominal	N/A	N/A
Input Frequency	25 kHz Nominal	25 kHz Nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	+15 V ± 5%	+15 V ± 5%
Voltage, Operating	N/A	N/A	+15 V ± 10%	+15 V ± 10%
Current, No Load (V_S = +15 V)	N/A	N/A	5 mA	5 mA
TEMPERATURE RANGE				
Rated Performance	0°C to +70°C	*	*	*
Operating	–40°C to +85°C	*	*	*
Storage	–40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08" × 0.250" × 0.625"	*	*	*
DIP Package (N)	2.10" × 0.700" × 0.350"	*	*	*

NOTES

Specifications same as AD204J.

[1]Nonlinearity is specified as a % deviation from a best straight line.

[2]1.0 µF min decoupling required (see text).

[3]3 mA with one supply loaded.

[4]Width is 0.25" typ, 0.26" max. For outline information see complete data sheet.

Specifications subject to change without notice.

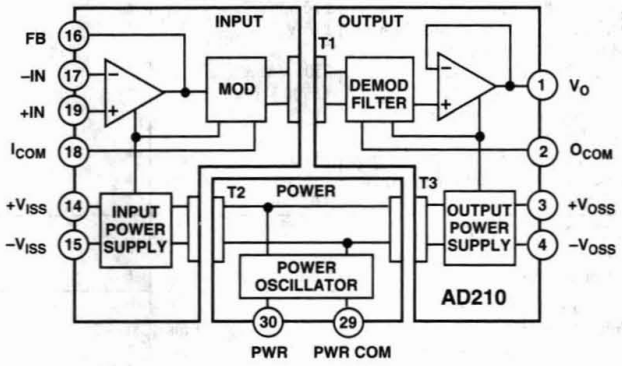
Precision, Wide Bandwidth, 3-Port Isolation Amplifier

AD210*

FEATURES
High CMV Isolation: 2500 V rms Continuous
±3500 V Peak Continuous
Small Size: 1.00" × 2.10" × 0.350"
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20 kHz Full-Power (–3 dB)
Low Gain Drift: ±25 ppm/°C max
High CMR: 120 dB (G = 100 V/V)
Isolated Power: ±15 V @ ±5 mA
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15 V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multichannel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may otherwise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500 V rms (Continuous) and ±3500 V peak (Continuous) common-mode voltage isolation between any two ports. Low input to output capacitance of 5 pF results in a 120 dB CMR at a gain of 100, and a low leakage current (2 μA rms max @ 240 V rms, 60 Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25 ppm/°C max, and input offset drift of (±10 ±30/G) μV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20 kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00" × 2.10" × 0.350". The low profile DIP package allows application in 0.5" card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15 V @ 5 mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required and facilitates many alternative input functions as required by the user.

*Covered by U.S. Patent No. 4,703,283.

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AD210–SPECIFICATIONS (typical @ +25°C, and V_S = +15 V unless otherwise noted)

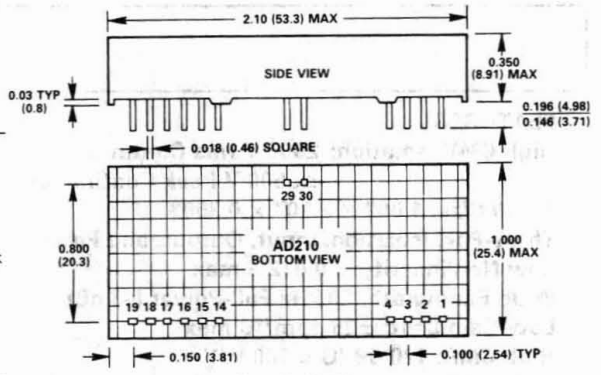
Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1 V/V – 100 V/V	*	*
Error	±2% max	±1% max	*
vs. Temperature (0°C to +70°C)	+25 ppm/°C max	*	*
(–25°C to +85°C)	±50 ppm/°C max	*	*
vs. Supply Voltage	±0.002%/V	*	*
Nonlinearity[1]	±0.025% max	±0.012% max	*
Nonlinearity vs. Isolated Supply Load	±0.002 %/mA	*	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10 V	*	*
Maximum Safe Differential Input	±15 V	*	*
Max. CMV Input-to-Output	*		
ac, 60 Hz, Continuous	2500 V rms	*	1500 V rms
dc, Continuous	±3500 V peak	*	±2000 V peak
Common-Mode Rejection			
60 Hz, G = 100 V/V			
$R_S \leq 500\ \Omega$ Impedance Imbalance	120 dB	*	*
Leakage Current Input-to-Output			
@ 240 V rms, 60 Hz	2 μA rms max	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\ \Omega$	*	*
Common Mode	5 GΩ‖5 pF	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	30 pA typ (400 pA max)	*	*
vs. Temperature (0°C to +70°C)	10 nA max	*	*
(–25°C to +85°C)	30 nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	5 pA typ (200 pA max)	*	*
vs. Temperature (0°C to +70°C)	2 nA max	*	*
(–25°C to +85°C)	10 nA max	*	*
INPUT NOISE			
Voltage (1 kHz)	18 nV/√Hz	*	*
(10 Hz to 10 kHz)	4 μV rms	*	*
Current (1 kHz)	0.01 pA/√Hz	*	*
FREQUENCY RESPONSE			
Bandwidth (–3 dB)			
G = 1 V/V	20 kHz	*	*
G = 100 V/V	15 kHz	*	*
Settling Time (±10 mV, 20 V Step)			
G = 1 V/V	150 μs	*	*
G = 100 V/V	500 μs	*	*
Slew Rate (G = 1 V/V)	1 V/μs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ +25°C	(±15 ±45/G) mV max	(±5 ±15/G) mV max	*
vs. Temperature (0°C to +70°C)	(±10 ±30/G) μV/°C	*	*
(–25°C to +85°C)	(±10 ±50/G) μV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2 kΩ Load	±10 V min	*	*
Impedance	1 Ω max	*	*
Ripple (Bandwidth = 100 kHz)	10 mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	±15 V	*	*
Accuracy	±10%	*	*
Current	±5 mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15 V dc ± 5%	*	*
Voltage, Operating	+15 V dc ± 10%	*	*
Current, Quiescent	50 mA	*	*
Current, Full Load – Full Signal	80 mA	*	*
TEMPERATURE RANGE			
Rated Performance	–25°C to +85°C	*	*
Operating	–40°C to +85°C	*	*
Storage	–40°C to +85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input.
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.

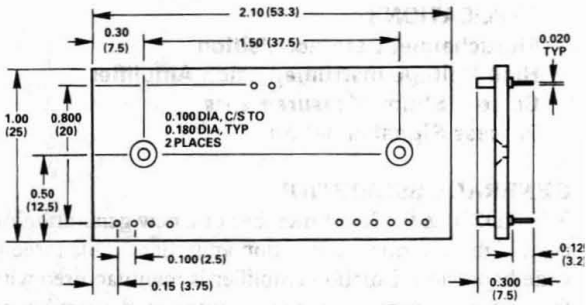
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 MATING SOCKET



AD210 PIN DESIGNATIONS

Pin	Designation	Function
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+Isolated Power @ Output
4	$-V_{OSS}$	–Isolated Power @ Output
14	$+V_{ISS}$	+Isolated Power @ Input
15	$-V_{ISS}$	–Isolated Power @ Input
16	FB	Input Feedback
17	–IN	–Input
18	I_{COM}	Input Common
19	+IN	+Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD210 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

120 kHz Bandwidth, Low Distortion, Isolation Amplifier

AD215

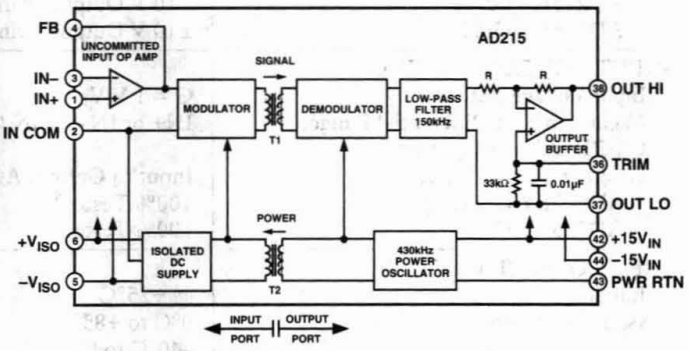
FEATURES

Isolation Voltage Rating: 1,500 V rms
Wide Bandwidth: 120 kHz, Full Power (–3 dB)
Rapid Slew Rate: 6 V/μs
Fast Settling Time: 9 μs
Low Harmonic Distortion: –80 dB @ 1 kHz
Low Nonlinearity: ±0.005%
Wide Output Range: ±10 V, min (Buffered)
Built-in Isolated Power Supply: ±15 V dc @ ±10 mA
Performance Rated over –40°C to +85°C

APPLICATIONS INCLUDE

High Speed Data Acquisition Systems
Power Line and Transient Monitors
Multichannel Muxed Input Isolation
Waveform Recording Instrumentation
Power Supply Controls
Vibration Analysis

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD215 is a high speed input isolation amplifier designed to isolate and amplify wide bandwidth analog signals. The innovative circuit and transformer design of the AD215 ensures wideband dynamic characteristics while preserving key dc performance specifications.

The AD215 provides complete galvanic isolation between the input and output of the device including the user-available front-end isolated power supplies. The functionally complete design, powered by a ±15 V dc supply, eliminates the need for a user supplied isolated dc/dc converter. This permits the designer to minimize circuit overhead and reduce overall system design complexity and component costs.

The design of the AD215 emphasizes maximum flexibility and ease of use in a broad range of applications where fast analog signals must be measured under high common-mode voltage (CMV) conditions. The AD215 has a ±10 V input/output range, a specified gain range of 1 V/V to 10 V/V, a buffered output with offset trim and a user-available isolated front-end power supply which produces ±15 V dc at ±10 mA.

PRODUCT HIGHLIGHTS

High Speed Dynamic Characteristics: The AD215 features a typical full-power bandwidth of 120 kHz (100 kHz min), rise time of 3 μs and settling time of 9 μs. The high speed performance of the AD215 allows for unsurpassed galvanic isolation of virtually any wideband dynamic signal.

Flexible Input and Buffered Output Stages: An uncommitted op amp is provided on the input stage of the AD215 to allow for input buffering or amplification and signal conditioning. The AD215 also features a buffered output stage to drive low impedance loads and an output voltage trim for zeroing the output offset where needed.

High Accuracy: The AD215 has a typical nonlinearity of ±0.005% (B grade) of full-scale range and the total harmonic distortion is typically –80 dB at 1 kHz. The AD215 provides designers with complete isolation of the desired signal without loss of signal integrity or quality.

Excellent Common-Mode Performance: The AD215BY (AD215AY) provides 1,500 V rms (750 V rms) common-mode voltage protection from its input to output. Both grades feature a low common-mode capacitance of 4.5 pF inclusive of the dc/dc power isolation. This results in a typical common-mode rejection specification of 105 dB and a low leakage current of 2.0 μA rms max (240 V rms, 60 Hz).

Isolated Power: An unregulated isolated power supply of ±15 V dc @ ±10 mA is available at the isolated input port of the AD215. This permits the use of ancillary isolated front-end amplifiers or signal conditioning components without the need for a separate dc/dc supply. Even the excitation of transducers can be accomplished in most applications.

Rated Performance over the –40°C to +85°C Temperature Range: With an extended industrial temperature range rating, the AD215 is an ideal isolation solution for use in many industrial environments.

ORDERING GUIDE

Model	Temperature Range	V_{CMV}	Nonlinearity[1]	Package Option[2]
AD215AY	–40°C to +85°C	750	0.01%	SIP
AD215BY	–40°C to +85°C	1500	0.005%	SIP

NOTES
[1]Typical @ +25°C, G = 1 V/V.
[2]For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD215–SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V dc, 2 kΩ output load, unless otherwise noted.)

Parameter	Conditions	AD215AY/BY Min	Typ	Max	Units
GAIN					
Range[1]		1		10	V/V
Error	G = 1 V/V, No Load on V_{ISO}		±0.5	±2	%
vs. Temperature	0°C to +85°C		+15		ppm/°C
	–40°C to 0°C		+50		ppm/°C
Nonlinearity[3]					
AD215BY Grade	±10 V Output Swing, G = 1 V/V		±0.005	±0.015	%
AD215AY Grade	±10 V Output Swing, G = 1 V/V		±0.01	±0.025	%
INPUT VOLTAGE RATINGS					
Input Voltage Rating	G = 1 V/V	±10			V
Maximum Safe Differential Range	IN+ or IN–, to IN COM		±15		V
CMRR of Input Op Amp			100		dB
Isolation Voltage Rating[4]	Input to Output, AC, 60 Hz				
AD215BY Grade	100% Tested[4]	1500			V rms
AD215AY Grade	100% Tested[4]	750			V rms
INPUT OFFSET VOLTAGE					
Initial	@ +25°C		±0.4	±2.0	mV
vs. Temperature	0°C to +85°C		±2		µV/°C
	–40°C to 0°C		±20		µV/°C
OUTPUT OFFSET VOLTAGE					
Initial	@ +25°C, Trimmable to Zero	0	–35	–80	mV
vs. Temperature	0°C to +85°C		±30		µV/°C
	–40°C to 0°C		±80		µV/°C
INPUT BIAS CURRENT					
Initial	@ +25°C		300		nA
vs. Temperature	–40°C to +85°C		±400		nA
DYNAMIC RESPONSE (2 kΩ Load)					
Full Signal Bandwidth (–3 dB)	G = 1 V/V, 20 V pk-pk Signal	100	120		kHz
Transport Delay[6]			2.2		µs
Slew Rate	±10 V Output Swing		6		V/µs
Rise Time	10% to 90%, ±10 V Output Swing		3		µs
DYNAMIC RESPONSE (2 kΩ Load) Cont.					
Settling Time	to ±0.10%, ±10 V Output Swing		9		µs
Overshoot			1		%
Harmonic Distortion Components	@ 1 kHz		–80		dB
	@ 10 kHz		–65		dB
Overload Recovery Time	G = 1 V/V, ±15 V Drive		5		µs
Output Overload Recovery Time	G > 5		10		µs
RATED OUTPUT					
Voltage	Out HI to Out LO	±10			V
Current	2 kΩ Load	±5			mA
ISOLATED POWER OUTPUT[8]					
Voltage	No Load	±14.25	±15	±17.25	V
vs. Temperature	0°C to +85°C		+20		mV/°C
	–40°C to 0°C		+25		mV/°C
Current at Rated Supply Voltage[2, 9]			±10		mA
POWER SUPPLY					
Supply Voltage	Rated Performance	±14.5	±15	±16.5	V dc
	Operating[10]	±14.25		±17	V dc
Current	Operating (+15 V dc/–15 V dc Supplies)		+40/–18		mA
TEMPERATURE RANGE					
Rated Performance		–40		+85	°C

Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD215 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Matched Transistors
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Matched Transistors–Selection Guides

Dual NPN

Model	V_{OS} max µV	TCV_{OS} max µV/°C	f_{FE} & IC = 1 µA	10 µA	1 mA	10 mA	f_{FE} Match %	e_{NOISE} max @ 10 Hz µV/√Hz	# Pins	Page No.	Comments	Fax-code
MAT01	500/100	2/0.5	590/430	770/560		840/610	8/3	7.5	6	9–3	Very Low IC Operation	1648
MAT02	150/50	0.5/0.1		550	605		4/2	3/2	6/20	9–5	Very Low Drift	1649
SSM2210	200	2		200	300		5	1	8	*	Low Cost, DIP & SOIC	

Dual PNP

Model	V_{OS} max µV	TCV_{OS} max µV/°C	f_{FE} & IC = 10 µA	1 mA	10 mA	f_{FE} Match %	e_{NOISE} max @ 10 Hz µV/√Hz	# Pins	Page No.	Comments	Fax-code
MAT03	200/100	1/0.5	400/300	400/300		4/2	4	14	9–7	Very High Beta	1650
SSM2220	200	2	60	70		6	1	8	*	Low Cost, DIP & SOIC	1800

Quad NPN

Model	V_{OS} max µV	TCV_{OS} max µV/°C	f_{FE} & IC = 10 µA	1 mA	10 mA	f_{FE} Match %	e_{NOISE} max @ 10 Hz µV/√Hz	# Pins	Page No.	Comments	Fax-code
MAT04	400/200	1.5	400/300	400/300		4/2	4	14	9–9		1652

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ANALOG DEVICES

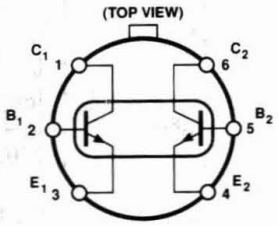
Matched Monolithic Dual Transistor

MAT01

FEATURES
Low V_{OS} (V_{BE} Match): 40 μV typ, 100 μV max
Low TCV_{OS}: 0.5 μV/°C max
High h_{FE}: 500 min
Excellent h_{FE} Linearity from 10 nA to 10 mA
Low Noise Voltage: 23 μV p-p—0.1 Hz to 10 Hz
High Breakdown: 45 V min
Available in Die Form

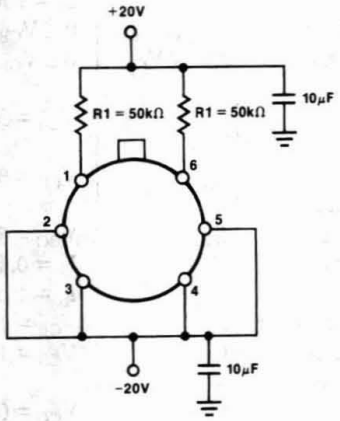
PIN CONNECTION

TO-78
(H Suffix)



NOTE: Substrate is connected to case.

BURN-IN CIRCUIT



PRODUCT DESCRIPTION

The MAT01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40 μV, temperature drift of 0.15 μV/°C, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10 nA. The high gain at low collector current makes the MAT01 ideal for use in low power, low level input stages.

ABSOLUTE MAXIMUM RATINGS[1]

Collector-Base Voltage (BV_{CBO})
MAT01AH, GH, N ..... 45 V
Collector-Emitter Voltage (BV_{CEO})
MAT01AH, GH, N ..... 45 V
Collector-Collector Voltage (BV_{CC})
MAT01AH, GH, N ..... 45 V
Emitter-Emitter Voltage (BV_{EE})
MAT01AH, GN, N ..... 45 V
Emitter-Base Voltage (BV_{EBO})[2] ..... 5 V
Collector Current (I_C) ..... 25 mA
Emitter Current (I_E) ..... 25 mA
Total Power Dissipation
Case Temperature ≤ 40°C[3] ..... 1.8 W
Ambient Temperature ≤ 70°C[4] ..... 500 mW
Operating Ambient Temperature ..... –55°C to +125°C
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
DICE Junction Temperature ..... –65°C to +150°C

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged devices.
[2]Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5 V rating shown.
[3]Rating applies to applications using heat sinking to control case temperature. Derate linearity at 16.4 mW/°C for case temperatures above 40°C.
[4]Rating applies to applications not using heat sinking; device in free air only. Derate linearity at 6.3 mW/°C for ambient temperatures above 70°C.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
MAT01AH[3]	0.1 mV	–55°C to +125°C	TO-78
MAT01GH	0.5 mV	–55°C to +125°C	TO-78

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

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MAT01–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{CB} = 15 V, I_C = 10 μA, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01AH Min	MAT01AH Typ	MAT01AH Max	MAT01GH Min	MAT01GH Typ	MAT01GH Min	Units
Breakdown Voltage	BV_{CEO}	I_C = 100 μA	45			45			V
Offset Voltage	V_{OS}			0.04	0.1		0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)		2.0			2.0		μV/Mo
Long Term		(Note 2)		0.2			0.2		μV/Mo
Offset Current	I_{OS}			0.1	0.6		0.2	3.2	nA
Bias Current	I_B			13	20		18	40	nA
Current Gain	h_{FE}	I_C = 10 nA		590			430		
		I_C = 10 μA	500	770		250	560		
		I_C = 10 mA		840			610		
Current Gain Match	Δh_{FE}	I_C = 10 μA		0.7	3.0		1.0	8.0	%
		100 nA ≤ I_C ≤ 10 mA		0.8			1.2		%
Low Frequency Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.23	0.4		0.23	0.4	μV p-p
Broadband Noise Voltage	e_n rms	1 Hz to 10 kHz		0.60			0.60		μV rms
Noise Voltage Density	e_n	f_O = 10 Hz[3]		7.0	9.0		7.0	9.0	nV/√Hz
		f_O = 100 Hz[3]		6.1	7.6		6.1	7.6	nV/√Hz
		f_O = 1000 Hz[3]		6.0	7.5		6.0	7.5	nV/√Hz
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30 V		0.5	3.0		0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30 V		2	15		3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 30 V, I_E = 0[4]		15	50		25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 30 V, V_{BE} = 0[4, 6]		50	200		90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 30 V[6]		20	200		30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1 mA, I_C = 1 mA		0.12	0.20		0.12	0.25	V
		I_B = 1 mA, I_C = 10 mA		0.8			0.8		V
Gain-Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 10 mA		450			450		MHz
Output Capacitance	C_{OB}	V_{CB} = 15 V, I_E = 0		2.8			2.8		pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0		8.5			8.5		pF

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_{CB} = 15 V, I_C = 10 μA, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01AH Min	MAT01AH Typ	MAT01AH Max	MAT01GH Min	MAT01GH Typ	MAT01GH Min	Units
Offset Voltage	V_{OS}			0.06	0.15		0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 7)		0.15	0.50		0.35	1.8	μV/°C
Offset Current	I_{OS}			0.9	8.0		1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)		10	90		15	150	pA/°C
Bias Current	I_B			28	60		36	130	nA
Current Gain	h_{FE}		167	400		77	300		
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 30 V, I_E = 0[4]		15	80		25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 30 V, V_{BE} = 0[4, 6]		50	300		90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 30 V, (Note 6)		30	200		50	400	nA

Specifications subject to change without notice.

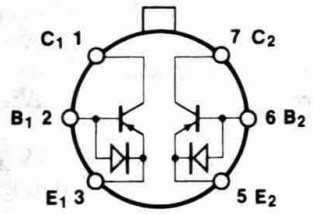
Low Noise, Matched Dual Monolithic Transistor

MAT02

FEATURES
Low Offset Voltage: 50 μV max
Low Noise Voltage at 100 Hz, 1 mA: 1.0 nV/√Hz max
High Gain (h_{FE}): 500 min at I_C = 1 mA
300 min at I_C = 1 μA
Excellent Log Conformance: $r_{BE} \simeq 0.3\ \Omega$
Low Offset Voltage Drift: 0.1 μV/°C max
Improved Direct Replacement for LM194/394
Available in Die Form

PIN CONNECTION

TO-78
(H Suffix)



NOTE
Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

PRODUCT DESCRIPTION

The design of the MAT02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE}. Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT02 include offset voltage of 50 μV max (A/E grades) and 150 μV max F grade. Device performance is specified over the full military temperature range as well as at 25°C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

The MAT02 should be used in any application where low noise is a priority. The MAT02 can be used as an input stage to make an amplifier with noise voltage of less than 1.0 nV/√Hz at 100 Hz. Other applications, such as log/antilog circuits, may use the excellent logging conformity of the MAT02. Typical bulk resistance is only 0.3 Ω to 0.4 Ω. The MAT02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1 μA to 10 mA. For applications requiring multiple devices see MAT04 Quad Matched Transistor data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Collector-Base Voltage (BV_{CBO})	40 V
Collector-Emitter Voltage (BV_{CEO})	40 V
Collector-Collector Voltage (BV_{CC})	40 V
Emitter-Emitter Voltage (BV_{EE})	40 V
Collector Current (I_C)	20 mA
Emitter Current (I_E)	20 mA
Total Power Dissipation	
Case Temperature ≤ 40°C[2]	1.8 W
Ambient Temperature ≤ 70°C[3]	500 mW
Operating Temperature Range	
MAT02A	–55°C to +125°C
MAT02E, F	–25°C to +85°C
Operating Junction Temperature	–55°C to +150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C
Junction Temperature	–65°C to +150°C

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged devices.
[2]Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4 mW/°C for case temperature above 40°C.
[3]Rating applies to applications not using a heat sinking; devices in free air only. Derate linearly at 6.3 mW/°C for ambient temperature above 70°C.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
MAT02AH[3]	50 μV	–55°C to +125°C	TO-78
MAT02EH	50 μV	–55°C to +125°C	TO-78
MAT02FH	150 μV	–55°C to +125°C	TO-78

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

MAT02–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{CB} = 15 V, I_C = 10 µA, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT02A/E Min	MAT02A/E Typ	MAT02A/E Max	MAT02F Min	MAT02F Typ	MAT02F Max	Units
Current Gain	h_{FE}	I_C = 1 mA[1]	500	605		400	605		
		I_C = 100 µA	500	590		400	590		
		I_C = 10 µA	400	550		300	550		
		I_C = 1 µA	300	485		200	485		
Current Gain Match	Δh_{FE}	10 µA ≤ I_C ≤ 1 mA[2]		0.5	2		0.5	4	%
Offset Voltage	V_{OS}	V_{CB} = 0, 1 µA ≤ I_C ≤ 1 mA[3]		10	50		80	150	µV
Offset Voltage	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX},[4]		10	25		10	50	µV
Change vs V_{CB}		1 µA ≤ I_C ≤ 1 mA[3]		10	25		10	50	µV
Offset Voltage Change	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0 V		5	25		5	50	µV
vs. Collector Current		1 µA ≤ I_C ≤ 1 mA[3]		5	25		5	50	µV
Offset Current									
Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX}		30	70		30	70	pA/V
Bulk Resistance	r_{BE}	10 µA ≤ I_C ≤ 10 mA[5]		0.3	0.5		0.3	0.5	Ω
Collector-Base									
Leakage Current	I_{CBO}	V_{CB} = V_{MAX}		25	200		25	400	pA
Collector-Collector									
Leakage Current	I_{CC}	V_{CC} = V_{MAX}[5, 6]		35	200		35	400	pA
Collector-Emitter		V_{CE} = V_{MAX}[5, 6]							
Leakage Current	I_{CES}	V_{BE} = 0		35	200		35	400	pA
Noise Voltage Density	e_n	I_C = 1 mA, V_{CB} = 0[7]							
		f_O = 10 Hz		1.6	2		1.6	3	nV/√Hz
		f_O = 100 Hz		0.9	1		0.9	2	nV/√Hz
		f_O = 1 kHz		0.85	1		0.85	2	nV/√Hz
		f_O = 10 kHz		0.85	1		0.85	2	nV/√Hz
Collector Saturation									
Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA		0.05	0.1		0.05	0.2	V
Input Bias Current	I_B	I_C = 10 µA			25			34	nA
Input Offset Current	I_{OS}	I_C = 10 µA			0.6			1.3	nA
Breakdown Voltage	BV_{CEO}		40			40			V
Gain-Bandwidth Product	f_T	I_C = 10 mA, V_{CE} = 10 V		200			200		MHz
Output Capacitance	C_{OB}	V_{CB} = 15 V, I_E = 0		23			23		pF
Collector-Collector									
Capacitance	C_{CC}	V_{CC} = 0		35			35		pF

NOTES

[1]Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.

[2]Current gain match (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100\ (\Delta I_B)\ (h_{FE}\ \text{min})}{I_C}$

[3]Measured at I_C = 10 µA and guaranteed by design over the specified range of I_C.

[4]This is the maximum change in V_{OS} as V_{CB} is swept from 0 V to 40 V.

[5]Guaranteed by design.

[6]I_{CC} and I_{CES} are verified by measurement of I_{CBO}.

[7]Sample tested.

Specifications subject to change without notice.

ANALOG DEVICES

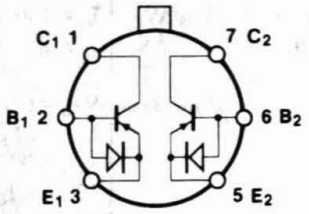
Low Noise, Matched Dual PNP Transistor

MAT03

FEATURES
Dual Matched PNP Transistor
Low Offset Voltage: 100 μV max
Low Noise: 1 nV/√Hz @ 1 kHz max
High Gain: 100 min
High Gain Bandwidth: 190 MHz typ
Tight Gain Matching: 3% max
Excellent Logarithmic Conformance: $r_{BE} \simeq 0.3\ \Omega$ typ
Available in Die Form

PIN CONNECTION

TO-78
(H Suffix)



GENERAL DESCRIPTION

The MAT03 dual monolithic PNP transistor offers excellent parametric matching and high frequency performance. Low noise characteristics (1 nV/√Hz max @ 1 kHz), high bandwidth (190 MHz typical), and low offset voltage (100 μV max), makes the MAT03 an excellent choice for demanding preamplifier applications. Tight current gain matching (3% max mismatch) and high current gain (100 min), over a wide range of collector current, makes the MAT03 an excellent choice for current mirrors. A low value of bulk resistance (typically 0.3 Ω) also makes the MAT03 an ideal component for applications requiring accurate logarithmic conformance.

Each transistor is individually tested to data sheet specifications. Device performance is guaranteed at 25°C and over the extended industrial and military temperature ranges. To insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
MAT03AH[3]	100 μV	–55°C to +125°C	TO-78
MAT03EH	100 μV	–40°C to +85°C	TO-78
MAT03FH	200 μV	–40°C to +85°C	TO-78

NOTES
[1]Burn-in is available on industrial temperature range parts.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

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MAT03–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT03A Min	MAT03A Typ	MAT03A Max	MAT03E Min	MAT03E Typ	MAT03E Max	MAT03F Min	MAT03F Typ	MAT03F Max	Units
Current Gain[1]	h_{FE}	V_{CB} = 0 V, –36 V										
		I_C = 1 mA	100	165		100	165		80	165		
		I_C = 100 µA	90	150		90	150		70	150		
		I_C = 10 µA	80	120		80	120		60	120		
Current Gain Matching[2]	Δh_{FE}	I_C = 100 µA, V_{CB} = 0 V		0.5	3		0.5	3		0.5	6	%
Offset Voltage[3]	V_{OS}	V_{CB} = 0 V, I_C = 100 µA		40	100		40	100		40	200	µV
Offset Voltage Change vs Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100 µA		11	150		11	150		11	200	µV
		V_{CB_1} = 0 V		11	150		11	150		11	200	µV
		V_{CB_2} = –36 V		11	150		11	150		11	200	µV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0 V		12	50		12	50		12	75	µV
		I_{C_1} = 10 µA, I_{C_2} = 1 mA		12	50		12	50		12	75	µV
Bulk Resistance	r_{BE}	V_{CB} = 0 V		0.3	0.75		0.3	0.75		0.3	0.75	Ω
		10 µA ≤ I_C ≤ 1 mA		0.3	0.75		0.3	0.75		0.3	0.75	Ω
Offset Current	I_{OS}	I_C = 100 µA, V_{CB} = 0 V		6	35		6	35		6	45	nA
Collector-Base Leakage Current	I_{CB_0}	V_{CB} = –36 V = V_{MAX}		50	200		50	200		50	400	pA
Noise Voltage Density[4]	e_N	I_C = 1 mA, V_{CB} = 0										
		f_O = 10 Hz		0.8	2		0.8			0.8		nV/√Hz
		f_O = 100 Hz		0.7	1		0.7			0.7		nV/√Hz
		f_O = 1 kHz		0.7	1		0.7			0.7		nV/√Hz
		f_O = 10 kHz		0.7	1		0.7			0.7		nV/√Hz
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA		0.025	0.1		0.025	0.1		0.025	0.1	V

NOTES

[1]Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0 V.

[2]Current gain matching (Δh_{FE}) is defined as: $\Delta h_{FE} = \frac{100\ (\Delta I_B)\ h_{FE}\ (MIN)}{I_C}$

[3]Offset voltage is defined as: $V_{OS} = V_{BE_1} - V_{BE_2}$, where V_{OS} is the differential voltage for $I_{C_1} = I_{C_2}$: $V_{OS} = V_{BE_1} - V_{BE_2} = \frac{KT}{q} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$.

[4]Sample tested. Noise tested and specified as equivalent input voltage for each transistor.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Collector-Base Voltage (BV_{CBO}) . . . . . 36 V
Collector-Emitter Voltage (BV_{CEO}) . . . . . 36 V
Collector-Collector Voltage (BV_{CC}) . . . . . 36 V
Emitter-Emitter Voltage (BV_{EE}) . . . . . 36 V
Collector Current (I_C) . . . . . 20 mA
Emitter Current (I_E) . . . . . 20 mA
Total Power Dissipation
  Ambient Temperature ≤ 70°C[2] . . . . . 500 mW
Operating Temperature Range
  MAT03A . . . . . –55°C to +125°C
  MAT03E/F . . . . . –40°C to +85°C
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Junction Temperature . . . . . –65°C to +150°C

NOTES

[1]Absolute maximum ratings apply to both DICE and packaged devices.

[2]Rating applies to TO-78 not using a heat sink, and LCC; devices in free air only. For TO-78, derate linearly at 6.3 mW/°C above 70°C ambient temperature; for LCC, derate at 7.8 mW/°C.

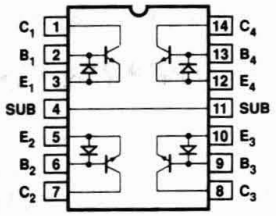
ANALOG DEVICES

Matched Monolithic Quad Transistor

MAT04

FEATURES
Low Offset Voltage: 200 μV max
High Current Gain: 400 min
Excellent Current Gain Match: 2% max
Low Noise Voltage at 100 Hz, 1 mA: 2.5 nV/√Hz max
Excellent Log Conformance: rBE = 0.6 Ω max
Matching Guaranteed for All Transistors
Available in Die Form

PIN CONNECTIONS
14-Pin Cerdip (Y Suffix)
14-Pin Plastic DIP (P Suffix)
14-Pin SO (S Suffix)



PRODUCT DESCRIPTION

The MAT04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and nonlinear circuit applications. Performance characteristics of the MAT04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5 nV/√Hz maximum at 100 Hz, I_C = 1 mA) and excellent logarithmic conformance. The MAT04 also features a low offset voltage of 200 μV and tight current gain matching, to within 2%. Each transistor of the MAT04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT04 makes it an excellent choice for use in log and antilog circuits. The MAT04 is an ideal choice in applications where low noise and high gain are required.

9

ORDERING GUIDE[1]

Model	T_A = +25°C V_{OS} max	Temperature Range	Package Description	Package Option[2]
MAT04AY	200 μV	–55°C to +125°C	Cerdip	Q-14
MAT04EY	200 μV	–25°C to +85°C	Cerdip	Q-14
MAT04FY	400 μV	–40°C to +85°C	Cerdip	Q-14
MAT04FP	400 μV	–40°C to +85°C	P-DIP-14	N-14
MAT04FS[3]	400 μV	–40°C to +85°C	14-Pin SO	SO-14

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

MAT04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ T_A = +25°C unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}, Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.)

Parameter	Symbol	Conditions	MAT04A/E Min	MAT04A/E Typ	MAT04A/E Max	MAT04F Min	MAT04F Typ	MAT04F Max	Units
Current Gain	h_{FE}	10 µA ≤ I_C ≤ 1 mA 0 V ≤ V_{CB} ≤ 30 V[1]	400	800		300	600		
Current Gain Match	Δh_{FE}	I_C = 100 µA 0 V ≤ V_{CB} ≤ 30 V[2]		0.5	2		1	4	%
Offset Voltage	V_{OS}	10 µA ≤ I_C ≤ 1 mA 0 V ≤ V_{CB} ≤ 30 V[4]		50	200		100	400	µV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	10 µA ≤ I_C ≤ 1 mA V_{CB} = 0 V[4]		5	25		10	50	µV
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	10 µA ≤ I_C ≤ 1 mA 0 V ≤ V_{CB} ≤ 30 V[4]		50	100		100	200	µV
Bulk Emitter Resistance	r_{BE}	10 µA ≤ I_C ≤ 1 mA V_{CB} = 0 V[5]		0.4	0.6		0.4	0.6	Ω
Input Bias Current	I_B	I_C = 100 µA 0 V ≤ V_{CB} ≤ 30 V		125	250		165	330	nA
Input Offset Current	I_{OS}	I_C = 100 µA; V_{CB} = 0 V		0.6	5		2	13	nA
Breakdown Voltage	BV_{CEO}	I_C = 10 µA	40			40			V
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 100 µA; I_C = 1 mA		0.03	0.06		0.03	0.06	V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 40 V		5			5		pA
Noise Voltage Density	e_n	V_{CB} = 0 V; f_O = 10 Hz		2	3		2	4	nV/√Hz
		I_C = 1 mA; f_O = 100 Hz		1.8	2.5		1.8	3	nV/√Hz
		f_O = 1 kHz[3]		1.8	2.5		1.8	3	nV/√Hz
Gain Bandwidth Product	f_T	I_C = 1 mA; V_{CE} = 10 V		300			300		MHz
Output Capacitance	C_{OBO}	V_{CB} = 15 V; I_E = 0 f = 1 MHz		10			10		pF
Input Capacitance	C_{EBO}	V_{BE} = 0 V; I_C = 0 f = 1 MHz		40			40		pF

NOTES

[1]Current gain measured at I_C = 10 µA, 100 µA and 1 mA.

[2]Current gain match is defined as: $\Delta h_{FE} = \frac{100(\Delta I_B)(h_{FE}\ \text{min})}{I_C}$

[3]Sample tested.

[4]Measured at I_C = 10 µA and guaranteed by design over the specified range of I_C.

[5]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Collector-Base Voltage (BV_{CBO}) ..... 40 V
Collector-Emitter Voltage (BV_{CEO}) ..... 40 V
Collector-Collector Voltage (BV_{CC}) ..... 40 V
Emitter-Emitter Voltage (BV_{EE}) ..... 40 V
Collector Current ..... 30 mA
Emitter Current ..... 30 mA
Substrate (Pin-4 to Pin-11) Current ..... 30 mA
Operating Temperature Range
MAT04AY, BY ..... –55°C to +125°C
MAT04EY ..... –25°C to +85°C
MAT04FY, FP, FS ..... –40°C to +85°C
Storage Temperature
Y Package ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES

[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

Operational Amplifiers
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Low Bias Current

Model	Open-Loop Gain V/μV	Common-Mode Rejection CMRR dB	Initial Offset E_{OS} ±mV max	E_{OS} vs. Temp ±μV/°C	I_B +25°C max ±pA	Supply Current I_Q mA	Unity Gain MHz	Slew Rate V/μs	# Pins	Page No.	Comments	Fax-code
Singles												
AD549	0.3	80	1		0.06–0.2	0.7	0.7	2	8	10–17	Electrometer Grade JFET	1157
AD515A	0.02	66	3	50	0.075–0.2	1.5	1	0.3	8	*	Electrometer Grade JFET	1138
AD548	0.076	2	2–20	20	0.25–20	0.2	0.8	1	8	10–15		1156
AD546	0.3	80	2	20	0.5–1	0.7	0.7	2	8	10–11		1154
AD645	0.1	90	0.5	5–10	1–5	3.5	2	1	8	10–19		1211
AD795	0.8	90	0.25–0.5	5–10	2	1.5	2	0.8	8	10–37		1392
AD820	0.5	70	0.5–1	10	5–10	0.9	2.25	1.2	8	10–57	Rail-to-Rail Output Stage	1406
AD542	0.25	80	0.5–2	5–20	25–50	1.5	1	2	8	10–13		1155
AD544	0.05	80	0.5–2	5–20	25–50	2.5	2	8	8	10–13		1155
AD711	0.15	76	0.25–2	20	25–50	3.4	3	16	8	10–27		1249
AD547	0.1	76	0.25–1	5	50	1.5	1	3	8	10–13		1155
OP150	TBD	60	5	TBD	60	0.5	5	2	8	*	Rail-to-Rail In/Out, CMOS	1950
AD744	0.2	1	0.45–2	100	100	5	8	45	8	10–31		1281
AD705	0.3	110	0.09	0.6–1.5	150	0.6	0.4	0.1	8	10–25		1245
OP97	0.2	110	0.025–0.075	2	150	0.6	0.4	0.1	8	10–121		1723
OP42	0.1	80	0.75–5	NS	200	6.5	10	40	8	10–117		1705
AD743	1	80	0.5–1	5	200–400	10	4.5	2.8	8/16	10–29	Very Low Noise JFET	1280
AD745	1	80	0.25–1	11	250–400	10	20	12.5	8/16	10–33	(Decomp'd 743, High Speed)	1282
Duals												
AD822	0.5	70	0.5–1	10	5–10	1.8	2	3.5		10–57	Rail-to-Rail Output Stage	1407
AD648	0.076	2	3–20	20	10–20	0.4	0.8	1	8	10–23		1213
AD823	0.02	60	0.8	20	25	8.4	12	14	8	10–59	Rail-to-Rail Output	1907
AD647	0.1	76	0.25–1	10	25–50	2.8	1	3	8	10–21		1212
AD642	0.1	76	0.5–2	NS	35–75	2.8	1	2	8	10–21		1209
AD644	0.03	76	0.5–2	NS	35–75	4.5	2	8	8	10–21		1210
AD712	0.15	76	0.3–3	20	50–75	6.8	3	16	8	10–27		1253
OP249	0.5	76	0.3–2	25	50–75	7	3.5	18	8	10–143		1686
OP250	TBD	60	5	TBD	60	1	5	2	8	*	Rail-to-Rail In/Out, CMOS	1950
OP297	0.8	110	0.05–0.2	2	100–200	1.25	0.5	0.05	8	10–159		1699
AD706	0.2	110	0.05–0.1	1.5	110–220	1.2	0.8	0.15	8	10–25		1246
AD746	0.08	78	1–1.5	20	150–250	10	16	45	8	10–35		1283
AD8532	TBD	60	5	TBD	250	1	5	3.4	8	10–105	Rail-to-Rail In/Out, CMOS	1980
OP282	0.070	3	10	100	500	0.5	4	7	8	10–153	CMV to + Rail	1692

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Operational Amplifiers–Selection Guides

Low Bias Current

Model	Open-Loop Gain V/μV	Common-Mode Rejection CMRR dB	Initial Offset E_{OS} ±mV max	E_{OS} vs. Temp ±μV/°C	I_B +25°C max ±pA	Supply Current I_Q mA	Unity Gain MHz	Slew Rate V/μs	# Pins	Page No.	Comments	Fax-code
Quads												
AD704	0.2	110	0.075–0.1	1.5	110–220	2.4	0.8	0.1	14/16	10–25		1244
OP497	1.2	114	0.05–0.15	1.5	200	2.5	0.5	0.05	14	10–169		1716
AD824	0.02	66	1	20	25	2.4	2	2	14	10–61	Rail-to-Rail Output Stage	1810
OP450	TBD	60	5	TBD	60	2	5	2	14	*	Rail-to-Rail In/Out, CMOS	1950
AD713	0.15	78	0.5–1.5	20	75–150	13.5	3	16	14/16	10–27		1254
OP482	0.070	3	20	100	500	1	4	7	14	10–153	CMV to + Rail	1711

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Precision

Model	Open-Loop Gain V/μV	Common-Mode Rejection CMRR dB	Initial Offset E_{OS} ±μV	E_{OS} vs. Temp ±μV/°C	I_B +25°C max ±nA	e_{NOISE} nV√Hz @ 1 kHz	Supply Current I_Q mA	Unity Gain MHz	# Pins	Page No.	Comments	Fax-code
Singles												
OP177	2	115–130	20–60	0.6	1.5–2.8	11	2	0.4	8	10–129	Ind. Std., Low Drift, 3rd Generation	1674
AD797	1	114	40–80	1	900–1500	1.2	10.5	20	8	10–39	Extremely Low Noise, 600 ns to 16 Bits	1394
OP77	2	106–120	25–100	1.2	2–2.8	4.7	2	0.5	8	10–119	Ind. Std., Low Drift, 2nd Generation	1720
OP113	1	96–100	75–150	1.5	600	4.7	2	3.4	8	10–123	Input & Output Pull Down to Zero Volts	1666
OP193	0.5	97	75–150	1.5	20	65	0.022	0.03	8	10–137	Rail-to-Rail Output	1856
OP27	0.7	100–114	25–100	1.8	40–80	3.7	4.7	5	8	10–113		1688
OP37	0.7	100	25–100	1.8	40–80	4.7	4.7	3	8	10–115		1701
OP07	0.12	94–106	75–150	2.5	4–12	11	4	0.4	8	10–111	Ind. Std., Low Drift, 1st Generation	1662
AD840	0.04	90–106	300–1000	10	0.7–1.5	4	14	400 A_V–10	8/20	*		1416
OP176	0.25	80	1000	5	350	6	2.5	10	8	10–127	Butler Input Stage	1673
AD841	0.04	86–103	1000	10	3.3–5	15	12	40	8/16/20	*		1418
AD842	0.04	86–103	1500	10	1.5–2.5	9	14	80 A_V = 2	8/16/20	10–71		1419
Duals												
AD708	3–8	120–130	90–15	1–0.1	2.5–1	9.6	5.8	0.5	8	*	Highest Performance	1248
OP200	1.5	110–120	75–200	2	2–5	11	1.45	0.5	8	10–141		1677
OP213	1	96–100	75–150	1.5	600	4.7	4	3.4	8	10–123	Input & Output Pull Down to Zero Volts	1666
OP227	0.7	100–114	80–180	1.8	40–80	3.8	4.7	5	8	*		1685
OP284	0.15	86	100–175	1–1.5	300	3.9	3.5	4.25	8	10–133	Rail-to-Rail Input & Output	1871
OP293	0.5	96–100	100–250	1–2	15–20	65	0.06	0.025	8	10–137	Rail-to-Rail Output	1856
OP270	1.5	90–106	75–250	1–3	20–60	5	6.5	5	8	10–145		1689
OP271	0.2	90–106	200–400	5	20–60	7.6	6.5	5	8	10–147		1690
OP285	0.5	80	250	5	350	7	4	9	8	10–155	Butler Input Stage	1694
OP295	1	90	500	10	20	51	0.3	0.08	8	10–157		1698
OP275	0.2	86	1000	20	150	7	4	8	8	10–149	Butler Input Stage	1691
Quads												
OP484	0.15	86	100–175	1	300	3.9	7	4.25	14	10–133	Rail-to-Rail Input & Output	1871
OP413	1	96–100	125–275	2	600	4.7	2	3.4	14/16	10–123	Input & Output Pull Down to Zero Volts	1505
OP493	0.5	96–100	125–275	4	15–20	65	0.12	0.01	14/16	10–137	Rail-to-Rail Output	1856
OP400	0.8	110–120	150–300	2.5	3–7	11	2.9	0.5	14/16	10–161	Quad OP07	1702
OP470	0.8	100–110	400–1000	15	25–60	5	4.7	6	14	10–165		1709
OP495	1	90	500	10	20	51	0.6	0.08	14/16	10–157		1698
OP471	0.3	100–105	800–1800	15	25–60	5	4.7	6.5	14	10–167		1710

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Operational Amplifiers–Selection Guides

High Speed

Model	Feedback Type	BW –3 dB MHz min	Gain Flatness 0.1 dB MHz	Slew Rate V/μs	Settling Time 0.10% ns	E_{OS} +25°C mV	I_B μA	I_{OUT} mA	I_Q mA	# Pins	Page No.	Comments	Fax-code
Singles													
Note: ±15 V Rails Amplifiers Also Specified at ±5 V													
AD8011	I	340	20	3500	25	5	15	15	1	8	10–85	±5 Rails, Very Low Power	1863
AD811	I	140	35	2500	50	3	15	100	18	8	10–43	±15 Rails	1401
AD9618	I	130		1800	10	2.2	45	60	43	8	*	±5 Rails, A_V = 2	1465
AD8015	I	180	NS	1500	3 to 3%	NA	NA	20	26	8	10–89	155 MHz Photodiode Preamp	1833
AD9617	I	145	NS	1400	10	2.2	50	60	48	8	*	±5 Rails	1464
AD844	I	60	NS	1200	100	0.3	1.5	20	7.5	8/16	*	±15 Rails	1421
AD9632	V	250	130	1200	11	5	7	70	18	8	10–107	±5 Rails, A_V = 2	1468
AD810	I	55	15	1000	50	6	5	40	8	8	10–41	±15 Rails, with Disable	1400
AD9631	V	220	130	1000	11	10	7	70	17	8	10–107	±5 Rails	1468
AD8001	I	650	85	960	10	5.5	25	50	5.5	8	10–79	±5 Rails	1396
AD8048	V	180	50	740	13	3	3.5	50	6.6	8	10–101	±5 Rails, A_V = 2 min	1868
ADEL2020	I	90	25	500	60	7.5	15	30	10	8/20	*	±15 Rails, with Disable	1491
AD8047	V	170	35	475	13	3	3.5	50	6.6	8	10–101	±5 Rails	1868
AD818	V	100	40	450	45	2	6.6	50	7.5	8	10–55	±15 Rails, A_V = 2 min	1405
AD846	I	80	NS	450	80	0.2	0.45	20	6.5	8/16	10–77	±15 Rails	1423
AD830	V	75	11	360	35	3	10	50	17	8	10–69	±15 Rails, Diff. Input Video Rcv	1412
AD840	V	40	NS	350	80	1	8	50	14	8/20	*	±15 Rails, A_V = 10 min	1416
AD817	V	45	40	300	45	2	6.6	50	7.5	8	10–53	±15 V Rails, Stable with Any Cap Load	1404
AD842	V	40	NS	300	80	1.5	8	100	14	8/16/20	10–71	±15 V Rails, A_V = 2 min	1419
AD829	V	750	NS	230	90 @ A_V = 19	1	7	20	6.8	8	10–67	±15 V Rails, Externally Compensated, Low e_{NOISE} –1.7 nV/√Hz	1411
AD847	V	50	NS	225	65	1	6.6	20	6	8	*	±15 V Rails, Stable with Any Cap Load	1424
AD848	V	175	NS	225	100	2.3	6.6	20	6	8	*	±15 V Rails, Stable with Any Cap Load	1425
AD849	V	725	NS	225	80	1	6.6	20	6	8	*	±15 V Rails, Stable with Any Cap Load	1425
AD841	V	40	NS	200	90	2	8	50	12	8/16/20	*	±15 Rails	1418
AD843	V	34	NS	160	95	2	0.0025	50	13	8/12/16	10–73	±15 V Rails, FET Input Stage	1420
AD8041	V	140	32	140	50	7	3	50	6.5	8	10–95	Rail-to-Rail Out, with Disable, +3, +5 or ±5 Rails	1925
AD845	V	12.8	NS	80	250	1.5	0.002	50	12	8/16	10–75	FET Input Stage	1422
AD8031	V	80	14	30	125	1	1	20	0.9	8	10–91	Rail-to-Rail In/Out, +2.5, +5 or ±5 Rails	1983
Buffers													
BUF04	V	110	NS	2000	60	1	5	50	8.5	8	10–109	±15 Rails	1613
AD9630	V	600	NS	1.2/1.5	16	8	35	50	48	8	*	±5 Rails	1467

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Model	Feedback Type	BW –3 dB MHz min	Gain Flatness 0.1 dB MHz	Slew Rate V/μs	Settling Time 0.10% ns	E_{OS} +25°C mV	I_B μA	I_{OUT} mA	I_Q mA	# Pins	Page No.	Comments	Fax-code
Clamp Amplifiers													
AD8037	V	200	130	1100	10	7	70	70	20	8	10–93	Clamp Mode, Noninverting Only, A_V = 2 min	1836
AD8036	V	150	130	900	10	7	60	70	20	8	10–93	Clamp Mode, Noninverting Only, A_V = 1 min	1836
Duals													
AD812	I	75	25	1400	40	5	20	40	11	8	10–45	±15 Rails	1402
AD8002	I	600	60	1200	12	6	25	70	12	8	10–81	IMD @ 10 MHz = 33 dBm, SFDR @ 5 MHz = –66 dB	1834
AD815	I	100	40	900	70	15	90	500	40	15	10–49	Balanced Diff. Input/Output	1938
AD8072	I	60	10	400	20	5	NS	30	6	8	10–103	±5 V or +5 V Rails	1977
AD828	V	100	30	400	45	2	6.6	50	NS	8	10–65	±15 Rails	1410
AD826	V	45	25	300	45	2	6.6	50	15	8	10–63	Stable with Any Cap Load	1408
AD827	V	50	NS	300	120	4	7	20	6	8	*	Stable with Any Cap Load	1409
AD8042	V	125	18	145	32	9.8	4.8	50	7	8	10–97	Rail-to-Rail Out, +3, +5 or ±5 Rails	1929
AD8032	V	80	14	30	125	1	1	20	1.8	8	10–91	Rail-to-Rail In/Out, +2.5, +5 or ±5 Rails	1984
Triples													
AD8013	I	110	60	600	18	5	7	25	12	14	10–87	With Disable/Amp, Can Drive 200 pF Load	1939
AD8073	I	60	10	400	20	5	TBD	30	6	14	10–103		1977
AD813	I	75	25	150	40	5	30	30	17	14	10–47	±15 Rails, with Disable/Amp	1403
Quads													
AD8004	I	250	30	3000	21	3.5	110	50	17	14	10–83	±5 V Rails	1835
AD816†	I	100	40	900	70	15	90	500	40	15	10–51	Diff. Transceiver, Drive Side Spec	1978
AD816‡	V	100	NS	150	NS	1	5	10	40	15	10–51	Receive Side Spec	1978
AD8044	V	85	1	150	40	6.5	4.5	30	14	14	10–99	Rail-to-Rail Out, +3, +5 or ±5 Rails	1940
OP467	V	28	NS	125	NS	0.5	0.6	20	10	14	10–163	±15 Rails	1708
High Current Drive													
AD815	I	100	40	900	70	15	90	500	40	15	10–49	Balanced Diff. Input/Output	1938
AD816†	I	100	40	900	70	15	90	500	40	15	10–51	Diff. Transceiver, Drive Side Spec	1978
AD816‡	V	100	NS	150	NS	1	5	10	40	15	10–51	Receive Side Spec	1978
AD811	I	140	35	2500	50	3	15	100	18	8	10–43	±15 Rails	1401

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†As a Driver
‡As a Receiver

Operational Amplifiers–Selection Guides

Single Supply

Singles

Model	Min Supply Volts	Open-Loop Gain V/μV	Common-Mode Rejection CMRR dB	Slew Rate V/μs	Initial Offset E_{OS} ±mV max	E_{OS} vs. Temp ±μV/°C	I_B +25°C max ±nA	I_Q +25°C max mA	I_{OUT} mA	# Pins	Page No.	Comments	Fax-code
Rail-to-Rail Input & Output													
AD8031	+5	NS	NS	30	1	2	1000	0.9	20	8	10–91	Current Feedback	1983
OP150	+3	TBD	60	5	5	TBD	60 pA	0.5	250	8	*	CMOS	1950
SSM2211	+2.7	TBD	60	3.4	5	TBD	250 pA	1	250	8	*	Audio Power Amp	1979
OP191	+5	0.025	70	0.4	0.5	15	50	0.4	5	8	10–135		1809
OP196	+3	0.1	60	0.3	0.3	5	30	0.05	4	8	10–139	Very Low Power	1926
OP184	+3	NS	60	2.5	0.125	1	300	1.1	NS	8	10–133		1871
Rail-to-Rail Output													
AD8041	+3	92 dB	80	120	3	40	2500	5.5	30	8	10–95	Wide Bandwidth	1925
OP162	+5	0.03	TBD	11	2	TBD	600	0.65	25	8	10–125		1951
AD820	+3	0.3	60	3	1	20	25 pA	0.8	10	8	10–57	Input CMV Range, 0–1 V	1406
Zero Input, Zero Output													
OP183	+3	0.1	70	5	1	20	0.6	1.5	25	8	10–131	0–2 V_{OUT}	1675
OP113	+5	2	90	0.6	0.175	4	650	1.75	30	8	10–123	0–4 V_{OUT}	1666
OP193	+2	0.06	NS	0.01	0.15	1.5	20	0.02	+1	8	10–137	Very Low Power, 0–2 V	1856

Duals

Rail-to-Rail Input & Output													
AD8032	+2.5	NS		14	1	2	1000	1.8	20	8	10–91	Current Feedback	1984
OP250	+3	TBD	60	5	5	TBD	60 pA	1	250	8	*	CMOS	1950
AD8532	+3	TBD	60	3.4	5	TBD	250 pA	1	250	8	10–105	CMOS	1980
OP279	+5	0.1	56	3	4	4	600	3.5	50	8	10–151	Audio Headphone Amp	1811
OP284	+3	NS	60	2.5	0.125	1	300	2.3	NS	8	10–133	OP27 Type Performance	1871
OP291	+3	0.025	70	0.4	0.7	5	50	0.7		8	10–135		1696
OP296	+3	0.1	60	0.3	0.3	5	30	0.1	4	8	10–139	Very Low Power	1926
Rail-to-Rail Output													
AD8042	+3	92 dB	80	120	3	40	2500	11	30	8	10–97	Voltage Feedback	1929
OP262	+5	0.03	TBD	11	2	TBD	600	1.3	25	8	10–125		1951
AD823	+3.3	0.015	54	13	1.5	20	25 pA	5.7	↓	8	10–59	JFET	1907
AD822	+3	0.3	60	3	1	20	25 pA	1.6	10	8	10–57	Input CMV Range, 0–1 V	1407
OP295	+3	0.75	90	0.03	NS	NS	20	0.3	NS	8	10–157	Low Power	1698

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Model	Min Supply Volts	Open-Loop Gain V/μV	Common-Mode Rejection CMRR dB	Slew Rate V/μs	Initial Offset E_{OS} ±mV max	E_{OS} vs. Temp ±μV/°C	I_B +25°C max ±nA	I_Q +25°C max mA	I_{OUT} mA	# Pins	Page No.	Comments	Fax-code
Zero Input, Zero Output													
OP283	+3	0.1	70	5	1	20	0.6	1.5	25	8	10–131	0–2 V_{OUT}	1693
OP292	+5	0.025	75	1.5	0.8	15	700	2.4	5	8	*	0–4 V_{OUT}	1697
OP213	+5	2	90	0.6	0.3	5	650	1.75	30	8	10–123	0–4 V_{OUT}	1680
SSM2135	+5	2	87	0.6	2	NS	750	4	30	8	16–17	0–4 V_{OUT}	1794
OP293	+2	0.06	94	0.01	0.25	2	20	0.04	+1	8	10–137	Very Low Power, 0–2 V_{OUT}	1856
													Quads
Rail-to-Rail Input & Output													
OP450	+3	TBD	60	5	5	TBD	60 pA	2	250	14	*	CMOS	1950
OP484	+3	0.05	60	2.5	0.125	1	300	2.3	NS	14	10–133	OP27 Type Performance	1871
OP491	+3	0.025	70	0.4	0.7	5	50	0.7		14	10–135		1696
Rail-to-Rail Output													
AD8044	+3	0.09	80	120	3	40	2500	11	30	14	10–99	Wide Bandwidth	1940
OP462	+5	0.03	TBD	11	2	TBD	600	2.6	25	14	10–125		1951
AD824	+3	0.25	60	3	1	20	25 pA	1.6	8	14	10–61	Input CMV Range, 0–1 V	1810
OP496	+3	0.1	60	0.3	0.3	5	30	0.2	5	14	10–139	Very Low Power	1926
OP495	+3	0.75	90	0.03	0.3	5	20	0.3	11	14/16	10–157		1698
Zero Input, Zero Output													
OP492	+5	0.025	75	1.5	1	25	700	4.8	5	14	*	0–4 V_{OUT}	1714
OP413	+5	2	90	0.6	0.325	5	650	1.75	30	14/16	10–123	0–4 V_{OUT}	1704
OP493	+2	0.06	94	0.01	0.275	5	20	0.09	+1	14/16	10–137	Very Low Power, 0–1 V_{OUT}	1856

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Operational Amplifiers–Selection Guides

Low Power†

Model	Min Rail Volts	Open-Loop Gain V/μV	Common-Mode Rejection CMRR dB	Initial Offset E_{OS} ±mV max	E_{OS} vs. Temp ±μV/°C	Total Supply Current I_Q μA	Slew Rate V/μs	Unity Gain MHz	# Pins	Page No.	Comments	Fax-code
Singles												
OP90	+5	0.4	80	0.45	5	15	0.005	NS	8	*		1722
OP193	+2	0.06	94	0.075	3	44	0.01	0.025	8	10–137	Input & Output Pull Down to V_{SS}	1856
OP196	+3	0.1	60	0.3	5	50	0.3	0.2	8	10–139	Rail-to-Rail Input & Output	1926
Duals												
OP290	+5	0.1	80	0.2–0.5	3–5	30	0.005	NS	8	*		1695
OP293	+2	0.06	NS	0.15	3	44	0.01	0.025	8	10–137	Input & Output Pull Down to V_{SS}	1856
OP296	+3	0.1	60	0.3	5	100	0.3	0.2	8	10–139	Rail-to-Rail Input & Output	1926
OP220	+5	0.3	75	0.75	3	135	0.05	NS	8	*		1683
OP295	+3	0.75 typ	90	0.5	5	300	0.03	0.075	8	10–157		1698
Quads												
OP490	+3 to 36	0.2	80	1	9	60	0.005	0.02	14/16	*		1712
OP493	+2	0.06	94	0.275	5	88	0.01	0.035	14/16	10–137	Input & Output Pull Down to V_{SS}	1856
OP420	+5	NS	83	6	25	200	0.25	0.15		*		1706
OP496	+3	0.1	60	0.3	5	200	0.3	0.2	14	10–139	Rail-to-Rail Input & Output	1926
OP495	+3	0.75 typ	90	0.5	5	600	0.03	0.075	14/16	10–157		1698

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.
†These amplifiers are also specified on the data sheet at ±6 V or ±15 V, +3 V & +5 V rails. They are depicted here at the minimum rail at which they are specified.

1 pA Monolithic Electrometer Operational Amplifier

AD546*

FEATURES

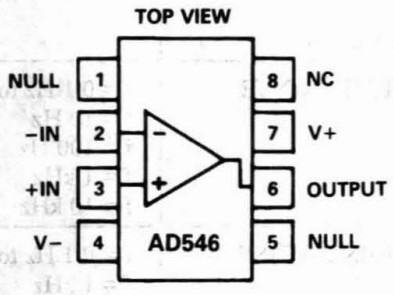
DC PERFORMANCE
- 1 mV max Input Offset Voltage
- Low Offset Drift: 20 μV/°C
- 1 pA max Input Bias Current
- Input Bias Current Guaranteed Over Full Common-Mode Voltage Range

AC PERFORMANCE
- 3 V/μs Slew Rate
- 1 MHz Unity Gain Bandwidth
- Low Input Voltage Noise: 4 μV p-p, 0.1 Hz to 10 Hz
- Available in a Low Cost, 8-Pin Plastic Mini-DIP
- Standard Op Amp Pinout

APPLICATIONS
- Electrometer Amplifiers
- Photodiode Preamps
- pH Electrode Buffers
- Log Ratio Amplifiers

CONNECTION DIAGRAM

8-Pin Plastic
Mini-DIP Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD546 is a monolithic electrometer combining the virtues of low (1 pA) input bias current with the cost effectiveness of a plastic mini-DIP package. Both input offset voltage and input offset voltage drift are laser trimmed, providing very high performance for such a low cost amplifier.

Input bias currents are reduced significantly by using "topgate" JFET technology. The 10^{15} Ω common-mode impedance, resulting from a bootstrapped input stage, insures that input bias current is essentially independent of common-mode voltage variations.

The AD546 is suitable for applications requiring both minimal levels of input bias current and low input offset voltage. Applications for the AD546 include use as a buffer amplifier for current output transducers such as photodiodes and pH probes. It may also be used as a precision integrator or as a low droop rate sample and hold amplifier. The AD546 is pin compatible with standard op amps; its plastic mini-DIP package is ideal for use with automatic insertion equipment.

The AD546 is available in two performance grades, all rated over the 0°C to +70°C commercial temperature range, and packaged in an 8-pin plastic mini-DIP.

*Protected by Patent No. 4,639,683.

PRODUCT HIGHLIGHTS

1. The input bias current of the AD546 is specified, 100% tested and guaranteed with the device in the fully warmed-up condition.
2. The input offset voltage of the AD546 is laser trimmed to less than 1 mV (AD546K).
3. The AD546 is packaged in a standard, low cost, 8-pin mini-DIP.
4. A low quiescent supply current of 700 μA minimizes any thermal effects which might degrade input bias current and input offset voltage specifications.

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AD546–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
INPUT BIAS CURRENT								
Either Input	V_{CM} = 0 V		0.2	**1**		0.2	**0.5**	pA
Either Input	V_{CM} = ±10 V		0.2	1		0.2	0.5	pA
Offset Current	V_{CM} = 0 V		0.17			0.09		pA
INPUT OFFSET VOLTAGE								
Initial Offset				**2**			**1**	mV
vs. Temperature			20			20		µV/°C
vs. Supply				**100**			**100**	µV/V
Long-Term Stability			20			20		µV/Month
INPUT VOLTAGE NOISE	f = 0.1 Hz to 10 Hz		4			4		µV p-p
	f = 10 Hz		90			90		nV/√Hz
	f = 100 Hz		60			60		nV/√Hz
	f = 1 kHz		35			35		nV/√Hz
	f = 10 kHz		35			35		nV/√Hz
INPUT CURRENT NOISE	f = 0.1 Hz to 10 Hz		1.3			1.3		fA rms
	f = 1 kHz		0.4			0.4		fA/√Hz
OPEN LOOP GAIN	V_O = ±10 V							
	R_{LOAD} = 10 kΩ	**300**	1000		**300**	1000		V/mV
	V_O = ±10 V							
	R_{LOAD} = 2 kΩ	**100**	250		**100**	250		V/mV
INPUT VOLTAGE RANGE								
Differential			±20			±20		V
Common-Mode Voltage		**–10**		**+10**	**–10**		**+10**	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	**80**	90		**84**	100		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} = 10 kΩ	**–12**		**+12**	**–12**		**+12**	V
	R_{LOAD} = 2 kΩ	**–10**		**+10**	**–10**		**+10**	V
Current	Short Circuit	**15**	20	35	**15**	20	35	mA
Load Capacitance Stability	Gain = +1		4000			4000		pF
FREQUENCY RESPONSE								
Gain BW, Small Signal	G = –1	0.7	1.0		0.7	1.0		MHz
Full Power Response	V_O = 20 V p-p		50			50		kHz
Slew Rate, Unity Gain	G = –1	2	3		2	3		V/µs
Settling Time	to 0.1%		4.5			4.5		µs
	to 0.01%		5			5		µs
Overload Recovery	50% Overdrive							
	Gain = –1		2			2		µs
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			0.60	**0.7**		0.60	**0.7**	mA
Transistor Count	# of Transistors		50			50		
PACKAGE OPTIONS*								
Plastic Mini-DIP (N-8)			AD546JN			AD546KN		

*For outline information see Package Information section.

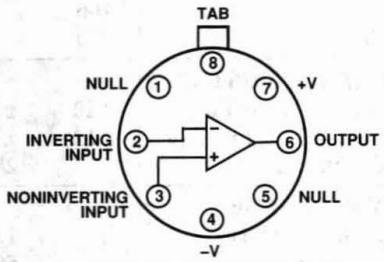
Specifications subject to change without notice.

High Performance, BiFET Operational Amplifiers

AD547/AD542/AD544

FEATURES
Ultralow Drift: 1 μV/°C (AD547L)
Low Offset Voltage: 0.25 mV (AD547L)
Low Input Bias Currents: 25 pA max
Low Quiescent Current: 1.5 mA
Low Noise: 2 μV p-p
High Open Loop Gain: 110 dB
High Slew Rate: 13 V/μs
Fast Settling to ±0.01%: 3 μs
Low Total Harmonic Distortion: 0.0025%
Available in Hermetic Metal Can and Die Form
Dual Versions Available: AD642, AD644, AD647

CONNECTION DIAGRAM



NOTE: PIN 4 CONNECTED TO CASE

PRODUCT DESCRIPTION

The BiFET series of precision, monolithic FET-input op amps are fabricated with the most advanced BiFET and laser trimming technologies. The AD542, AD544, AD547 series offers bias currents significantly lower than currently available BiFET devices, 25 pA max, warmed up.

In addition, the offset voltage is laser trimmed to less than 0.25 mV on the AD547L, which is achieved by utilizing Analog Devices' exclusive laser wafer trimming (LWT) process. When combined with the AD547's low offset drift (1 μV/°C), these features offer the user performance superior to existing BiFET op amps at low BiFET pricing.

The AD542 or AD547 is recommended for any operational amplifier application requiring excellent dc performance at low to moderate cost. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common-mode rejection (80 dB, min on the "K" and "L" grades) and high open-loop gain, even under heavy loading, ensures better than "12-bit" linearity in high impedance buffer applications.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing results in the lowest bias current available in a monolithic FET op amp.
2. Advanced laser wafer trimming techniques reduce offset voltage drift to 1 μV/°C max and offset voltage to only 0.25 mV max on the AD547L.
3. Low voltage noise (2 μV p-p) and low offset voltage drift enhance performance as a precision op amp.
4. High slew rate (13 V/μs) and fast settling time to 0.01% (3 μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
5. Low harmonic distortion (0.0025%) make the AD544 an ideal choice in audio applications.

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ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Settling Time to ±0.012% for a 10 V Step	Package Description	Package Option*
AD542JH	2.0 mV	20 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542KH	1.0 mV	10 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542LH	0.5 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD542SH	1.0 mV	15 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD544JH	2.0 mV	20 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544KH	1.0 mV	10 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544LH	0.5 mV	5 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD544SH	1.0 mV	15 μV/°C	3 μs	8-Pin Hermetic Metal Can	H-08A
AD547JH	1.0 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547KH	0.5 mV	2 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547LH	0.25 mV	1 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A
AD547SH/883B	0.5 mV	5 μV/°C	5 μs	8-Pin Hermetic Metal Can	H-08A

*For outline information see Package Information section.

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AD547/AD542/AD544–SPECIFICATIONS ($V_S = \pm 15$ V @ $T_A = +25°C$ unless otherwise noted)

Parameter	AD542 Min	AD542 Typ	AD542 Max	AD544 Min	AD544 Typ	AD544 Max	AD547 Min	AD547 Typ	AD547 Max	Units
OPEN-LOOP GAIN										
$V_{OUT} = \pm 10$ V, $R_L = 2$ kΩ										
J Grade	**100**			**30**			**100**			V/mV
K, L, S Grades	**250**			**50**			**250**			V/mV
$T_A = T_{MIN}$ to T_{MAX}										
J Grade	100			20			100			V/mV
S Grade	**100**			**20**			**100**			V/mV
K, L Grades	**250**			**40**			**250**			V/mV
OUTPUT CHARACTERISTICS										
$R_L = 2$ kΩ $T_A = T_{MIN}$ to T_{MAX}	**±10**	±12		**±10**	±12		**±10**	±12		V
$R_L = 10$ kΩ $T_A = T_{MIN}$ to T_{MAX}	**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2.0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**8.0**	13.0		**2.0**	3.0		V/μs
INPUT OFFSET VOLTAGE										
J Grade			**2.0**			**2.0**			**1.0**	mV
K Grade			**1.0**			**1.0**			**0.5**	mV
L Grade			**0.5**			**0.5**			**0.25**	mV
S Grade			**1.0**			**1.0**			**0.5**	mV
vs. Temperature										
J Grade			20			20			**5**	μV/°C
K Grade			**10**			**10**			**2**	μV/°C
L Grade			**5**			**5**			**1**	μV/°C
S Grade			**15**			**15**			**5**	μV/°C
INPUT BIAS CURRENT										
Either Input										
J Grade			**50**			**50**			**50**	pA
K, L, S Grades		10	**25**		10	**25**		10	**25**	pA
Input Offset Current										
J Grade		5	**15**		5	**15**		5	**15**	pA
K, L, S Grades		2	**15**		2	**15**		2	**15**	pA
INPUT VOLTAGE										
Differential		±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		V
Common-Mode Rejection										
$V_{IN} = \pm 10$ V										
J Grade	**76**			**76**			**76**			dB
K, L, S Grades	**80**			**80**			**80**			dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current		1.1	**1.5**		1.8	**2.5**		1.1	**1.5**	mA
VOLTAGE NOISE										
0.1 Hz to 10 Hz										
J Grade		2.0			2.0			2.0		μV p-p
K, L, S Grades		2.0			2.0				**4.0**	μV p-p
10 Hz		70			35			70		$nV/\sqrt{Hz}$
100 Hz		45			22			45		$nV/\sqrt{Hz}$
1 kHz		30			18			30		$nV/\sqrt{Hz}$
10 kHz		25			16			25		$nV/\sqrt{Hz}$
TEMPERATURE RANGE										
Operating, Rated Performance										
J, K, L Grades		0 to +70			0 to +70			0 to +70		°C
S Grade		–55 to +125			–55 to +125			–55 to +125		°C

Specifications subject to change without notice.

ANALOG DEVICES

Precision, Low Power BiFET Op Amp

AD548

FEATURES

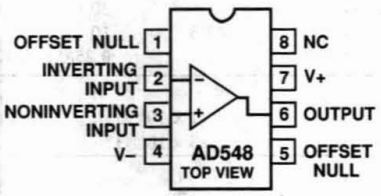
Enhanced Replacement for LF441 and TL061
DC Performance:
- **200 μA max Quiescent Current**
- **10 pA max Bias Current, Warmed Up (AD548C)**
- **250 μV max Offset Voltage (AD548C)**
- **2 μV/°C max Drift (AD548C)**
- **2 μV p-p Noise, 0.1 Hz to 10 Hz**

AC Performance:
- **1.8 V/μs Slew Rate**
- **1 MHz Unity Gain Bandwidth**

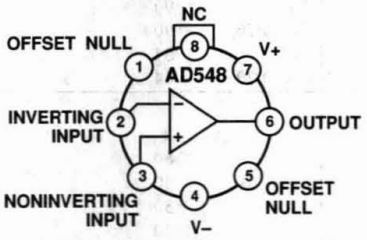
Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages and in Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Dual Version Available: AD648
Surface Mount (SOIC) Package Available

CONNECTION DIAGRAMS

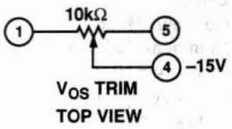
Plastic Mini-DIP (N) Package, Cerdip (Q) Package and SOIC (R) Package



TO-99 (H) Package



NOTE : PIN 4 CONNECTED TO CASE
NC = NO CONNECT



PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It offers both low bias current (10 pA max, warmed up) and low quiescent current (200 μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2 mV and an input offset voltage drift of less than 20 μV/°C. The C grade reduces input offset voltage to less than 0.25 mV and offset voltage drift to less than 2 μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Four additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86 dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in six performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0°C to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of –40°C to +85°C. The AD548S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, surface mount (SOIC), or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high performance, low power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2 mV max) and drift (20 μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. Enhanced replacement for LF441 and TL061.

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AD548—SPECIFICATIONS (@ +25°C and V_S = ±15 V dc unless otherwise noted)

Model	AD548J/A/S			AD548K/B			AD548C			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	2.0		0.3	0.5		0.10	0.25	mV
T_{MIN} to T_{MAX}			3.0/3.0/3.0			0.7/0.8			0.4	mV
vs. Temperature			20			5			2.0	µV/°C
vs. Supply	80			86			86			dB
vs. Supply, T_{MIN} to T_{MAX}	76/76/76			80			80			dB
Long-Term Offset Stability		15			15			15		µV/Month
INPUT BIAS CURRENT										
Either Input[2], V_{CM} = 0		5	20		3	10		3	10	pA
Either Input[2] at T_{MAX}, V_{CM} = 0			0.45/1.3/20			0.25/0.65			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			30			15			15	pA
Offset Current, V_{CM} = 0		5	10		2	5		2	5	pA
Offset Current at T_{MAX}			0.25/0.65/10			0.15/0.35			0.35	nA
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	±11	±12		±11	±12		±11	±12		V
Common-Mode Rejection										
V_{CM} = ±10 V	76	90		82	92		86	98		dB
T_{MIN} to T_{MAX}	76/76/76	90		82	92		86	98		dB
V_{CM} = ±11 V	70	84		76	86		76	90		dB
T_{MIN} to T_{MAX}	70/70/70	84		76	86		76	90		dB
INPUT VOLTAGE NOISE										
Voltage 0.1 Hz to 10 Hz		2			2			2	4.0	µV p-p
f = 10 Hz		80			80			80		$nV/\sqrt{Hz}$
f = 100 Hz		40			40			40		$nV/\sqrt{Hz}$
f = 1 kHz		30			30			30		$nV/\sqrt{Hz}$
f = 10 kHz		30			30			30		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE										
f = 1 kHz		1.8			1.8			1.8		$fA/\sqrt{Hz}$
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	1.0	1.8		1.0	1.8		1.0	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN										
V_O = ±10 V, $R_L \geq$ 10 kΩ	300	1000		300	1000		300	1000		V/mV
T_{MIN} to T_{MAX}, $R_L \geq$ 10 kΩ	300/300/300	700		300	700		300	700		V/mV
V_O = ±10 V, $R_L \geq$ 5 kΩ	150	500		150	500		150	500		V/mV
T_{MIN} to T_{MAX}, $R_L \geq$ 5 kΩ	150/150/150	300		150	300		150	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq$ 10 kΩ,	±12	±13		±12	±13		±12	±13		V
T_{MIN} to T_{MAX}	±12/±12/±12			±12			±12			
Voltage @ $R_L \geq$ 5 kΩ,	±11	±12.3		±11	±12.3		±11	±12.3		V
T_{MIN} to T_{MAX}	±11/±11/±11			±11			±11			
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		170	200		170	200		170	200	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0°C to +70°C)		AD548J			AD548K					
Industrial (–40°C to +85°C)		AD548A			AD548B			AD548C		
Military (–55°C to +125°C)		AD548S								
PACKAGE OPTIONS[4]										
SOIC (R-8)	AD548JR			AD548KR, AD548BR						
Plastic (N-8)	AD548JN			AD548KN						
Cerdip (Q-8)	AD548AQ							AD548CQ		
Metal Can (H-08A)	AD548AH			AD548BH						
Tape and Reel	AD548JR-REEL			AD548KR-REEL, AD548BR-REEL						
Chips Available	AD548JCHIPS									

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Defined as voltages between inputs, such that neither exceeds ±10 V from ground.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

Ultralow Input Bias Current Operational Amplifier

AD549*

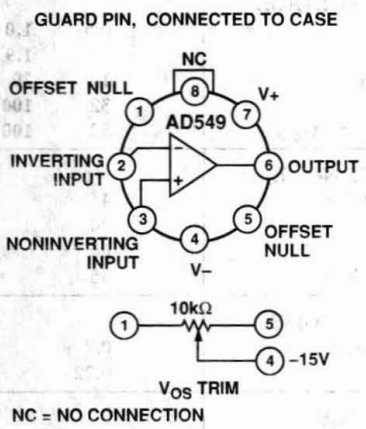
FEATURES

Ultralow Bias Current: 60 fA max (AD549L)
250 fA max (AD549J)
Input Bias Current Guaranteed Over Common-Mode Voltage Range
Low Offset Voltage: 0.25 mV max (AD549K)
1.00 mV max (AD549J)
Low Offset Drift: 5 μV/°C max (AD549K)
20 μV/°C max (AD549J)
Low Power: 700 μA max Supply Current
Low Input Voltage Noise: 4 μV p-p 0.1 Hz to 10 Hz
MIL-STD-883B Parts Available

APPLICATIONS

Electrometer Amplifiers
Photodiode Preamp
pH Electrode Buffer
Vacuum Ion Gage Measurement

CONNECTION DIAGRAM



NC = NO CONNECTION

PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" FET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The 10^{15} Ω common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

Protected by Patent No. 4,639,683.

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range 0°C to +70°C. The S grade is specified over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. Plus screening includes 168-hour burn-in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25 mV and 5 μV/°C (AD549K), 1 mV and 20 μV/°C (AD549J).
3. A maximum quiescent supply current of 700 μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1 MHz unity gain bandwidth and 3 V/μs slew rate. Settling time for a 10 V input step is 5 μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.

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AD549—SPECIFICATIONS (@ +25°C and V_S = +15 V dc, unless otherwise noted)

Model	AD549J			AD549K			AD549L			AD549S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT BIAS CURRENT													
Either Input, V_{CM} = 0 V		150	**250**		75	**100**		40	**60**		75	**100**	fA
Either Input, V_{CM} = ±10 V		150	250		75	100		40	60		75	100	fA
Offset Current		50			30			20			30		fA
Offset Current at T_{MAX}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE													
Initial Offset		0.5	**1.0**		0.15	**0.25**		0.3	**0.5**		0.3	**0.5**	mV
Offset at T_{MAX}			**1.9**			**0.4**			**0.9**			**2.0**	mV
vs. Temperature		10	**20**		2	**5**		5	**10**		10	**15**	µV/°C
vs. Supply		32	**100**		10	**32**		10	**32**		10	**32**	µV/V
vs. Supply, T_{MIN} to T_{MAX}		32	**100**		10	**32**		10	**32**		32	**50**	µV/V
INPUT VOLTAGE NOISE													
f = 0.1 Hz to 10 Hz		4			4	**6**		4			4		µV p-p
f = 10 Hz		90			90			90			90		$nV/\sqrt{Hz}$
f = 100 Hz		60			60			60			60		$nV/\sqrt{Hz}$
f = 1 kHz to 10 kHz		35			35			35			35		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE													
f = 0.1 Hz to 10 Hz		0.7			0.5			0.36			0.5		fA rms
f = 1 kHz		0.22			0.16			0.11			0.16		$fA/\sqrt{Hz}$
INPUT IMPEDANCE													
Differential													
V_{DIFF} = ±1		$10^{13}\|\|1$			$10^{13}\|\|1$			$10^{13}\|\|1$			$10^{13}\|\|1$		Ω‖pF
Common Mode													
V_{CM} = ±10		$10^{15}\|\|0.8$			$10^{15}\|\|0.8$			$10^{15}\|\|0.8$			$10^{15}\|\|0.8$		Ω‖pF
OPEN-LOOP GAIN													
V_O @ ±10 V, R_L = 10 k	**300**	1000		**300**	1000		**300**	1000		**300**	1000		V/mV
V_O = ±10 V, R_L = 2 k	**100**	250		**100**	250		**100**	250		**100**	250		V/mV
INPUT VOLTAGE RANGE													
Differential			±20			±20			±20			±20	V
Common-Mode Voltage	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	V
Common-Mode Rejection Ratio													
V = +10 V, –10 V	**80**	90		**90**	100		**90**	100		**90**	100		dB
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 10 k,													
T_{MIN} to T_{MAX}	**–12**		**+12**	**–12**		**+12**	**–12**		**+12**	**–12**		**+12**	V
Voltage @ R_L = 2 k,													
T_{MIN} to T_{MAX}	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	V
Short Circuit Current	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	mA
Load Capacitance Stability													
G = +1		4000			4000			4000			4000		pF
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/µs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		µs
0.01%		5			5			5			5		µs
Overload Recovery,													
50% Overdrive, G = –1		2			2			2			2		µs
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	–55		+125	°C
PACKAGE OPTION													
TO-99 (H-08A)	AD549JH			AD549KH			AD549LH			AD549SH, AD549SH/883B			
Chips	AD549JCHIPS												

Specifications subject to change without notice.

ANALOG DEVICES

Low Noise, Low Drift FET Op Amp

AD645

FEATURES
Improved Replacement for Burr-Brown OPA-111 and OPA-121 Op Amp

LOW NOISE
2 μV p-p max, 0.1 Hz to 10 Hz
10 nV/√Hz max at 10 kHz
11 fA p-p Current Noise 0.1 Hz to 10 Hz

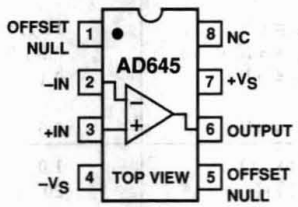
IMPROVED DRIFT

HIGH DC ACCURACY
250 μV max Offset Voltage
1 μV/°C max Drift
1.5 pA max Input Bias Current
114 dB Open-Loop Gain
Available in Plastic Mini-DIP, 8-Pin Header Packages, or Chip Form

APPLICATIONS
Low Noise Photodiode Preamps
CT Scanners
Precision I-V Converters

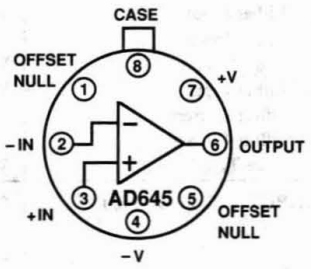
CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



NC = NO CONNECT

TO-99 (H) Package



NOTE: CASE IS CONNECTED TO PIN 8

PRODUCT DESCRIPTION

The AD645 is a low noise, precision FET input op amp. It offers the pico amp level input currents of a FET input device coupled with offset drift and input voltage noise comparable to a high performance bipolar input amplifier.

The AD645 has been improved to offer the lowest offset drift in a FET op amp, 1 μV/°C. Offset voltage drift is measured and trimmed at wafer level for the lowest cost possible. An inherently low noise architecture and advanced manufacturing techniques result in a device with a guaranteed low input voltage noise of 2 μV p-p, 0.1 Hz to 10 Hz. This level of dc performance along with low input currents make the AD645 an excellent choice for high impedance applications where stability is of prime concern.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD645JN	0°C to +70°C	N-8
AD645KN	0°C to +70°C	N-8
AD645AH	−40°C to +85°C	H-08A
AD645BH	−40°C to +85°C	H-08A
AD645CH	−40°C to +85°C	H-08A
AD645SH/883B	−55°C to +125°C	H-08A

NOTES
[1]Chips are also available.
[2]N = Plastic Mini-DIP; H = Metal Can. For outline information see Package Information section.

The AD645 is available in six performance grades. The AD645J and AD645K are rated over the commercial temperature range of 0°C to +70°C. The AD645A, AD645B, and the ultra-precision AD645C are rated over the industrial temperature range of −40°C to +85°C. The AD645S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B.

The AD645 is available in an 8-pin plastic mini-DIP, 8-pin header, or in die form.

PRODUCT HIGHLIGHTS

1. Guaranteed and tested low frequency noise of 2 μV p-p max and 20 nV/√Hz at 100 Hz makes the AD645C ideal for low noise applications where a FET input op amp is needed.
2. Low V_{OS} drift of 1 μV/°C max makes the AD645C an excellent choice for applications requiring ultimate stability.
3. Low input bias current and current noise (11 fA p-p 0.1 Hz to 10 Hz) allow the AD645 to be used as a high precision preamp for current output sensors such as photodiodes, or as a buffer for high source impedance voltage output sensors.

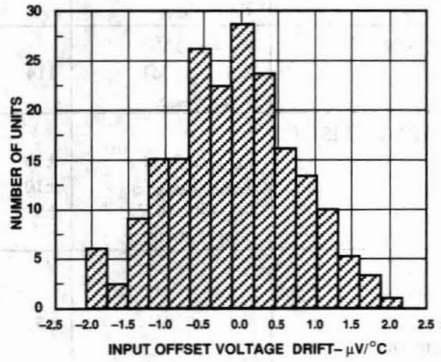


Figure 2. Typical Distribution of Average Input Offset Voltage Drift (196 Units)

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AD645–SPECIFICATIONS (@ +25°C, and ±15 V dc, unless otherwise noted)

Model	Conditions	AD645J/A			AD645K/B			AD645C			AD645S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]														
Initial Offset			100	500		50	250		50	250		100	500	µV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400		75	300		500	1500	µV
Drift (Average)			3	10/5		1	5/2		0.5	1		4	10	µV/°C
vs. Supply (PSRR)		90	110		94	110		94	110		90	110		dB
vs. Supply	T_{MIN}–T_{MAX}		100		90	100		90	100		86	95		dB
INPUT BIAS CURRENT[2]														
Either Input	V_{CM} = 0 V		0.7/1.8	3/5		0.7/1.8	1.5/3		1.8	3		1.8	5	pA
Either Input @ T_{MAX}	V_{CM} = 0 V		16/115			16/115			115			1800		pA
Either Input	V_{CM} = +10 V		0.8/1.9			0.8/1.9			1.9			1.9		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	0.5		0.1	1.0	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V		2/6			2/6			6			100		pA
INPUT VOLTAGE NOISE	0.1 to 10 Hz		1.0	3.0		1.0	2.5		1	2		1.0	3.3	µV p-p
	f = 10 Hz		20	50		20	40		20	40		20	50	nV/√Hz
	f = 100 Hz		10	**30**		10	**20**		10	**20**		10	**30**	nV/√Hz
	f = 1 kHz		9	15		9	12		9	12		9	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 to 10 Hz		11	20		11	15		11	15		11	20	fA p-p
	f = 0.1 thru 20 kHz		0.6	1.1		0.6	0.8		0.6	0.8		0.6	1.1	fA/√Hz
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	V_O = 20 V p-p													
	R_{LOAD} = 2 kΩ	16	32		16	32		16	32		16	32		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p-p													
	R_{LOAD} = 2 kΩ	1	2		1	2		1	2		1	2		V/µs
SETTLING TIME[3]														
To 0.1%			6			6			6			6		µs
To 0.01%			8			8			8			8		µs
Overload Recovery[4]	50% Overdrive		5			5			5			5		µs
Total Harmonic Distortion	f = 1 kHz, R_{LOAD} ≥ 2 kΩ, V_O = 3 V rms		0.0006			0.0006			0.0006			0.0006		%
INPUT IMPEDANCE														
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common-Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE														
Differential[5]			±20			±20			±20			±20		V
Common-Mode Voltage		±10	+11, –10.4		±10	+11, –10.4		±10	+11, –10.4		±10	+11, –10.4		V
Over Max Oper. Range		±10			±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		94	110		90	110		dB
	T_{MIN}–T_{MAX}		100		90	100		90	100		86	100		dB
OPEN-LOOP GAIN	V_O = ±10 V													
	R_{LOAD} ≥ 2 kΩ	114	130		120	130		120	130		114	130		dB
	T_{MIN}–T_{MAX}				114			114			110			dB
OUTPUT CHARACTERISTICS														
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
	T_{MIN}–T_{MAX}	±10			±10			±10			±10			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15			±15		mA
POWER SUPPLY														
Rated Performance			±15			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			3.0	3.5		3.0	3.5		3.0	3.5		3.0	3.5	mA
Transistor Count	# of Transistors		62			62			62			62		

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Gain = –1, R_{LOAD} = 2 kΩ.

[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.

[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

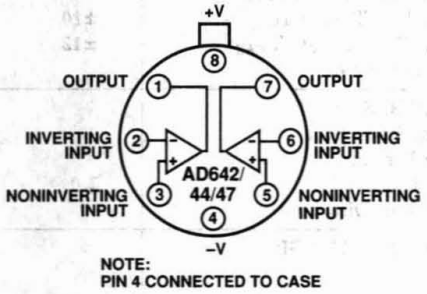
Dual, Low Cost, Precision BiFET Operational Amplifiers

AD647/AD642/AD644

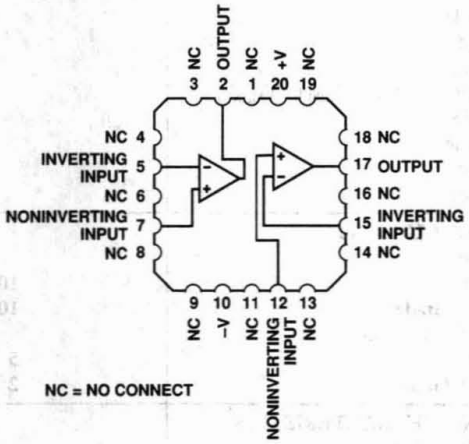
FEATURES

Matched Offset Voltage
Matched Offset Voltage over Temperature
Matched Bias Current
Crosstalk: –124 dB @ 1 kHz
Low Bias Current: 35 pA max (Warmed Up)
Low Offset Voltage: 250 μV max (AD647L)
Low Input Voltage Noise: 2.0 μV p-p
High Slew Rate: 13 V/μs (AD644)
Low Quiescent Current
Low Total Harmonic Distortion (0.0015%–AD644)
Standard Dual Amplifier Pin-out
MIL-STD-883B Versions Available
Single Versions Offered: AD542, AD544, AD547

CONNECTION DIAGRAMS



NOTE:
PIN 4 CONNECTED TO CASE



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD642/AD644/AD647 series of precision, monolithic FET-input op amps are pairs of matched, high speed, BiFET op amps fabricated with the most advanced BiFET and laser trimming technologies. The AD642, AD644, AD647 series offers matched bias currents significantly lower than currently available dual, BiFET devices, 35 pA max., warmed up. In addition, the offset voltage is laser trimmed to less than 0.25 mV on the AD647L, using Analog Devices' laser wafer trimming (LWT) process.

PRODUCT HIGHLIGHTS

1. Tight matching specifications ensure high performance and eliminate the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage to only 0.25 mV max and matched side to side to 0.25 mV (AD647L), thus eliminating the need for external nulling.
4. Low voltage noise (2 μV p-p) and high open-loop gain enhance performance as a precision op amp.
5. High slew rate (13 V/μs) and fast settling time to 0.01% (3.0 μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0015%) and low crosstalk (–124 dB) make the AD644 an ideal choice in stereo audio applications
7. Bare die are available for use in hybrid circuit applications.

ORDERING GUIDE

Model	Package Description	Package Option*
AD642JCHIPS	Bare Die	
AD642JH	8-Pin Hermetic Metal Can	H-08A
AD642KH	8-Pin Hermetic Metal Can	H-08A
AD642LH	8-Pin Hermetic Metal Can	H-08A
AD642SH	8-Pin Hermetic Metal Can	H-08A
AD642SH/883B	8-Pin Hermetic Metal Can	H-08A
AD644JH	8-Pin Hermetic Metal Can	H-08A
AD644LH	8-Pin Hermetic Metal Can	H-08A
AD644SH	8-Pin Hermetic Metal Can	H-08A
AD644SH/883B	8-Pin Hermetic Metal Can	H-08A
AD647JH	8-Pin Hermetic Metal Can	H-08A
AD647KH	8-Pin Hermetic Metal Can	H-08A
AD647LH	8-Pin Hermetic Metal Can	H-08A
AD647SE	20-Pin Hermetic LCC	E-20A
AD647SE/883B	20-Pin Hermetic LCC	E-20A
AD647SH/883B	8-Pin Hermetic Metal Can	H-08A

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD647/AD642/AD644–SPECIFICATIONS

(V_{CM} = 0 V, V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	AD642 Min	AD642 Typ	AD642 Max	AD644 Min	AD644 Typ	AD644 Max	AD647 Min	AD647 Typ	AD647 Max	Units
OPEN-LOOP GAIN										
V_{OUT} = ±10 V, R_L = 2 kΩ										
J Grade	100			30			100			V/mV
K, L, S Grades	250			50			250			V/mV
OUTPUT CHARACTERISTICS										
R_L = 2 kΩ, T_A = T_{MIN} to T_{MAX}	±10	±12		±10	±12		±10	±12		V
R_L = 10 kΩ, T_A = T_{MIN} to T_{MAX}	±12	±13		±12	±13		±12	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2.0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	2.0	3.0		8.0	13.0		2.0	3.0		V/μs
Total Harmonic Distortion					0.0015					%
INPUT OFFSET VOLTAGE										
Initial Offset										
J Grade			2.0			2.0			1.0	mV
K Grade			1.0			1.0			0.5	mV
L Grade			0.5			0.5			0.25	mV
S Grade			1.0			1.0			0.5	mV
Input Offset Voltage, T_{MIN} to T_{MAX}										
J Grade			3.5			3.5			1.5	mV
K Grade			2.0			2.0			1.0	mV
L Grade			1.0			1.0			0.5	mV
S Grade			3.5			3.5			1.5	mV
INPUT BIAS CURRENT[2]										
Either Input										
J Grade		10	75		10	75		10	75	pA
K, L, S Grades		10	35		10	35		10	35	pA
Input Offset Current										
J Grade		5			10			5		pA
K, L, S Grades		2			5			2		pA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage										
J Grade			1.0			1.0			1.0	mV
K Grade			0.5			0.5			0.5	mV
L Grade			0.25			0.25			0.25	mV
S Grade			0.5			0.5			0.5	mV
Input Bias Current										
J, S Grades			35			35			35	pA
K, L Grades			25			25			25	pA
Crosstalk		–124			–124			–124		dB
INPUT IMPEDANCE										
Differential		10^{12}‖6			10^{12}‖6			10^{12}‖6		Ω‖pF
Common Mode		10^{12}‖6			10^{12}‖3			10^{12}‖6		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common Mode	±10	±12		±10	±12		±10	±12		V
Common Mode Rejection										
J Grade	76			76			76			dB
K, L, S Grades	80			80			80			dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	V
Quiescent Current			2.8		3.5	4.5			2.8	mA
VOLTAGE NOISE										
0.1 Hz to 10 Hz										
J Grade		2.0			2.0			2.0		μV p-p
K, L, S Grades		2.0			2.0				4.0	μV p-p
10 Hz		70			35			70		nV/√Hz
100 Hz		45			22			45		nV/√Hz
1 kHz		30			18			30		nV/√Hz
10 kHz		25			16			25		nV/√Hz

Specifications subject to change without notice.

ANALOG DEVICES

Dual Precision, Low Power BiFET Op Amp

AD648

FEATURES

DC Performance
- 400 μA max Quiescent Current
- 10 pA max Bias Current, Warmed Up (AD648C)
- 300 μV max Offset Voltage (AD648C)
- 3 μV/°C max Drift (AD648C)
- 2 μV p-p Noise, 0.1 Hz to 10 Hz

AC Performance
- 1.8 V/μs Slew Rate
- 1 MHz Unity Gain Bandwidth

Available in Plastic Mini-DIP, Cerdip, Plastic SOIC and Hermetic Metal Can Packages

MIL-STD-883B Parts Available

Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

Single Version: AD548

PRODUCT DESCRIPTION

The AD648 is a matched pair of low power, precision monolithic operational amplifiers. It offers both low bias current (10 pA max, warmed up) and low quiescent current (400 μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD648's entire common-mode voltage range.

The economical J grade has a maximum guaranteed offset voltage of less than 2 mV and an offset voltage drift of less than 20 μV/°C. The C grade reduces offset voltage to less than 0.30 mV and offset voltage drift to less than 3 μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

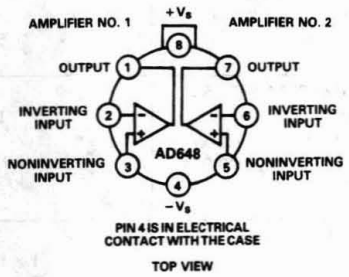
The AD648 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD648's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86 dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD648 is pinned out in a standard dual op amp configuration and is available in seven performance grades. The AD648J and AD648K are rated over the commercial temperature range of 0°C to +70°C. The AD648A, AD648B and AD648C are rated over the industrial temperature range of –40°C to +85°C. The AD648S and AD648T are rated over the military temperature range of –55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

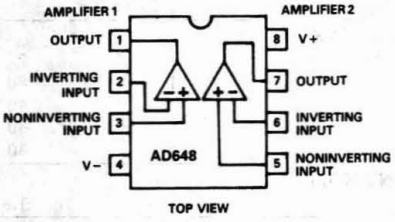
The AD648 is available in an 8-pin plastic mini-DIP, cerdip, SOIC, TO-99 metal can, or in chip form.

CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Package, Plastic SOIC (R) Package and Cerdip (Q) Package



PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD648 the ideal op amp for high performance, low power applications.
2. The AD648 is pin compatible with industry standard dual op amps such as the LF442, TL062, and AD642, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2 mV max) and drift (20 μV/°C max) for the AD648J are achieved utilizing Analog Devices' laser drift trimming technology.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. Matching characteristics are excellent for all grades. The input offset voltage matching between amplifiers in the AD648J is within 2 mV, for the C grade matching is within 0.4 mV.
6. Crosstalk between amplifiers is less than –120 dB at 1 kHz.
7. The AD648 is available in chip form.

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AD648—SPECIFICATIONS (@ +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	AD648J/A/S			AD648K/B/T			AD648C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	2.0		0.3	1.0		0.10	0.3	mV
T_{MIN} to T_{MAX}			3.0/3.0/3.0			1.5/1.5/2.0			0.5	mV
vs. Temperature			20			10			3.0	µV/°C
vs. Supply	80			86			86			dB
vs. Supply, T_{MIN} to T_{MAX}	76/76/76			80			80			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input,[2] V_{CM} = 0		5	20		3	10		3	10	pA
Either Input[2] at T_{MAX}, V_{CM} = 0			0.45/1.3/20			0.25/0.65/10			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			30			15			15	pA
Offset Current, V_{CM} = 0		5	10		2	5		2	5	pA
Offset Current at T_{MAX}			0.25/0.7/10			0.15/0.35/5			0.35	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage		1.0	2.0		0.5	1.0		0.2	0.4	mV
Input Offset Voltage T_{MIN} to T_{MAX}			3.0/3.0/3.0			1.5/1.5/2.0			0.5	mV
Input Offset Voltage vs. Temperature		8			5			2.5		µV/°C
Input Bias Current			10			5			5	pA
Crosstalk		–120			–120			–120		dB
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common Mode	±11	±12		±11	±12		±11	±12		V
Common-Mode Rejection										
V_{CM} = ±10 V	76			82			86			dB
T_{MIN} to T_{MAX}	76/76/76			82			86			dB
V_{CM} = ±11 V	70			76			76			dB
T_{MIN} to T_{MAX}	70/70/70			76			76			dB
INPUT VOLTAGE NOISE										
Voltage 0.1 Hz to 10 Hz		2			2			2	4.0	µV p-p
f = 10 Hz		80			80			80		nV/√Hz
f = 100 Hz		40			40			40		nV/√Hz
f = 1 kHz		30			30			30		nV/√Hz
f = 10 kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1 kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	1.0	1.8		1.0	1.8		1.0	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN-LOOP GAIN										
V_O = ±10 V, $R_L \geq 10$ kΩ	300	1000		300	1000		300	1000		V/mV
T_{MIN} to T_{MAX}, $R_L \geq 10$ kΩ	300/300/300	700		300	700		300	700		V/mV
V_O = ±10 V, $R_L \geq 5$ kΩ	150	500		150	500		150	500		V/mV
T_{MIN} to T_{MAX}, $R_L \geq 5$ kΩ	150/150/150	300		150	300		150	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10$ kΩ, T_{MIN} to T_{MAX}	±12/±12/±12	±13		±12	±13		±12	±13		V
Voltage @ $R_L \geq 5$ kΩ, T_{MIN} to T_{MAX}	±11/±11/±11	±12		±11	±12		±11	±12		V
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current (Both Amplifiers)		340	400		340	400		340	400	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0°C to +70°C)		AD648J			AD648K					
Industrial (–40°C to +85°C)		AD648A			AD648B			AD648C		
Military (–55°C to +125°C)		AD648S			AD648T					
PACKAGE OPTIONS*										
SOIC (R-8)		AD648JR			AD648KR					
Plastic (N-8)		AD648JN			AD648KN					
Cerdip (Q-8)	AD648AQ, AD648SQ, AD648SQ/883B			AD648BQ, AD648TQ/883B			AD648CQ			
Metal Can (H-08A)	AD648AH			AD648BH, AD648TH/883B						
Tape and Reel	AD648JR-REEL, AD648JR-REEL7			AD648KR-REEL, AD648KR-REEL7						
Chips Available	AD648JCHIPS, AD648SCHIPS									

*For outline information see Package Information section.
Specifications subject to change without notice.

Picoampere Input Current, Bipolar Operational Amplifiers

AD704/AD705/AD706

FEATURES

HIGH DC PRECISION
- Low Offset Voltage (75 μV max: AD704)
- Low Offset Drift (1.0 μV/°C max: AD704)
- Low Input Bias Currents (150 pA max: AD704)

LOW NOISE
- 0.5 μV p-p typ Voltage Noise (0.1 Hz to 10 Hz)

LOW POWER
- 600 μA max Supply Current per Amplifier

AC PERFORMANCE
- 0.15 V/μs Slew Rate
- 500 kHz Unity Gain Crossover Frequency

MIL-STD-883B Versions Available (Single or Quad)

APPLICATIONS

Industrial/Process Controls
Weigh Scales
Medical Instrumentation (ECG/EKG)
Low Frequency Active Filters
Precision Integrators

PRODUCT DESCRIPTION

The AD704/AD705/AD706 series are low power, bipolar op amps that have the low input bias current of BiFET amplifiers, but offer a significantly lower I_B drift over temperature. This series offers many of the advantages of BiFET and bipolar op amps without their inherent disadvantages. They utilize superbeta bipolar input transistors to achieve the picoampere input bias current levels of FET input amplifiers (at room temperature), while their I_B typically increases 5 times vs. BiFET amplifiers which exhibit a 1000× increase over temperature. Superbeta bipolar technology also permits these amplifiers to achieve the microvolt offset voltages and low noise characteristics of a precision bipolar input amplifier.

Since these amplifiers have only 1/20 of the input bias current of an industry standard OP07, the AD704/AD705/AD706 do not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP07, which makes these amplifiers usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP07, these amplifiers are better suited for today's higher density systems and battery powered applications.

The AD704, AD705 and AD706 are excellent choices for use in low frequency active filters for 12- and 14-bit data acquisition systems, in precision instrumentation, and as high quality integrators. These amplifiers are internally compensated for unity gain and are available in various performance grades.

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD704AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD704AQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD704AR-16	–40°C to +85°C	16-Pin Plastic SOIC	R-16
AD704AR-16-REEL	–40°C to +85°C	16-Pin Plastic SOIC	R-16
AD704AR-16-REEL7	–40°C to +85°C	16-Pin Plastic SOIC	R-16
AD704BQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD704JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD704JR-16	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD704JR-16-REEL	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD704JR-16-REEL7	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD704KN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD704SE/883B	–55°C to +125°C	20-Pin Ceramic LCC	E-20A
AD704TQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD705AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD705JN	0°C to +70°C	8-Pin Plastic DIP	N-8

Model	Temperature Range	Package Description	Package Option*
AD705JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD705TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD706AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD706AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD706AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD706AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD706AR-REEL7	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD706BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD706JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD706JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD706JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD706JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD706KN	0°C to +70°C	8-Pin Plastic	N-8

*For outline information see Package Information section.

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AD704/AD705/AD706–SPECIFICATIONS (V_{CM} = 0 V, V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	Conditions	Model	J/A Min	J/A Typ	J/A Max	K/B/S Min	K/B/S Typ	K/B/S Max	C/T Min	C/T Typ	C/T Max	Units
INPUT OFFSET VOLTAGE												
Initial Offset		AD704		50	150		30	75		30	100	µV
		AD705		30	90		10	35		10	25	µV
		AD706		30	100		10	50		10	50	µV
Offset	T_{MIN} to T_{MAX}	AD704		100	250		50	150		80	150	µV
		AD705		45	150		25	60		25	60	µV
		AD706		40	150		25	100		25	100	µV
vs. Temp, Average TC		AD704		0.2	1.5		0.2	1.0			1.0	µV/°C
		AD705		0.2	1.2		0.2	0.6		0.2	0.6	µV/°C
		AD706		0.2	1.5		0.2	0.6		0.2	0.6	µV/°C
INPUT BIAS CURRENT	V_{CM} = 0 V	AD704		100	270		80	150		80	200	pA
		AD705		60	150		30	100		30	100	pA
		AD706		50	200		30	110		30	120	pA
	V_{CM} = ±13.5 V	AD704			300			200			250	pA
		AD705		80	200		50	150		50	150	pA
		AD706			250			160			170	pA
vs. Temp, Average TC		AD704		0.3			0.2			1.0		pA/°C
		AD705		0.3			0.3			0.6		pA/°C
		AD706		0.3			0.2			0.2		pA/°C
INPUT OFFSET CURRENT	V_{CM} = 0 V	AD704		80	250		30	100		50	150	pA
		AD705		40	150		30	100		30	100	pA
		AD706		30	150		30	100		30	100	pA
	V_{CM} = ±13.5 V	AD704			300			150			200	pA
		AD705		40	200		30	150		30	150	pA
		AD706			250			200			200	pA
MATCHING CHARACTERISTICS												
Offset Voltage		AD704			250			130			150	µV
		AD706			150			75			75	µV
Input Bias Current[2]		AD706			300			150			200	pA
Common-Mode Rejection[3]		AD704	94			110			104			dB
		AD706	106			110			110			dB
Power Supply Rejection[4]		AD704	94			110			110			dB
		AD706	106			110			110			dB
Crosstalk @ f = 10 Hz	R_L = 2 kΩ	AD704/6		150			150			150		dB
INPUT OFFSET VOLTAGE UNITY GAIN												
Crossover Frequency		All		0.5			0.5			0.5		MHz
Slew Rate	G = –1	All		0.15			0.15			0.15		V/µs
INPUT IMPEDANCE												
Differential		All		40‖2			40‖2			40‖2		MΩ‖pF
Common Mode		All		300‖2			300‖2			300‖2		GΩ‖pF
INPUT VOLTAGE RANGE												
Common-Mode Voltage		All	±13.5	±14		±13.5	±14		±13.5	±14		V
CMRR	V_{CM} = ±13.5 V	AD704	100	132		114	132		110	132		dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz	All		3			3			3		pA p-p
	f = 10 Hz	All		50			50			50		fA/√Hz
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	AD704		0.5			0.5	2.0		0.5	2.0	µV p-p
		AD705/6		0.5			0.5	1.0		0.5	1.0	µV p-p
	f = 10 Hz	All		17			17			17		nV/√Hz
	f = 1 kHz	All		15	22		15	22		15	22	nV/√Hz
OPEN LOOP GAIN	V_O = ±12 V, R_L = 10 kΩ	All	200	2000		400	2000		400	2000		V/mV
	V_O = ±10 V, R_L = 2 kΩ	All	200	1000		300	1000		200	1000		V/mV
OUTPUT CHARACTERISTICS												
Voltage Swing, R_L = 10 kΩ	T_{MIN} to T_{MAX}	All	±13	±14		±13	±14		±13	±14		V
Current	Short Circuit	All		±15			±15			±15		mA
Capacitive Load Drive	G = +1	All		10,000			10,000			10,000		pF
POWER SUPPLY												
Rated Performance		All		±15				±15		±15		V
Operating Range		All	±2		±18	±2		±18	±2		±18	V
Quiescent Current		AD704		1.5	2.4		1.5	2.4		1.5	2.4	mA
		AD705		0.38	0.6		0.38	0.6		0.38	0.6	mA
		AD706		0.75	1.2		0.75	1.2		0.75	1.2	mA

Specifications subject to change without notice.

Precision, Low Cost, High Speed, BiFET Op Amps

AD711/AD712/AD713

FEATURES

Enhanced Replacements for
TL081; TL082; TL084
LF411; LF412; LF347

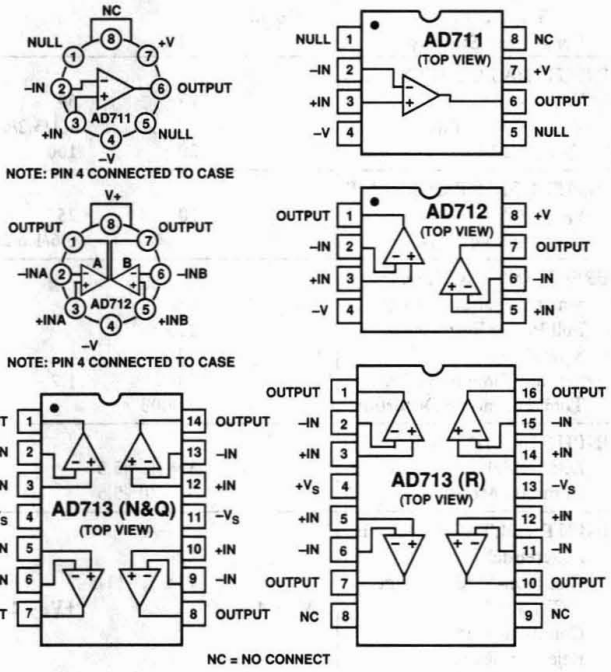
AC PERFORMANCE
Settles to ±0.01% in 1.0 μs
16 V/μs min Slew Rate
3 MHz min Unity Gain Bandwidth
0.0003% Total Harmonic Distortion (THD)

DC PERFORMANCE
Low Offset Voltages
(0.25 mV max—AD711C)
(0.30 mV max—AD712C)
(0.50 mV max—AD713K)
Low Offset Drift
(3 μV/°C max—AD711C)
(5 μV/°C max—AD712C)
200 V/mV min Open-Loop Gain
Low Noise (0.1 Hz to 10 Hz)
(4 μV p-p max—AD711C)
(4 μV p-p max—AD712C)
MIL-STD-883B Versions Available
Single: AD711
Dual: AD712
Quad: AD713

APPLICATIONS

Active Filters
Output Buffers for 12- and 14-Bit DACs
Input Buffers for Precision ADCs
Photo Diode Preamplifier Applications

CONNECTION DIAGRAMS



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ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD711AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711BH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD711CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD711JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD711JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD711KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD711SCHIPS	–55°C to +125°C	Bare Die	
AD711SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD711TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712ACHIPS	–40°C to +85°C	Bare Die	
AD712AH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712CH	–40°C to +85°C	8-Pin Metal Can	H-08A
AD712CQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD712JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD712JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD712KR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712KR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD712SCHIPS	–55°C to +125°C	Bare Die	
AD712SQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712SQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712TQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD712TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD713AQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713BQ	–40°C to +85°C	14-Pin Ceramic DIP	Q-14
AD713JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713JR-16	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713JR-16-REEL7	0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713KN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD713SCHIPS	–55°C to +125°C	Bare Die	
AD713SQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713SQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD713TQ/883B	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063301MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
5962-9063302MCA	–55°C to +125°C	14-Pin Ceramic DIP	Q-14

NOTES
[1]Request complete data sheet for ordering information on the AD712 and AD713.
[2]For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD711/AD712/AD713–SPECIFICATIONS

AD711[1] (V_S = ±15 V @ T_A = +25°C unless otherwise noted)

Parameter	J/A/S Min	J/A/S Typ	J/A/S Max	K/B/T Min	K/B/T Typ	K/B/T Max	C Min	C Typ	C Max	Units
INPUT OFFSET VOLTAGE										
Initial Offset		0.3	**2/1/1**		0.2	**0.5**		0.10	**0.25**	mV
T_{MIN} to T_{MAX}			3/2/2			**1.0**			**0.45**	mV
vs. Temp		7	20/20/**20**		5	**10**		2	5	µV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
T_{MIN} to T_{MAX}	76/76/**76**			**80**			**86**			dB
Long-Term Stability		15			15			15		µV/Month
INPUT BIAS CURRENT										
V_{CM} = 0 V		15	**50**		15	**50**		15	**25**	pA
V_{CM} = 0 V @ T_{MAX}			1.1/3.2/**51**			1.1/3.2/**51**			1.6	nA
V_{CM} = ±10 V		20	**100**		20	**100**		20	**50**	pA
INPUT OFFSET CURRENT										
V_{CM} = 0 V		10	**25**		5	**25**		5	**10**	pA
V_{CM} = 0 V @ T_{MAX}			0.6/1.6/**26**			0.6/1.6/**26**			0.65	nA
FREQUENCY RESPONSE										
Small Signal Bandwidth	3.0	4.0		3.4	4.0		3.4	4.0		MHz
Full Power Response		200			200			200		kHz
Slew Rate	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%		1.0	1.2		1.0	1.2		1.0	1.2	µs
Total Harmonic Distortion		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential		±20			±20			±20		V
Common-Mode Voltage		+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		
T_{MIN} to T_{MAX}	**$-V_S$ + 4**		**$+V_S$ – 2**	**$-V_S$ + 4**		**$+V_S$ – 2**	**$-V_S$ + 4**		**$+V_S$ – 2**	V
Common-Mode Rejection Ratio										
V_{CM} = ±10 V	**76**	88		**80**	88		**86**	94		dB
T_{MIN} to T_{MAX}	76/76/**76**	84		**80**	84		**86**	90		dB
V_{CM} = ±11 V	**70**	84		**76**	84		**76**	90		dB
T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE		2			2			2	**4**	µV p-p
		45			45			45		nV/√Hz
		22			22			22		nV/√Hz
		18			18			18		nV/√Hz
		16			16			16		nV/√Hz
INPUT CURRENT NOISE		0.01			0.01			0.01		pA/√Hz
OPEN-LOOP GAIN	**150**	400		**200**	400		**200**	400		V/mV
	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage	**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		V
	±12/±12/**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		V
Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		2.5	**3.4**		2.5	**3.0**		2.5	**2.8**	mA

NOTES

[1]Request complete data sheet for AD712 and AD713 specifications.

Specifications subject to change without notice.

ANALOG DEVICES

Ultralow Noise BiFET Op Amp

AD743

FEATURES

ULTRALOW NOISE PERFORMANCE
- 2.9 nV/$\sqrt{Hz}$ at 10 kHz
- 0.38 μV p-p, 0.1 Hz to 10 Hz
- 6.9 fA/$\sqrt{Hz}$ Current Noise at 1 kHz

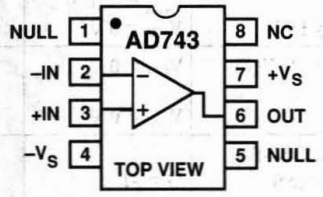
EXCELLENT DC PERFORMANCE
- 0.5 mV max Offset Voltage
- 250 pA max Input Bias Current
- 1000 V/mV min Open-Loop Gain

AC PERFORMANCE
- 2.8 V/μs Slew Rate
- 4.5 MHz Unity-Gain Bandwidth
- THD = 0.0003% @ 1 kHz
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
- Sonar Preamplifiers
- High Dynamic Range Filters (>140 dB)
- Photodiode and IR Detector Amplifiers
- Accelerometers

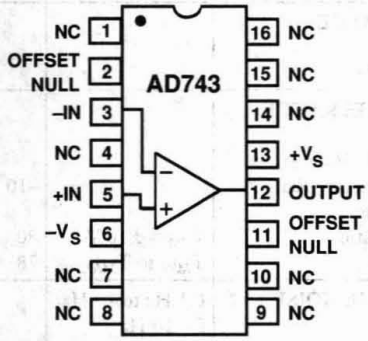
CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and 8-Pin Cerdip (Q) Packages



NC = NO CONNECT

16-Pin SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD743 is an ultralow noise precision, FET input, monolithic operational amplifier. It offers a combination of the ultralow voltage noise generally associated with bipolar input op amps and the very low input current of a FET-input device. Furthermore, the AD743 does not exhibit an output phase reversal when the negative common-mode voltage limit is exceeded.

The AD743's guaranteed, maximum input voltage noise of 4.0 nV/$\sqrt{Hz}$ at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is the maximum 1.0 μV p-p, 0.1 Hz to 10 Hz noise. The AD743 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage. The AD743 is specifically designed for use as a preamp in capacitive sensors, such as ceramic hydrophones.

PRODUCT HIGHLIGHTS

1. The low offset voltage and low input offset voltage drift of the AD743 coupled with its ultralow noise performance mean that the AD743 can be used for upgrading many applications now using bipolar amplifiers.
2. The combination of low voltage and low current noise make the AD743 ideal for charge sensitive applications such as accelerometers and hydrophones.
3. The low input offset voltage and low noise level of the AD743 provide >140 dB dynamic range.
4. The typical 10 kHz noise level of 2.9 nV/$\sqrt{Hz}$ permits a three op amp instrumentation amplifier, using three AD743s, to be built which exhibits less than 4.2 nV/$\sqrt{Hz}$ noise at 10 kHz and which has low input bias currents.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD743JN	0°C to +70°C	N-8
AD743KN	0°C to +70°C	N-8
AD743JR-16	0°C to +70°C	R-16
AD743KR-16	0°C to +70°C	R-16
AD743BQ	–40°C to +85°C	Q-8
AD743SQ/883B	–55°C to +125°C	Q-8
AD743JR-16-REEL	0°C to +70°C	Tape & Reel
AD743KR-16-REEL	0°C to +70°C	Tape & Reel

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip.

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AD743–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD743J Min	AD743J Typ	AD743J Max	AD743K/B Min	AD743K/B Typ	AD743K/B Max	AD743S Min	AD743S Typ	AD743S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0/0.8		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{MIN} to T_{MAX}			1.5			1.0/0.50			2.0	mV
vs. Temp.	T_{MIN} to T_{MAX}		2			1			2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{MIN} to T_{MAX}	88			98	100		88			dB
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		150	400		150	250		150	400	pA
Either Input @ T_{MAX}	V_{CM} = 0 V			8.8/25.6			5.5/16			413	nA
Either Input	V_{CM} = +10 V		250	600		250	400		300	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200		30	125		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150		30	75		40	150	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = –1		4.5			4.5			4.5		MHz
Full Power Response	V_O = 20 V p-p		25			25			25		kHz
Slew Rate, Unity Gain	G = –1		2.8			2.8			2.8		V/μs
Settling Time to 0.01%			6			6			6		μs
Total Harmonic Distortion[4] (Figure 16)	f = 1 kHz G = –1		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$1 \times 10^{10}\|\|20$			$1 \times 10^{10}\|\|20$			$1 \times 10^{10}\|\|20$		Ω||pF
Common Mode			$3 \times 10^{11}\|\|18$			$3 \times 10^{11}\|\|18$			$3 \times 10^{11}\|\|18$		Ω||pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+13.3, –10.7			+13.3, –10.7			+13.3, –10.7		V
Over Max Operating Range[6]		–10		+12	–10		+12	–10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		90	102		80	95		dB
	T_{MIN} to T_{MAX}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5	10.0		5.5		$nV/\sqrt{Hz}$
	f = 100 Hz		3.6			3.6	6.0		3.6		$nV/\sqrt{Hz}$
	f = 1 kHz		3.2	5.0		3.2	5.0		3.2	5.0	$nV/\sqrt{Hz}$
	f = 10 kHz		2.9	4.0		2.9	4.0		2.9	4.0	$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		$fA/\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±10 V										
	$R_{LOAD} \geq 2$ kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{MIN} to T_{MAX}	800			1800			800			V/mV
	R_{LOAD} = 600 Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq 600$ Ω	+13, –12			+13, –12			+13, –12			V
	$R_{LOAD} \geq 600$ Ω		+13.6, –12.6			+13.6, –12.6			+13.6, –12.6		V
	T_{MIN} to T_{MAX}	+12, –10			+12, –10			+12, –10			V
	$R_{LOAD} \geq 2$ kΩ	±12	+13.8, –13.1		±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8.1	10.0		8.1	10.0		8.1	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.

[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[4]Gain = –1, R_L = 2 kΩ, C_L = 10 pF.

[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.

[6]Thc AD743 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

Precision, 500 ns Settling BiFET Op Amp

AD744

FEATURES

AC PERFORMANCE
- 500 ns Settling to 0.01% for 10 V Step
- 1.5 μs Settling to 0.0025% for 10 V Step
- 75 V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13 MHz Gain Bandwidth – Internal Compensation
- >200 MHz Gain Bandwidth (G = 1000) External Decompensation
- >1000 pF Capacitive Load Drive Capability with 10 V/μs Slew Rate – External Compensation

DC PERFORMANCE
- 0.25 mV max Offset Voltage (AD744C)
- 3 μV/°C max Drift (AD744C)
- 250 V/mV min Open-Loop Gain (AD744B)
- 4 μV p-p max Noise, 0.1 Hz to 10 Hz (AD744C)
- Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form
- MIL-STD-883B Processing Available
- Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

PRODUCT DESCRIPTION

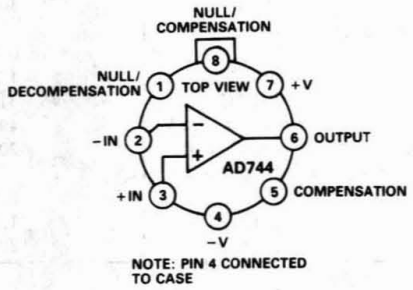
The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13 MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

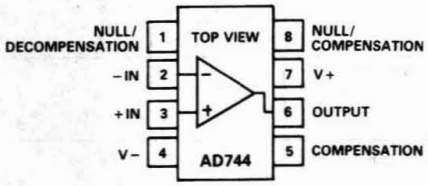
The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000 pF capacitive loads, slewing at 10 V/μs with full stability. Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200 MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

CONNECTION DIAGRAMS

TO-99 (H) Package



8-Pin Plastic Mini-DIP (N), 8-Pin SOIC (R) Package and 8-Pin Cerdip (Q) Packages



The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0°C to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of –40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of –55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin small outline, 8-pin cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OPA602/OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ionimplanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4 μV p-p, 0.1 Hz to 10 Hz (AD744C).

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AD744—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	AD744J/A/S Typ	AD744J/A/S Max	AD744K/B/T Min	AD744K/B/T Typ	AD744K/B/T Max	AD744C Min	AD744C Typ	AD744C Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	**1.0**		0.25	**0.5**		0.10	**0.25**	mV
Offset	T_{MIN} to T_{MAX}			2/2/2			**1.0**			**0.45**	mV
vs. Temp.			5	20/20/**20**		5	**10**		2	**3**	µV/°C
vs. Supply[2]		**82**	95		**88**	100		**92**	110		dB
vs. Supply	T_{MIN} to T_{MAX}	82/82/**82**			**88**			**92**			dB
Long-Term Stability			15			15			15		µV/month
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		30	**100**		30	**100**		30	**50**	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V										
J, K	70°C		0.7	2.3		0.7	2.3				nA
A, B, C	85°C		1.9	6.4		1.9	6.4		1.9	3.2	nA
S, T	125°C		31	102		31	102				nA
Either Input	V_{CM} = +10 V		40	150		40	**150**		40	**100**	pA
Offset Current	V_{CM} = 0 V		20	**50**		10	**50**		10	**20**	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V										
J, K	70°C		0.4	1.1		0.2	1.1				nA
A, B, C	85°C		1.3	3.2		0.6	3.2		0.6	1.3	nA
S, T	125°C		20	52		10	52				nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = –1	8	13		9	13		9	13		MHz
Full Power Response	V_O = 20 V p-p		1.2			1.2			1.2		MHz
Slew Rate, Unity Gain	G = –1	**45**	75		**50**	75		**50**	75		V/µs
Settling Time to 0.01%[4]	G = –1		0.5	0.75		0.5	0.75		0.5	0.75	µs
Total Harmonic	f = 1 kHz										
Distortion	R1 ≥ 2 kΩ										
	V_O = 3 V rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$		Ω||pF
Common Mode			$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$			$3 \times 10^{12}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		V
Over Max Operating Range[6]		**–11**		**+13**	**–11**		**+13**	**–11**		**+13**	V
Common-Mode											
Rejection Ratio	V_{CM} = ±10 V	**78**	88		**82**	88		**86**	94		dB
	T_{MIN} to T_{MAX}	76/76/**76**	84		**80**	84		**86**	90		dB
	V_{CM} = ±11 V	**72**	84		**78**	84		**80**	90		dB
	T_{MIN} to T_{MAX}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		2			2			2	**4**	µV p-p
	f = 10 Hz		45			45			45		nV/√Hz
	f = 100 Hz		22			22			22		nV/√Hz
	f = 1 kHz		18			18			18		nV/√Hz
	f = 10 kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[7]	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	**200**	400		250	400		**250**	400		V/mV
	T_{MIN} to T_{MAX}	100/100/**100**			**100**			**150**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 2 kΩ	**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12/±12/**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		**±12**	+13.8, –13.1		V
Current	Short Circuit		25			25			25		mA
Capacitive Load[8]	Gain = –1			**1000**			**1000**			**1000**	pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			3.5	**5.0**		3.5	**4.0**		3.5	**4.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]PSRR test conditions: $+V_S$ = 15 V, $-V_S$ = –12 V to –18 V and $+V_S$ = +12 V to +18 V, $-V_S$ = –15 V.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[4]Gain = –1, R_L = 2 k, C_L = 10 pF, refer to Figure 25.

[5]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[6]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]Capacitive load drive specified for C_{COMP} = 20 pF with the device connected as shown in Figure 32. Under these conditions, slew rate = 14 V/µs and 0.01% settling time = 1.5 µs typical. Refer to Table II for optimum compensation while driving a capacitive load.

[9]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ANALOG DEVICES

Ultralow Noise, High Speed, BiFET Op Amp

AD745

FEATURES

ULTRALOW NOISE PERFORMANCE
2.9 nV/√Hz at 10 kHz
0.38 μV p-p, 0.1 Hz to 10 Hz
6.9 fA/√Hz Current Noise at 1 kHz

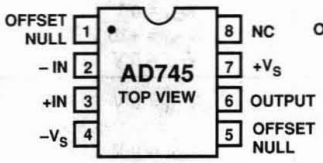
EXCELLENT AC PERFORMANCE
12.5 V/μs Slew Rate
20 MHz Gain Bandwidth Product
THD = 0.0002% @ 1 kHz
Internally Compensated for Gains of +5 (or –4) or Greater

EXCELLENT DC PERFORMANCE
0.5 mV max Offset Voltage
250 pA max Input Bias Current
2000 V/mV min Open Loop Gain
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
Sonar
Photodiode and IR Detector Amplifiers
Accelerometers
Low Noise Preamplifiers
High Performance Audio

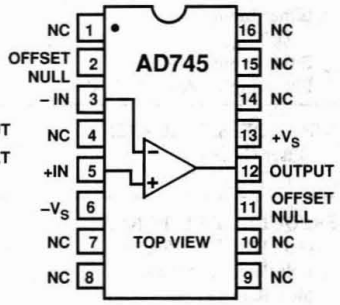
CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



NC = NO CONNECT

16-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD745 is an ultralow noise, high speed, FET input operational amplifier. It offers both the ultralow voltage noise and high speed generally associated with bipolar input op amps and the very low input currents of FET input devices. Its 20 MHz bandwidth and 12.5 V/μs slew rate makes the AD745 an ideal amplifier for high speed applications demanding low noise and high dc precision. Furthermore, the AD745 does not exhibit an output phase reversal.

The AD745's guaranteed, tested maximum input voltage noise of 4 nV/√Hz at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is its maximum 1.0 μV p-p noise in a 0.1 Hz to 10 Hz bandwidth. The AD745 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains. The AD745 is available in five performance grades. The AD745J and AD745K are rated over the commercial temperature range of 0°C to +70°C. The AD745A and AD745B are rated over the industrial temperature range of –40°C to +85°C. The AD745S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

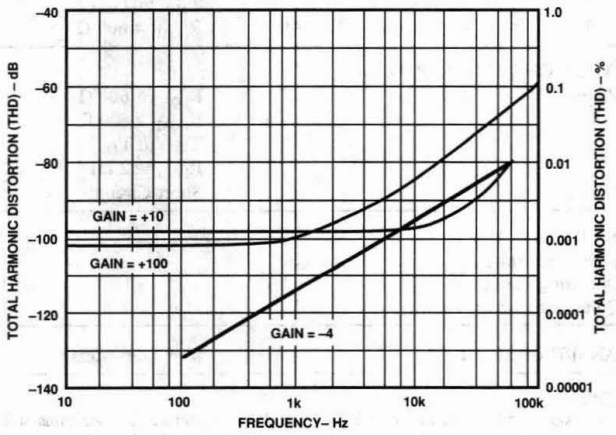
The AD745 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.

10

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD745JN	0°C to +70°C	N-8
AD745AN	–40°C to +85°C	N-8
AD745JR-16	0°C to +70°C	R-16

*N = Plastic DIP; R = Small Outline IC. For outline information see Package Information section.



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AD745—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD745J/A Min	AD745J/A Typ	AD745J/A Max	Units
INPUT OFFSET VOLTAGE[1]					
Initial Offset			0.25	1.0/0.8	mV
Initial Offset	T_{MIN} to T_{MAX}			1.5	mV
vs. Temp.	T_{MIN} to T_{MAX}		2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		dB
vs. Supply (PSRR)	T_{MIN} to T_{MAX}	88			dB
INPUT BIAS CURRENT[3]					
Either Input	V_{CM} = 0 V		150	400	pA
Either Input @ T_{MAX}	V_{CM} = 0 V			8.8/25.6	nA
Either Input	V_{CM} = +10 V		250	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V			2.2/6.4	nA
FREQUENCY RESPONSE					
Gain BW, Small Signal	G = –4		20		MHz
Full Power Response	V_O = 20 V p-p		120		kHz
Slew Rate	G = –4		12.5		V/μs
Settling Time to 0.01%			5		μs
Total Harmonic Distortion[4]	f = 1 kHz, G = –4		0.0002		%
INPUT IMPEDANCE					
Differential			$1 \times 10^{10} \| 20$		Ω‖pF
Common Mode			$3 \times 10^{11} \| 18$		Ω‖pF
INPUT VOLTAGE RANGE					
Differential[5]			±20		V
Common-Mode Voltage			+13.3, –10.7		V
Over Max Operating Range[6]		–10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		dB
	T_{MIN} to T_{MAX}	78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38		μV p-p
	f = 10 Hz		5.5		$nV/\sqrt{Hz}$
	f = 100 Hz		3.6		$nV/\sqrt{Hz}$
	f = 1 kHz		3.2	5.0	$nV/\sqrt{Hz}$
	f = 10 kHz		2.9	4.0	$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		6.9		$fA/\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±10 V, R_{LOAD} ≥ 2 kΩ	1000	4000		V/mV
	T_{MIN} to T_{MAX}	800			V/mV
	R_{LOAD} = 600 Ω		1200		V/mV
OUTPUT CHARACTERISTICS					
Voltage	R_{LOAD} ≥ 600 Ω	+13, –12			V
	R_{LOAD} ≥ 600 Ω		+13.6, –12.6	V	
	T_{MIN} to T_{MAX}	+12, –10			V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, –13.1	V	
Current	Short Circuit	20	40		mA
POWER SUPPLY					
Rated Performance			±15		V
Operating Range		±4.8		±18	V
Quiescent Current			8	10.0	mA
TRANSISTOR COUNT	# of Transistors		50		

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operations at T_A = +25°C.

[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.

[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[4]Gain = –4, R_L = 2 kΩ, C_L = 10 pF.

[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.

[6]The AD745 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

Dual Precision, 500 ns Settling, BiFET Op Amp

AD746

FEATURES

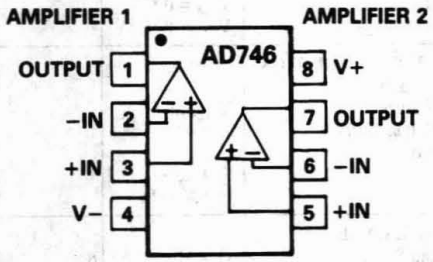
AC PERFORMANCE
- 500 ns Settling to 0.01% for 10 V Step
- 75 V/μs Slew Rate
- 0.0001% Total Harmonic Distortion (THD)
- 13 MHz Gain Bandwidth
- Internal Compensation for Gains of +2 or Greater

DC PERFORMANCE
- 0.5 mV max Offset Voltage (AD746B)
- 10 μV/°C max Drift (AD746B)
- 175 V/mV min Open Loop Gain (AD746B)
- 2 μV p-p Noise, 0.1 Hz to 10 Hz
- Available in Plastic Mini-DIP, Cerdip and Surface Mount Packages
- Available in Tape and Reel in Accordance with EIA-481A Standard
- MIL-STD-883B Processing also Available
- Single Version: AD744

APPLICATIONS
- Dual Output Buffers for 12- and 14-Bit DACs
- Input Buffers for Precision ADCs, Wideband Preamplifiers and Low Distortion Audio Circuitry

CONNECTION DIAGRAM

Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



PRODUCT DESCRIPTION

The AD746 is a dual operational amplifier, consisting of two AD744 BiFET op amps on a single chip. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates and ample bandwidths. In addition, the AD746 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single pole response of the AD746 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. Furthermore, the AD746's low total harmonic distortion (THD) level of 0.0001% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD746 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of 2 or greater. It is available in four performance grades. The AD746J is rated over the commercial temperature range of 0°C to +70°C. The AD746A and AD746B are rated over the industrial temperature range of –40°C to +85°C. The AD746S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD746 is available in three 8-pin packages: plastic mini-DIP, hermetic cerdip and surface mount (SOIC).

PRODUCT HIGHLIGHTS

1. The AD746 offers exceptional dynamic response for high speed data acquisition systems. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD746B).
2. Outstanding dc precision is provided by a combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
3. Differential and multichannel systems will benefit from the AD746's very close matching of ac characteristics. Input offset voltage specs are fully tested and guaranteed to a maximum of 0.5 mV (AD746B).
4. The AD746 has very close, guaranteed matching of input bias current between its two amplifiers.
5. Unity gain stable version AD712 also available.

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AD746—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD746J/A Min	AD746J/A Typ	AD746J/A Max	AD746B Min	AD746B Typ	AD746B Max	AD746S Min	AD746S Typ	AD746S Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			0.3	**1.5**		0.25	**0.5**		0.3	**1.0**	mV
Offset	T_{MIN} to T_{MAX}			2.0			**0.7**			**1.5**	mV
vs. Temperature			12	20		5	**10**		12	**20**	µV/°C
vs. Supply (PSRR)		**80**	95		**84**	100		**80**	95		dB
vs. Supply (PSRR)	T_{MIN} to T_{MAX}	80			**84**			**80**			dB
Long Term Stability			15			15			15		µV/month
INPUT BIAS CURRENT											
Either Input	V_{CM} = 0 V		110	**250**		110	**150**		110	**250**	pA
Either Input @ T_{MAX}	V_{CM} = 0 V		2.5/7	5.7/16		7	9.6		113	256	nA
Either Input	V_{CM} = +10 V		145	350		145	**200**		145	**350**	pA
Offset Current	V_{CM} = 0 V		45	**125**		45	**75**		45	**125**	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V		1.0/3	2.8/8		3	4.8		45	128	nA
MATCHING CHARACTERISTICS											
Input Offset Voltage			0.6	**1.5**		0.3	**0.5**		0.6	**1.0**	mV
Input Offset Voltage	T_{MIN} to T_{MAX}			2.0			**0.7**			**1.5**	mV
Input Offset Voltage Drift				20			20			20	µV/°C
Input Bias Current				**125**			**75**			**125**	pA
Crosstalk	@ 1 kHz		120			120			120		dB
	@ 100 kHz		90			90			90		dB
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = –1	8	13		9	13		8	13		MHz
Slew Rate, Unity Gain	G = –1	**45**	75		**50**	75		**45**	75		V/µs
Full Power Response	V_O = 20 V p-p		600			600			600		kHz
Settling Time to 0.01%	G = 1		0.5	0.75		0.5	0.75		0.5	0.75	µs
Total Harmonic Distortion	f = 1 kHz, R1 ≥ 2 kΩ, V_O = 3 V rms		0.0001			0.0001			0.0001		%
INPUT IMPEDANCE											
Differential			$2.5 \times 10^{11} \| 5.5$			$2.5 \times 10^{11} \| 5.5$			$2.5 \times 10^{11} \| 5.5$		Ω‖pF
Common Mode			$2.5 \times 10^{11} \| 5.5$			$2.5 \times 10^{11} \| 5.5$			$2.5 \times 10^{11} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE											
Differential			±20			±20			±20		V
Common-Mode Voltage			+14.5, –11.5			+14.5, –11.5			+14.5, –11.5		V
Over Max Operating Range		**–11**		**+13**	**–11**		**+13**	**–11**		**+13**	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	**78**	88		**82**	88		**78**	88		dB
	T_{MIN} to T_{MAX}	76	84		**80**	84		**76**	84		dB
	V_{CM} = ±11 V	**72**	84		**78**	84		**72**	84		dB
	T_{MIN} to T_{MAX}	70	80		**74**	80		**70**	80		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		2			2			2		µV p-p
	f = 10 Hz		45			45			45		$nV/\sqrt{Hz}$
	f = 100 Hz		22			22			22		$nV/\sqrt{Hz}$
	f = 1 kHz		18			18			18		$nV/\sqrt{Hz}$
	f = 10 kHz		16			16			16		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±10 V, R_{LOAD} ≥ 2 kΩ	**150**	300		**175**	300		**150**	300		V/mV
	T_{MIN} to T_{MAX}	75	200		75	200		**65**	175		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 2 kΩ	**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		**+13, –12.5**	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12	+13.8, –13.1		±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current	Short Circuit		25			25			25		mA
Max Capacitive Load	Gain = –1		50			50			50		pF
Driving Capability	Gain = –10		500			500			500		pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			7	**10**		7	**8.0**		7	**10**	mA
TEMPERATURE RANGE											
Rated Performance			0 to +70/–40 to +85			–40 to +85			–55 to +125		°C
PACKAGE OPTIONS[1]											
8-Pin Plastic Mini-DIP (N-8)			AD746JN								
8-Pin Cerdip (Q-8)			AD746AQ			AD746BQ			AD746SQ		
8-Pin Surface Mount (R-8)			AD746JR								
Tape and Reel			AD746JR-REEL								
Chips									AD746SCHIPS		
TRANSISTOR COUNT			54			54			54		

NOTE
[1]For outline information see Package Information section.
Specifications subject to change without notice.

Low Power, Low Noise Precision FET Op Amp

AD795

FEATURES

Low Power Replacement for Burr-Brown OPA-111, OPA-121 Op Amps
Low Noise
- **2.5 μV p-p max, 0.1 Hz to 10 Hz**
- **11 nV/√Hz max at 10 kHz**
- **0.6 fA/√Hz at 1 kHz**

High DC Accuracy
- **250 μV max Offset Voltage**
- **3 μV/°C max Drift**
- **1 pA max Input Bias Current**
- **Low Power: 1.5 mA max Supply Current**

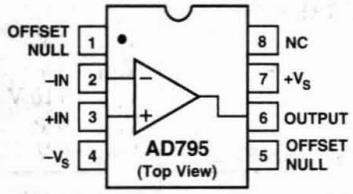
Available in Low Cost Plastic Mini-DIP and Surface Mount (SOIC) Packages

APPLICATIONS

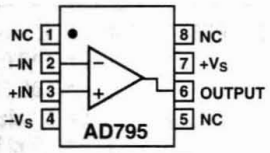
Low Noise Photodiode Preamps
CT Scanners
Precision I-to-V Converters

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD795 is a low noise, precision, FET input operational amplifier. It offers both the low voltage noise and low offset drift of a bipolar input op amp and the very low bias current of a FET-input device. The 10^{14} Ω common-mode impedance insures that input bias current is essentially independent of common-mode voltage and supply voltage variations.

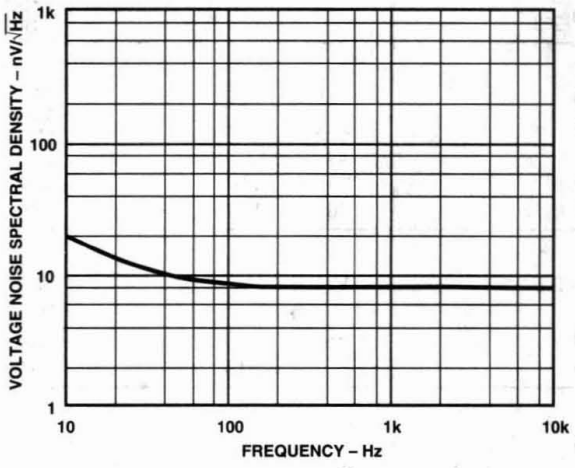
The AD795 has both excellent dc performance and a guaranteed and tested maximum input voltage noise. It features 1 pA maximum input bias current and 250 μV maximum offset voltage, along with low supply current of 1.5 mA max.

Furthermore, the AD795 features a guaranteed low input noise of 2.5 μV p-p (0.1 Hz to 10 Hz) and a 11 nV/√Hz max noise level at 10 kHz. The AD795 has a fully specified and tested input offset voltage drift of only 3 μV/°C max.

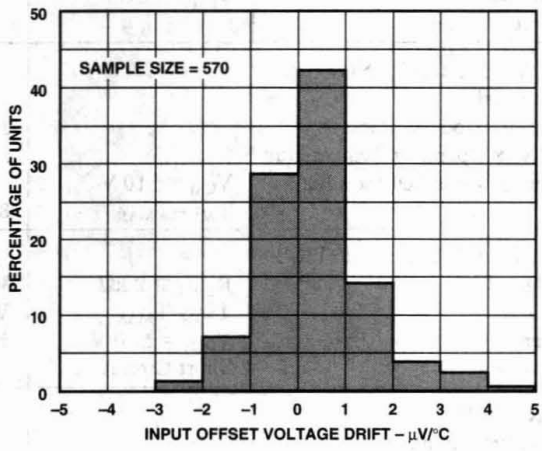
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD795JN	0°C to +70°C	N-8
AD795KN	0°C to +70°C	N-8
AD795JR	0°C to +70°C	SO-8
AD795JR-REEL	0°C to +70°C	SO-8
AD795JR-REEL7	0°C to +70°C	SO-8

*N = Plastic mini-DIP; SO = SOIC package. For outline information see Package Information section.



AD795 Voltage Noise Spectral Density



Typical Distribution of Average Input Offset Voltage Drift

AD795–SPECIFICATIONS (@ +25°C and ±15 V dc unless otherwise noted)

Parameter	Conditions	AD795JN/JR Min	AD795JN/JR Typ	AD795JN/JR Max	AD795K Min	AD795K Typ	AD795K Max	Units
INPUT OFFSET VOLTAGE								
Initial Offset			100	500		50	250	μV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400	μV
vs. Temperature			3	10		1	3	μV/°C
vs. Supply (PSRR)		86	110		90	110		dB
vs. Supply (PSRR)	T_{MIN}–T_{MAX}	84	100		87	100		dB
INPUT BIAS CURRENT								
Either Input	V_{CM} = 0 V		1	2/3		1	1	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V		23			23		pA
Either Input	V_{CM} = +10 V		1			1		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V		2			2		pA
OPEN-LOOP GAIN	V_O = ±10 V							
	R_{LOAD} ≥ 10 kΩ	110	120		110	120		dB
	R_{LOAD} ≥ 10 kΩ	100	108		100	108		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		1.0	3.3		1.0	2.5	μV p-p
	f = 10 Hz		20	50		20	40	nV/√Hz
	f = 100 Hz		12	40		12	30	nV/√Hz
	f = 1 kHz		11	17		11	15	nV/√Hz
	f = 10 kHz		9	11		9	11	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 Hz to 10 Hz		13			13		fA p-p
	f = 1 kHz		0.6			0.6		fA/√Hz
FREQUENCY RESPONSE								
Unity Gain, Small Signal	G = –1		1.6			1.6		MHz
Full Power Response	V_O = 20 V p-p							
	R_{LOAD} = 2 kΩ		16			16		kHz
Slow Rate, Unity Gain	V_{OUT} = 20 V p-p							
	R_{LOAD} = 2 kΩ		1			1		V/μs
SETTLING TIME								
To 0.1%	10 V Step		10			10		μs
To 0.01%	10 V Step		11			11		μs
Overload Recovery	50% Overdrive		2			2		μs
Total Harmonic Distortion	f = 1 kHz, R1 ≥ 10 kΩ, V_O = 3 V rms		–108			–108		dB
INPUT IMPEDANCE								
Differential	V_{DIFF} = ±1 V		10^{12}‖2			10^{12}‖2		Ω‖pF
Common Mode			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE								
Differential			±20			±20		V
Common-Mode Voltage		±10	±11		±10	±11		V
Over Max Operating Temperature		±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		dB
	T_{MIN}–T_{MAX}	86	100		90	100		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} ≥ 2 kΩ	V_S – 4	V_S – 2.5		V_S – 4	V_S – 2.5		V
	T_{MIN}–T_{MAX}	V_S – 4			V_S – 4			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		mA
	Short Circuit		±15			±15		mA
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4		±18	±4		±18	V
Quiescent Current			1.3	1.5		1.3	1.5	mA

Specifications subject to change without notice.

ANALOG DEVICES

Ultralow Distortion, Ultralow Noise Op Amp

AD797*

FEATURES

Low Noise
- 0.9 nV/√Hz typ (1.2 nV/√Hz max) Input Voltage Noise at 1 kHz
- 50 nV p-p Input Voltage Noise, 0.1 Hz to 10 Hz

Low Distortion
- –120 dB Total Harmonic Distortion at 20 kHz

Excellent AC Characteristics
- 800 ns Settling Time to 16 Bits (10 V Step)
- 110 MHz Gain Bandwidth (G = 1000)
- 8 MHz Bandwidth (G = 10)
- 280 kHz Full Power Bandwidth at 20 V p-p
- 20 V/μs Slew Rate

Excellent DC Precision
- 80 μV max Input Offset Voltage
- 1.0 μV/°C V_{OS} Drift

Specified for ±5 V and ±15 V Power Supplies

High Output Drive Current of 50 mA

APPLICATIONS

Professional Audio Preamplifiers

IR, CCD, and Sonar Imaging Systems

Spectrum Analyzers

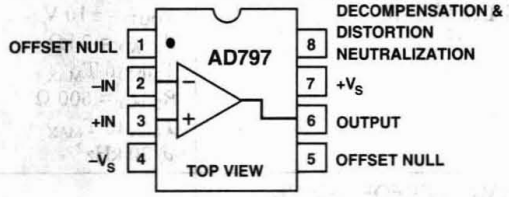
Ultrasound Preamplifiers

Seismic Detectors

ΣΔ ADC/DAC Buffers

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD797AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BR	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797BR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797BR-REEL7	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797AR	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD797AR-REEL7	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
5962-9313301MPA	–55°C to +125°C	8-Pin Cerdip	Q-8

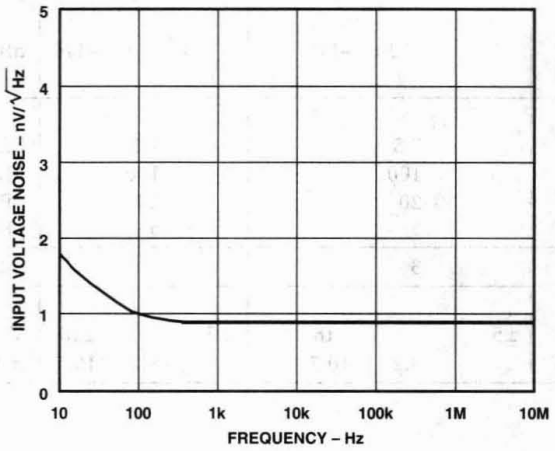
*For outline information see Package Information section.

10

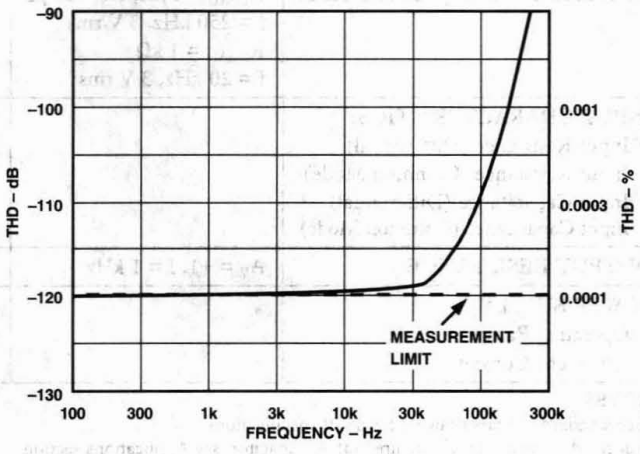
PRODUCT DESCRIPTION

The AD797 is a very low noise, low distortion operational amplifier ideal for use as a preamplifier. The low noise of 0.9 nV/√Hz and low total harmonic distortion of –120 dB at audio bandwidths give the AD797 the wide dynamic range necessary for preamps in microphones and mixing consoles. Furthermore, the AD797's excellent slew rate of 20 V/μs and 110 MHz gain bandwidth make it highly suitable for low frequency ultrasound applications.

The AD797 is also useful in IR and Sonar Imaging applications where the widest dynamic range is necessary. The low distortion and 16-bit settling time of the AD797 make it ideal for buffering the inputs to ΣΔ ADCs or the outputs of high resolution DACs especially when they are used in critical applications such as seismic detection and spectrum analyzers. Key features such as a 50 mA output current drive and the specified power supply voltage range of ±5 to ±15 volts make the AD797 an excellent general purpose amplifier.



AD797 Voltage Noise Spectral Density



THD vs. Frequency

*Patent pending.

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AD797–SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD797A/S[1] Min	AD797A/S[1] Typ	AD797A/S[1] Max	AD797B Min	AD797B Typ	AD797B Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		25	80		10	40	µV
	T_{MIN} to T_{MAX}			50	125/180		30	60	µV
Offset Voltage Drift		±5 V, ±15 V		0.2	1.0		0.2	0.6	µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		0.25	1.5		0.25	0.9	µA
	T_{MIN} to T_{MAX}			0.5	3.0		0.25	2.0	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		100	400		80	200	nA
	T_{MIN} to T_{MAX}			120	600/700		120	300	nA
OPEN-LOOP GAIN	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 2 kΩ		1	20		2	20		V/µV
	T_{MIN} to T_{MAX}		1	6		2	10		V/µV
	R_{LOAD} = 600 Ω		1	15		2	15		V/µV
	T_{MIN} to T_{MAX}		1	5		2	7		V/µV
	@ 20 kHz[2]		14000	20000		14000	20000		V/V
DYNAMIC PERFORMANCE									
Gain Bandwidth Product	G = 1000	±15 V		110			110		MHz
	G = 1000[2]	±15 V		450			450		MHz
–3 dB Bandwidth	G = 10	±15 V		8			8		MHz
Full Power Bandwidth[3]	V_O = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		280			280		kHz
Slew Rate	R_{LOAD} = 1 kΩ	±15 V	12.5	20		12.5	20		V/µs
Settling Time to 0.0015%	10 V Step	±15 V		800	1200		800	1200	ns
COMMON-MODE REJECTION	V_{CM} = CMVR	±5 V, ±15 V	114	130		120	130		dB
	T_{MIN} to T_{MAX}		110	120		114	120		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±18 V		114	130		120	130		dB
	T_{MIN} to T_{MAX}		110	120		114	120		dB
INPUT VOLTAGE NOISE	f = 0.1 Hz to 10 Hz	±15 V		50			50		nV p-p
	f = 10 Hz	±15 V		1.7			1.7	2.5	nV/√Hz
	f = 1 kHz	±15 V		0.9	1.2		0.9	1.2	nV/√Hz
	f = 10 Hz–1 MHz	±15 V		1.0	1.3		1.0	1.2	µV rms
INPUT CURRENT NOISE	f = 1 kHz	±15 V		2.0			2.0		pA/√Hz
INPUT COMMON-MODE		±15 V	±11	±12		±11	±12		V
VOLTAGE RANGE		±5 V	±2.5	±3		±2.5	±3		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 2 kΩ	±15 V	±12	±13		±12	±13		V
	R_{LOAD} = 600 Ω	±15 V	±11	±13		±11	±13		V
	R_{LOAD} = 600 Ω	±5 V	±2.5	±3		±2.5	±3		V
Short-Circuit Current		±5 V, ±15 V		80			80		mA
Output Current[4]		±5 V, ±15 V	30	50		30	50		mA
TOTAL HARMONIC DISTORTION	R_{LOAD} = 1 kΩ, C_N = 50 pF f = 250 kHz, 3 V rms	±15 V		–98	–90		–98	–90	dB
	R_{LOAD} = 1 kΩ f = 20 kHz, 3 V rms	±15 V		–120	–110		–120	–110	dB
INPUT CHARACTERISTICS									
Input Resistance (Differential)				7.5			7.5		kΩ
Input Resistance (Common Mode)				100			100		MΩ
Input Capacitance (Differential)[5]				20			20		pF
Input Capacitance (Common Mode)				5			5		pF
OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			3			3		mΩ
POWER SUPPLY									
Operating Range			±5		±18	±5		±18	V
Quiescent Current		±5 V, ±15 V		8.2	10.5		8.2	10.5	mA

NOTES

[1]See standard military drawing for 883B specifications.

[2]Specified using external decompensation capacitor, see Applications section.

[3]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.

[4]Output Current for $|V_S - V_{OUT}| > 4$ V, $A_{OL} > 200$ kΩ.

[5]Differential input capacitance consists of 1.5 pF package capacitance and 18.5 pF from the input differential pair.

Specifications subject to change without notice.

ANALOG DEVICES

Low Power Video Op Amp with Disable

AD810

FEATURES

High Speed
- 80 MHz Bandwidth (3 dB, G = +1)
- 75 MHz Bandwidth (3 dB, G = +2)
- 1000 V/μs Slew Rate
- 50 ns Settling Time to 0.1% (V_O = 10 V Step)

Ideal for Video Applications
- 30 MHz Bandwidth (0.1 dB, G = +2)
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 2.9 nV/√Hz Input Voltage Noise
- 13 pA/√Hz Inverting Input Current Noise

Low Power
- 8.0 mA Supply Current max
- 2.1 mA Supply Current (Power-Down Mode)

High Performance Disable Function
- Turn-Off Time 100 ns
- Break Before Make Guaranteed
- Input to Output Isolation of 64 dB (OFF State)

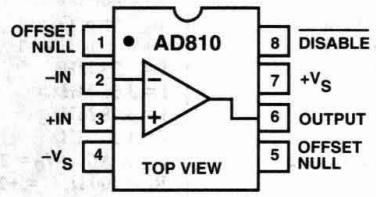
Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.9 V Output Swing Into a 150 Ω Load (V_S = ±5 V)

APPLICATIONS

Professional Video Cameras
Multimedia Systems
NTSC, PAL & SECAM Compatible Systems
Video Line Driver
ADC/DAC Buffer
DC Restoration Circuits

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), SOIC (R) and Cerdip (Q) Packages



PRODUCT DESCRIPTION

The AD810 is a composite and HDTV compatible, current feedback, video operational amplifier, ideal for use in systems such as multimedia, digital tape recorders and video cameras. The 0.1 dB flatness specification at bandwidth of 30 MHz (G = +2) and the differential gain and phase of 0.02% and 0.04° (NTSC) make the AD810 ideal for any broadcast quality video system.

The AD810 is ideal for power sensitive applications such as video cameras, offering a low power supply current of 8.0 mA max. The disable feature reduces the power supply current to only 2.1 mA, while the amplifier is not in use, to conserve power. Furthermore the AD810 is specified over a power supply range of ±5 V to ±15 V. The AD810 works well as an ADC or DAC buffer in video systems due to its unity gain bandwidth of 80 MHz.

Because the AD810 is a transimpedance amplifier, this bandwidth can be maintained over a wide range of gains while featuring a low noise of 2.9 nV/√Hz for wide dynamic range applications.

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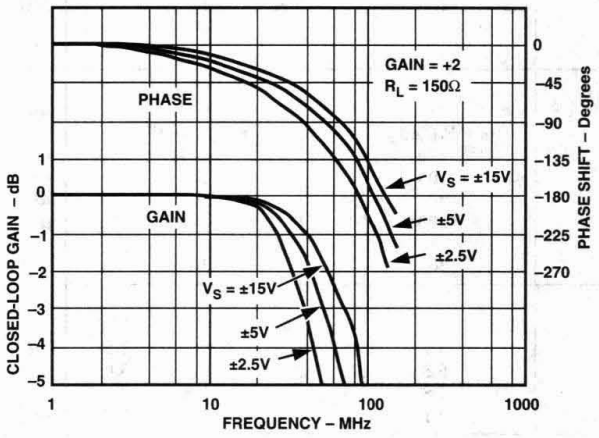
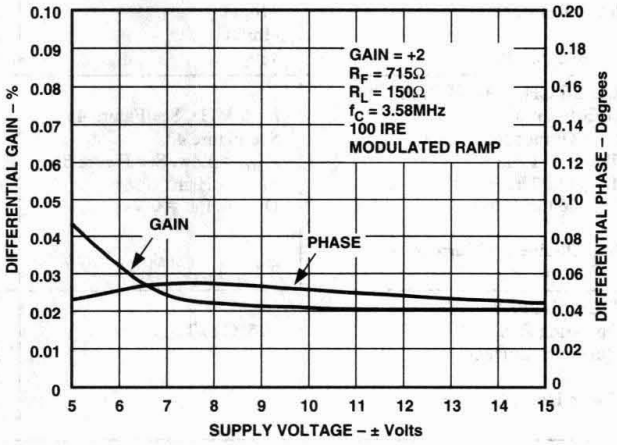
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD810AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD810AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD810AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8
5962-9313201MPA	–55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.



Closed-Loop Gain and Phase vs. Frequency, G = +2, R_L = 150, R_F = 715 Ω



Differential Gain and Phase vs. Supply Voltage

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AD810–SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_L = 150 Ω unless otherwise noted)

Parameter	Conditions	V_S	AD810A Min	AD810A Typ	AD810A Max	AD810S Min	AD810S Typ	AD810S Max	Units
DYNAMIC PERFORMANCE									
3 dB Bandwidth	(G = +2) R_{FB} = 715	±5 V	40	50		40	50		MHz
	(G = +2) R_{FB} = 715	±15 V	55	75		55	75		MHz
	(G = +1) R_{FB} = 1000	±15 V	40	80		40	80		MHz
	(G = +10) R_{FB} = 270	±15 V	50	65		50	65		MHz
0.1 dB Bandwidth	(G = +2) R_{FB} = 715	±5 V	13	22		13	22		MHz
	(G = +2) R_{FB} = 715	±15 V	15	30		15	30		MHz
Full Power Bandwidth	V_O = 20 V p-p, R_L = 400 Ω	±15 V		16			16		MHz
Slew Rate	R_L = 150 Ω	±5 V		350			350		V/µs
	R_L = 400 Ω	±15 V		1000			1000		V/µs
Settling Time to 0.1%	10 V Step, G = –1	±15 V		50			50		ns
Settling Time to 0.01%	10 V Step, G = –1	±15 V		125			125		ns
Differential Gain	f = 3.58 MHz	±15 V		0.02	0.05		0.02	0.05	%
	f = 3.58 MHz	±5 V		0.04	0.07		0.04	0.07	%
Differential Phase	f = 3.58 MHz	±15 V		0.04	0.07		0.04	0.07	Degrees
	f = 3.58 MHz	±5 V		0.045	0.08		0.045	0.08	Degrees
Total Harmonic Distortion	f = 10 MHz, V_O = 2 V p-p, R_L = 400 Ω, G = +2	±15 V		–61			–61		dBc
INPUT OFFSET VOLTAGE		±5 V, ±15 V		1.5	6		1.5	6	mV
	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	7.5		4	15	mV
Offset Voltage Drift				7			15		µV/°C
INPUT BIAS CURRENT									
–Input	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.7	5		0.8	5	µA
+Input	T_{MIN}–T_{MAX}	±5 V, ±15 V		2	7.5		2	10	µA
OPEN-LOOP TRANSRESISTANCE	T_{MIN}–T_{MAX}, V_O = ±10 V, R_L = 400 Ω	±15 V	1.0	3.5		1.0	3.5		MΩ
OPEN-LOOP DC VOLTAGE GAIN	T_{MIN}–T_{MAX}, V_O = ±10 V, R_L = 400 Ω	±15 V	86	100		80	100		dB
	V_O = ±2.5 V, R_L = 100 Ω	±5 V	76	88		72	88		dB
COMMON-MODE REJECTION	T_{MIN}–T_{MAX}								
V_{OS}	V_{CM} = ±12 V	±15 V	56	64		56	64		dB
±Input Current	T_{MIN}–T_{MAX}	±5 V, ±15 V		0.1	0.4		0.1	0.4	µA/V
POWER SUPPLY REJECTION		±4.5 V to ±18 V							
V_{OS}	T_{MIN}–T_{MAX}		65	72		60	72		dB
±Input Current	T_{MIN}–T_{MAX}			0.05	0.3		0.05	0.3	µA/V
INPUT VOLTAGE NOISE	f = 1 kHz	±5 V, ±15 V		2.9			2.9		nV/√Hz
INPUT CURRENT NOISE	$-I_{IN}$, f = 1 kHz	±5 V, ±15 V		13			13		pA/√Hz
	$+I_{IN}$, f = 1 kHz	±5 V, ±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V	±2.5	±3.0		±2.5	±3		V
		±15 V	±12	±13		±12	±13		V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 150 Ω, T_{MIN}–T_{MAX}	±5 V	±2.5	±2.9		±2.5	±2.9		V
	R_L = 400 Ω	±15 V	±12.5	±12.9		±12.5	±12.9		V
Output Current	T_{MIN}–T_{MAX}	±5 V, ±15 V	40	60		30	60		mA
OUTPUT RESISTANCE	Open Loop (5 MHz)			15			15		Ω
INPUT CHARACTERISTICS									
Input Resistance	+Input	±15 V	2.5	10		2.5	10		MΩ
	–Input	±15 V		40			40		Ω
Input Capacitance	+Input	±15 V		2			2		pF
DISABLE CHARACTERISTICS									
OFF Isolation	f = 5 MHz, See Figure 43			64			64		dB
OFF Output Impedance	See Figure 43			$(R_F + R_G)\|\|13$ pF			$(R_F + R_G)\|\|13$ pF		
Turn On Time	Z_{OUT} = Low, See Figure 54			170			170		ns
Turn Off Time	Z_{OUT} = High			100			100		ns
Disable Pin Current	Disable Pin = 0 V	±5 V		50	75		50	75	µA
		±15 V		290	400		290	400	µA
Min Disable Pin Current to Disable	T_{MIN}–T_{MAX}	±5 V, ±15 V		30			30		µA
POWER SUPPLY									
Operating Range	+25°C to T_{MAX}		±2.5		±18	±2.5		±18	V
Quiescent Current		±5 V		6.7	7.5		6.7	7.5	mA
		±15 V		6.8	8.0		6.8	8.0	mA
Power-Down Current		±5 V		1.8	2.3		1.8	2.3	mA
		±15 V		2.1	2.8		2.1	2.8	mA

Specification subject to change without notice.

ANALOG DEVICES

High Performance Video Op Amp

AD811

FEATURES

High Speed
- 140 MHz Bandwidth (3 dB, G = +1)
- 120 MHz Bandwidth (3 dB, G = +2)
- 35 MHz Bandwidth (0.1 dB, G = +2)
- 2500 V/μs Slew Rate
- 25 ns Settling Time to 0.1% (For a 2 V Step)
- 65 ns Settling Time to 0.01% (For a 10 V Step)

Excellent Video Performance (R_L =150 Ω)
- 0.01% Differential Gain, 0.01° Differential Phase
- Voltage Noise of 1.9 nV/√Hz

Low Distortion: THD = –74 dB @ 10 MHz

Excellent DC Precision
- 3 mV max Input Offset Voltage

Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.3 V Output Swing into a 75 Ω Load (V_S = ±5 V)

APPLICATIONS

Video Crosspoint Switchers, Multimedia Broadcast Systems

HDTV Compatible Systems

Video Line Drivers, Distribution Amplifiers

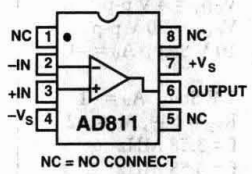
ADC/DAC Buffers

DC Restoration Circuits

Medical—Ultrasound, PET, Gamma & Counter Applications

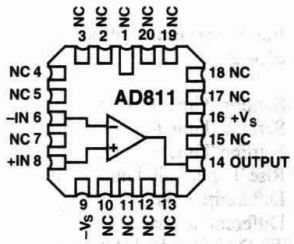
CONNECTION DIAGRAMS

8-Pin Plastic (N-8)
Cerdip (Q-8)
SOIC (SO-8) Packages



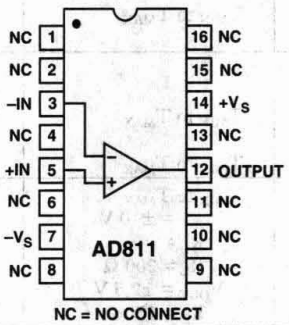
NC = NO CONNECT

20-Pin LCC (E-20A) Package



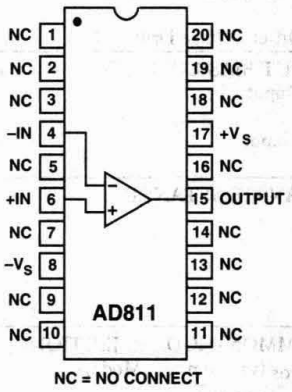
NC = NO CONNECT

16-Pin SOIC (R-16) Package



NC = NO CONNECT

20-Pin SOIC (R-20) Package



NC = NO CONNECT

10

PRODUCT DESCRIPTION

The AD811 is a wideband current-feedback operational amplifier, optimized for broadcast quality video systems. The –3 dB bandwidth of 120 MHz at a gain of +2 and differential gain and phase of 0.01% and 0.01° (R_L = 150 Ω) make the AD811 an excellent choice for all video systems. The AD811 is designed to meet a stringent 0.1 dB gain flatness specification to a bandwidth of 35 MHz (G = +2) in addition to the low differential gain and phase errors. This performance is achieved whether driving one or two back terminated 75 Ω cables, with a low power supply current of 16.5 mA. Furthermore, the AD811 is specified over a power supply range of ±4.5 V to ±18 V.

The AD811 is also excellent for pulsed applications where transient response is critical. It can achieve a maximum slew rate of greater than 2500 V/μs with a settling time of less than 25 ns to 0.1% on a 2 volt step and 65 ns to 0.01% on a 10 volt step.

The AD811 is ideal as an ADC or DAC buffer in data acquisition systems due to its low distortion up to 10 MHz and its wide unity gain bandwidth. Because the AD811 is a current feedback amplifier, this bandwidth can be maintained over a wide range of gains. The AD811 also offers low voltage and current noise of 1.9 nV/√Hz and 20 pA/√Hz, respectively, and excellent dc accuracy for wide dynamic range applications.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD811AN	–40°C to +85°C	N-8
AD811AR-16	–40°C to +85°C	R-16
AD811AR-20	–40°C to +85°C	R-20
AD811JR	0°C to +70°C	SO-8
AD811SQ/883B	–55°C to +125°C	Q-8
5962-9313001MPA	–55°C to +125°C	Q-8
AD811SE/883B	–55°C to +125°C	E-20A
5962-9313001M2A	–55°C to +125°C	E-20A
AD811JR-REEL	0°C to +70°C	SO-8
AD811JR-REEL7	0°C to +70°C	SO-8
AD811AR-16-REEL	–40°C to +85°C	R-16
AD811AR-16-REEL7	–40°C to +85°C	R-16
AD811AR-20-REEL	–40°C to +85°C	R-20
AD811ACHIPS	–40°C to +85°C	Die
AD811SCHIPS	–55°C to +125°C	Die

*E = Ceramic Leadless Chip Carrier; N = Plastic DIP; Q = Cerdip; SO (R) = Small Outline IC (SOIC). For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD811—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_{LOAD} = 150 Ω unless otherwise noted)

Model	Conditions	V_S	AD811J/A[1] Min	AD811J/A[1] Typ	AD811J/A[1] Max	AD811S[2] Min	AD811S[2] Typ	AD811S[2] Max	Units
DYNAMIC PERFORMANCE									
Small Signal Bandwidth (No Peaking)									
–3 dB									
G = +1	R_{FB} = 562 Ω	±15 V		140			140		MHz
G = +2	R_{FB} = 649 Ω	±15 V		120			120		MHz
G = +2	R_{FB} = 562 Ω	±5 V		80			80		MHz
G = +10	R_{FB} = 511 Ω	±15 V		100			100		MHz
0.1 dB Flat									
G = +2	R_{FB} = 562 Ω	±5 V		25			25		MHz
	R_{FB} = 649 Ω	±15 V		35			35		MHz
Full Power Bandwidth[3]	V_{OUT} = 20 V p-p	±15 V		40			40		MHz
Slew Rate	V_{OUT} = 4 V p-p	±5 V		400			400		V/µs
	V_{OUT} = 20 V p-p	±15 V		2500			2500		V/µs
Settling Time to 0.1%	10 V Step, A_V = –1	±15 V		50			50		ns
Settling Time to 0.01%				65			65		ns
Settling Time to 0.1%	2 V Step, A_V = –1	±5 V		25			25		ns
Rise Time, Fall Time	R_{FB} = 649, A_V = +2	±15 V		3.5			3.5		ns
Differential Gain	f = 3.58 MHz	±15 V		0.01			0.01		%
Differential Phase	f = 3.58 MHz	±15 V		0.01			0.01		Degree
THD @ f_C = 10 MHz	V_{OUT} = 2 V p-p, A_V = +2	±15 V		–74			–74		dBc
Third Order Intercept[4]	@ f_C = 10 MHz	±5 V		36			36		dBm
		±15 V		43			43		dBm
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.5	3		0.5	3	mV
	T_{MIN} to T_{MAX}				5			5	mV
Offset Voltage Drift				5			5		µV/°C
INPUT BIAS CURRENT									
–Input		±5 V, ±15 V		2	5		2	5	µA
	T_{MIN} to T_{MAX}				15			30	µA
+Input		±5 V, ±15 V		2	10		2	10	µA
	T_{MIN} to T_{MAX}				20			25	µA
TRANSRESISTANCE	T_{MIN} to T_{MAX}								
	V_{OUT} = ±10 V								
	R_L = ∞	±15 V	0.75	1.5		0.75	1.5		MΩ
	R_L = 200 Ω	±15 V	0.5	0.75		0.5	0.75		MΩ
	V_{OUT} = ±2.5 V								
	R_L = 150 Ω	±5 V	0.25	0.4		0.125	0.4		MΩ
COMMON-MODE REJECTION									
V_{OS} (vs. Common Mode)									
T_{MIN} to T_{MAX}	V_{CM} = ±2.5	±5 V	56	60		50	60		dB
T_{MIN} to T_{MAX}	V_{CM} = ±10 V	±15 V	60	66		56	66		dB
Input Current (vs. Common Mode)	T_{MIN} to T_{MAX}			1	3		1	3	µA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V								
V_{OS}	T_{MIN} to T_{MAX}		60	70		60	70		dB
+Input Current	T_{MIN} to T_{MAX}			0.3	2		0.3	2	µA/V
–Input Current	T_{MIN} to T_{MAX}			0.4	2		0.4	2	µA/V
INPUT VOLTAGE NOISE	f = 1 kHz			1.9			1.9		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz			20			20		pA/√Hz
OUTPUT CHARACTERISTICS									
Voltage Swing, Useful Operating Range[5]		±5 V		±2.9			±2.9		V
		±15 V		±12			±12		V
Output Current	T_J = +25°C			100			100		mA
Short-Circuit Current				150			150		mA
Output Resistance	(Open Loop @ 5 MHz)			9			9		Ω
INPUT CHARACTERISTICS									
+Input Resistance				1.5			1.5		MΩ
–Input Resistance				14			14		Ω
Input Capacitance	+Input			7.5			7.5		pF
Common-Mode Voltage Range		±5 V		±3			±3		V
		±15 V		±13			±13		V
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		14.5	16.0		14.5	16.0	mA
		±15 V		16.5	18.0		16.5	18.0	mA
TRANSISTOR COUNT	# of Transistors			40			40		

NOTES

[1]The AD811JR is specified with ±5 V power supplies only, with operation up to ±12 volts.

[2]See Analog Devices' military data sheet for 883B tested specifications.

[3]FPBW = slew rate/(2 π V_{PEAK}).

[4]Output power level, tested at a closed loop gain of two.

[5]Useful operating range is defined as the output voltage at which linearity begins to degrade.

Specifications subject to change without notice.

Dual, Current Feedback Low Power Op Amp

AD812

FEATURES

Two Video Amplifiers in One 8-Pin SOIC Package
Optimized for Driving Cables in Video Systems
Excellent Video Specifications (R_L = 150 Ω):
- **Gain Flatness 0.1 dB to 40 MHz**
- **0.02% Differential Gain Error**
- **0.02° Differential Phase Error**

Low Power
- **Operates on Single +3 V Supply**
- **5.5 mA/Amplifier Max Power Supply Current**

High Speed
- **145 MHz Unity Gain Bandwidth (3 dB)**
- **1600 V/μs Slew Rate**

Easy to Use
- **50 mA Output Current**
- **Output Swing to 1 V of Rails (150 Ω Load)**

APPLICATIONS

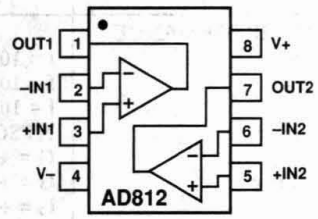
Video Line Driver
Professional Cameras
Video Switchers
Special Effects

PRODUCT DESCRIPTION

The AD812 is a low power, single supply, dual video amplifier. Each of the amplifiers have 50 mA of output current and are optimized for driving one back terminated video load (150 Ω) each. Each amplifier is a current feedback amplifier and features gain flatness of 0.1 dB to 40 MHz while offering differential gain and phase error of 0.02% and 0.02°.

PIN CONFIGURATION

8-Pin Plastic Mini-DIP & SOIC



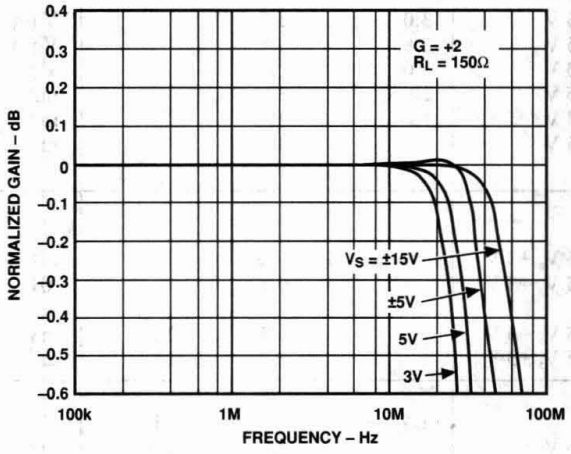
The AD812 offers low power of 4.0 mA per amplifier max (V_S = +5 V) and can run on a single +3 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals of 1 V p-p. Also, at gains of +2 the AD812 can swing 3 V p-p on a single +5 V power supply.

The outstanding bandwidth and high slew rate make the AD812 useful in many general purpose high speed applications where a single +5 V or dual power supplies up to ±15 V are available. The AD812 is available in the industrial temperature range of –40°C to +85°C.

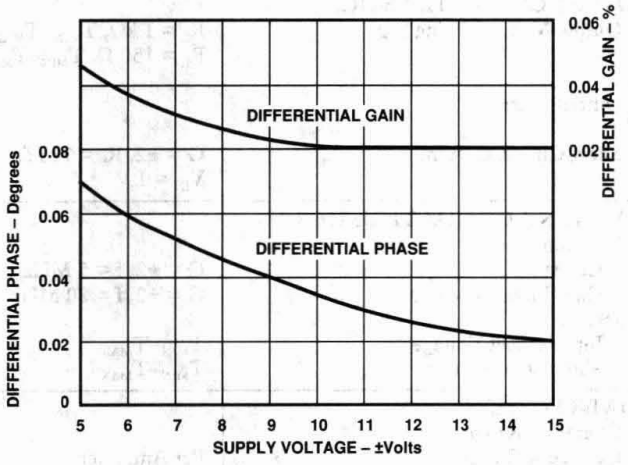
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD812AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD812AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.



Fine-Scale Gain Flatness vs. Frequency, Gain = +2, R_L = 150 Ω



Differential Gain and Phase vs. Supply Voltage, Gain = +2, R_L = 150 Ω

AD812–SPECIFICATIONS

Single Supply (@ T_A = +25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD812A Min	AD812A Typ	AD812A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	+5 V	35	50		MHz
		+3 V	30	40		MHz
Bandwidth for 0.1 dB Flatness	G = +2	+5 V	13	20		MHz
		+3 V	10	18		MHz
Slew Rate	G = +2, R_L = 1 kΩ	+5 V		125		V/µs
		+3 V		60		V/µs
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	f = 10 kHz	+5 V, +3 V		3.5		nV/√Hz
Input Current Noise	f = 10 kHz, +In	+5 V, +3 V		1.5		pA/√Hz
	f = 10 kHz, –In	+5 V, +3 V		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω	+5 V		0.07		%
	G = +1	+3 V		0.15		%
Differential Phase Error	G = +2	+5 V		0.06		Degrees
	G = +1	+3 V		0.15		Degrees
DC PERFORMANCE						
Input Offset Voltage		+5 V, +3 V		1.5	3	mV
Offset Drift		+5 V, +3 V		7		µV/°C
–Input Bias Current		+5 V, +3 V		2	10	µA
+Input Bias Current		+5 V, +3 V		0.2	1.0	µA
Open-Loop Voltage Gain	V_O = +2.5 V p-p	+5 V	69	73		dB
	V_O = +0.7 V p-p	+3 V		70		dB
Open-Loop Transresistance	V_O = +2.5 V p-p	+5 V	250	400		kΩ
	V_O = +0.7 V p-p	+3 V		300		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	+5 V		15		MΩ
	–Input	+5 V		90		Ω
Input Capacitance	+Input			2		pF
Input Common-Mode Voltage Range		+5 V	1.0		4.0	V
		+3 V	1.0		2.0	V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = 1.25 V to 3.75 V	+5 V	52	55		dB
–Input Current				3	5	µA/V
+Input Current				0.1	0.2	µA/V
Input Offset Voltage	V_{CM} = 1 V to 2 V	+3 V		52		dB
–Input Current				3.5		µA/V
+Input Current				0.1		µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing p-p	R_L = 1 kΩ, T_{MIN}–T_{MAX}	+5 V	3.0	3.2		V p-p
	R_L = 150 Ω, T_{MIN}–T_{MAX}	+5 V	2.8	3.1		V p-p
		+3 V	1.0	1.3		V p-p
Output Current		+5 V	20	30		mA
		+3 V	15	25		mA
Short Circuit Current	G = +2, R_F = 715 Ω	+5 V		40		mA
	V_{IN} = 1 V					
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, +3 V		–72		dB
Gain Flatness Match	G = +2, f = 20 MHz	+5 V, +3 V		0.1		dB
DC						
Input Offset Voltage	T_{MIN}–T_{MAX}	+5 V, +3 V		0.5	2.8	mV
–Input Bias Current	T_{MIN}–T_{MAX}	+5 V, +3 V		2	11	µA
POWER SUPPLY						
Operating Range			2.4		36	V
Quiescent Current	Per Amplifier	+5 V		3.2	4.0	mA
		+3 V		3.0	3.5	mA
	T_{MIN}–T_{MAX}	+5 V			4.5	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = +3 V to +30 V		72	80		dB
–Input Current				0.3	0.6	µA/V
+Input Current				0.005	0.05	µA/V

NOTES

For dual supply specifications, request complete data sheet.

Specifications subject to change without notice.

Single Supply, Low Power Triple Video Amplifier

AD813

FEATURES

Low Cost
Three Video Amplifiers in One Package
Optimized for Driving Cables in Video Systems
Excellent Video Specifications (R_L = 150 Ω)
- **Gain Flatness 0.1 dB to 50 MHz**
- **0.03% Differential Gain Error**
- **0.06° Differential Phase Error**

Low Power
- **Operates on Single +3 V to ±15 V Power Supplies**
- **5.5 mA/Amplifier Max Power Supply Current**

High Speed
- **125 MHz Unity Gain Bandwidth (–3 dB)**
- **500 V/μs Slew Rate**

High Speed Disable Function per Channel
- **Turn-Off Time 80 ns**

Easy to Use
- **50 mA Output Current**
- **Output Swing to 1 V of Rails**

APPLICATIONS

Video Line Driver
LCD Drivers
Computer Video Plug-In Boards
Ultrasound
RGB Amplifier
CCD Based Systems

PRODUCT DESCRIPTION

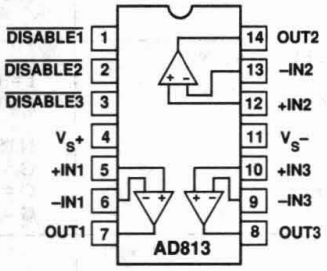
The AD813 is a low power, single supply triple video amplifier. Each of the three current feedback amplifiers is optimized for driving one back terminated video load (150 Ω). The AD813 is ideal for broadcast and consumer video electronics.

The AD813 offers low power per amplifier max and runs on a single +3 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals. While operating on a single +5 V supply the AD813 still achieves 0.1 dB flatness to 20 MHz and 0.05% & 0.05° of differential gain and phase performance.

The outstanding bandwidth and fast slew rate make the AD813 useful in many general purpose, high speed applications where a single +3 V or dual power supplies up to ±15 V are needed. Furthermore the AD813 contains a high speed disable function for each amplifier in order to power down the amplifier or high impedance the output. This can then be used in video multiplexing applications.

PIN CONFIGURATION

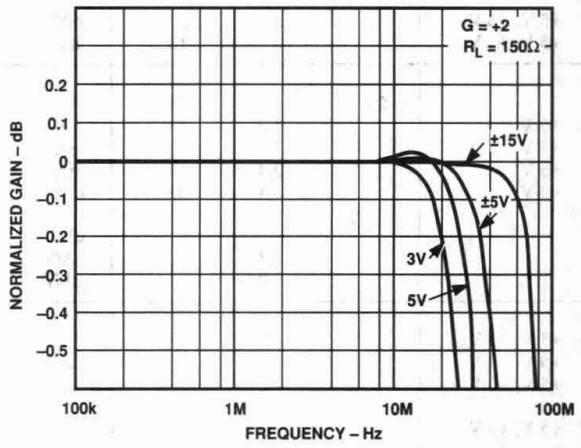
14-Pin DIP & SOIC Package



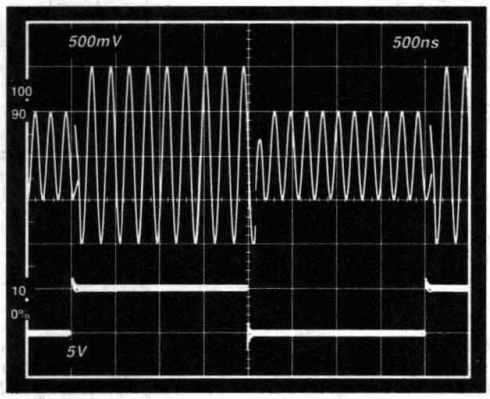
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD813AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD813AR-14	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD813A Chips	–40°C to +85°C	Die Form	

*For outline information see Package Information section.



Fine-Scale Gain Flatness vs. Frequency, G = +2, R_L = 150 Ω



Channel Switching Characteristics for a 3:1 Mux

AD813–SPECIFICATIONS

Single Supply (@ T_A = + 25°C, R_L = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD813A Min	AD813A Typ	AD813A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	G = +2, No Peaking	+5 V	35	50		MHz
		+3 V	25	40		MHz
Bandwidth for 0.1 dB						
Flatness	G = +2	+5 V	12	20		MHz
		+3 V	8	15		MHz
Slew Rate	G = +2, R_L = 1 kΩ	+5 V		100		V/µs
		+3 V		50		V/µs
NOISE/HARMONIC PERFORMANCE						
Input Voltage Noise	f = 10 kHz	+5 V, +3 V		3.5		$nV\sqrt{Hz}$
Input Current Noise	f = 10 kHz, +In	+5 V, +3 V		1.5		$pA\sqrt{Hz}$
	–In	+5 V, +3 V		18		$pA\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω	+5 V		0.05		%
	G = +1	+3 V		0.2		%
Differential Phase Error	G = +2	+5 V		0.05		Degrees
	G = +1	+3 V		0.2		Degrees
DC PERFORMANCE						
Input Offset Voltage		+5 V, +3 V		1.5	3	mV
Offset Drift		+5 V, +3 V		7		µV/°C
–Input Bias Current		+5 V, +3 V		7	30	µA
+Input Bias Current		+5 V, +3 V		0.5	1.5	µA
Open-Loop Voltage Gain	V_O = +2.5 V p-p	+5 V	67	70		dB
Open-Loop Transresistance	V_O = +3 V p-p	+5 V	200	300		kΩ
	V_O = +1 V p-p	+3 V		225		kΩ
INPUT CHARACTERISTICS						
Input Resistance	+Input	+5 V, +3 V		15		MΩ
	–Input	+5 V		90		Ω
Input Capacitance	+Input			2		pF
Input Common Mode		+5 V	1.0		4.0	V
Voltage Range		+3 V	1.0		2.0	V
Common-Mode Rejection Ratio						
Input Offset Voltage	V_{CM} = 1.25 V to 3.75 V	+5 V	54	58		dB
–Input Current				3	5	µA/V
+Input Current				0.1	0.2	µA/V
Input Offset Voltage	V_{CM} = 1 V to 2 V	+3 V		56		dB
–Input Current				3.5		µA/V
+Input Current				0.1		µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing p-p	R_L = 150 Ω, T_{MIN}–T_{MAX}	+5 V	3.0	3.2		±V p-p
		+3 V	1.0	1.3		±V p-p
Output Current		+5 V	20	30		mA
		+3 V	15	25		mA
Short Circuit Current	G = +2, R_F = 715 Ω	+5 V		40		mA
	V_{IN} = 1 V					
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, +3 V		–65		dB
Gain Flatness Match	G = +2, f = 20 MHz	+5 V, +3 V		0.1		dB
DC						
Input Offset Voltage	T_{MIN}–T_{MAX}	+5 V, +3 V		0.5	2.5	mV
–Input Bias Current	T_{MIN}–T_{MAX}	+5 V, +3 V		2	10	µA
POWER SUPPLY						
Operating Range			2.4		36	V
Quiescent Current	Per Amplifier	+5 V		3.2	4.0	mA
		+3 V		3.0	3.5	mA
Quiescent Current, Powered Down	Per Amplifier	+5 V		0.4	0.5	mA
		+3 V		0.4	0.5	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = +3.0 V to +30 V			76		dB
–Input Current				0.3		µA/V
+Input Current				0.005		µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 5 MHz	+5 V, +3 V		–55		dB
Off Output Impedance	G = +1	+5 V, +3 V		13		pF
Channel-to-Channel Isolation	2 or 3 Channel Mux, f = 5 MHz	+5 V, +3 V		–65		dB
Turn-On Time		+5 V, +3 V		100		ns
Turn-Off Time				80		ns

NOTES
For dual supply specifications, request complete data sheet.
Specifications subject to change without notice.

High Output Current Differential Driver

AD815

FEATURES

Flexible Configuration
- Differential Input & Output Driver or Two Single-Ended Drivers

High Output Power
- Power Package
  - 26 dBm Differential Line Drive for ADSL Application
  - 40 V p-p Differential Output Voltage, R_L = 50 Ω
  - 500 mA Minimum Output Drive/Amp, R_L = 5 Ω
- Thermally Enhanced SOIC
  - 200 mA Minimum Output Drive/Amp, R_L = 10 Ω

Low Distortion
- –66 dB @ 1 MHz THD, R_L = 200 Ω, V_{OUT} = 40 V p-p
- 0.05% & 0.45° Differential Gain & Phase, R_L = 25 Ω (6 Back-Terminated Video Loads)

High Speed
- 120 MHz Bandwidth (–3 dB)
- 900 V/μs Differential Slew Rate
- 70 ns Settling Time to 0.1%

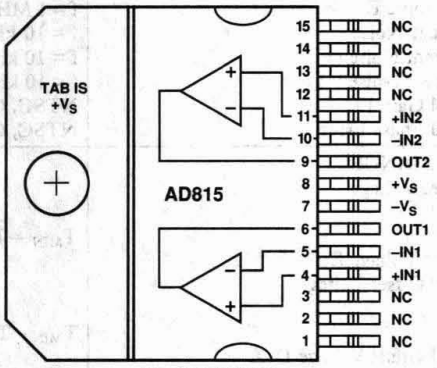
Thermal Shutdown

APPLICATIONS

ADSL, HDSL & VDSL Line Interface Driver
Coil or Transformer Driver
CRT Convergence & Astigmatism Adjustment
Video Distribution Amp
Twisted Pair Cable Driver

FUNCTIONAL BLOCK DIAGRAM

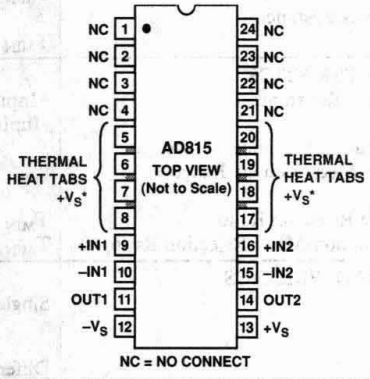
15-Pin Through-Hole SIP (Y) & Surface-Mount DDPAK(VR)



NC = NO CONNECT
REFER TO PAGE 3 FOR 24-PIN SOIC PACKAGE

PIN CONFIGURATION

24-Pin Thermally-Enhanced SOIC (RB-24)



NC = NO CONNECT
*HEAT TABS ARE CONNECTED TO THE POSITIVE SUPPLY.

PRODUCT DESCRIPTION

The AD815 consists of two high speed amplifiers capable of supplying a minimum of 500 mA. They are typically configured as a differential driver enabling an output signal of 40 V p-p on ±15 V supplies. This can be increased further with the use of a coupling transformer with a greater than 1:1 turns ratio. The low harmonic distortion of –66 dB @ 1 MHz into 200 Ω combined with the wide bandwidth and high current drive make the differential driver ideal for communication applications such as subscriber line interfaces for ADSL, HDSL and VDSL.

The AD815 differential slew rate of 900 V/μs and high load drive are suitable for fast dynamic control of coils or transformers, and the video performance of 0.05% & 0.45° differential gain & phase into a load of 25 Ω enable up to 12 back-terminated loads to be driven.

Three package styles are available, and all work over the industrial temperature range (–40°C to +85°C). Maximum driver performance is achieved with the power package available as through hole (Y) and surface-mount (VR), while the 24-pin SOIC (RB) driver performance is reduced due to the smaller package which has a higher thermal resistance.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD815AY	–40°C to +85°C	15-Pin Through Hole SIP with Staggered Leads	Y-15
AD815AVR	–40°C to +85°C	15-Pin Surface Mount DDPAK	VR-15
AD815ARB-24	–40°C to +85°C	24-Pin Thermally Enhanced SOIC	RB-24
AD815ARB-24-REEL	–40°C to +85°C	24-Pin Thermally Enhanced SOIC	RB-24

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD815–SPECIFICATIONS (@ T_A = +25°C, V_S = ±15 V dc, R_{FB} = 1 kΩ and R_{LOAD} = 100 Ω unless otherwise noted)

Model	Conditions	V_S	AD815A Min	AD815A Typ	AD815A Max	Units
DYNAMIC PERFORMANCE						
Small Signal Bandwidth (–3 dB)	G = +1	±15	100	120		MHz
	G = +1	±5	90	110		MHz
Bandwidth (0.1 dB)	G = +2	±15		40		MHz
	G = +2	±5		10		MHz
Differential Slew Rate	V_{OUT} = 20 V p-p, G = +2	±15	800	900		V/µs
Settling Time to 0.1%	10 V Step, G = +2	±15		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f = 1 MHz, R_{LOAD} = 200 Ω, V_{OUT} = 40 V p-p	±15		–66		dBc
Input Voltage Noise	f = 10 kHz, G = +2 (Single Ended)	±5, ±15		1.85		nV/√Hz
Input Current Noise (+I_{IN})	f = 10 kHz, G = +2	±5, ±15		1.8		pA/√Hz
Input Current Noise (–I_{IN})	f = 10 kHz, G = +2	±5, ±15		19		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_{LOAD} = 25 Ω	±15		0.05		%
Differential Phase Error	NTSC, G = +2, R_{LOAD} = 25 Ω	±15		0.45		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5		5	8	mV
		±15		10	15	mV
	T_{MIN} – T_{MAX}				30	mV
Input Offset Voltage Drift				20		µV/°C
Differential Offset Voltage		±5		0.5	2	mV
		±15		0.5	4	mV
	T_{MIN} – T_{MAX}				5	mV
Differential Offset Voltage Drift				10		µV/°C
–Input Bias Current		±5, ±15		10	90	µA
	T_{MIN} – T_{MAX}				150	µA
+Input Bias Current		±5, ±15		2	5	µA
	T_{MIN} – T_{MAX}				5	µA
Differential Input Bias Current		±5, ±15		10	75	µA
	T_{MIN} – T_{MAX}				100	µA
Open-Loop Transresistance		±5, ±15	1.0	5.0		MΩ
	T_{MIN} – T_{MAX}		0.5			MΩ
INPUT CHARACTERISTICS						
Differential Input Resistance	+Input	±15		7		MΩ
	–Input			15		Ω
Differential Input Capacitance		±15		1.4		pF
Input Common-Mode Voltage Range		±15		13.5		±V
		±5		3.5		±V
Common-Mode Rejection Ratio	T_{MIN} – T_{MAX}	±5, ±15	57	65		dB
Differential Common-Mode Rejection Ratio	T_{MIN} – T_{MAX}	±5, ±15	80	100		dB
OUTPUT CHARACTERISTICS						
Voltage Swing	Single Ended, R_{LOAD} = 25 Ω	±15	11.0	11.7		±V
		±5	1.1	1.8		±V
	Differential, R_{LOAD} = 50 Ω	±15	21	23		±V
	T_{MIN} – T_{MAX}	±15	22.5	24.5		±V
Output Current[1, 2]						
VR, Y	R_{LOAD} = 5 Ω	±15	500	750		mA
		±5	350	400		mA
RB-24	R_{LOAD} = 10 Ω	±15	200	250		mA
Short Circuit Current		±15		1.0		A
Output Resistance		±15		13		Ω
MATCHING CHARACTERISTICS						
Crosstalk	f = 1 MHz	±15		–65		dB
POWER SUPPLY						
Operating Range[3]	T_{MIN} – T_{MAX}				±18	V
Quiescent Current		±5		23	30	mA
		±15		30	40	mA
	T_{MIN} – T_{MAX}	±5			40	mA
		±15			55	mA
Power Supply Rejection Ratio	T_{MIN} – T_{MAX}	±5, ±15	–55	–66		dB

NOTES
[1]Output current is limited in the 24-pin SOIC package to the maximum power dissipation. See absolute maximum ratings and derating curves.
[2]See Figure 12 for bandwidth, gain, output drive recommended operation range.
[3]Observe derating curves for maximum junction temperature.

Specifications subject to change without notice.

ANALOG DEVICES

Quad, High Speed, High Current Drive Amplifier

AD816

FEATURES

Flexible Configuration
- Two Low Noise Voltage Feedback Amplifiers with High Current Drive, Ideal for ADSL Receivers or Drivers for Low Impedance Loads such as CRT Coils
- Two High Current Drive Amplifiers, Ideal for an ADSL Differential Driver or Single Ended Drivers for Low Impedance Loads such as CRT Coils

CURRENT FEEDBACK AMPLIFIERS/DRIVERS

High Output Drive
- 26 dBm Differential Line Drive for ADSL Transmitters
- 40 V p-p Differential Output Voltage, R_L = 50 Ω @ 1 MHz
- 500 mA Peak Current, R_L = 5 Ω

Low Distortion
- –66 dB @ 1 MHz THD, R_L = 200 Ω, V_O = 40 V p-p

High Speed
- 120 MHz Bandwidth (–3 dB)
- 900 V/µs Slew Rate
- 70 ns Settling Time to 0.1%

VOLTAGE FEEDBACK AMPLIFIERS/RECEIVERS

High Input Performance
- 4 nV/√Hz Voltage Noise
- 2 mV Max Input Offset Voltage

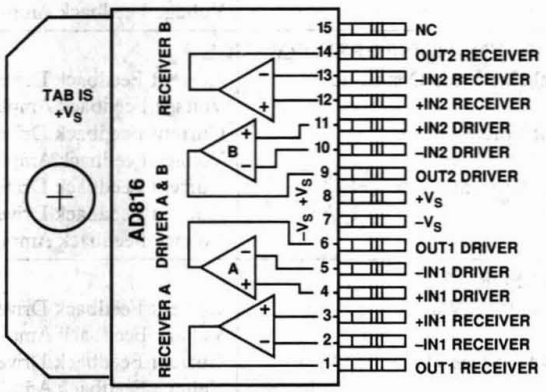
Low Distortion
- –66 dB @ 1 MHz THD, V_O = 10 V p-p

High Speed
- 100 MHz Bandwidth (–3 dB)
- 150 V/µs Slew Rate

High Output Drive
- 70 mA Output Current Drive

APPLICATIONS
- ADSL, VDSL & HDSL Line Interface Driver & Receiver
- CRT Convergence & Astigmatism Adjustment
- Coil & Transformer Drivers
- Composite Audio Amplifiers

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD816AY	–40°C to +85°C	15-Pin Through Hole SIP with Staggered Leads & 90° Lead Form.
AD816AYS	–40°C to +85°C	15-Pin Through Hole SIP with Staggered Leads & Straight Lead Form
AD816AVR	–40°C to +85°C	15-Pin Surface Mount DDPAK

*For outline information see Package Information section.

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PRODUCT DESCRIPTION

The AD816 consists of two high current drive and two low noise amplifiers. These can be configured differentially for driving low impedance loads and receiving signals over twisted pair cable or could be used independently for single ended driving application such as correction circuits within high resolution CRT Monitors.

The two high output drive amplifiers are capable of supplying a minimum of 500 mA output current and when configured differentially, 40 V p-p differential output swing can be achieved on ±15 V supplies into a load of 50 Ω. The drivers have 120 MHz of bandwidth and 900 V/µs of slew rate while featuring total harmonic distortion of –66 dB at 1 MHz into a 50 Ω load, features required for high frequency telecommunication subscriber line drivers.

The low noise voltage feedback amplifiers are fully independent and can be configured differentially for use as receiver amplifiers within a subscriber line hybrid interface or individually for signal conditioning or filtering. The low noise of 4 nV/√Hz and distortion of –68 dB at 1 MHz enable low level signals to be resolved and amplified in the presence of large common-mode voltages. 100 MHz of bandwidth and 150 V/µs of slew rate combined with a load drive capability of 70 mA enable these amplifiers to drive passive filters and low inductance coils. The AD816 is available in low thermal resistance power packages and will operate over the industrial temperature range (–40°C to +85°C).

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD816–SPECIFICATIONS (@ T_A = +25°C, V_S = ±15 V, Current Feedback Driver, R_{FB} = 1 kΩ and R_L = 100 Ω, Voltage Feedback, R_L = 500 Ω unless otherwise noted)

Parameter		Conditions	AD816A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
–3 dB Small Signal Bandwidth	Current Feedback Drivers	G = +1	TBD	120		MHz
	Voltage Feedback Amplifiers	G = –1	TBD	100		MHz
Slew Rate: Differential	Current Feedback Drivers	V_O = 20 V p-p		900		V/µs
Single Ended	Voltage Feedback Amplifiers	V_O = 4 V p-p		150		V/µs
Settling Time to 0.1%	Current Feedback Driver	G = +2, V_O = 10 V Step		70		ns
	Voltage Feedback Amplifiers	G = +2, V_O = 10 V Step		45		ns
DISTORTION/NOISE PERFORMANCE						
Total Harmonic Distortion	Current Feedback Drivers	f_C = 1 MHz, V_O = 20 V p-p, G = +2		–66		dBc
	Voltage Feedback Amplifiers	f_C = 1 MHz, V_O = 2 V p-p, G = +2		–68		dBc
Input Voltage Noise	Current Feedback Drivers	f = 10 kHz, G = +2 (Single Ended)		1.85		nV/√Hz
	Voltage Feedback Amplifiers	f = 10 kHz, G = +2 (Single Ended)		4		nV/√Hz
Input Current Noise ($+I_{IN}$)	Current Feedback Drivers	f = 10 kHz, G = +2		1.8		pA/√Hz
($-I_{IN}$)	Current Feedback Drivers	f = 10 kHz, G = +2		19		pA/√Hz
	Voltage Feedback Amplifiers	f = 10 kHz, G = +2		2		pA/√Hz
DC PERFORMANCE						
Input Offset Voltage	Current Feedback Drivers			10	15	mV
	Voltage Feedback Amplifiers			1	2	mV
Offset Voltage Drift	Current Feedback Drivers			20		µV/°C
	Voltage Feedback Amplifiers			10		µV/°C
Differential Offset Voltage	Current Feedback Drivers			2	5	mV
Differential Offset Voltage Drift	Current Feedback Drivers			10		µV/°C
– Input Bias Current	Current Feedback Drivers			10		µA
+Input Bias Current	Current Feedback Drivers			2		µA
Input Bias Current	Voltage Feedback Amplifiers			5		µA
Differential Input Bias Current	Current Feedback Drivers			10		µA
Offset Current	Voltage Feedback Amplifiers				25	µA
Open Loop Transresistance	Current Feedback Drivers		1.0	5		MΩ
Open Loop Gain	Voltage Feedback Amplifiers			150		dB
INPUT CHARACTERISTICS						
Input Resistance	Current Feedback Drivers	Differential + Input		7		kΩ
		–Input		15		Ω
	Voltage Feedback Amplifiers			300		kΩ
Input Capacitance	Current Feedback Drivers	Differential		1.4	TBD	pF
	Voltage Feedback Amplifiers			1.5		pF
Common-Mode Voltage Range	Current Feedback Drivers			±13.5		V
	Voltage Feedback Amplifiers			–13.4 to +14.3		V
Common-Mode Rejection Range	Current Feedback Drivers	Single Ended	TBD	63		dB
	Current Feedback Drivers	Differential		100		dB
	Voltage Feedback Amplifiers			TBD		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	Current Feedback Drivers	Single Ended, R_L = 25 Ω		23.4		V p-p
	Current Feedback Drivers	Differential, R_L = 50 Ω		46	TBD	V p-p
	Voltage Feedback Amplifiers	Single Ended, R_L = 150 Ω		25		V p-p
Output Current	Current Feedback Drivers	R_L = 5 Ω, 500 kHz	500	750		mA
	Voltage Feedback Amplifiers	R_L = 5 Ω, 500 kHz	70	85		mA
Short Circuit Current	Current Feedback Drivers			1.0		A
	Voltage Feedback Amplifiers			110		mA
MATCHING CHARACTERISTICS						
Cross Talk	Driver to Driver	f = 1 MHz, V_O = 40 V p-p		TBD		dB
	Drivers to Amplifiers	f = 1 MHz, V_O = 40 V p-p		TBD		dB
	Amplifiers to Amplifiers	f = 1 MHz, V_O = 40 V p-p		TBD		dB
POWER SUPPLY						
Operating Range			±5		±18	V
Quiescent Current				30	TBD	mA
Power Supply Rejection Ratio	Current Feedback Drivers		TBD	–66		dB
Voltage Feedback Amplifiers		TBD		–80		dB

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

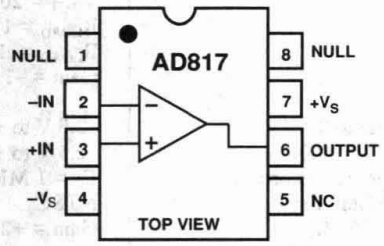
High Speed, Low Power Wide Supply Range Amplifier

AD817

FEATURES
Low Cost
High Speed
50 MHz Unity Gain Bandwidth
350 V/μs Slew Rate
45 ns Settling Time to 0.1% (10 V Step)
Flexible Power Supply
Specified for Single (+5 V) and Dual (±5 V to ±15 V) Power Supplies
Low Power: 7.5 mA max Supply Current
High Output Drive Capability
Drives Unlimited Capacitive Load
50 mA Minimum Output Current
Excellent Video Performance
70 MHz 0.1 dB Bandwidth (Gain = +1)
0.04% & 0.08° Differential Gain & Phase Errors @ 3.58 MHz
Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N) and SOIC (R) Packages



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD817 is a low cost, low power, single/dual supply, high speed op amp which is ideally suited for a broad spectrum of signal conditioning and data acquisition applications. This breakthrough product also features high output current drive capability and the ability to drive an unlimited capacitive load while still maintaining excellent signal integrity.

The 50 MHz unity gain bandwidth, 350 V/μs slew rate and settling time of 45 ns (0.1%) make possible the processing of high speed signals common to video and imaging systems. Furthermore, professional video performance is attained by offering differential gain & phase errors of 0.04% & 0.08° @ 3.58 MHz and 0.1 dB flatness to 70 MHz (gain = +1).

The AD817 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 7.5 mA and excellent ac characteristics under all power supply conditions, make the AD817 the ideal choice for many demanding yet power sensitive applications.

In applications such as ADC buffers and line drivers the AD817 simplifies the design task with its unique combination of a 50 mA minimum output current and the ability to drive unlimited capacitive loads.

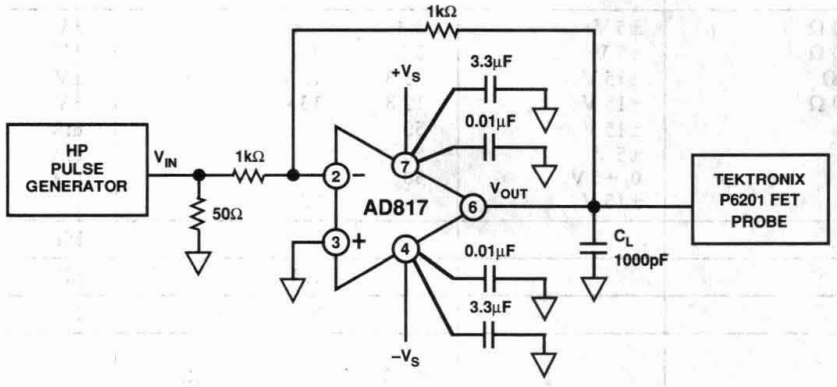
The AD817 is available in 8-pin plastic mini-DIP and SOIC packages.

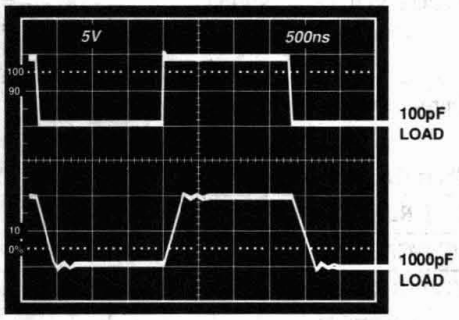
10

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD817AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD817AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.





AD817 Driving a Large Capacitive Load

AD817—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD817A Min	AD817A Typ	AD817A Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	18	30		MHz
		±15 V	40	70		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth[1]	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = –1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		70		ns
Total Harmonic Distortion	F_C = 1 MHz	±15 V		63		dB
Differential Gain Error	NTSC	±15 V		0.04	0.08	%
(R_{LOAD} = 150 Ω)	Gain = +2	±5 V		0.05	0.1	%
		0, +5 V		0.11		%
Differential Phase Error	NTSC	±15 V		0.08	0.1	Degrees
(R_{LOAD} = 150 Ω)	Gain = +2	±5 V		0.06	0.1	Degrees
		0, +5 V		0.14		Degrees
INPUT OFFSET VOLTAGE		±5 V to ±15 V		0.5	2	mV
Offset Drift				10		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	6.6	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		25	200	nA
Offset Current Drift				0.3		nA/°C
OPEN LOOP GAIN	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		4	6		V/mV
	V_{OUT} = ±7.5 V	±15 V				
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5	78	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V, ±15 V		15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
INPUT COMMON-MODE		±5 V	+3.8	+4.3		V
VOLTAGE RANGE			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
INPUT RESISTANCE				300		kΩ
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		7.0	7.5	mA
		±15 V			7.5	mA

Specifications subject to change without notice.

Low Cost, Low Power Video Op Amp

AD818

FEATURES

Low Cost
Excellent Video Performance
- **55 MHz 0.1 dB Bandwidth (Gain = +2)**
- **0.01% & 0.05° Differential Gain & Phase Errors**

High Speed
- **130 MHz Bandwidth (3 dB, G = +2)**
- **100 MHz Bandwidth (3 dB, G+ = –1)**
- **500 V/μs Slew Rate**
- **80 ns Settling Time to 0.01% (V_O = 10 V Step)**

High Output Drive Capability
- **50 mA Minimum Output Current**
- **Ideal for Driving Back Terminated Cables**

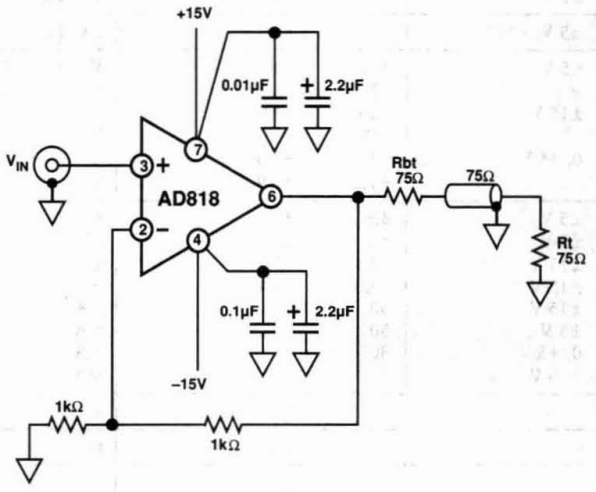
Flexible Power Supply
- **Specified for Single (+5 V) and Dual (±5 V to ±15 V) Power Supplies**
- **Low Power: 7.5 mA max Supply Current**

Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

PRODUCT DESCRIPTION

The AD818 is a low cost, video op amp optimized for use in video applications which require gains equal to or greater than +2 or –1. The AD818 low differential gain and phase errors, single supply functionality, low power and high output drive make it ideal for cable driving applications such as video cameras and professional video equipment.

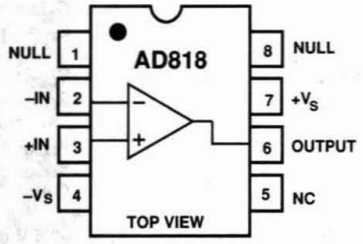
With video specs like 0.1 dB flatness to 55 MHz and low differential gain and phase errors of 0.01% and 0.05°, along with 50 mA of output current, the AD818 is an excellent choice for any video application. The 130 MHz 3 dB bandwidth (G = +2) and 500 V/μs slew rate make the AD818 useful in many high speed applications including: video monitors, CATV, color copiers, image scanners and fax machines.



AD818 Video Line Driver

CONNECTION DIAGRAMS

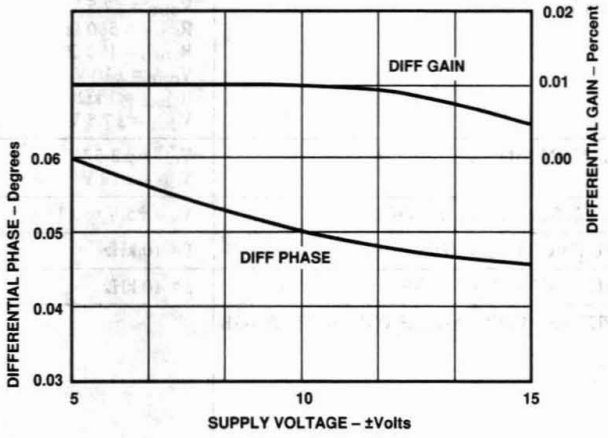
8-Pin Plastic Mini-DIP (N), and SOIC (R) Packages



NC = NO CONNECT

The AD818 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 7.5 mA and excellent ac characteristics under all power supply conditions, make the AD818 the ideal choice for many demanding yet power sensitive applications.

The AD818 is a voltage feedback op amp and excels as a gain stage in high speed and video systems (gain = >2 or –1). It achieves a settling time of 45 ns to 0.1%, with a low input offset voltage of 2 mV max.



AD818 Differential Gain and Phase vs. Supply

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD818AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD818AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD818AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD818—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD818A Min	AD818A Typ	AD818A Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	Gain = +2	±5 V	70	95		MHz
		±15 V	100	130		MHz
		0, +5 V	40	55		MHz
	Gain = –1	±5 V	50	70		MHz
		±15 V	70	100		MHz
		0, +5 V	30	50		MHz
Bandwidth for 0.1 dB Flatness	Gain = +2	±5 V	20	43		MHz
	C_C = 2 pF	±15 V	40	55		MHz
		0, +5 V	10	18		MHz
	Gain = –1	±5 V	18	34		MHz
	C_C = 2 pF	±15 V	40	72		MHz
		0, +5 V	10	19		MHz
Full Power Bandwidth	V_{OUT} = 5 V p-p					
	R_{LOAD} = 500 Ω	±5 V		25.5		MHz
	V_{OUT} = 20 V p-p					
	R_{LOAD} = 1 kΩ	±15 V		8.0		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	350	400		V/µs
	Gain = –1	±15 V	450	500		V/µs
		0, +5 V	250	300		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		80		ns
Total Harmonic Distortion	F_C = 1 MHz	±15 V		63		dB
Differential Gain Error	NTSC	±15 V		0.005	0.01	%
(R_L = 150 Ω)	Gain = +2	±5 V		0.01	0.02	%
		0, +5 V		0.08		%
Differential Phase Error	NTSC	±15 V		0.045	0.09	Degrees
(R_L = 150 Ω)	Gain = +2	±5 V		0.06	0.09	Degrees
		0, +5 V		0.1		Degrees
Cap Load Drive				10		pF
INPUT OFFSET VOLTAGE		±5 V to ±15 V		0.5	2	mV
Offset Drift				10		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	6.6	nA
INPUT OFFSET CURRENT		±5 V, ±15 V		25	200	nA
Offset Current Drift				0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		3	5		V/mV
	R_{LOAD} = 150 Ω		2	4		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		6	9		V/mV
	V_{OUT} = ±7.5 V	±15 V				
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	82	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		80	90		dB
INPUT VOLTAGE NOISE	f = 10 kHz	±5 V, ±15 V		10		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V	+3.8	+4.3		V
			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
INPUT RESISTANCE				300		kΩ
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		7.0	7.5	mA
		±15 V			7.5	mA

Specifications subject to change without notice.

Single Supply, Rail-to-Rail Low Power FET-Input Op Amps

AD820/AD822

FEATURES

TRUE SINGLE SUPPLY OPERATION
- Output Swings Rail to Rail
- Input Voltage Range Extends Below Ground
- Single Supply Capability from +3 V to +36 V
- Dual Supply Capability from ±1.5 V to ±18 V

HIGH LOAD DRIVE
- Capacitive Load Drive of 350 pF, G = 1
- Minimum Output Current of 15 mA

EXCELLENT AC PERFORMANCE FOR LOW POWER
- 800 μA Max Quiescent Current per Amplifier
- Unity Gain Bandwidth: 1.8 MHz
- Slew Rate of 3.0 V/μs

GOOD DC PERFORMANCE
- 800 μV Max Input Offset Voltage
- 2 μV/°C Typ Offset Voltage Drift
- 25 pA Max Input Bias Current

LOW NOISE
- 13 nV/√Hz @ 10 kHz

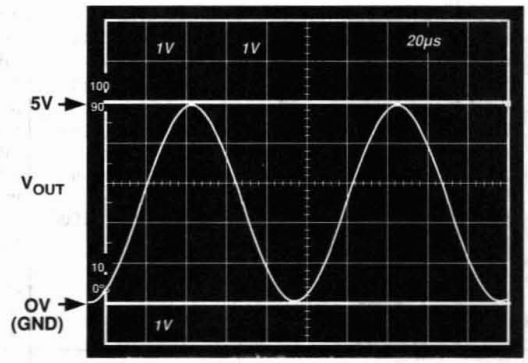
NO PHASE INVERSION

APPLICATIONS

Battery Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

PRODUCT DESCRIPTION

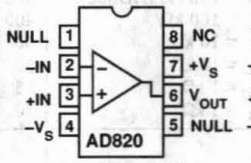
The AD820/AD822 is a precision, low power FET input op amp that can operate from a single supply of +3.0 V to +36 V, or dual supplies of ±1.5 V to ±18 V. They have true single supply capability with an input voltage range extending below the negative rail, allowing them to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.



Gain of +2 Amplifier; V_S = +5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 Volts, R_L = 100 kΩ

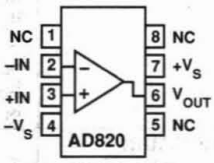
CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP



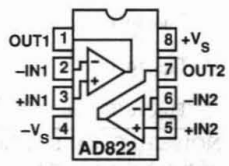
NC = NO CONNECT

8-Pin SOIC



NC = NO CONNECT

8-Pin Plastic DIP, Cerdip and SOIC



Offset voltage of 800 μV max, offset voltage drift of 2 μV/°C, input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz and 3 V/μs slew rate are provided with a low supply current of 800 μA per amplifier. The AD820 and AD822 drive up to 350 pF of direct capacitive load as a follower, and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD820AN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD820BN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD820AR	–40°C to +85°C	8-Pin SOIC	R-8
AD820BR	–40°C to +85°C	8-Pin SOIC	R-8
AD820AR-3V	–40°C to +85°C	8-Pin SOIC	R-8
AD820AN-3V	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD820AR-REEL	–40°C to +85°C	8-Pin SOIC	R-8
AD820AR-REEL7	–40°C to +85°C	8-Pin SOIC	R-8
AD820AR-3V-REEL	–40°C to +85°C	8-Pin SOIC	R-8
AD820AR-3V-REEL7	–40°C to +85°C	8-Pin SOIC	R-8
AD820BR-REEL	–40°C to +85°C	8-Pin SOIC	R-8
AD820BR-REEL7	–40°C to +85°C	8-Pin SOIC	R-8
AD822AR-REEL	–40°C to +85°C	8-Pin SOIC	R-8
AD822AR-REEL7	–40°C to +85°C	8-Pin SOIC	R-8
AD822AR-3V-REEL	–40°C to +85°C	8-Pin SOIC	R-8
AD822AR-3V-REEL7	–40°C to +85°C	8-Pin SOIC	R-8
AD822BR-REEL	–40°C to +85°C	8-Pin SOIC	R-8
AD822BR-REEL7	–40°C to +85°C	8-Pin SOIC	R-8
AD822AN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822BN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822AR	–40°C to +85°C	8-Pin SOIC	R-8
AD822BR	–40°C to +85°C	8-Pin SOIC	R-8
AD822AR-3V	–40°C to +85°C	8-Pin SOIC	R-8
AD822AN-3V	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD822ACHIPS	–40°C to +85°C	Die	
Standard Military Drawing[3]	–55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1]AD822 Spice model is available on ADI Model Disc.
[2]For outline information see Package Information section.
[3]Contact factory for availability.

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AD820/AD822–SPECIFICATIONS (V_S = 0, 5 V @ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A/AD822A Min	AD820A/AD822A Typ	AD820A/AD822A Max	AD820B/AD822B Min	AD820B/AD822B Typ	AD820B/AD822B Max	AD822S[1] Min	AD822S[1] Typ	AD822S[1] Max	Units
DC PERFORMANCE											
Initial Offset			0.1	0.8		0.1	0.4		0.1	0.8	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9		0.5		mV
Offset Drift			2.0			2.0			2.0		µV/°C
Input Bias Current	V_{CM} = 0 V to 4 V		2	25		2	10		2	25	pA
at T_{MAX}			0.5	5		0.5	2.5		0.5		nA
Input Offset Current			2	20		2	10		2	20	pA
at T_{MAX}			0.5			0.5			1.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V										
	R_L = 100 kΩ (AD820)	400	1000		400	1000					V/mV
	R_L = 100 kΩ (AD822)	500	1000		500	1000		500	1000		V/mV
T_{MIN} to T_{MAX}	R_L = 100 kΩ	400			400						V/mV
	R_L = 10 kΩ	80	150		80	150		80	150		V/mV
T_{MIN} to T_{MAX}	R_L = 10 kΩ	80			80						V/mV
	R_L = 1 kΩ	15	30		15	30		15	30		V/mV
T_{MIN} to T_{MAX}	R_L = 1 kΩ	10			10						V/mV
NOISE/HARMONIC PERFORMANCE											
Input Voltage Noise											
	0.1 Hz to 10 Hz		2			2			2		µV p-p
	f = 10 Hz		25			25			25		nV/√Hz
	f = 100 Hz		21			21			21		nV/√Hz
	f = 1 kHz		16			16			16		nV/√Hz
	f = 10 kHz		13			13			13		nV/√Hz
Input Current Noise	0.1 Hz to 10 Hz		18			18			18		fA p-p
	f = 1 kHz		0.8			0.8			0.8		fA/√Hz
Harmonic Distortion	R_L = 10 kΩ										
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93			–93		dB
DYNAMIC PERFORMANCE											
Unity Gain Frequency			1.8			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210			210		kHz
Slew Rate			3			3			3		V/µs
Settling Time											
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4			1.4		µs
to 0.01%			1.8			1.8			1.8		µs
MATCHING CHARACTERISTICS	AD822 Only										
Initial Offset				1.0			0.5			1.6	mV
Max Offset over Temperature				1.6			1.3				mV
Offset Drift			3			3			3		µV/°C
Input Bias Currents				20			10			20	pA
Crosstalk @ f = 1 kHz	R_L = 5 kΩ		–130			–130			–130		dB
f = 100 kHz			–93			–93			–93		dB
INPUT CHARACTERISTICS											
Common-Mode Voltage Range[1]		–0.2		4	–0.2		4	–0.2		4	V
T_{MIN} to T_{MAX}		–0.2		4	–0.2		4				V
CMRR (AD820)	V_{CM} = 0 V to +2 V	66	80		72	80					dB
CMRR (AD822)	V_{CM} = 0 V to +2 V	66	80		69	80		66	80		dB
T_{MIN} to T_{MAX}		66			66						dB
Input Impedance											
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω‖pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω‖pF
OUTPUT CHARACTERISTICS											
Output Saturation Voltage[2]											
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10				mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20				mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80				mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160				mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000				mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900				mV
Operating Output Current		15			15			15			mA
T_{MIN} to T_{MAX}		12			12						mA
Short Circuit Current			25			25			25		mA
Capacitive Load Drive			350			350			350		pF
POWER SUPPLY											
Quiescent Current/Amplifier			620	800		620	800		620		µA
	T_{MIN} to T_{MAX}			800			800				µA
Power Supply Rejection		70	80		66	80		70	80		dB
	T_{MIN} to T_{MAX}	70			66						dB

NOTE: For dual-supply specifications, request complete data sheet.
Specifications subject to change without notice.

Dual, 16 MHz, Rail-to-Rail FET Input Amplifier

AD823

FEATURES

Single Supply Operation
- Output Swings Rail to Rail
- Input Voltage Range Extends Below Ground
- Single Supply Capability from +3 V to +36 V

High Load Drive
- Capacitive Load Drive of 500 pF, G = +1
- Output Current of 15 mA, 0.5 V from Supplies

Excellent AC Performance on 2.6 mA/Amplifier
- –3 dB Bandwidth of 16 MHz, G = +1
- 350 ns Settling Time to 0.01% (2 V Step)
- Slew Rate of 22 V/μs

Good DC Performance
- 800 μV Max Input Offset Voltage
- 2 μV/°C Offset Voltage Drift
- 25 pA Max Input Bias Current

Low Distortion
- –108 dBc Worst Harmonic @ 20 kHz

Low Noise
- 16 nV/$\sqrt{\text{Hz}}$ @ 10 kHz

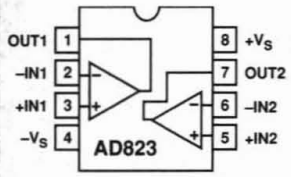
No Phase Inversion with Inputs to the Supply Rails

APPLICATIONS

Battery Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 16-Bit Data Acquisition Systems
Medical Instrumentation

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP
and
8-Lead SOIC



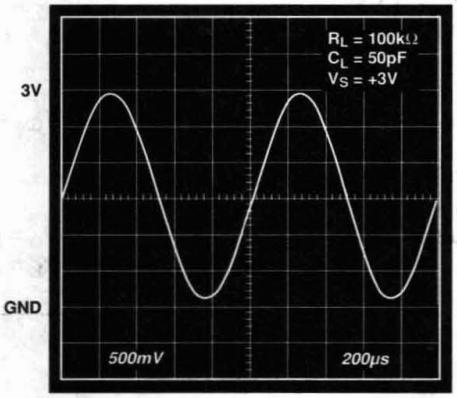


Figure 1. Output Swing, V_S = +3 V, G = +1

PRODUCT DESCRIPTION

The AD823 is a dual precision, 16 MHz, JFET input op amp that can operate from a single supply of +3.0 V to +36 V, or dual supplies of ±1.5 V to ±18 V. It has true single supply capability with an input voltage range extending below ground in single supply mode. Output voltage swing extends to within 50 mV of each rail for $I_{OUT} \leq 100$ μA providing outstanding output dynamic range.

Offset voltage of 800 μV max, offset voltage drift of 2 μV/°C, input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigohm. 16 MHz, –3 dB bandwidth, –108 dB THD @ 20 kHz and 22 V/μs slew rate are provided with a low supply current of 2.6 mA per amplifier. The AD823 drives up to 500 pF of direct capacitive load as a follower, and provides an output current of 15 mA, 0.5 V from the supply rails. This allows the amplifier to handle a wide range of load conditions.

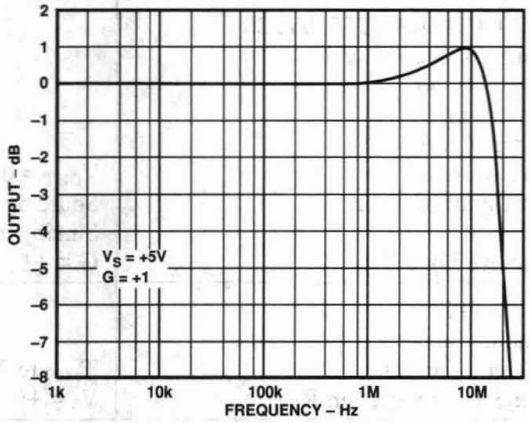


Figure 2. Small Signal Bandwidth, G = +1

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD823AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD823AR	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD823AR-REEL	–40°C to +85°C	SOIC on Reel	SO-8

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD823—SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to +2.5 V, unless otherwise noted)

Parameter	Conditions	AD823A Min	AD823A Typ	AD823A Max	Units
DYNAMIC PERFORMANCE					
–3 dB Bandwidth, $V_O \le 0.2$ V p-p	G = +1	12	16		MHz
Full Power Response	V_O = 2 V p-p		3.5		MHz
Slew Rate	G = –1, V_O = 4 V Step	14	22		V/μs
Settling Time	G = –1, V_O = 2 V Step				
to 0.1%			320		ns
to 0.01%			350		ns
NOISE/DISTORTION PERFORMANCE					
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 1 kHz		1		fA/√Hz
Harmonic Distortion	R_L = 600 Ω to 2.5 V, V_O = 2 V p-p, f = 20 kHz		–108		dBc
Crosstalk					
f = 1 kHz	R_L = 5 kΩ		–130		dB
f = 1 MHz	R_L = 5 kΩ		–93		dB
DC PERFORMANCE					
Initial Offset			0.2	0.8	mV
Max Offset Over Temperature			0.3	2.0	mV
Offset Drift			2		μV/°C
Input Bias Current	V_{CM} = 0 V to +4 V		3	25	pA
at T_{MAX}			0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V				
	R_L = 2 kΩ	20	45		V/mV
T_{MIN} to T_{MAX}		20			V/mV
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		–0.2 to 3	–0.2 to 3.8		V
Input Resistance			10^{13}		Ω
Input Capacitance			1.8		pF
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3 V	60	76		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
I_L = ±100 μA			0.025 to 4.975		V
I_L = ±2 mA			0.08 to 4.92		V
I_L = ±10 mA			0.25 to 4.75		V
Output Current	V_{OUT} = 0.5 V to 4.5 V		16		mA
Short Circuit Current	Sourcing to 2.5 V		40		mA
	Sinking to 2.5 V		30		mA
Capacitive Load Drive	G = +1		500		pF
POWER SUPPLY					
Operating Range		+3		+36	V
Quiescent Current	T_{MIN} to T_{MAX}, Total		5.2	5.6	mA
Power Supply Rejection Ratio	V_S = +5 V to +15 V, T_{MIN} to T_{MAX}	70	80		dB

Specification subject to change without notice.

NOTE: For 3.3 V and ±15 V specifications, request complete data sheets.

Single Supply, Rail-to-Rail Low Power, FET-Input Op Amp

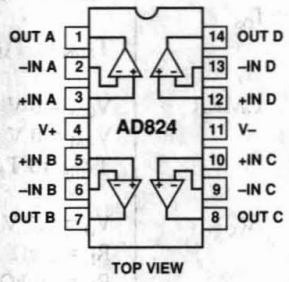
AD824

FEATURES
- Single-Supply Operation: 3 to 30 Volts
- Very Low Input Bias Current: 2 pA
- Wide Input Voltage Range
- Rail-to-Rail Output Swing
- Low Supply Current: 500 μA/Amp
- Wide Bandwidth: 2 MHz
- Slew Rate: 2 V/μs
- No Phase Reversal

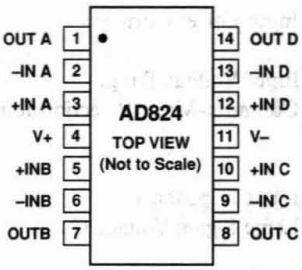
APPLICATIONS
- Photo Diode Preamplifier
- Battery Powered Instrumentation
- Power Supply Control and Protection
- Medical Instrumentation
- Remote Sensors
- Low Voltage Strain Gage Amplifiers
- DAC Output Amplifier

PIN CONFIGURATIONS

14-Lead Epoxy DIP (N Suffix)



14-Lead Epoxy SO (R Suffix)



GENERAL DESCRIPTION

The AD824 is a quad, FET input single-supply amplifier featuring rail-to-rail outputs. The combination of FET inputs and rail-to-rail outputs makes the AD824 useful in a wide variety of low voltage applications where low input current is a primary consideration.

The AD824 is guaranteed to operate from a 3 V single supply up to ±15 volt dual supplies.

Fabricated on ADI's complementary bipolar process, the AD824 has a unique input stage that allows the input voltage to safely extend beyond the negative supply and to the positive supply without any phase inversion or latchup. The output voltage swings to within 15 millivolts of the supplies. Capacitive loads to 350 pF can be handled without oscillation.

The FET input combined with laser trimming provides an input that has extremely low bias currents with guaranteed offsets below 300 μV. This enables high accuracy designs even with high source impedances. Precision is combined with low noise making the AD824 ideal for use in battery powered medical equipment.

Applications for the AD824 include portable medical equipment, photo diode preamplifiers, and high impedance transducer amplifiers.

The ability of the output to swing rail-to-rail enables designers to build multistage filters in single supply systems and maintain high signal-to-noise ratios.

The AD824 is specified over the extended industrial (–40°C to +85°C) temperature range and is available in 14-pin DIPs and narrow 14-pin SO packages.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD824AN	–40°C to +85°C	14-Pin Plastic DIP
AD824BN	–40°C to +85°C	14-Pin Plastic DIP
AD824AR-14	–40°C to +85°C	14-Pin SOIC
AD824AR-14-REEL	–40°C to +85°C	14-Pin SOIC
AD824AR-14-3V	–40°C to +85°C	14-Pin SOIC
AD824AR-14-3V-REEL	–40°C to +85°C	14-Pin SOIC
AD824AR-16	–40°C to +85°C	16-Pin SOIC
AD824AR-16-REEL	–40°C to +85°C	16-Pin SOIC
AD824ACHIPS	+25°C	DICE

*For outline information see Package Information section.

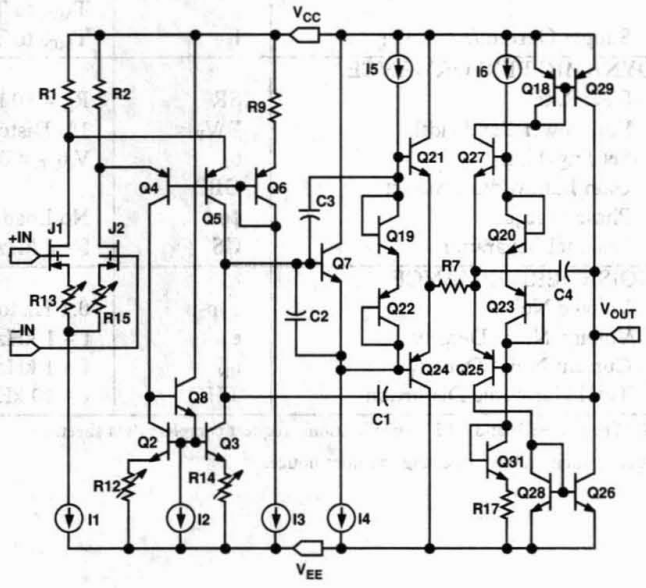


Figure 1. Simplified Schematic of 1/4 AD824

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD824–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 0 V, V_{OUT} = 0.2 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage AD824A	V_{OS}			0.1	1.0	mV
		T_{MIN} to T_{MAX}			1.5	mV
Offset Voltage AD824B	V_{OS}				300	µV
		T_{MIN} to T_{MAX}			900	µV
Input Bias Current	I_B			2	12	pA
		T_{MIN} to T_{MAX}		300	4000	pA
Input Offset Current	I_{OS}			2	10	pA
		T_{MIN} to T_{MAX}		300		pA
Input Voltage Range			–0.2		3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2 V	66	80		dB
		V_{CM} = 0 V to 3 V	60	74		dB
		T_{MIN} to T_{MAX}	60			dB
Input Impedance				$10^{13}\|\|3.3$		Ω||pF
Large Signal Voltage Gain	A_{VO}	V_O = 0.2 V to 4.0 V				
		R_L = 2 kΩ	20	40		V/mV
		R_L = 10 kΩ	50	100		V/mV
		R_L = 100 kΩ	250	1000		V/mV
		T_{MIN} to T_{MAX}, R_L = 100 kΩ	180	400		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_{SOURCE} = 20 µA	4.975	4.988		V
		T_{MIN} to T_{MAX}	4.97	4.985		V
		I_{SOURCE} = 2.5 mA	4.80	4.85		V
		T_{MIN} to T_{MAX}	4.75	4.82		V
Output Voltage Low	V_{OL}	I_{SINK} = 20 µA		15	25	mV
		T_{MIN} to T_{MAX}		20	30	mV
		I_{SINK} = 2.5 mA		120	150	mV
		T_{MIN} to T_{MAX}		140	200	mV
Short Circuit Limit	I_{SC}	Sink/Source		±12		mA
		T_{MIN} to T_{MAX}		±10		mA
Open-Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		100		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	70	80		dB
		T_{MIN} to T_{MAX}	66			dB
Supply Current/Amplifier	I_{SY}	T_{MIN} to T_{MAX}		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		2		V/µs
Full-Power Bandwidth	BW_P	1% Distortion, V_O = 4 V p-p		150		kHz
Settling Time	t_S	V_{OUT} = 0.2 V to 4.5 V, to 0.01%		2.5		µs
Gain Bandwidth Product	GBP			2		MHz
Phase Margin	ϕo	No Load		50		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		–123		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		16		nV/√Hz
Current Noise Density	i_{IN}	f = 1 kHz		0.8		fA/√Hz
Total Harmonic Distortion	THD	f = 10 kHz, R_L = 0, A_V = +1		0.005		%

NOTE: For +3 V and ±15 V specifications, request complete data sheet.

Specifications subject to change without notice.

ANALOG DEVICES

High Speed, Low Power Dual Operational Amplifier

AD826

FEATURES

High Speed:
- 50 MHz Unity Gain Bandwidth
- 350 V/μs Slew Rate
- 70 ns Settling Time to 0.01%

Low Power:
- 7.5 mA Max Power Supply Current Per Amp

Easy to Use:
- Drives Unlimited Capacitive Loads
- 50 mA Min Output Current Per Amplifier
- Specified for +5 V, ±5 V and ±15 V Operation
- 2.0 V p-p Output Swing into a 150 Ω Load (V_S = +5 V)

Good Video Performance
- Differential Gain & Phase Error of 0.07% & 0.11°

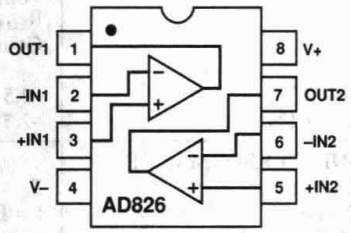
Excellent DC Performance:
- 2.0 mV Max Input Offset Voltage

APPLICATIONS

Unity Gain ADC/DAC Buffer
Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video Line Driver
Active Filters

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP and SO Package



PRODUCT DESCRIPTION

The AD826 is a dual, high speed voltage feedback op amp. It is ideal for use in applications which require unity gain stability and high output drive capability, such as buffering and cable driving. The 50 MHz bandwidth and 350 V/μs slew rate make the AD826 useful in many high speed applications including: video, CATV, copiers, LCDs, image scanners and fax machines.

The AD826 features high output current drive capability of 50 mA min per amp, and is able to drive unlimited capacitive loads. With a low power supply current of 15 mA max for both amplifiers, the AD826 is a true general purpose operational amplifier.

The AD826 is ideal for power sensitive applications such as video cameras and portable instrumentation. The AD826 can operate from a single +5 V supply, while still achieving 25 MHz of bandwidth. Furthermore the AD826 is fully specified from a single +5 V to ±15 V power supplies.

The AD826 excels as an ADC/DAC buffer or active filter in data acquisition systems and achieves a settling time of 70 ns to 0.01%, with a low input offset voltage of 2 mV max. The AD826 is available in small 8-pin plastic mini-DIP and SO packages.

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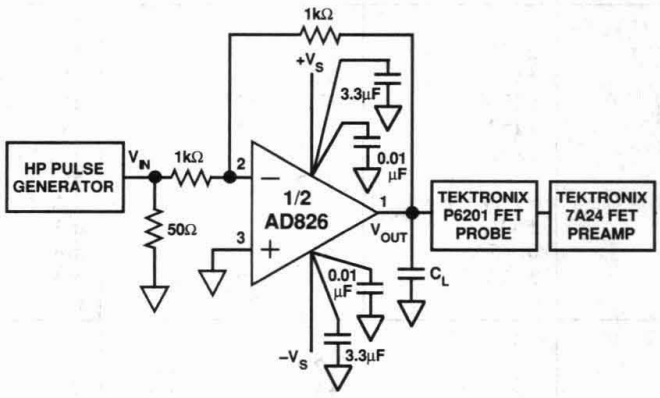
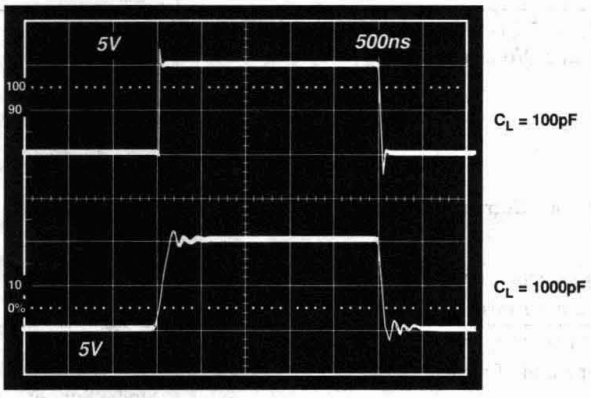
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD826AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD826AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD826AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.





Driving a Large Capacitive Load

AD826–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V	30	35		MHz
		±15 V	45	50		MHz
		0, +5 V	25	29		MHz
Bandwidth for 0.1 dB Flatness	Gain = +1	±5 V	10	20		MHz
		±15 V	25	55		MHz
		0, +5 V	10	20		MHz
Full Power Bandwidth	V_{OUT} = 5 V p-p, R_{LOAD} = 500 Ω	±5 V		15.9		MHz
	V_{OUT} = 20 V p-p, R_{LOAD} = 1 kΩ	±15 V		5.6		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	200	250		V/µs
	Gain = –1	±15 V	300	350		V/µs
		0, +5 V	150	200		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V, ±15 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V, ±15 V		70		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		–78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		15		nV/√Hz
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
Differential Gain Error	NTSC	±15 V		0.07	0.1	%
(R1 = 150 Ω)	Gain = +2	±5 V		0.12	0.15	%
		0, +5 V		0.15		%
Differential Phase Error	NTSC	±15 V		0.11	0.15	Degrees
(R1 = 150 Ω)	Gain = +2	±5 V		0.12	0.15	Degrees
		0, +5 V		0.15		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V to ±15 V		0.5	2	mV
Offset Drift				10		µV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	µA
Input Offset Current		±5 V, ±15 V		25	200	nA
Offset Current Drift				0.3		nA/°C
Open-Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	4		V/mV
	R_{LOAD} = 150 Ω		1.5	3		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		3.5	6		V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		2	4		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
			–2.7	–3.4		V
		±15 V	+13	+14.3		V
			–12	–13.4		V
		0, +5 V	+3.8	+4.3		V
			+1.2	+0.9		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}	±5 V	80	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			V
Output Current		±15 V	50			mA
		±5 V	50			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current/Amplifier		±5 V		6.6	7.5	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN} to T_{MAX}		75	86		dB

Specifications subject to change without notice.

ANALOG DEVICES

Dual, Low Power Video Op Amp

AD828

FEATURES

Excellent Video Performance
- Differential Gain & Phase Error of 0.01% & 0.05°

High Speed
- 130 MHz 3 dB Bandwidth (G = +2)
- 450 V/μs Slew Rate
- 80 ns Settling Time to 0.01%

Low Power
- 15 mA Max Power Supply Current

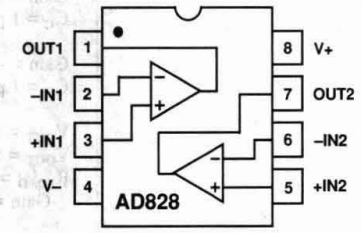
High Output Drive Capability:
- 50 mA Minimum Output Current per Amplifier
- Ideal for Driving Back Terminated Cables

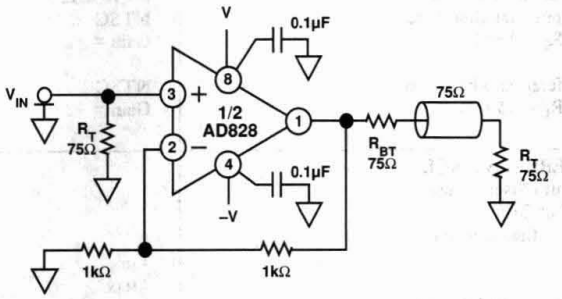
Flexible Power Supply
- Specified for +5 V, ±5 V and ±15 V Operation
- ±3.2 V min Output Swing into a 150 Ω Load (V_S = ±5 V)

Excellent DC Performance
- 2.0 mV Input Offset Voltage

Available in 8-Pin SOIC and 8-Pin Plastic Mini-DIP

FUNCTIONAL BLOCK DIAGRAM





AD828 Video Line Driver

PRODUCT DESCRIPTION

The AD828 is a low cost, dual video op amp optimized for use in video applications which require gains of +2 or greater and high output drive capability, such as cable driving. Due to its low power and single supply functionality, along with excellent differential gain and phase errors, the AD828 is ideal for power sensitive applications such as video cameras and professional video equipment.

With video specs like 0.1 dB flatness to 40 MHz and low differential gain and phase errors of 0.01% and 0.05°, along with 50 mA of output current per amplifier, the AD828 is an excellent choice for any video application. The 130 MHz gain bandwidth and 450 V/μs slew rate make the AD828 useful in many high speed applications including: video monitors, CATV, color copiers, image scanners and fax machines.

The AD828 is fully specified for operation with a single +5 V power supply and with dual supplies from ±5 V to ±15 V. This power supply flexibility, coupled with a very low supply current of 15 mA and excellent ac characteristics under all power supply conditions, make the AD828 the ideal choice for many demanding yet power sensitive applications.

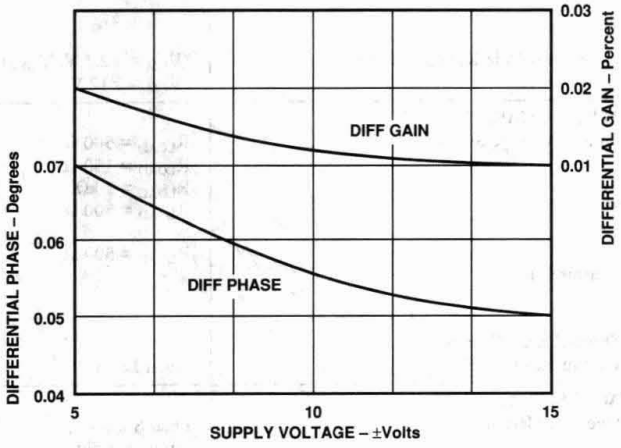
The AD828 is a voltage feedback op amp which excels as a gain stage (gains >+2) or active filter in high speed and video systems and achieves a settling time of 45 ns to 0.1%, with a low input offset voltage of 2 mV max.

The AD828 is available in low cost, small 8-pin plastic mini-DIP and SOIC packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD828AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD828AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD828AR-REEL	–40°C to +85°C	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.



AD828—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD828 Min	AD828 Typ	AD828 Max	Units
DYNAMIC PERFORMANCE						
–3 dB Bandwidth	Gain = +2	±5 V	60	85		MHz
		±15 V	100	130		MHz
		0, +5 V	30	45		MHz
	Gain = –1	±5 V	35	55		MHz
		±15 V	60	90		MHz
		0, +5 V	20	35		MHz
Bandwidth for 0.1 dB Flatness	Gain = +2 C_C = 1 pF	±5 V, ±15 V	30	43		MHz
		0, +5 V	10	18		MHz
	Gain = –1	±5 V	15	25		MHz
	C_C = 1 pF	±15 V	30	50		MHz
		0, +5 V	10	19		MHz
Full Power Bandwidth	V_{OUT} = 5 V p-p, R_{LOAD} = 500 Ω	±5 V		22.3		MHz
	V_{OUT} = 20 V p-p, R_{LOAD} = 1 kΩ	±15 V		7.2		MHz
Slew Rate	R_{LOAD} = 1 kΩ	±5 V	300	350		V/µs
	Gain = –1	±15 V	400	450		V/µs
		0, +5 V	200	250		V/µs
Settling Time to 0.1%	–2.5 V to +2.5 V	±5 V		45		ns
to 0.01%	–2.5 V to +2.5 V	±5 V		80		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	F_C = 1 MHz	±15 V		–78		dB
Input Voltage Noise	f = 10 kHz	±5 V, ±15 V		10		nV/√Hz
Input Current Noise	f = 10 kHz	±5 V, ±15 V		1.5		pA/√Hz
Differential Gain Error	NTSC	±15 V		0.01	0.02	%
(R_L = 150 Ω)	Gain = +2	±5 V		0.02	0.03	%
		0, +5 V		0.08		%
Differential Phase Error	NTSC	±15 V		0.05	0.09	Degrees
(R_L = 150 Ω)	Gain = +2	±5 V		0.07	0.1	Degrees
		0, +5 V		0.1		Degrees
DC PERFORMANCE						
Input Offset Voltage		±5 V, ±15 V		0.5	2	mV
Offset Drift				10		µV/°C
Input Bias Current		±5 V, ±15 V		3.3	6.6	µA
	T_{MIN}				10	µA
	T_{MAX}				4.4	µA
Input Offset Current		±5 V, ±15 V		25	200	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
Open Loop Gain	V_{OUT} = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		3	5		V/mV
	T_{MIN} to T_{MAX}		2			V/mV
	R_{LOAD} = 150 Ω		2	4		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		5.5	9		V/mV
	T_{MIN} to T_{MAX}		2.5			V/mV
	V_{OUT} = ±7.5 V	±15 V				
	R_{LOAD} = 150 Ω (50 mA Output)		3	5		V/mV
INPUT CHARACTERISTICS						
Input Resistance				300		kΩ
Input Capacitance				1.5		pF
Input Common-Mode Voltage Range		±5 V	+3.8	+4.3		V
		±15 V	+13	+14.3		V
		0, +5 V	+3.8	+4.3		V
Common-Mode Rejection Ratio	V_{CM} = +2.5 V, T_{MIN} to T_{MAX}	±5 V	82	100		dB
	V_{CM} = ±12 V	±15 V	86	120		dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.3	3.8		±V
	R_{LOAD} = 150 Ω	±5 V	3.2	3.6		±V
	R_{LOAD} = 1 kΩ	±15 V	13.3	13.7		±V
	R_{LOAD} = 500 Ω	±15 V	12.8	13.4		±V
	R_{LOAD} = 500 Ω	0, +5 V	+1.5, +3.5			±V
Output Current		±15 V	50			mA
		±5 V	40			mA
		0, +5 V	30			mA
Short-Circuit Current		±15 V		90		mA
Output Resistance	Open Loop			8		Ω
POWER SUPPLY						
Operating Range	Dual Supply		±2.5		±18	V
	Single Supply		+5		+36	V
Quiescent Current		±5 V		14.0	15	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V, T_{MIN} to T_{MAX}		80	90		dB

Specifications subject to change without notice.

ANALOG DEVICES

High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = –1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 1.7 nV/√Hz Input Voltage Noise
- 1.5 pA/√Hz Input Current Noise

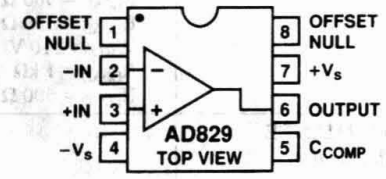
Excellent DC Precision
- 1 mV max Input Offset Voltage (Over Temp)
- 0.3 μV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

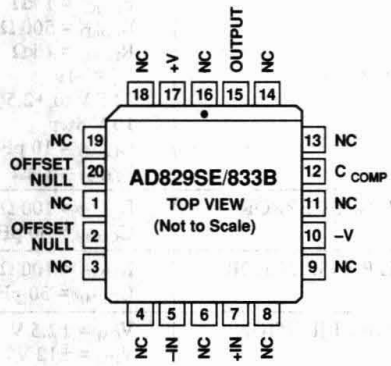
Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



20-Pin LCC Pinout



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD829 is a low noise (1.7 nV/√Hz), high speed op amp with custom compensation that provides the user with gains from ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth product while requiring only 5 mA of current from the power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the –3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. In addition, the AD829's output can also be clamped at its external compensation pin.

The AD829 has excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 1.7 nV/√Hz, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/√Hz, current noise of 1.5 pA/√Hz and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make it an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. Available in plastic, cerdip, and small outline packages. Chips and MIL-STD-883B parts are also available.

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AD829—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.1	0.5	mV
	T_{MIN} to T_{MAX}				1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7	µA
	T_{MIN} to T_{MAX}				8.2			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		30	65		30	65		V/mV
	R_{LOAD} = 150 Ω			40			40		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		50	100		50	100		V/mV
	R_{LOAD} = 500 Ω			85			85		V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth Product		±5 V		600			600		MHz
		±15 V		750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p								
	R_{LOAD} = 500 Ω	±5 V		25			25		MHz
	V_O = 20 V p-p								
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230		V/µs
Settling Time to 0.1%	A_V = –19								
	–2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step	±15 V		90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		dB
	T_{MIN} to T_{MAX}		94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				–3.8			–3.8		V
		±15 V		+14.3			+14.3		V
				–13.8			–13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 50 Ω	±5 V		1.4			1.4		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short Circuit Current		±5 V, ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance (Differential)				13			13		kΩ
Input Capacitance (Differential)[4]				5			5		pF
Input Capacitance (Common Mode)				1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2		mΩ
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		5	6.5		5	6.5	mA

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL & SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.

Specifications subject to change without notice.

ANALOG DEVICES

High Speed, Video Difference Amplifier

AD830

FEATURES

Differential Amplification
- Wide Common-Mode Voltage Range: +12.8 V, –12 V
- Differential Voltage Range: ±2 V
- High CMRR: 60 dB @ 4 MHz
- Built-in Differential Clipping Level: ±2.3 V

Fast Dynamic Performance
- 85 MHz Unity Gain Bandwidth
- 35 ns Settling Time to 0.1%
- 360 V/μs Slew Rate

Symmetrical Dynamic Response

Excellent Video Specifications
- Differential Gain Error: 0.06%
- Differential Phase Error: 0.08°
- 15 MHz (0.1 dB) Bandwidth

Flexible Operation
- High Output Drive of ±50 mA min
- Specified with Both ±5 V and ±15 V Supplies

Low Distortion: THD = –72 dB @ 4 MHz

Excellent DC Performance: 3 mV max Input Offset Voltage

APPLICATIONS

Differential Line Receiver

High Speed Level Shifter

High Speed In-Amp

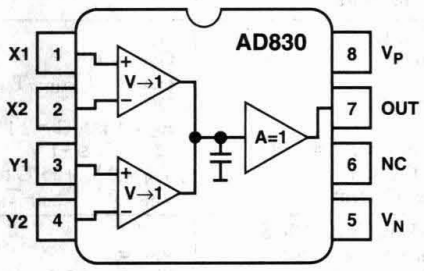
Differential to Single Ended Conversion

Resistorless Summation and Subtraction

High Speed A/D Driver

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



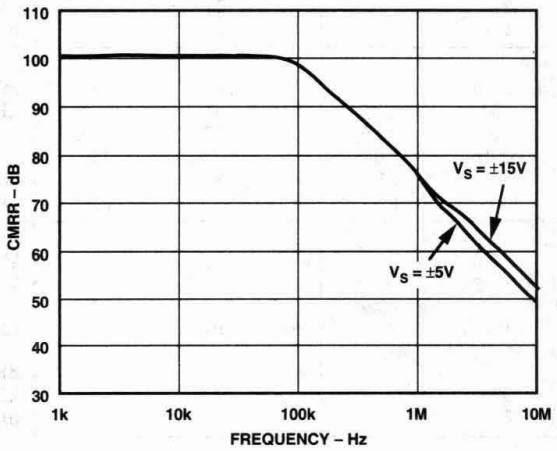
NC = NO CONNECT

PRODUCT DESCRIPTION

The AD830 is a wideband, differencing amplifier designed for use at video frequencies but also useful in many other applications. It accurately amplifies a fully differential signal at the input and produces an output voltage referred to a user-chosen level. The undesired common-mode signal is rejected, even at high frequencies. High impedance inputs ease interfacing to finite source impedances and thus preserve the excellent common-mode rejection. In many respects, it offers significant improvements over discrete difference amplifier approaches, in particular in high frequency common-mode rejection.

The wide common-mode and differential-voltage range of the AD830 make it particularly useful and flexible in level shifting applications, but at lower power dissipation than discrete solutions. Low distortion is preserved over the many possible differential and common-mode voltages at the input and output.

Good gain flatness and excellent differential gain of 0.06% and phase of 0.08° make the AD830 suitable for many video system applications. Furthermore, the AD830 is suited for general purpose signal processing from dc to 10 MHz.



Common-Mode Rejection Ratio vs. Frequency

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD830AN	–40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD830JR	0°C to +70°C	8-Pin SOIC	R-8
5962-9313001MPA[2]	–55°C to +125°C	8-Pin Cerdip	Q-8

NOTES
[1] For outline information see Package Information section.
[2]See Standard Military Drawing for specifications.

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AD830—SPECIFICATIONS (V_S = ±15 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted)

Parameter	Conditions	AD830J/A Min	AD830J/A Typ	AD830J/A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Units
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = 1, V_{OUT} = 100 mV rms	75	85		75	85		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, V_{OUT} = 100 mV rms	11	15		11	15		MHz
Differential Gain Error	0 to +0.7 V, Frequency = 4.5 MHz		0.06	0.09		0.06	0.09	%
Differential Phase Error	0 to +0.7 V, Frequency = 4.5 MHz		0.08	0.12		0.08	0.12	Degrees
Slew Rate	2 V Step, R_L = 500 Ω		360			360		V/µs
3 dB Large Signal Bandwidth	Gain = 1, V_{OUT} = 1 V rms	38	45		38	45		MHz
Settling Time, Gain = 1	V_{OUT} = 2 V Step, to 0.1%		25			25		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		–82			–82		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = 1		±1.5	±3		±1.5	±3	mV
	Gain = 1, T_{MIN}–T_{MAX}			±5			±7	mV
Open Loop Gain	DC	64	69		64	69		dB
Gain Error	R_L = 1 kΩ, G = ±1		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L= 1 kΩ,	–1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
Input Bias Current	V_{IN} = 0 V, +25°C to T_{MAX}		5	10		5	10	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN}–T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level	Pins 1 and 2 Inputs Only	±2.1	±2.3		±2.1	±2.3		V
Common-Mode Voltage Range	V_{DM} = ±1 V	–12.0		+12.8	–12.0		+12.8	V
CMRR	DC, Pins 1, 2, ±10 V	90	100		90	100		dB
	DC, Pins 1, 2, ±10 V, T_{MIN}–T_{MAX}	88			86			dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 1 kΩ	±12	+13.8, –13.8		±12	+13.8, –13.8		V
	R_L ≥ 1 kΩ, ±16.5 V_S	±13	+15.3, –14.7		±13	+15.3, –14.7		V
Output Current	R_L = 150 Ω	±50			±50			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN}–T_{MAX}		14.5	17		14.5	17	mA
(V_S = ±5 V, R_{LOAD} = 150 Ω, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted)								
DYNAMIC CHARACTERISTICS								
3 dB Small Signal Bandwidth	Gain = 1, V_{OUT} = 100 mV rms	35	40		35	40		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, V_{OUT} = 100 mV rms	5	6.5		5	6.5		MHz
Differential Gain Error	0 to +0.7 V, Frequency = 4.5 MHz, G = +2		0.14	0.18		0.14	0.18	%
Differential Phase Error	0 to +0.7 V, Frequency = 4.5 MHz, G = +2		0.32	0.4		0.32	0.4	Degrees
Slew Rate, Gain = 1	2 V Step, R_L = 500 Ω		210			210		V/µs
3 dB Large Signal Bandwidth	Gain = 1, V_{OUT} = 1 V rms	30	36		30	36		MHz
Settling Time	V_{OUT} = 2 V Step, to 0.1%		35			35		ns
Harmonic Distortion	2 V p-p, Frequency = 1 MHz		–69			–69		dBc
Input Voltage Noise	Frequency = 10 kHz		27			27		nV/√Hz
Input Current Noise			1.4			1.4		pA/√Hz
DC PERFORMANCE								
Offset Voltage	Gain = 1		±1.5	±3		±1.5	±3	mV
Open Loop Gain	DC	60	65		60	65		dB
Unity Gain Accuracy	R_L = 1 kΩ		±0.1	±0.6		±0.1	±0.6	%
Peak Nonlinearity, R_L= 1 kΩ	–1 V ≤ X ≤ +1 V		0.01	0.03		0.01	0.03	% FS
Input Bias Current	V_{IN} = 0 V, +25°C to T_{MAX}		5	10		5	10	µA
Input Offset Current	V_{IN} = 0 V, T_{MIN}–T_{MAX}		0.1	1		0.1	1	µA
INPUT CHARACTERISTICS								
Differential Voltage Range	V_{CM} = 0		±2.0			±2.0		V
Differential Clipping Level	Pins 1 and 2 Inputs Only	±2.0	±2.2		±2.0	±2.2		V
Common-Mode Voltage Range	V_{DM} = ±1 V	–2.0		+2.9	–2.0		+2.9	V
CMRR	DC, Pins 1, 2, +4 V to –2 V	90	100		90	100		dB
	DC, Pins 1, 2, +4 V to –2 V, T_{MIN}–T_{MAX}	88			86			dB
Input Resistance			370			370		kΩ
Input Capacitance			2			2		pF
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L ≥ 150 Ω	±3.2	±3.5		±3.2	±3.5		V
	R_L ≥ 150 Ω, ±4 V_S	±2.2	+2.7, –2.4		±2.2	+2.7, –2.4		V
Output Current		±40			±40			mA
POWER SUPPLIES								
Operating Range		±4		±16.5	±4		±16.5	V
Quiescent Current	T_{MIN}–T_{MAX}		13.5	16		13.5	16	mA

Specifications subject to change without notice.

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

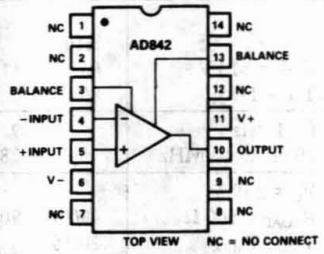
AC PERFORMANCE
- Gain Bandwidth Product: 80 MHz (Gain = 2)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 375 V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 6.0 MHz for 20 V p-p

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Offset Drift: 14 μV/°C
- Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 90 V/mV into a 500 Ω Load
- Output Current: 100 mA min
- Quiescent Supply Current: 14 mA max

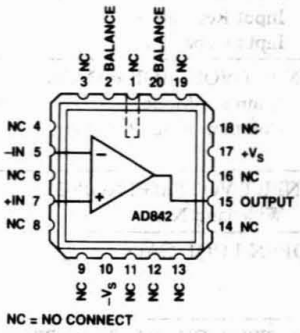
APPLICATIONS
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP, Hermetic Metal Can, Hermetic Cerdip, SOIC and LCC Packages and in Chip Form
- MIL-STD-883B Parts Available
- Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAMS

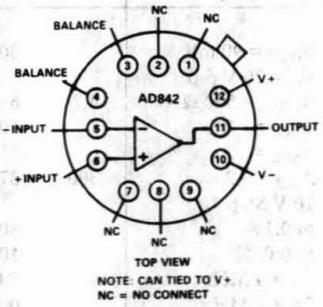
Plastic DIP (N) Package and Cerdip (Q) Package



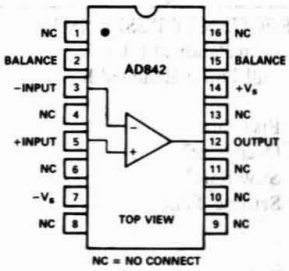
LCC (E) Package



TO-8 (H) Package



SOIC (R-16) Package



PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/μs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD842–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J/JR[1] Min	AD842J/JR[1] Typ	AD842J/JR[1] Max	AD842K Min	AD842K Typ	AD842K Max	AD842S[2] Min	AD842S[2] Typ	AD842S[2] Max	Units
INPUT OFFSET VOLTAGE[3]			0.5	**1.5**		0.3	**1.0**		0.5	**1.5**	mV
	T_{MIN}–T_{MAX}			2.5/3			**1.5**			3.5	mV
Offset Drift			14			14			14		µV/°C
INPUT BIAS CURRENT			4.2	**8**		3.5	**5**		4.2	**8**	µA
	T_{MIN}–T_{MAX}			10			**6**			**12**	µA
Input Offset Current			0.1	**0.4**		0.05	**0.2**		0.1	**0.4**	µA
	T_{MIN}–T_{MAX}			0.5			**0.3**			**0.6**	µA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**			**±10**			**±10**			V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	115		**90**	115		**86**	115		dB
	T_{MIN}–T_{MAX}	80			**86**			**80**			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 500 Ω	**40/30**	90		**50**	90		**40**	90		V/mV
	T_{MIN}–T_{MAX}	20/15			**25**			**20**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω	**±10**			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**100**			**100**			**100**			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[4]	V_O = 20 V p-p										
	R_{LOAD} ≥ 500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[5]	A_{VCL} = –2		10			10			10		ns
Overshoot[5]	A_{VCL} = –2		20			20			20		%
Slew Rate[5]	A_{VCL} = –2	300	375		300	375		300	375		V/µs
Settling Time[5]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			13/14	**14/16**		13	**14**		13	**14**	mA
	T_{MIN}–T_{MAX}			16/19.5			**16**			**19**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**86**	100		**90**	105		**86**	100		dB
	T_{MIN}–T_{MAX}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[6]		0		+75	0		+75	–55		+125	°C
PACKAGE OPTIONS[7]											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ, AD842SQ/883B		
SOIC (R-16)			AD842JR-16								
Tape and Reel			AD842JR-16-REEL								
			AD842JR-16-REEL7								
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		
LCC (E-20A)									AD842SE/883B		
Chips			AD842JCHIPS						AD842SCHIPS		

NOTES

[1]AD842JR specifications differ from those of the AD842JN, JQ and JH due to the thermal characteristics of the SOIC package.

[2]Standard Military Drawing available 5962-8964201xx
2A – (SE/883B); XA – (SH/883B); CA – (SQ/883B).

[3]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[4]Full power bandwidth = slew rate/2 π V_{PEAK}.

[5]Refer to Figures 22 and 23.

[6]"S" grade T_{MIN}–T_{MAX} specifications are tested with automatic test equipment at T_A = –55°C and T_A = +125°C.

[7]For outline information see Package Information section.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

34 MHz, CBFET Fast Settling Op Amp

AD843

FEATURES

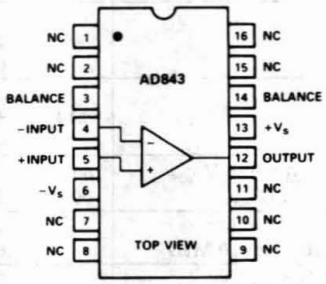
AC PERFORMANCE
- Unity Gain Bandwidth: 34 MHz
- Fast Settling: 135 ns to 0.01%
- Slew Rate: 250 V/μs
- Stable at Gains of 1 or Greater
- Full Power Bandwidth: 3.9 MHz

DC PERFORMANCE
- Input Offset Voltage: 1 mV max (AD843K/B)
- Input Bias Current: 0.6 nA typ
- Input Voltage Noise: 19 nV/√Hz
- Open Loop Gain: 30 V/mV into a 500 Ω Load
- Output Current: 50 mA min
- Supply Current: 13 mA max
- Available in 8-Pin Plastic Mini-DIP & Cerdip, 16-Pin SOIC, 20-Pin LCC and 12-Pin Hermetic Metal Can Packages
- Available in Tape and Reel in Accordance with EIA-481A Standard
- Chips and MIL-STD-883B Parts Also Available

APPLICATIONS
- High Speed Sample-and-Hold Amplifiers
- High Bandwidth Active Filters
- High Speed Integrators
- High Frequency Signal Conditioning

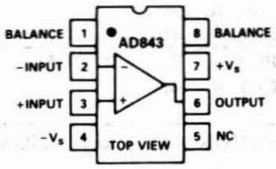
CONNECTION DIAGRAMS

16-Pin SOIC (R-16) Package



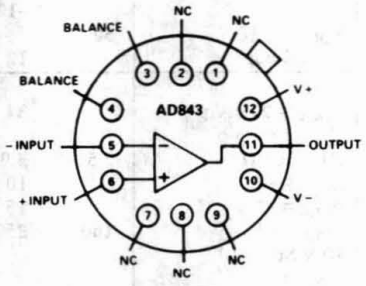
NC = NO CONNECT

Plastic (N-8) and Cerdip (Q-8) Package



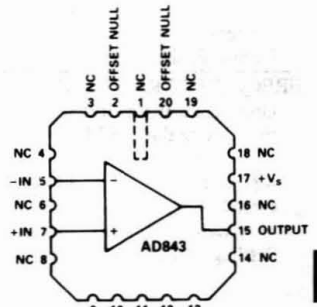
NC = NO CONNECT

TO-8 (H-12A) Package



NOTE CAN TIED TO V+
NC = NO CONNECT

LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD843 is a fast settling, 34 MHz, CBFET input op amp. The AD843 combines the low (0.6 nA) input bias currents characteristic of a FET input amplifier while still providing a 34 MHz bandwidth and a 135 ns settling time (to within 0.01% of final value for a 10 volt step). The AD843 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp.

The 250 V/μs slew rate and 0.6 nA input bias current of the AD843 ensure excellent performance in high speed sample-and-hold applications and in high speed integrators. This amplifier is also ideally suited for high bandwidth active filters and high frequency signal conditioning circuits.

Unlike many high frequency amplifiers, the AD843 requires no external compensation and it remains stable over its full operating temperature range. It is available in five performance grades: the AD843J and AD843K are rated over the commercial temperature range of 0°C to +70°C. The AD843A and AD843B are rated over the industrial temperature range of –40°C to +85°C. The AD843S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD843 is offered in either 8-pin plastic DIP or hermetic cerdip packages, in 16-pin SOIC, 20-Pin LCC, or in a 12-pin metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time and low input bias current of the AD843 make it the ideal amplifier for 12-bit D/A and A/D buffers, for high speed sample-and-hold amplifiers and for high speed integrator circuits. The AD843 can replace many FET input hybrid amplifiers such as the LH0032, LH4104 and OPA600.
2. Fully differential inputs provide outstanding performance in all standard high frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 1 mV max (AD843K and AD843B).
4. Although external offset nulling is unnecessary in many applications, offset null pins are provided.
5. The AD843 does not require external compensation at closed loop gains of 1 or greater.

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AD843—SPECIFICATIONS (@ T_A = +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD843J/A Min	AD843J/A Typ	AD843J/A Max	AD843K/B Min	AD843K/B Typ	AD843K/B Max	AD843S[1] Min	AD843S[1] Typ	AD843S[1] Max	Units
INPUT OFFSET VOLTAGE[1]			1.0	**2.0**		0.5	**1.0**		1.0	**2.0**	mV
	T_{MIN}-T_{MAX}		1.7	4.0		1.2	**2.0**		3.0	**4.5**	mV
Offset Drift			12			12	35		12		µV/°C
INPUT BIAS CURRENT	Initial (T_J = +25°C)		50			40			50		pA
	Warmed-Up[2]		0.8	**2.5**		0.6	**1.0**		0.8	**2.5**	nA
	T_{MIN}-T_{MAX}			60/160			23/65			2600	nA
INPUT OFFSET CURRENT	Initial (T_J = +25°C)		30			20			30		pA
	Warmed-Up[2]		0.25	**1.0**		0.2	**0.4**		0.25	**1.0**	nA
	T_{MIN}-T_{MAX}			23/64			9/26			1025	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{10}			10^{10}			10^{10}		Ω
Input Capacitance			6			6			6		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	+12, −13		**±10**	+12, −13		**±10**	+12, −13		V
COMMON-MODE REJECTION	V_{CM} = ±10 V	**60**	72		**70**	76		**60**	72		dB
	T_{MIN}-T_{MAX}	60	72		**68**	76		**60**	72		dB
INPUT VOLTAGE NOISE	f = 10 kHz		19			19			19		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		60			60			60		µV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 500 Ω	**15**	25		**20**	30		**15**	30		V/mV
	T_{MIN}-T_{MAX}	10	20		**10**	25		**10**	25		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω	**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		12			12			12		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p-p		34			34			34		MHz
Full Power Bandwidth[3]	V_O = 20 V p-p										
	R1 ≥ 500 Ω	2.5	3.9		2.5	3.9		2.5	3.9		MHz
Rise Time	A_{VCL} = −1		10			10			10		ns
Overshoot	A_{VCL} = −1		15			15			15		%
Slew Rate	A_{VCL} = −1	160	250		160	250		160	250		V/µs
Settling Time	10 V Step										
	A_{VCL} = −1										
	to 0.1%		95			95			95		ns
	to 0.01%		135			135			135		ns
Overdrive Recovery	–Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
Differential Gain	f = 4.4 MHz		0.025			0.025			0.025		%
Differential Phase	f = 4.4 MHz		0.025			0.025			0.025		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			12	**13**		12	**13**		12	**13**	mA
	T_{MIN}-T_{MAX}		12.3	14		12.3	**14**		12.5	**16**	mA
Rejection Ratio	±5 V to ±18 V	**65**	76		**70**	80		**65**	76		dB
Rejection Ratio	T_{MIN}-T_{MAX}	62	76		**68**	80		**62**	76		dB
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0°C to +70°C)			AD843J			AD843K					
Industrial (–40°C to +85°C)			AD843A			AD843B					
Military (–55°C to +125°C)[4]									AD843S		
PACKAGE OPTIONS[5]											
Plastic (N-8)			AD843JN			AD843KN					
Cerdip (Q-8)			AD843AQ			AD843BQ			AD843SQ, AD843SQ/883B		
Metal Can (H-12A)						AD843BH			AD843SH, AD843SH/883B		
LCC (E-20A)									AD843SE/883B		
SOIC (R-16)			AD843JR-16								
Tape & Reel			AD843JR-16-REEL								
			AD843JR-16-REEL7								
Chips			AD843JCHIPS						AD843SCHIPS		

NOTES

[1]Standard Military Drawings Available: 5962-9098001M2A (SE/883B), 5962-9098001MXA (SH/883B), 5962-9098001MPA (SQ/883B).

[2]Specifications are guaranteed after 5 minutes at T_A = +25°C.

[3]Full power bandwidth = Slew Rate/2 πV peak.

[4]All "S" grade T_{MIN}-T_{MAX} specifications are tested with automatic test equipment at T_A = –55°C and T_A = +125°C

[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested on all production units.

Precision, 16 MHz CBFET Op Amp

AD845

FEATURES

Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:

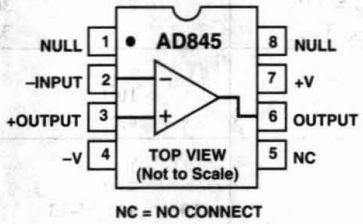
Settles to 0.01% in 350 ns
100 V/μs Slew Rate
12.8 MHz min Unity-Gain Bandwidth
1.75 MHz Full-Power Bandwidth at 20 V p-p

DC PERFORMANCE:

0.25 mV max Input Offset Voltage
5 μV/°C max Offset Voltage Drift
0.5 nA Input Bias Current
250 V/mV min Open-Loop Gain
4 μV p-p max Voltage Noise, 0.1 Hz to 10 Hz
94 dB min CMRR
Available in Plastic Mini-DIP, Hermetic Cerdip and SOIC Packages. Also Available in Tape and Reel in Accordance with EIA-481A Standard

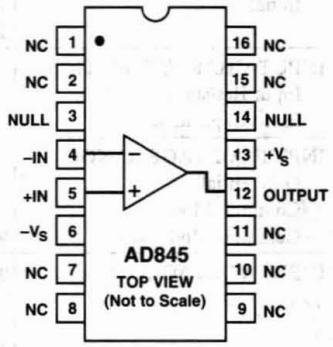
CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



NC = NO CONNECT

16-Pin SOIC (R-16) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/μs, a stable unity-gain bandwidth of 16 MHz, and a settling time of 350 ns 0.01%—while driving a parallel load of 100 pF and 500 Ω—represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

The AD845 is ideal for use in applications such as active filters, high speed integrators, photo diode preamps, sample-and-hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250 μV max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a ±10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity-gain buffer circuits.

The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0°C to +70°C temperature range. AD845A and AD845B devices are specified for operation over the –40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of –55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP and 16-pin SOIC; "J" and "S" grade chips are also available.

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD845JN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD845KN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD845JR-16	0°C to +70°C	16-Pin SOIC	R-16
AD845AQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD845BQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD845SQ	–55°C to +125°C	8-Pin Cerdip	Q-8
AD845SQ/883B	–55°C to +125°C	8-Pin Cerdip	Q-8
5962-8964501PA	–55°C to +125°C	8-Pin Cerdip	Q-8
AD845JCHIPS	0°C to +70°C	Die	
AD845SCHIPS	–55°C to +125°C	Die	
AD845JR-16-REEL	0°C to +70°C	Tape & Reel	
AD845JR-16-REEL7	0°C to +70°C	Tape & Reel	

*N = Plastic DIP: Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

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AD845—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD845J/A Min	AD845J/A Typ	AD845J/A Max	AD845K/B Min	AD845K/B Typ	AD845K/B Max	AD845S Min	AD845S Typ	AD845S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.7	**1.5**		0.1	**0.25**		0.25	**1.0**	mV
	T_{MIN}–T_{MAX}			2.5			**0.4**			2.0	mV
Offset Drift				20		1.5	**5.0**			**10**	µV/°C
INPUT BIAS CURRENT[2]											
Initial	V_{CM} = 0 V		0.75	**2**		0.5	**1**		0.75	**2**	nA
	T_{MIN}–T_{MAX}			45/75			**18/38**			**500**	nA
INPUT OFFSET CURRENT											
Initial	V_{CM} = 0 V		25	**300**		15	**100**		25	**300**	pA
	T_{MIN}–T_{MAX}			3/6.5			**1.2/2.6**			**20**	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{11}			10^{11}			10^{11}		kΩ
Input Capacitance			4.0			4.0			4.0		pF
INPUT VOLTAGE RANGE											
Differential			±20			±20			±20		V
Common Mode		**±10**	+10.5/–13		**±10**	+10.5/–13		**±10**	+10.5/–13		V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	110		**94**	113		**86**	110		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		4			4			4		µV p-p
	f = 10 Hz		80			80			80		nV/√Hz
	f = 100 Hz		60			60			60		nV/√Hz
	f = 1 kHz		25			25			25		nV/√Hz
	f = 10 kHz		18			18			18		nV/√Hz
	f = 100 kHz		12			12			12		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.1			0.1			0.1		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	**200**	500		**250**	500		**200**	500		V/mV
	R_{LOAD} ≥ 500 Ω	**100**	250		**125**	250		**100**	250		V/mV
	T_{MIN}–T_{MAX}	70			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 500 Ω	**±12.5**			**±12.5**			**±12.5**			V
Current	Short Circuit		50			50			50		mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Small Signal	Unity Gain	12.8	16		13.6	16		13.6	16		MHz
Full Power Bandwidth[3]	V_O = ±10 V										
	R_{LOAD} = 500 Ω		1.75			1.75			1.75		MHz
Rise Time			20			20			20		ns
Overshoot			20			20			20		%
Slew Rate		**80**	100		**94**	100		**94**	100		V/µs
Settling Time	10 V Step										
	C_{LOAD} = 100 pF										
	R_{LOAD} = 500 Ω										
	to 0.01%		350			350	500		350	500	ns
	to 0.1%		250			250			250		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.04			0.04			0.04		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.02			0.02			0.02		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.75**		**±18**	**±4.75**		**±18**	**±4.75**		**±18**	V
Rejection Ratio	V_S = ±5 to ±15 V	**88**	110		**95**	113		**88**	110		dB
Quiescent Current	T_{MIN} to T_{MAX}		10	12		10	**12**		10	**12**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.

[3]FPBW = slew rate/2 π V peak.

[4]"S" grade T_{MIN}–T_{MAX} are tested with automatic test equipment at T_A = –55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

450 V/μs, Precision, Current-Feedback Op Amp

AD846

FEATURES

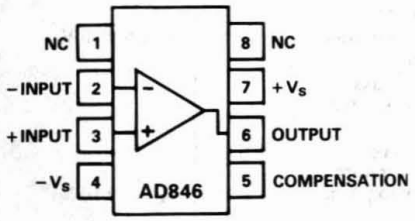
AC PERFORMANCE
- Small Signal Bandwidth: 80 MHz (A_V = –1)
- Slew Rate: 450 V/μs
- Full Power Bandwidth: 6.8 MHz at 20 V p-p, R_L = 500 Ω
- Fast Settling: for 10 V Step: 110 ns to 0.01%, 80 ns to 0.1%
- Differential Gain: <0.01% @ 4.4 MHz
- Differential Phase: <0.028° @ 4.4 MHz
- Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
- Open-Loop Transimpedance: 200 MΩ
- Input Voltage Noise: 2 nV/√Hz

DC PERFORMANCE
- Input Offset Voltage: 75 μV max (B Grade)
- Input Offset Drift: 3.5 μV/°C max (B Grade)
- Quiescent Supply Current: 6.5 mA max

APPLICATIONS
- High Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



NC = NO CONNECT
TOP VIEW

PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from –1 to gains greater than –100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of –1 to –10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of –1 to –100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

10

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD846AN	–40°C to +85°C	N-8
AD846BN	–40°C to +85°C	N-8
AD846AQ	–40°C to +85°C	Q-8
AD846BQ	–40°C to +85°C	Q-8
AD846SQ	–55°C to +125°C	Q-8
AD846SQ/883B	–55°C to +125°C	Q-8
5962-8964601PA	–55°C to +125°C	Q-8

NOTES
[1]"A" and "S" grade chips are also available.
[2]N = Plastic DIP Package; Q = Cerdip Package. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD846–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	**200**		25	75		25	**200**	µV
T_{MIN}–T_{MAX}			50	350		50	**125**		100	**350**	µV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	µV/°C
vs. Supply (PSRR)	5 V–18 V[2]										
Initial		**110**	125		**120**	125		**110**	125		dB
vs. Common Mode (CMRR)	V_{CM} = ±10 V										
Initial		**110**	125		**120**	125		**110**	125		dB
INPUT BIAS CURRENT[3]											
–Input Bias Current											
Initial			150	**450**		100	**250**		150	**450**	nA
T_{MIN}–T_{MAX}			450	1200		400	**750**		1000	**1500**	nA
vs. Temperature			6	20		6	**17**		9	20	nA/°C
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**10**		3	**5**		5	**10**	nA/V
T_{MIN}–T_{MAX}			5	15		3	7		5	**20**	nA/V
+Input Bias Current											
Initial			3	**15**		3	**5**		3	**15**	µA
T_{MIN}–T_{MAX}			4	20		4	7		5	**20**	µA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**15**		3	**10**		5	**15**	nA/V
T_{MIN}–T_{MAX}			5	15		3	**10**		5	**20**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/√Hz
Input Current Noise											
–Input	1 kHz		20			20			20		pA/√Hz
+Input	1 kHz		6			6			6		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V, R_{LOAD} = 500 Ω	**100**	200		**150**	200		**100**	200		MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**±10**			**±10**			**±10**			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = –1 R_F = 1k		80			80			80		MHz
(–3 dB)	A_V = –10 R_F = 875 Ω		31			31			31		MHz
	A_V = –30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} = 20 V p-p										
	R_L = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = –1		10			10			10		ns
Overshoot	A_V = –1		20			20			20		%
Slew Rate	A_V = –1		450			450			450		V/µs
Settling Time											
10 V Step, A_V = –1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%
DIFFERENTIAL GAIN	F = 4.4 MHz, R_L = 100 Ω		0.01			0.01			0.01		%
DIFFERENTIAL PHASE	F = 4.4 MHz, R_L = 100 Ω		0.028			0.028			0.028		Degrees
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current	T_{MIN}–T_{MAX}		5	**6.5**		5	**6.5**		5	7	mA

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Test Conditions: $+V_S$ = 15 V, $-V_S$ = 5 V to 18 V and $+V_S$ = 5 V to 18 V, $-V_S$ = 15 V.
[3]Bias Current Specifications are guaranteed maximum after 5 minutes at T_A = +25°C.
[4]FPBW = Slew Rate/2 π V_{PEAK}.
[5]Total Harmonic Distortion.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

800 MHz, 50 mW Current Feedback Amplifier

AD8001

FEATURES

Excellent Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 100 MHz
- 0.01% Differential Gain Error
- 0.025° Differential Phase Error

Low Power
- 5.5 mA max Power Supply Current (55 mW)

High Speed and Fast Settling
- 880 MHz, –3 dB Bandwidth (G = +1)
- 440 MHz, –3 dB Bandwidth (G = +2)
- 1200 V/μs Slew Rate
- 10 ns Settling Time to 0.1%

Low Distortion
- –65 dBc THD, f_C = 5 MHz
- 33 dBm 3rd Order Intercept, F_1 = 10 MHz
- –66 dB SFDR, f = 5 MHz

High Output Drive
- 70 mA Output Current
- Drives Up to 4 Back-Terminated Loads (75 Ω Each) While Maintaining Good Differential Gain/Phase Performance (0.05%/0.25°)

APPLICATIONS

A-to-D Driver
Video Line Driver
Professional Cameras
Video Switchers
Special Effects
RF Receivers

PRODUCT DESCRIPTION

The AD8001 is a low power, high speed amplifier designed to operate on ±5 V supplies. The AD8001 features unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance on only 50 mW of power. The AD8001 is a current feedback amplifier and features gain flatness of 0.1 dB to 100 MHz while offering differential gain and phase error of 0.01% and 0.025°. This makes the AD8001 ideal for professional video electronics such as cameras and video switchers. Additionally, the AD8001's low distortion and fast settling make it ideal for buffer high speed A-to-D converters.

The AD8001 offers low power of 5.5 mA max (V_S = ±5 V) and can run on a single +12 V power supply, while being capable of delivering up to 70 mA of load current. All this is offered in a small 8-pin DIP or 8-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power is critical.

The outstanding bandwidth of 800 MHz along with 1200 V/μs of slew rate make the AD8001 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8001 is available in the industrial temperature range of –40°C to +85°C.

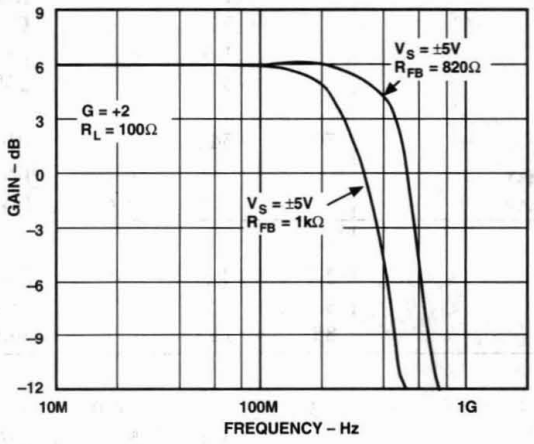
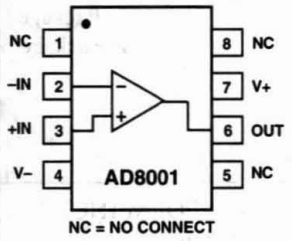


Figure 1. Frequency Response of AD8001

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD8001AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD8001AR	–40°C to +85°C	8-Pin Plastic SOIC	R-8
AD8001ACHIPS	–40°C to +85°C	Die Form	
AD8001SMD[2]	–55°C to +125°C	8-Pin Cerdip	Q-8
AD8001R-EB+2[3]		SOIC Eval Board, G = +2	

NOTES
[1]For outline information see Package Information section.
[2]Standard Military Drawing Device. Ordering Number TBD. Contact our local sales office, representative or distributor for availability.
[3]Refer to Evaluation Board section.

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AD8001–SPECIFICATIONS (@ T_A = + 25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted)

Model	Conditions	AD8001A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, N Package	G = +2, < 0.1 dB Peaking, R_F = 750 Ω	350	440		MHz
	G = +1, < 1 dB Peaking, R_F = 1 kΩ	650	880		MHz
R Package	G = +2, < 0.1 dB Peaking, R_F = 681 Ω	350	440		MHz
	G = +1, < 0.1 dB Peaking, R_F = 845 Ω	575	715		MHz
Bandwidth for 0.1 dB Flatness					
N Package	G = +2, R_F = 750 Ω	85	110		MHz
R Package	G = +2, R_F = 681 Ω	100	125		MHz
Slew Rate	G = +2, V_O = 2 V Step	800	1000		V/µs
	G = –1, V_O = 2 V Step	960	1200		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step		10		ns
Rise & Fall Time	G = –1, V_O = 2 V Step, R_F = 649 Ω		1.4		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p		–65		dBc
	G = +2, R_L = 100 Ω				
Input Voltage Noise	f = 10 kHz		2.0		nV/√Hz
Input Current Noise	f = 10 kHz, +In		2.0		pA/√Hz
	–In		18		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01	0.025	%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.025	0.04	Degree
Third Order Intercept	f = 10 MHz		33		dBm
1 dB Gain Compression	f = 10 MHz		14		dBm
SFDR	f = 5 MHz		–66		dB
DC PERFORMANCE					
Input Offset Voltage			2.0	5.5	mV
	T_{MIN}–T_{MAX}		2.0	9.0	mV
Offset Drift			10		µV/°C
–Input Bias Current			5.0	25	±µA
	T_{MIN}–T_{MAX}			35	±µA
+Input Bias Current			3.0	6.0	±µA
	T_{MIN}–T_{MAX}			10	±µA
Open Loop Transresistance	V_O = ±2.5 V	250	900		kΩ
	T_{MIN}–T_{MAX}	175			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		10		MΩ
	–Input		50		Ω
Input Capacitance	+Input		1.5		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	50	54		dB
–Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.3	1.0	µA/V
+Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.2	0.7	µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	2.7	3.1		±V
Output Current	R_L = 37.5 Ω	50	70		mA
Short Circuit Current		85	110		mA
POWER SUPPLY					
Operating Range		±3.0		±6.0	V
Quiescent Current	T_{MIN}–T_{MAX}		5.0	5.5	mA
Power Supply Rejection Ratio	$+V_S$ = +4 V to +6 V, $–V_S$ = –5 V	60	75		dB
	$–V_S$ = –4 V to –6 V, $+V_S$ = +5 V	50	56		dB
–Input Current	T_{MIN}–T_{MAX}		0.5	2.5	µA/V
+Input Current	T_{MIN}–T_{MAX}		0.1	0.5	µA/V

Specifications subject to change without notice.

Dual 600 MHz, 50 mW Current Feedback Amplifier

AD8002

FEATURES

Excellent Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 60 MHz
- 0.01% Differential Gain Error
- 0.02° Differential Phase Error

Low Power
- 5.5 mA/Amp max Power Supply Current (55 mW)

High Speed and Fast Settling
- 600 MHz, –3 dB Bandwidth (G = +1)
- 500 MHz, –3 dB Bandwidth (G = +2)
- 1200 V/μs Slew Rate
- 16 ns Settling Time to 0.1%

Low Distortion
- –65 dBc THD, f_C = 5 MHz
- 33 dBm 3rd Order Intercept, F_1 = 10 MHz
- –66 dB SFDR, f = 5 MHz
- –60 dB Crosstalk, f = 5 MHz

High Output Drive
- Over 70 mA Output Current
- Drives Up to 8 Back-Terminated 75 Ω Loads (4 Loads/Side) While Maintaining Good Differential Gain/Phase Performance (0.01%/0.17°)

Available in Small 8-Pin PDIP or SOIC

APPLICATIONS

A-to-D Driver
Video Line Driver
Differential Line Driver
Professional Cameras
Video Switchers
Special Effects
RF Receivers

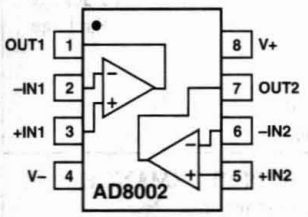
PRODUCT DESCRIPTION

The AD8002 is a dual, low power, high speed amplifier designed to operate on ±5 V supplies. The AD8002 features unique transimpedance linearization circuitry. This allows it to drive video loads with excellent differential gain and phase performance on only 50 mW of power per amplifier. The AD8002 is a current feedback amplifier and features gain flatness of 0.1 dB to 60 MHz while offering differential gain and phase error of 0.01% and 0.02°. This makes the AD8002 ideal for professional video electronics such as cameras and video switchers. Additionally, the AD8002's low distortion and fast settling make it ideal for buffer high speed A-to-D converters.

The AD8002 offers low power of 5.5 mA/amplifier max (V_S = ±5 V) and can run on a single +12 V power supply, while being capable of delivering over 70 mA of load current. All this is offered in a small 8-pin DIP or 8-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power is critical.

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



The outstanding bandwidth of 600 MHz along with 1200 V/μs of slew rate make the AD8002 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from 6 V to 12 V are needed. The AD8002 is available in the industrial temperature range of –40°C to +85°C.

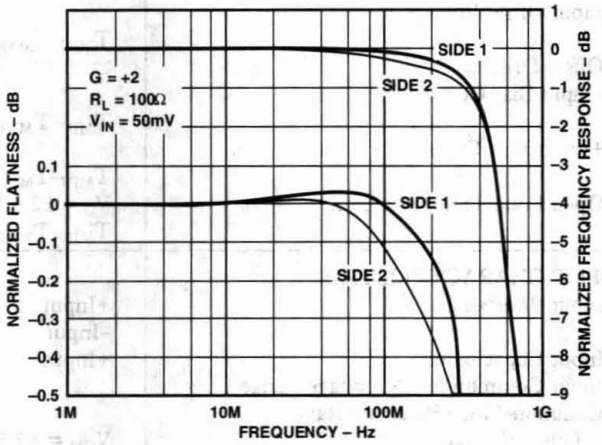


Figure 1. Frequency Response and Flatness, G = +2

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8002AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD8002AR	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD8002AR-REEL	–40°C to +85°C	REEL SOIC	SO-8

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD8002–SPECIFICATIONS (@ T_A = + 25°C, V_S = ±5 V, R_L = 100 Ω, R_C[1] = 75 Ω, unless otherwise noted)

Model		Conditions	AD8002A Min	Typ	Max	Units
DYNAMIC PERFORMANCE						
–3 dB Small Signal Bandwidth,	N Package	G = +2, R_F = 750 Ω		500		MHz
		G = +1, R_F = 1.21 kΩ		600		MHz
	R Package	G = +2, R_F = 681 Ω		500		MHz
		G = +1, R_F = 953 Ω		600		MHz
Bandwidth for 0.1 dB Flatness						
	N Package	G = +2, R_F = 750 Ω		60		MHz
	R Package	G = +2, R_F = 681 Ω		90		MHz
Slew Rate		G = +2, V_O = 2 V Step		700		V/µs
		G = –1, V_O = 2 V Step		1200		V/µs
Settling Time to 0.1%		G = +2, V_O = 2 V Step		16		ns
Rise & Fall Time		G = +2, V_O = 2 V Step, R_F = 750 Ω		2.4		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion		f_C = 5 MHz, V_O = 2 V p-p G = +2, R_L = 100 Ω		–65		dBc
Crosstalk, Output to Output		f = 5 MHz, G = +2		–60		dB
Input Voltage Noise		f = 10 kHz, R_C = 0 Ω		2.0		nV/√Hz
Input Current Noise		f = 10 kHz, +In		2.0		pA/√Hz
		–In		18		pA/√Hz
Differential Gain Error		NTSC, G = +2, R_L = 150 Ω		0.01		%
Differential Phase Error		NTSC, G = +2, R_L = 150 Ω		0.02		Degree
Third Order Intercept		f = 10 MHz		33		dBm
1 dB Gain Compression		f = 10 MHz		14		dBm
SFDR		f = 5 MHz		–66		dB
DC PERFORMANCE						
Input Offset Voltage				2.0	6	mV
		T_{MIN}–T_{MAX}		2.0	9	mV
Offset Drift				10		µV/°C
–Input Bias Current				5.0	25	±µA
		T_{MIN}–T_{MAX}			35	±µA
+Input Bias Current				3.0	6.0	±µA
		T_{MIN}–T_{MAX}			10	±µA
Open Loop Transresistance		V_O = ±2.5 V	250	900		kΩ
		T_{MIN}–T_{MAX}	175			kΩ
INPUT CHARACTERISTICS						
Input Resistance		+Input		10		MΩ
		–Input		50		Ω
Input Capacitance		+Input		1.5		pF
Input Common-Mode Voltage Range				3.2		±V
Common-Mode Rejection Ratio						
Offset Voltage		V_{CM} = ±2.5 V	49	54		dB
–Input Current		V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.3	1.0	µA/V
+Input Current		V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		0.2	0.9	µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing		R_L = 150 Ω	2.7	3.1		±V
Output Current[2]				70		mA
Short Circuit Current[2]			85	110		mA
POWER SUPPLY						
Operating Range			±3.0		±6.0	V
Quiescent Current/Both Amplifiers		T_{MIN}–T_{MAX}		10.0	11.5	mA
Power Supply Rejection Ratio		+V_S = +4 V to +6 V, –V_S = –5 V	60	75		dB
		–V_S = –4 V to –6 V, +V_S = +5 V	49	56		dB
–Input Current		T_{MIN}–T_{MAX}		0.5	2.5	µA/V
+Input Current		T_{MIN}–T_{MAX}		0.1	0.5	µA/V

NOTES

[1]R_C is recommended to reduce peaking and minimize input reflections at frequencies above 300 MHz. However, R_C is not required.

[2]Output current is limited by the maximum power dissipation in the package. See the power derating curves.

Specifications subject to change without notice.

Quad 3000 V/μs, 35 mW Current Feedback Amplifier

AD8004

FEATURES

High Speed
- 250 MHz –3 dB Bandwidth (G = +1)
- 3000 V/μs Slew Rate
- 21 ns Settling Time to 0.1%
- 1.8 ns Rise Time for 2 V Step

Low Power
- 3.5 mA/Amp Power Supply Current (35 mW/Amp)

Single Supply Operation
- Fully Specified for +5 V Supply

Good Video Specifications (R_L = 150 Ω, G = +2)
- Gain Flatness 0.1 dB to 30 MHz
- 0.04% Differential Gain Error
- 0.10° Differential Phase Error

Low Distortion
- –78 dBc THD at 5 MHz
- –61 dBc THD at 20 MHz

High Output Current of 50 mA

Available in a 14-Pin PDIP and SOIC

APPLICATIONS

Image Scanners

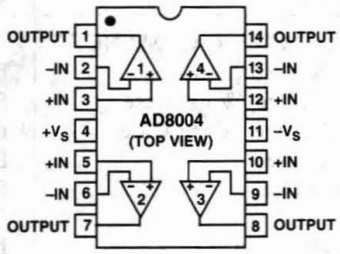
Active Filters

Video Switchers

Special Effects

CONNECTION DIAGRAM

Plastic (N) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD8004 is a quad, low power, high speed amplifier designed to operate on single or dual supplies. It utilizes a current feedback architecture and features high slew rate of 3000 V/μs making the AD8004 ideal for handling large amplitude pulses. Additionally, the AD8004 provides gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase error of 0.04% and 0.10°. This makes the AD8004 suitable for video electronics such as cameras and video switchers.

The AD8004 offers low power of 3.5 mA/amplifier and can run on a single +4 V to +12 V power supply, while being capable of delivering up to 50 mA of load current. All this is offered in a small 14-pin DIP or 14-pin SOIC package. These features make this amplifier ideal for portable and battery powered applications where size and power are critical.

The outstanding bandwidth of 250 MHz along with 3000 V/μs of slew rate make the AD8004 useful in many general purpose, high speed applications where dual power supplies of up to ±6 V and single supplies from 4 V to 12 V are needed. The AD8004 is available in the industrial temperature range of –40°C to +85°C.

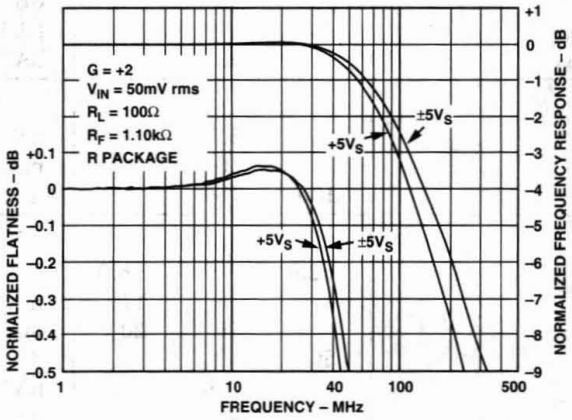


Figure 1. Frequency Response and Flatness, G = +2

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8004AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD8004AR-14	–40°C to +85°C	14-Pin SOIC	R-14
AD8004AR-14-REEL	–40°C to +85°C	14-Pin SOIC	R-14
AD8004AR-14-REEL7	–40°C to +85°C	14-Pin SOIC	R-14

*For outline information see Package Information section.

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AD8004–SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, R_L = 100 Ω, unless otherwise noted)

Parameter	Conditions	AD8004A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Bandwidth, N Package	G = +2, R_F = 698 Ω		185		MHz
	G = +1, R_F = 806 Ω		250		MHz
Bandwidth for 0.1 dB Flatness	G = +2		30		MHz
Slew Rate	G = +2, V_O = 4 V Step		3000		V/µs
	G = –2, V_O = 4 V Step		2000		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		21		ns
Rise & Fall Time (10% to 90%)	G = +2, V_O = 2 V Step		1.8		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–78		dBc
Crosstalk, R Package, Worst Case	f = 5 MHz, G = +2, R_L = 1 kΩ		–69		dB
Crosstalk, N Package, Worst Case	f = 5 MHz, G = +2, R_L = 1 kΩ		–64		dB
Input Voltage Noise	f = 10 kHz		1.5		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz, +In		38		$pA/\sqrt{Hz}$
	–In		38		$pA/\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω, R_F = 1.21 kΩ		0.04		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω, R_F = 1.21 kΩ		0.10		Degree
Differential Gain Error	NTSC, G = +2, R_L = 1 kΩ, R_F = 1.21 kΩ		0.01		%
Differential Phase Error	NTSC, G = +2, R_L = 1 kΩ, R_F = 1.21 kΩ		0.04		Degree
DC PERFORMANCE					
Input Offset Voltage			1.0	3.5	mV
	T_{MIN}–T_{MAX}		1.5	5	mV
Offset Drift			15		µV/°C
–Input Bias Current			35	90	±µA
	T_{MIN}–T_{MAX}			110	±µA
+Input Bias Current			40	110	±µA
	T_{MIN}–T_{MAX}			120	±µA
Open-Loop Transresistance	V_O = ±2.5 V	170	290		kΩ
	T_{MIN}–T_{MAX}		220		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		2		MΩ
	–Input		50		Ω
Input Capacitance	+Input		1.5		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	52	58		dB
–Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		1		µA/V
+Input Current	V_{CM} = ±2.5 V, T_{MIN}–T_{MAX}		12		µA/V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω		3.9		±V
Output Current			50		mA
Short Circuit Current		100	180		mA
POWER SUPPLY					
Operating Range		±2.0		±6.0	V
Total Quiescent Current			14	17	mA
	T_{MIN}–T_{MAX}		16	20	mA
Power Supply Rejection Ratio	ΔV_S = ±2 V	56	62		dB
–Input Current	T_{MIN}–T_{MAX}		0.5		µA/V
+Input Current	T_{MIN}–T_{MAX}		4		µA/V

NOTES

For single-supply +5 V specifications, request complete data sheet.

Specifications subject to change without notice.

300 MHz, 1 mA Current Feedback Amplifier

AD8011*

FEATURES

Easy to Use
Low Power
- **1 mA Power Supply Current (5 mW on +5 V_S)**

High Speed and Fast Settling on +5 V
- **300 MHz, –3 dB Bandwidth (G = +1)**
- **180 MHz, –3 dB Bandwidth (G = +2)**
- **2000 V/μs Slew Rate**
- **29 ns Settling Time to 0.1%**

Good Video Specifications (R_L = 1 kΩ, G = +2)
- **Gain Flatness 0.1 dB to 25 MHz**
- **0.02% Differential Gain Error**
- **0.06° Differential Phase Error**

Low Distortion
- **–70 dBc Worst Harmonic @ 5 MHz**
- **–62 dBc Worst Harmonic @ 20 MHz**

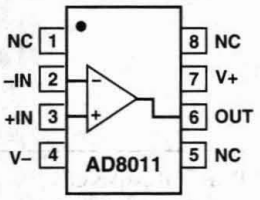
Single Supply Operation
- **Fully Specified for +5 V Supply**

APPLICATIONS

Power Sensitive, High Speed Systems
Video Switchers
Distribution Amplifiers
A-to-D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



PRODUCT DESCRIPTION

The AD8011 is a very low power, high speed amplifier designed to operate on +5 V or ±5 V supplies. With wide bandwidth, low distortion and low power, this device is ideal as a general purpose amplifier. It also can be used to replace high speed amplifiers consuming more power. The AD8011 is a current feedback amplifier and features gain flatness of 0.1 dB to 25 MHz while offering differential gain and phase error of 0.02% and 0.06° on a single +5 V supply. This makes the AD8011 ideal for professional video electronics such as cameras, video switchers or any high speed portable equipment. Additionally, the AD8011's low distortion and fast settling make it ideal for buffering high speed 8-, 10-, 12-bit A-to-D converters.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD8011AN	–40°C to +85°C	8-Pin Plastic DIP
AD8011AR	–40°C to +85°C	8-Pin SOIC
AD8011-EB		Eval Board, SOIC, G = +2

*For outline information see Package Information section.

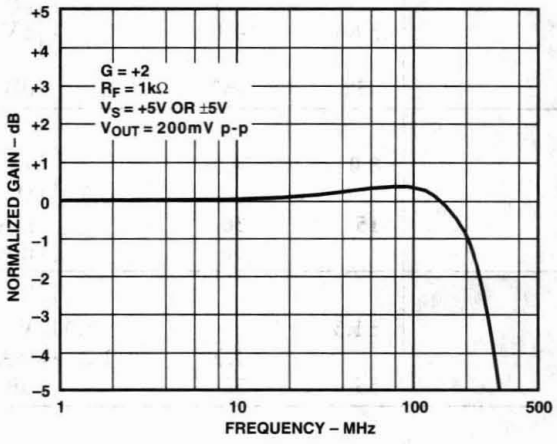


Figure 1. Frequency Response; G = +2, V_S = +5 V or ±5 V

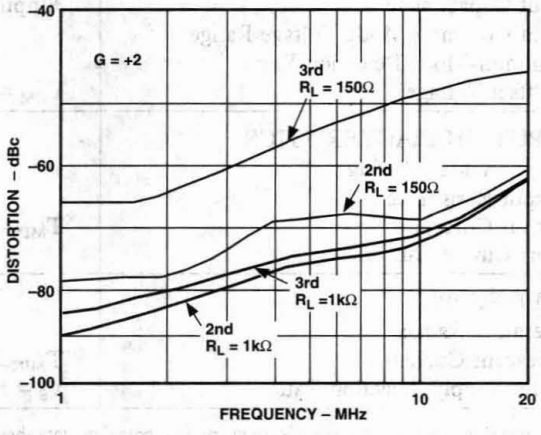


Figure 2. Distortion vs. Frequency; V_S = ±5 V

*Patent pending.

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AD8011–SPECIFICATIONS

DUAL SUPPLY (@ T_A = +25°C, V_S = ±5 V, G = +2, R_F = 1 kΩ, R_L = 1 kΩ, unless otherwise noted)

Model		AD8011A			
	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 1 V p-p	G = +1	340	400		MHz
–3 dB Small Signal Bandwidth, V_O < 1 V p-p	G = +2	180	210		MHz
–3 dB Large Signal Bandwidth, V_O = 5 V p-p	G = +10, R_F = 500 Ω		57		MHz
Bandwidth for 0.1 dB Flatness	G = +2	20	25		MHz
Slew Rate	G = +2, V_O = 4 V Step		3500		V/µs
	G = –1, V_O = 4 V Step		1100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		25		ns
Rise and Fall Time	G = +2, V_O = 2 V Step		0.4		ns
	G = –1, V_O = 2 V Step		3.7		ns
NOISE/HARMONIC PERFORMANCE					
2nd Harmonic	f_C = 5 MHz, V_O = 2 V p-p, G = +2				
	R_L = 1 kΩ		–75		dB
	R_L = 150 Ω		–67		dB
3rd Harmonic	R_L = 1 kΩ		–70		dB
	R_L = 150 Ω		–54		dB
Input Voltage Noise	f = 10 kHz		2		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz, +In		5		$pA/\sqrt{Hz}$
	–In		5		$pA/\sqrt{Hz}$
Differential Gain Error	NTSC, G = +2, R_L = 1 kΩ		0.02		%
	R_L = 150 Ω		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 1 kΩ		0.06		Degrees
	R_L = 150 Ω		0.3		Degrees
DC PERFORMANCE					
Input Offset Voltage			2	5	±mV
	T_{MIN}–T_{MAX}		2	6	±mV
Offset Drift			10		µV/°C
–Input Bias Current			5	15	±µA
	T_{MIN}–T_{MAX}			20	±µA
+Input Bias Current			5	15	±µA
	T_{MIN}–T_{MAX}			20	±µA
Open-Loop Transresistance		800	1300		kΩ
	T_{MIN}–T_{MAX}	550			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		450		kΩ
Input Capacitance	+Input		2.3		pF
Input Common-Mode Voltage Range		3.8	4.1		±V
Common-Mode Rejection Ratio					
Offset Voltage	V_{CM} = ±2.5 V	–52	–57		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		3.9	4.1		±V
Output Resistance			0.1	0.3	Ω
Output Current	T_{MIN}–T_{MAX}	15	30		mA
Short Circuit Current			60		mA
POWER SUPPLY					
Operating Range		±1.5		±6.0	V
Quiescent Current	T_{MIN}–T_{MAX}		1.0	1.2	mA
Power Supply Rejection Ratio	V_S = ±5 V ± 1 V	55	58		dB

NOTE: For single-supply +5 V specifications, request complete data sheet.

Specifications subject to change without notice.

Single Supply, Low Power, Triple Video Amplifier

AD8013

FEATURES

Three Video Amplifiers in One Package
Drives Large Capacitive Load
Excellent Video Specifications (R_L = 150 Ω)
- **Gain Flatness 0.1 dB to 60 MHz**
- **0.02% Differential Gain Error**
- **0.06° Differential Phase Error**

Low Power
- **Operates on Single +5 V to +13 V Power Supplies**
- **4 mA/Amplifier Max Power Supply Current**

High Speed
- **140 MHz Unity Gain Bandwidth (3 dB)**
- **Fast Settling Time of 18 ns (0.1%)**
- **1000 V/μs Slew Rate**

High Speed Disable Function per Channel
- **Turn-Off Time 30 ns**

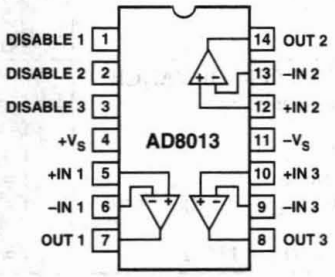
Easy to Use
- **95 mA Short Circuit Current**
- **Output Swing to Within 1 V of Rails**

APPLICATIONS

LCD Displays
Video Line Driver
Broadcast and Professional Video
Computer Video Plug-In Boards
Consumer Video
RGB Amplifier in Component Systems

PIN CONFIGURATION

14-Pin DIP & SOIC Package



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD8013AN	–40°C to +85°C	14-Pin Plastic DIP	N-14
AD8013AR-14	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD8013AR-14-REEL	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD8013AR-14-REEL7	–40°C to +85°C	14-Pin Plastic SOIC	R-14
AD8013ACHIPS	–40°C to +85°C	Die Form	

*For outline information see Package Information section.

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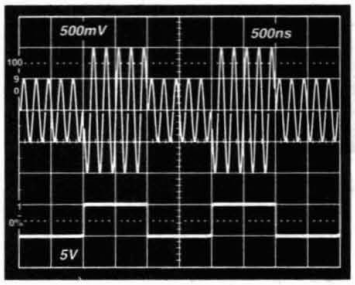
PRODUCT DESCRIPTION

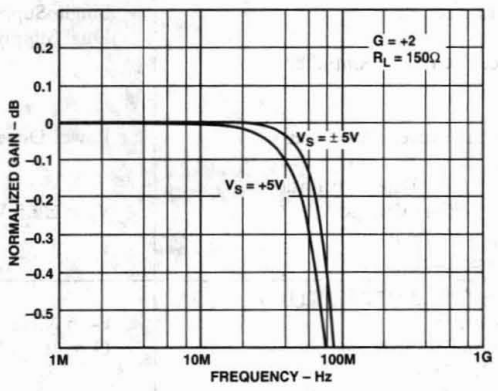
The AD8013 is a low power, single supply, triple video amplifier. Each of the three amplifiers has 30 mA of output current, and is optimized for driving one back terminated video load (150 Ω) each. Each amplifier is a current feedback amplifier and features gain flatness of 0.1 dB to 60 MHz while offering differential gain and phase error of 0.02% and 0.06°. This makes the AD8013 ideal for broadcast and professional video electronics.

The AD8013 offers low power of 4 mA per amplifier max and runs on a single +5 V to +13 V power supply. The outputs of each amplifier swing to within one volt of either supply rail to easily accommodate video signals. The AD8013 is unique among current feedback op amps by virtue of its large capacitive load drive. Each op amp is capable of driving large capacitive loads while still achieving rapid settling time. For instance it can settle in 18 ns driving a resistive load, and achieves 40 ns (0.1%) settling while driving 200 pF.

The outstanding bandwidth of 140 MHz along with 1000 V/μs of slew rate make the AD8013 useful in many general purpose high speed applications where a single +5 V or dual power supplies up to ±6.5 V are required. Furthermore the AD8013's high speed disable function can be used to power down the amplifier or to put the output in a high impedance state. This can then be used in video multiplexing applications. The AD8013 is available in the industrial temperature range of –40°C to +85°C.



Channel Switching Characteristics for a 3:1 Mux



Fine-Scale Gain Flatness vs. Frequency, G = +2, R_L = 150 Ω

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AD8013—SPECIFICATIONS (@ T_A = +25°C, R_{LOAD} = 150 Ω, unless otherwise noted)

Model	Conditions	V_S	AD8013A Min	AD8013A Typ	AD8013A Max	Units
DYNAMIC PERFORMANCE						
Bandwidth (3 dB)	No Peaking, G = +2	+5 V	100	125		MHz
	No Peaking, G = +2	±5 V	110	140		MHz
Bandwidth (0.1 dB)	No Peaking, G = +2	+5 V		50		MHz
	No Peaking, G = +2	±5 V		60		MHz
Slew Rate	2 V Step	+5 V		400		V/µs
	6 V Step	±5 V	600	1000		V/µs
Settling Time to 0.1%	0 V to +2 V	±5 V		18		ns
	4.5 V Step, C_{LOAD} = 200 pF R_{LOAD} > 1 kΩ, R_{FB} = 4 kΩ	±6 V		40		ns
NOISE/HARMONIC PERFORMANCE						
Total Harmonic Distortion	f_C = 5 MHz, R_L = 1 k	±5 V		–76		dBc
	f_C = 5 MHz, R_L = 150 Ω	±5 V		–66		dBc
Input Voltage Noise	f = 10 kHz	+5 V, ±5 V		3.5		nV/√Hz
Input Current Noise	f = 10 kHz ($-I_{IN}$)	+5 V, ±5 V		12		pA/√Hz
Differential Gain (R_L = 150 Ω)	f = 3.58 MHz, G = +2	+5 V		0.05		%
		±5 V		0.02	0.05	%
Differential Phase (R_L = 150 Ω)	f = 3.58 MHz, G = +2	+5 V, ±5 V		0.06		Degrees
DC PERFORMANCE						
Input Offset Voltage	T_{MIN} to T_{MAX}	+5 V, ±5 V		2	5	mV
Offset Drift				7		µV/°C
Input Bias Current (–)		+5 V, ±5 V		2	10	µA
Input Bias Current (+)	T_{MIN} to T_{MAX}	+5 V, ±5 V		3	15	µA
Open-Loop Transresistance		+5 V	650	800		kΩ
		±5 V	800 k	1.1 M		Ω
INPUT CHARACTERISTICS						
Input Resistance	+Input	±5 V		200		kΩ
	–Input	±5 V		150		Ω
Input Capacitance		±5 V		2		pF
Input Common-Mode Voltage Range		±5 V		3.8		±V
		+5 V	1.2		3.8	+V
Common-Mode Rejection Ratio						
Input Offset Voltage		+5 V, ±5 V	52	56		dB
–Input Current		+5 V, ±5 V		0.2	0.4	µA/V
+Input Current		+5 V, ±5 V		5	7	µA/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing						
R_L = 1 kΩ	V_{OL}–V_{EE}, V_{CC}–V_{OH}			0.8	1.0	V
R_L = 150 Ω	V_{OL}–V_{EE}, V_{CC}–V_{OH}			1.1	1.3	V
Output Current		+5 V, ±5 V		30		mA
Short-Circuit Current		±5 V		95		mA
Capacitive Load Drive		±5 V		1000		pF
MATCHING CHARACTERISTICS						
Dynamic						
Crosstalk	G = +2, f = 5 MHz	+5 V, ±5 V		70		dB
Gain Flatness Match	f = 20 MHz	±5 V		0.1		dB
POWER SUPPLY						
Operating Range	Single Supply		+4.2		+13	V
	Dual Supply		±2.1		±6.5	V
Quiescent Current/Amplifier		+5 V		3.0	3.5	mA
		±5 V		3.4	4.0	mA
		±6.5 V		3.5		mA
Quiescent Current/Amplifier	Power Down	+5 V		0.25	0.35	mA
		±5 V		0.3	0.4	mA
Power Supply Rejection Ratio						
Input Offset Voltage	V_S = ±2.5 V to ±5 V		70	76		dB
–Input Current		+5 V, ±5 V		0.03	0.2	µA/V
+Input Current		+5 V, ±5 V		0.07	1.0	µA/V
DISABLE CHARACTERISTICS						
Off Isolation	f = 6 MHz	+5 V, ±5 V		–70		dB
Off Output Impedance	G = +1	+5 V, ±5 V		12		pF
Turn-On Time				50		ns
Turn-Off Time				30		ns
Switching Threshold		$-V_S$ + xV	1.3	1.6	1.9	V

Specifications subject to change without notice.

Wideband/Differential Output Transimpedance Amplifier

AD8015

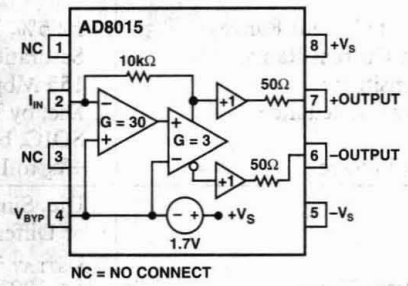
FEATURES

Low Cost, Wide Bandwidth, Low Noise
Bandwidth: 240 MHz
Pulse Width Modulation: 500 ps
Rise Time/Fall Time: 1.5 ns
Input Current Noise: 3.0 pA/$\sqrt{Hz}$ @ 100 MHz
Total Input RMS Noise: 26.5 nA to 100 MHz
Wide Dynamic Range
Optical Sensitivity: –36 dBm @ 155.52 Mbps
Peak Input Current: ±350 μA
Differential Outputs
Low Power: 5 V @ 25 mA
Wide Operating Temperature Range: –40°C to +85°C

APPLICATIONS

Fiber Optic Receivers: SONET/SDH, FDDI, Fibre Channel
Stable Operation with High Capacitance Detectors
Low Noise Preamplifiers
Single-Ended to Differential Conversion
I-to-V Converters

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD8015 is a wide bandwidth, single supply transimpedance amplifier optimized for use in a fiber optic receiver circuit. It is a complete, single chip solution for converting photodiode current into a differential voltage output. The 240 MHz bandwidth enables AD8015 application in FDDI receivers and SONET/SDH receivers with data rates up to 155 Mbps. This high bandwidth supports data rates beyond 300 Mbps. The differential outputs drive ECL directly, or can drive a comparator/ fiber optic post amplifier.

In addition to fiber optic applications, this low cost, silicon alternative to GaAs-based transimpedance amplifiers is ideal for systems requiring a wide dynamic range preamplifier or single-ended to differential conversion. The IC can be used with a standard ECL power supply (–5.2 V) or a PECL (+5 V) power supply; the common mode at the output is ECL compatible. The AD8015 is available in die form, or in an 8-pin SOIC package.

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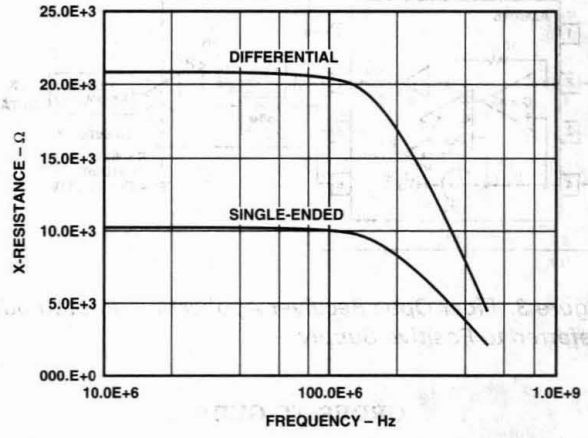


Figure 1. Differential/Single-Ended Transimpedance vs. Frequency

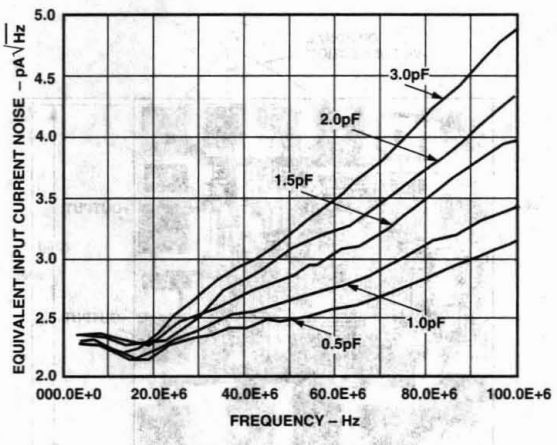


Figure 2. Noise vs. Frequency (SO-8 Package with Added Capacitance)

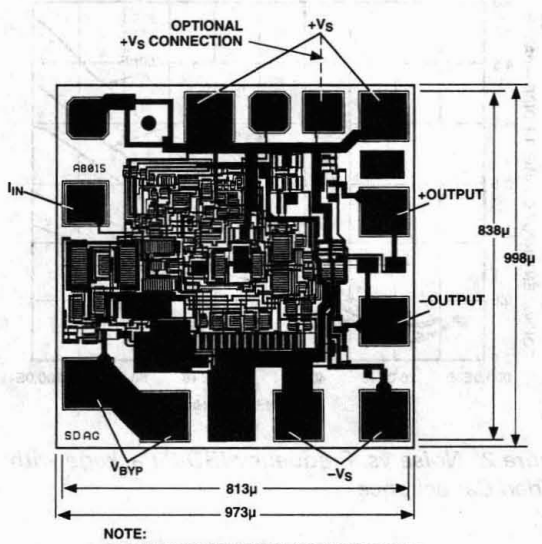
AD8015–SPECIFICATIONS (SO Package @ T_A = +25°C and V_S = +5 V, unless otherwise noted)

Parameter	Conditions	AD8015AR Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
Bandwidth	3 dB	180	240		MHz
Pulse Width Modulation	10 µA to 200 µA Peak		500		ps
Rise and Fall Time	10% to 90%		1.5		ns
Settling Time	to 3%, 0.5 V Diff Output Step		3		ns
INPUT					
Linear Input Current Range	±2.5%, Nonlinearity	±25	±30		µA
Max Input Current Range	Saturation	±200	±350		µA
Optical Sensitivity	155 Mbps, Avg Power		–36		dBm
Input Stray Capacitance	Die, by Design		0.2		pF
	SOIC, by Design		0.4		pF
Input Bias Voltage	$+V_S$ to I_{IN} and V_{BYP}	1.6	1.8	2.0	V
NOISE	Die, Single Ended at P_{OUT}, or Differential (P_{OUT}–N_{OUT}), C_{STRAY} = 0.3 pF				
Input Current Noise	f = 100 MHz		3.0		pA/√Hz
Total Input RMS Noise	DC to 100 MHz		26.5		nA
TRANSFER CHARACTERISTICS					
Transresistance	Single Ended	8	10	12	kΩ
	Differential	16	20	24	kΩ
Power Supply	Single Ended		37.0		dB
Rejection Ratio	Differential		40		dB
OUTPUT					
Differential Offset			6	20	mV
Output Common-Mode Voltage	From Positive Supply	–1.5	–1.3	–1.1	V
Voltage Swing (Differential)	Positive Input Current, R_L = ∞		1.0		V p-p
	Positive Input Current, R_L = 50 Ω		600		mV p-p
Output Impedance		40	50	60	Ω
POWER SUPPLY	T_{MIN} to T_{MAX}				
Operating Range	Single Supply	+4.5	+5	+11	V
	Dual Supply	±2.25		±5.5	V
Current			25	26	mA

Specifications subject to change without notice.

METALIZATION PHOTOGRAPH

Dimensions shown in microns. Not to scale.



NOTE:
FOR BEST PERFORMANCE ATTACH PACKAGE SUBSTRATE TO $+V_S$.
MATERIAL AT BACK OF DIE IS SILICON. USE OF $+V_S$ OR $-V_S$ FOR DIE ATTACH IS ACCEPTABLE.

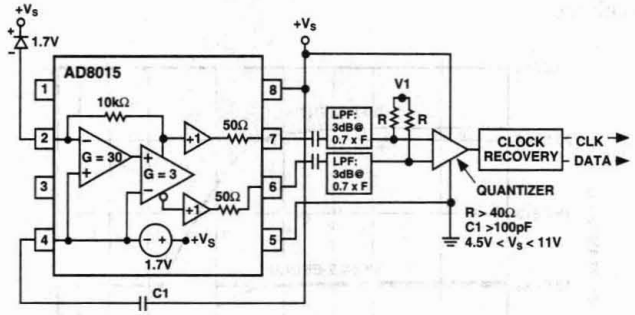


Figure 3. Fiber Optic Receiver Application: Photodiode Referred to Positive Supply

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8015AR	–40°C to +85°C	8-Pin Plastic SOIC	SO-8
AD8015ACHIPS	–40°C to +85°C	Die Form	

*For outline information see Package Information section.

+2.7 V, 800 μA, 80 MHz Rail-to-Rail I/O Amplifiers

AD8031/AD8032

FEATURES

Low Power
- Supply Current 800 μA/Amplifier
- Fully Specified at +2.7 V, 5 V and ±5 V Supplies

High Speed and Fast Settling on +5 V
- 80 MHz –3 dB Bandwidth (G = +1)
- 30 V/μs Slew Rate
- 125 ns Settling Time to 0.1%

Rail-to-Rail Input and Output
- No Phase Reversal with Input 0.5 V Beyond Supplies
- Input CMVR Extends Beyond Rails by 500 mV
- Output Swing to Within 20 mV of Either Rail

Low Distortion
- –62 dB @ 1 MHz, V_O = 2 V p-p
- –86 dB @ 100 kHz, V_O = 4.6 V p-p

Output Current: 15 mA

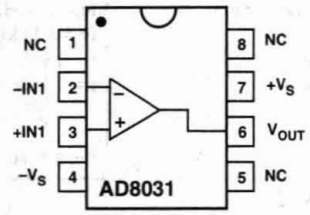
APPLICATIONS

High Speed Battery Operated Systems
High Component Density Systems
Loop Powered Systems
Portable Test Instruments

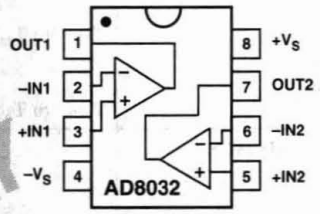
FUNCTIONS

A/D Buffer
Signal Conditioning Amplifier
Active Filter
High Speed Set and Demand Amplifier

CONNECTION DIAGRAMS



NC = NO CONNECT



PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD8031AN	–40°C to +85°C	8-Lead P-DIP
AD8031BN	–40°C to +85°C	8-Lead P-DIP
AD8031AR	–40°C to +85°C	8-Lead SOIC
AD8031BR	–40°C to +85°C	8-Lead SOIC
AD8032AN	–40°C to +85°C	8-Lead P-DIP
AD8032BN	–40°C to +85°C	8-Lead P-DIP
AD8032AR	–40°C to +85°C	8-Lead SOIC
AD8032BR	–40°C to +85°C	8-Lead SOIC

*For outline information see Package Information section.

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PRODUCT DESCRIPTION

The AD8031 (single) and AD8032 (dual) single supply voltage feedback amplifiers feature high speed performance with 80 MHz of bandwidth, 30 V/μs slew rate and 125 ns settling time. This performance is possible while consuming less than 4.0 mW of power from a single +5 V supply. Features that increase the operation time of high speed battery powered systems without reducing dynamic performance.

The products have true single supply capability with rail-to-rail input and output performance and are specified to operate on +2.7 V, +5 V and ±5 V. The differential voltage range can extend up to 500 mV beyond each rail. The output voltage swing extends to within 20 mV of each rail providing the maximum output dynamic range.

The AD8031 and AD8032 also offer excellent signal quality for only 800 μA of supply current per amplifier; THD is –62 dBc at 1 MHz and differential gain and phase errors are 0.14% and 0.21°C. The low distortion and fast settling time make them ideal as buffers to single supply, A-to-D converters.

Operating on supplies from +2.7 V to +12 V and dual supplies up to ±6 V, the AD8031 and AD8032 are ideal for a wide range of applications, from battery operated systems with large bandwidth requirements to high speed systems where component density requires lower power dissipation. The AD8031 and AD8032 are available in 8-pin plastic DIP and SOIC packages.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD8031/AD8032–SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 1 kΩ to +2.5 V, R_F = 2.5 kΩ unless otherwise noted)

Parameter	Conditions	AD8031A/AD8032A Min	Typ	Max	AD8031B/AD8032B Min	Typ	Max	Units
DYNAMIC PERFORMANCE								
–3 dB Small Signal Bandwidth	G = +1, V_O < 0.4 V p-p	TBD	80		TBD	80		MHz
Slew Rate	G = –1, V_O = 2 V Step		30			30		V/μs
Settling Time to 0.1%	G = –1, V_O = 2 V Step, C_L = 10 pF		125			125		ns
Settling Time to 0.01%	G = –1, V_O = 2 V Step, C_L =10 pF		175			175		ns
DISTORTION/NOISE PERFORMANCE								
Total Harmonic Distortion	fc = 1 MHz, V_O = 2 V p-p, G = +2		–62			–62		dBc
	fc = 100 kHz, V_O = 2 V p-p, G = +2		–86			–86		dBc
Input Voltage Noise	f = 1 kHz		15			15		nV/√Hz
Input Current Noise	f = 1 kHz		TBD			TBD		pA/√Hz
Differential Gain			0.14			0.14		%
Differential Phase			0.21			0.21		Degrees
Worst Case Crosstalk (AD8032 only)	f = 5 MHz		–60			–60		dB
DC PERFORMANCE								
Input Offset Voltage			±1	±5		±0.8	±1.5	mV
	T_{MIN} to T_{MAX}			TBD			TBD	mV
Offset Drift			5			5		μV/°C
Input Bias Current			0.45	1		0.45	1	μA
	T_{MIN} to T_{MAX}		0.45			0.45		μA
Input Offset Current			50			50		nA
Open Loop Gain		80	82		80	82		dB
	T_{MIN} to T_{MAX}		TBD			TBD		dB
INPUT CHARACTERISTICS								
Input Resistance			TBD			TBD		Ω
+Input Resistance			TBD			TBD		MΩ
Input Capacitance			TBD			TBD		pF
Input Voltage Range		–0.5		+5.5	–0.5		+5.5	V
Input Common Mode Voltage Range			–0.2 to 5.2			–0.2 to 5.2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 5 V		65			65		dB
	V_{CM} = 0 V to 3.5 V		92			92		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing	R_L = 10 kΩ		+0.02 to +4.98			+0.02 to +4.98		V
	R_L = 1 kΩ		TBD			TBD		V
Output Current			15			15		mA
Short Circuit Current	Sourcing		19			19		mA
	Sinking		–31			–31		mA
Capacitive Load Drive	G = +1		TBD			TBD		pF
POWER SUPPLY								
Operating Range		+2.7		+12	+2.7		+12	V
Quiescent Current per Amplifier			800	900		800	900	μA
Power Supply Rejection Ratio	V_S = 0 V to –1 V or							
	V_S+ = +5 V to +6 V		80			80		dB

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Distortion, Wide Bandwidth Voltage Feedback Clamp Amps

AD8036/AD8037

FEATURES

Superb Clamping Characteristics
- 3 mV Clamp Error
- 1.5 ns Overdrive Recovery
- Minimized Nonlinear Clamping Region
- 240 MHz Clamp Input Bandwidth
- ±3.9 V Clamp Input Range

Wide Bandwidth

	AD8036	AD8037
Small Signal	240 MHz	270 MHz
Large Signal (4 V p-p)	195 MHz	190 MHz

Good DC Characteristics
- 2 mV Offset
- 10 μV/°C Drift

Ultralow Distortion, Low Noise
- –72 dBc typ @ 20 MHz
- 4.5 nV/√Hz Input Voltage Noise

High Speed
- Slew Rate 1500 V/μs
- Settling 10 ns to 0.1%, 16 ns to 0.01%

±3 V to ±5 V Supply Operation

APPLICATIONS

- ADC Buffer
- IF/RF Signal Processing
- High Quality Imaging
- Broadcast Video Systems
- Video Amplifier
- Full Wave Rectifier

PRODUCT DESCRIPTION

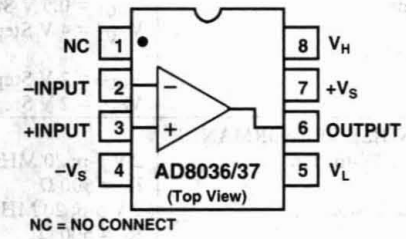
The AD8036 and AD8037 are wide bandwidth, low distortion clamping amplifiers. The AD8036 is unity gain stable. The AD8037 is stable at a gain of two or greater. These devices allow the designer to specify a high (V_{CH}) and low (V_{CL}) output clamp voltage. The output signal will clamp at these specified levels. Clamp error is typically 3 mV or less and distortion in the clamp region is minimized. This product can be used as a classical op amp or a clamp amplifier where a high and low output voltage are specified.

The AD8036 and AD8037, which utilize a voltage feedback architecture, meet the requirements of many applications which previously depended on current feedback amplifiers. The AD8036 and AD8037 exhibit an exceptionally fast and accurate pulse response, extremely wide small-signal and large-signal bandwidths and ultralow distortion. Superb ac and dc characteristics make the AD8036/AD8037 ideal for driving as well as buffering flash and high resolution ADCs.

In addition to static dc clamp levels, signals with speeds up to 240 MHz can be applied to the clamp pins. The clamp values can also be set to any value within the output voltage range provided that V_H is greater that V_L. Due to these clamp characteristics, the AD8036 and AD8037 can be used in nontraditional applications such as a full-wave rectifier, a pulse generator, or an amplitude modulator.

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q), and SO (R) Packages



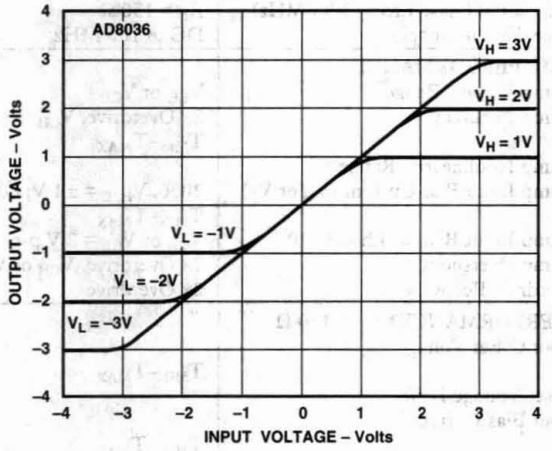


Figure 1. Clamp DC Accuracy vs. Input Voltage

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8036AN	–40°C to +85°C	Plastic DIP	N-8
AD8036AR	–40°C to +85°C	SOIC	R-8
AD8036SQ/883B	–55°C to +125°C	Cerdip	Q-8
AD8036ACHIPS	–40°C to +85°C	Chips	
AD8036-EB		Evaluation Board	
AD8037AN	–40°C to +85°C	Plastic DIP	N-8
AD8037AR	–40°C to +85°C	SOIC	R-8
AD8037-EB		Evaluation Board	

*N = Plastic DIP; Q = Cerdip; R= SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

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AD8036/AD8037–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = +1$ (AD8036); $A_V = +2$ (AD8037), V_H, V_L open, unless otherwise noted)

Parameter	Conditions	AD8036A Min	AD8036A Typ	AD8036A Max	AD8037A Min	AD8037A Typ	AD8037A Max	Units
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	150	240		200	270		MHz
Large Signal[1]	8036, V_{OUT} = 2.5 V p-p; 8037, V_{OUT} = 3.5 V p-p	160	195		160	190		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} \le 0.4$ V p-p							
	8036, $R_F = 140\ \Omega$; 8037, $R_F = 274\ \Omega$		130			130		MHz
Slew Rate, Average +/–	V_{OUT} = 4 V Step, 10–90%	900	1200		1100	1500		V/µs
Rise/Fall Time	V_{OUT} = 0.5 V Step, 10–90%		1.4			1.2		ns
	V_{OUT} = 4 V Step, 10–90%		2.6			2.2		ns
Settling Time								
To 0.1%	V_{OUT} = 2 V Step		10			10		ns
To 0.01%	V_{OUT} = 2 V Step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
2nd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–59	–52		–52	–45	dBc
	$R_L = 500\ \Omega$		–66	–59		–72	–65	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–68	–61		–70	–63	dBc
	$R_L = 500\ \Omega$		–72	–65		–80	–73	dBc
3rd Order Intercept	25 MHz		+46			+41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		6.7			4.5		$nV\sqrt{Hz}$
Input Current Noise	1 MHz to 200 MHz		2.2			2.1		$pA\sqrt{Hz}$
Average Equivalent Integrated								
Input Noise Voltage	0.1 MHz to 200 MHz		95			60		µV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.05	0.09		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	DC to 100 MHz		1.1			1.1		Degree
CLAMP PERFORMANCE								
Clamp Voltage Range[2]	V_{CH} or V_{CL}	±3.3	±3.9		±3.3	±3.9		V
Clamp Accuracy	2× Overdrive, V_{CH} = +2 V, V_{CL} = –2 V		±3	±10		±3	±10	mV
	T_{MIN}–T_{MAX}			±20			±20	mV
Clamp Nonlinearity Range[3]			100			100		mV
Clamp Input Bias Current (V_H or V_L)	8036, $V_{H,L} = \pm 1$ V; 8037, $V_{H,L} = \pm 0.5$ V		±40	±60		±50	±70	µA
	T_{MIN}–T_{MAX}			±80			±90	µA
Clamp Input Bandwidth (–3 dB)	V_{CH} or V_{CL} = 2 V p-p	150	240		180	270		MHz
Clamp Overshoot	2× Overdrive, V_{CH} or V_{CL} = 2 V p-p		1	5		1	5	%
Overdrive Recovery	2× Overdrive		1.5			1.3		ns
DC PERFORMANCE[4] $R_L = 150\ \Omega$								
Input Offset Voltage[5]			2	7		2	7	mV
	T_{MIN}–T_{MAX}			11			10	mV
Offset Voltage Drift			±10			±10		µV/°C
Input Bias Current			4	10		3	9	µA
	T_{MIN}–T_{MAX}			15			15	µA
Input Offset Current			0.3	3		0.1	3	µA
	T_{MIN}–T_{MAX}			5			5	µA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2$ V	66	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	48	55		54	60		dB
	T_{MIN}–T_{MAX}	40			46			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±2.5			±2.5		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			20.5	21.5		18.5	19.5	mA
	T_{MIN}–T_{MAX}			25			24	mA
Power Supply Rejection Ratio	T_{MIN}–T_{MAX}	50	60		56	66		dB

NOTES
[1]See Max Ratings and Theory of Operation sections of data sheet.
[2]See Max Ratings.
[3]Nonlinearity is defined as the voltage delta between the set input clamp voltage (V_H or V_L) and the voltage at which V_{OUT} starts deviating from V_{IN} (see Figure 73).
[4]Measured at $A_V = 50$.
[5]Measured with respect to the inverting input.

Specifications subject to change without notice.

160 MHz Rail-to-Rail Amplifier with Disable

AD8041

FEATURES

Fully Specified for +3 V, +5 V, and ±5 V Supplies
Output Swings Rail to Rail
Input Voltage Range Extends 200 mV Below Ground
No Phase Reversal with Inputs 1 V Beyond Supplies
Disable/Power-Down Capability
Low Power of 5.2 mA (26 mW on +5 V)
High Speed and Fast Settling on +5 V:
- **160 MHz –3 dB Bandwidth (G = +1)**
- **160 V/μs Slew Rate**
- **30 ns Settling Time to 0.1%**

Good Video Specifications (R_L = 150 Ω, G = +2)
- **Gain Flatness of 0.1 dB to 30 MHz**
- **0.03% Differential Gain Error**
- **0.03° Differential Phase Error**

Low Distortion
- **–69 dBc Worst Harmonic @ 10 MHz**

Outstanding Load Drive Capability
- **Drives 50 mA 0.5 V from Supply Rails**

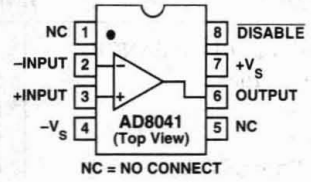
Cap Load Drive of 45 pF

APPLICATIONS

Power Sensitive High Speed Systems
Video Switchers
Distribution Amplifiers
A/D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



PRODUCT DESCRIPTION

The AD8041 is a low power voltage feedback, high speed amplifier designed to operate on +3 V, +5 V or ±5 V supplies. It has true single supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

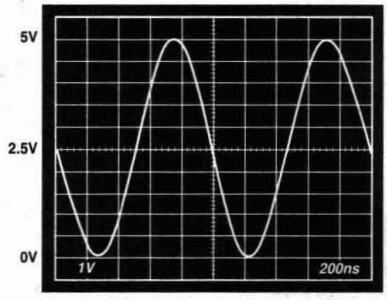


Figure 1. Output Swing: Gain = –1, V_S = +5 V

The output voltage swing extends to within 50 mV of each rail, providing the maximum output dynamic range. The AD8041 is ideal for buffering high speed A-to-D converters in professional video electronics such as cameras, video switchers or any high speed portable equipment.

The AD8041 has a high speed disable feature useful for multiplexing or for reducing power consumption. The disable logic interface is compatible with CMOS or open-collector logic. The AD8041 offers low power supply current of 5.8 mA max and can run on a single +3 V power supply.

The AD8041s 160 MHz wide bandwidth and 160 V/μs slew rate on a single +5 V supply make the AD8041 useful in many general purpose high speed applications where dual power supplies of up to ±6 V and single supplies from +3 V to +12 V are needed.

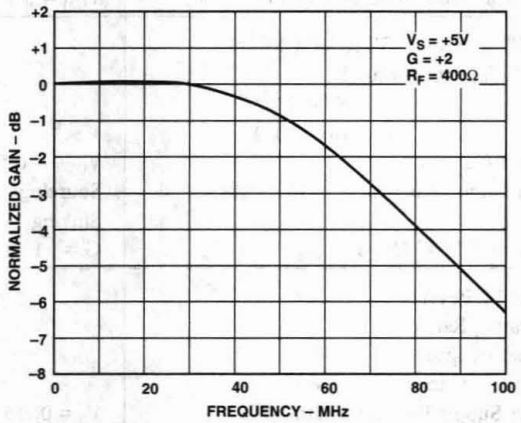


Figure 2. Frequency Response: Gain = +2, V_S = +5 V

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD8041AN	–40°C to +85°C	8-Pin Plastic DIP
AD8041AR	–40°C to +85°C	8-Pin Plastic SOIC
AD8041AR-REEL		REEL-SOIC
AD8041-EB		Evaluation Board

*For outline information see Package Information section.

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AD8041—SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted)

Parameter	Conditions	AD8041A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	130	160		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		30		MHz
Slew Rate	G = –1, V_O = 2 V Step	130	160		V/μs
Full Power Response	V_O = 2 V p-p		24		MHz
Settling Time to 0.1%	G = –1, V_O = 2 V Step		35		ns
Settling Time to 0.01%			55		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–72		dB
Input Voltage Noise	f = 10 kHz		16		nV/√Hz
Input Current Noise	f = 10 kHz		600		fA/√Hz
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.03		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.03		Degrees
	G = +2, R_L = 75 Ω to 2.5 V		0.01		%
	G = +2, R_L = 75 Ω to 2.5 V		0.19		Degrees
DC PERFORMANCE					
Input Offset Voltage			2	7	mV
	T_{MIN}–T_{MAX}			8	mV
Offset Drift			10		μV/°C
Input Bias Current			1.2	2	μA
	T_{MIN}–T_{MAX}			3	μA
Input Offset Current			0.2	0.5	μA
Open-Loop Gain	R_L = 1 kΩ	86	95		dB
	T_{MIN}–T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			160		kΩ
Input Capacitance			1.8		pF
Input Common-Mode Voltage Range			–0.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	74	80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing: R_L = 10 kΩ			0.05 to 4.95		V
R_L = 1 kΩ		0.35 to 4.75	0.1 to 4.9		V
R_L = 50 Ω		0.4 to 4.4	0.3 to 4.5		V
Output Current	V_{OUT} = 0.5 V to 4.5 V		50		mA
Short Circuit Current	Sourcing		90		mA
	Sinking		150		mA
Capacitive Load Drive	G = +1		45		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			5.2	5.8	mA
Quiescent Current (Disabled)			1.4	1.7	mA
Power Supply Rejection Ratio	V_S = 0, +5 V, ±1 V	72	80		dB
DISABLE CHARACTERISTICS	V_O = 2 V p-p @ 10 MHz, G = + 2				
Turn-Off Time	R_F = R_L = 2 kΩ		120		ns
Turn-On Time	R_F = R_L = 2 kΩ		230		ns
Off Isolation (Pin 8 Tied to $-V_S$)	R_L = 100 Ω, f = 5 MHz, G = +2, R_F = 1 kΩ		70		dB
Off Voltage (Device Disabled)			<+V_S – 0.25		V
On Voltage (Device Enabled)			Open or +V_S		V

NOTE: For +3 V and ±5 V specifications, request complete data sheet.

Specifications subject to change without notice.

Dual 160 MHz Rail-to-Rail Amplifier

AD8042

FEATURES

Single AD8041 and Quad AD8044 also Available
Fully Specified at +3 V, +5 V, and ±5 V Supplies
Output Swings to Within 30 mV of Either Rail
Input Voltage Range Extends 200 mV Below Ground
No Phase Reversal with Inputs 0.5 V Beyond Supplies
Low Power of 5.2 mA per Amplifier
High Speed and Fast Settling on +5 V:
- **160 MHz –3 dB Bandwidth (G = +1)**
- **200 V/μs Slew Rate**
- **39 ns Settling Time to 0.1%**

Good Video Specifications (R_L = 150 Ω, G = +2)
- **Gain Flatness of 0.1 dB to 14 MHz**
- **0.02% Differential Gain Error**
- **0.04° Differential Phase Error**

Low Distortion
- **–64 dBc Worst Harmonic @ 10 MHz**

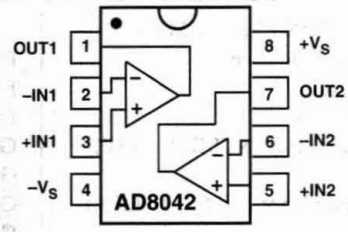
Drives 50 mA 0.5 V from Supply Rails

APPLICATIONS

Video Switchers
Distribution Amplifiers
A/D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP and SOIC



PRODUCT DESCRIPTION

The AD8042 is a low power voltage feedback, high speed amplifier designed to operate on +3 V, +5 V or ±5 V supplies. It has true single supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

The output voltage swing extends to within 30 mV of each rail, providing the maximum output dynamic range. Additionally, it features gain flatness of 0.1 dB to 14 MHz while offering differential gain and phase error of 0.04% and 0.06° on a single +5 V supply. This makes the AD8042 useful for professional video electronics such as cameras, video switchers or any high speed portable equipment. The AD8042's low distortion and fast settling make it ideal for buffering single supply, high speed A-to-D converters.

The AD8042 offers low power supply current of 12 mA max and can run on a single +3.3 V power supply. These features are ideally suited for portable and battery powered applications where size and power are critical.

The wide bandwidth of 160 MHz along with 200 V/μs of slew rate on a single +5 V supply make the AD8042 useful in many general purpose, high speed applications where single supplies from +3.3 V to +12 V and dual power supplies of up to ±6 V are needed. The AD8042 is available in 8-pin plastic DIP and SOIC.

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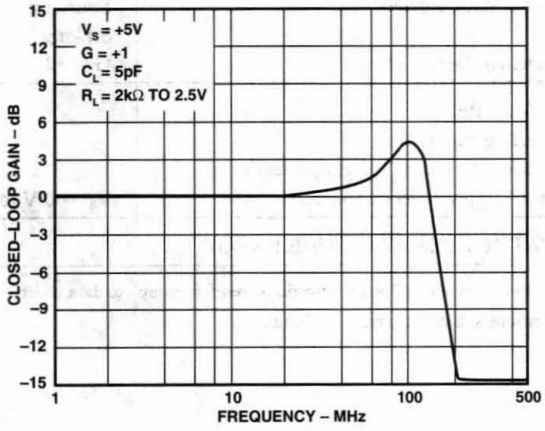
ORDERING GUIDE

Model	Supply Voltage	Temperature Range	Package Option*
AD8042AN	+5 V, ±5 V	–40°C to +85°C	8-Pin Plastic DIP
AD8042AN	+3 V	0°C to +70°C	8-Pin Plastic DIP
AD8042AR	+5 V, ±5 V	–40°C to +85°C	8-Pin Plastic SOIC
AD8042AR	+3 V	0°C to +70°C	8-Pin Plastic SOIC
AD8042AR-REEL			REEL-SOIC

*For outline information see Package Information section.



Frequency Response

AD8042–SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted)

Parameter	Conditions	AD8042A Min	AD8042A Typ	AD8042A Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	125	160		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω. R_F = 200 Ω		14		MHz
Slew Rate	G = –1, V_O = 2 V Step	130	200		V/μs
Full Power Response	V_O = 2 V p-p		30		MHz
Settling Time to 1%	G = –1, V_O = 2 V Step		26		ns
Settling Time to 0.1%			39		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–73		dB
Input Voltage Noise	f = 10 kHz		15		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz		700		$fA/\sqrt{Hz}$
Differential Gain Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω to 2.5 V		0.04	0.06	%
	G = +2, R_L = 75 Ω to 2.5 V		0.04		%
Differential Phase Error (NTSC, 100 IRE)	G = +2, R_L = 150 Ω to 2.5 V		0.06	0.12	Degrees
	G = +2, R_L = 75 Ω to 2.5 V		0.24		Degrees
Worst Case Crosstalk	f = 5 MHz, R_L = 150 Ω to 2.5 V		–63		dB
DC PERFORMANCE					
Input Offset Voltage			3	9	mV
	T_{MIN}–T_{MAX}			12	mV
Offset Drift			12		μV/°C
Input Bias Current			1.2	3.2	μA
	T_{MIN}–T_{MAX}			4.8	μA
Input Offset Current			0.2	0.5	μA
Open-Loop Gain	R_L = 1 kΩ	90	100		dB
	T_{MIN}–T_{MAX}		90		dB
INPUT CHARACTERISTICS					
Input Resistance			300		kΩ
Input Capacitance			1.5		pF
Input Common-Mode Voltage Range			–0.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	68	74		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to 2.5 V		0.03 to 4.97		V
	R_L = 1 kΩ to 2.5 V	0.10 to 4.9	0.05 to 4.95		V
	R_L = 50 Ω to 2.5 V	0.4 to 4.4	0.36 to 4.45		V
Output Current	T_{MIN} to T_{MAX}, V_{OUT} = 0.5 V to 4.5 V		50		mA
Short Circuit Current	Sourcing		90		mA
	Sinking		100		mA
Capacitive Load Drive	G = +1		20		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current (Per Amplifier)			5.2	6	mA
Power Supply Rejection Ratio	V_S^- = 0 V to –1 V, or V_S^+ = +5 V to +6 V	72	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTE: For +3 V and ±5 V specifications, request complete data sheet.

Specifications subject to change without notice.

ANALOG DEVICES

Quad 150 MHz Rail-to-Rail Amplifier

AD8044

FEATURES

Single AD8041 and Dual AD8042 Also Available
Fully Specified at +3 V, +5 V, and ±5 V Supplies
Output Swings to Within 25 mV of Either Rail
Input Voltage Range Extends 200 mV Below Ground
No Phase Reversal with Inputs 1 V Beyond Supplies
Low Power of 2.75 mA/Amplifier
High Speed and Fast Settling on +5 V:
- **150 MHz –3 dB Bandwidth (G = +1)**
- **170 V/μs Slew Rate**
- **40 ns Settling Time to 0.1%**

Good Video Specifications (R_L = 150 Ω, G = +2)
- **Gain Flatness of 0.1 dB to 12 MHz**
- **0.06% Differential Gain Error**
- **0.15° Differential Phase Error**

Low Distortion
- **–75 dBc Total Harmonic @ 5 MHz**

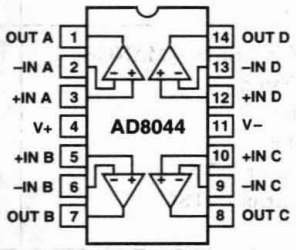
Outstanding Load Drive Capability
- **Drives 30 mA 0.5 V from Supply Rails**

APPLICATIONS

Active Filters
Video Switchers
Distribution Amplifiers
A/D Driver
Professional Cameras
CCD Imaging Systems
Ultrasound Equipment (Multichannel)

CONNECTION DIAGRAM

14-Pin Plastic Mini-DIP and SOIC



TOP VIEW

PRODUCT DESCRIPTION

The AD8044 is a quad low power, voltage feedback, high speed amplifier designed to operate on +3 V, +5 V or ±5 V supplies. It has true single-supply capability with an input voltage range extending 200 mV below the negative rail and within 1 V of the positive rail.

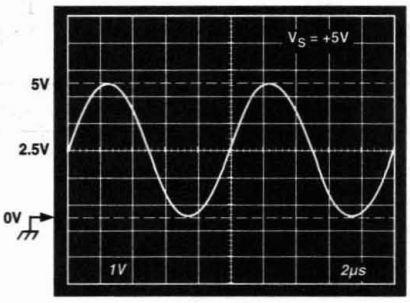


Figure 1. Output Swing: Gain = –1, R_L = 2 kΩ

The output voltage swing extends to within 25 mV of each rail, providing the maximum output dynamic range. Additionally, it features gain flatness of 0.1 dB to 12 MHz while offering differential gain and phase error of 0.04% and 0.22° on a single +5 V supply. This makes the AD8044 useful for video electronics such as cameras, video switchers or any high speed portable equipment. The AD8044's low distortion and fast settling make it ideal for active filter applications.

The AD8044 offers low power supply current of 13.1 mA max and can run on a single +3.3 V power supply. These features are ideally suited for portable and battery powered applications where size and power are critical.

The wide bandwidth of 150 MHz along with 170 V/μs of slew rate on a single +5 V supply make the AD8044 useful in many general purpose, high speed applications where dual power supplies of up to ±6 V and single supplies from +3 V to +12 V are needed. The AD8044 is available in 14-pin plastic DIP and SOIC.

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ORDERING GUIDE

Model	Supply Voltage	Temperature Range	Package Description*
AD8044AN	+5, ±5	–40°C to +85°C	14-Pin Plastic DIP (N-14)
AD8044AN	+3	0°C to +70°C	14-Pin Plastic DIP (N-14)
AD8044AR	+5, ±5	–40°C to +85°C	14-Pin Plastic SOIC (R-14)
AD8044AR	+3	0°C to +70°C	14-Pin Plastic SOIC (R-14)
AD8044AR-REEL			REEL-SOIC (R-14)

*For outline information see Package Information section.

AD8044–SPECIFICATIONS (@ T_A = +25°C, V_S = +5 V, R_L = 2 kΩ to 2.5 V, unless otherwise noted)

Parameter	Conditions	AD8044A Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O < 0.5 V p-p	G = +1	80	150		MHz
Bandwidth for 0.1 dB Flatness	G = +2, R_L = 150 Ω		12		MHz
Slew Rate	G = –1, V_O = 4 V Step	140	170		V/μs
Full Power Response	V_O = 2 V p-p		26		MHz
Settling Time to 1%	G = –1, V_O = 2 V Step		30		ns
Settling Time to 0.1%			40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, G = +2, R_L = 1 kΩ		–75		dB
Input Voltage Noise	f = 10 kHz		16		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz		850		$fA/\sqrt{Hz}$
Differential Gain Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.04		%
Differential Phase Error (NTSC)	G = +2, R_L = 150 Ω to 2.5 V		0.22		Degrees
Crosstalk	f = 5 MHz, R_L = 1 kΩ, G = +2		–60		dB
DC PERFORMANCE					
Input Offset Voltage			1.0	6	mV
	T_{MIN}–T_{MAX}			8	mV
Offset Drift			8		μV/°C
Input Bias Current			2	4.5	μA
	T_{MIN}–T_{MAX}			4.5	μA
Input Offset Current			0.2	1.2	μA
Open-Loop Gain	R_L = 1 kΩ	82	94		dB
	T_{MIN}–T_{MAX}		88		dB
INPUT CHARACTERISTICS					
Input Resistance			225		kΩ
Input Capacitance			1.6		pF
Input Common-Mode Voltage Range			–0.2 to 4		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3.5 V	80	90		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 10 kΩ to 2.5 V		0.03 to 4.975		V
	R_L = 1 kΩ to 2.5 V	0.25 to 4.75	0.075 to 4.91		V
	R_L = 150 Ω to 2.5 V	0.55 to 4.4	0.25 to 4.65		V
Output Current	T_{MIN}–T_{MAX}, V_{OUT} = 0.5 V to 4.5 V		30		mA
Short Circuit Current	Sourcing		45		mA
	Sinking		85		mA
Capacitive Load Drive	G = +2		40		pF
POWER SUPPLY					
Operating Range		3		12	V
Quiescent Current			11	13.1	mA
Power Supply Rejection Ratio	V_S = 0, +5 V, ±1 V	70	80		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTE: For +3 V and ±5 V specifications, request complete data sheet.

Specifications subject to change without notice.

250 MHz, General Purpose Voltage Feedback Op Amps

AD8047/AD8048

FEATURES

Wide Bandwidth	AD8047, G = +1	AD8048, G = +2
Small Signal	250 MHz	260 MHz
Large Signal (2 V p-p)	130 MHz	160 MHz

5.8 mA Typical Supply Current
Low Distortion, (SFDR) Low Noise
–66 dBc typ @ 5 MHz
–54 dBc typ @ 20 MHz
5.2 nV/√Hz (AD8047), 3.8 nV/√Hz (AD8048) Noise
Drives 50 pF Capacitive Load
High Speed
Slew Rate 750 V/μs (AD8047), 1000 V/μs (AD8048)
Settling 30 ns to 0.01%, 2 V Step
±3 V to ±6 V Supply Operation

APPLICATIONS

Low Power ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current to Voltage Conversion
Baseband and Video Communications
Pin Diode Receivers
Active Filters/Integrators

PRODUCT DESCRIPTION

The AD8047 and AD8048 are very high speed and wide bandwidth amplifiers. The AD8047 is unity gain stable. The AD8048 is stable at gains of two or greater. The AD8047 and AD8048, which utilize a voltage feedback architecture, meet the requirements of many applications that previously depended on current feedback amplifiers.

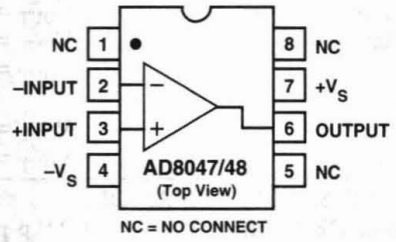
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8047AN	–40°C to +85°C	Plastic DIP	N-8
AD8047AR	–40°C to +85°C	SOIC	R-8
AD8047-EB		Evaluation Board	
AD8048AN	–40°C to +85°C	Plastic DIP	N-8
AD8048AR	–40°C to +85°C	SOIC	R-8
AD8048-EB		Evaluation Board	

*N = Plastic DIP; R= SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SO (R) Packages

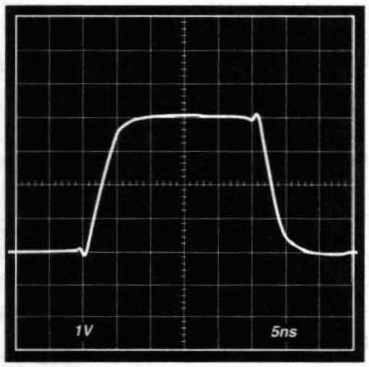


NC = NO CONNECT

A proprietary circuit has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. For the power (6.6 mA max) the AD8047 and AD8048 exhibit fast and accurate pulse response (30 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and low distortion. The AD8047 achieves –54 dBc distortion at 20 MHz and 250 MHz small signal and 130 MHz large signal bandwidths.

The AD8047 and AD8048's low distortion and cap load drive make the AD8047/AD8048 ideal for buffering high speed ADCs. They are suitable for 12 bit/10 MSPS or 8 bit/60 MSPS ADCs. Additionally, the balanced high impedance inputs of the voltage feedback architecture allow maximum flexibility when designing active filters.

The AD8047 and AD8048 are offered in industrial (–40°C to +85°C) temperature ranges and are available in 8-pin plastic DIP and SOIC packages.



AD8047 Large Signal Transient Response, V_O = 4 V p-p, G = +1

AD8047/AD8048–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = 1$ (AD8047); $A_V = 2$ (AD8048), unless otherwise noted)

Parameter	Conditions	AD8047A Min	AD8047A Typ	AD8047A Max	AD8048A Min	AD8048A Typ	AD8048A Max	Units
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	170	250		180	260		MHz
Large Signal[1]	$V_{OUT} = 2$ V p-p	100	130		135	160		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 300$ mV p-p							
	8047, $R_F = 0\ \Omega$; 8048, $R_F = 200\ \Omega$		35			50		MHz
Slew Rate, Average +/–	$V_{OUT} = 4$ V Step	475	750		740	1000		V/μs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step		1.1			1.2		ns
	$V_{OUT} = 4$ V Step		4.3			3.2		ns
Settling Time								
To 0.1%	$V_{OUT} = 2$ V Step		13			13		ns
To 0.01%	$V_{OUT} = 2$ V Step		30			30		ns
HARMONIC/NOISE PERFORMANCE								
2nd Harmonic Distortion	2 V p-p; 20 MHz		–54			–48		dBc
	$R_L = 1$ kΩ		–64			–60		dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz		–60			–56		dBc
	$R_L = 1$ kΩ		–61			–65		dBc
Input Voltage Noise	f = 100 kHz		5.2			3.8		$nV/\sqrt{Hz}$
Input Current Noise	f = 100 kHz		1.0			1.0		$pA/\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 10 MHz		16			11		μV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$, G = +2		0.02			0.01		%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$, G = +2		0.03			0.02		Degree
DC PERFORMANCE[2], $R_L = 150\ \Omega$								
Input Offset Voltage[3]			1	3		1	3	mV
	T_{MIN}–T_{MAX}			4			4	mV
Offset Voltage Drift			±5			±5		μV/°C
Input Bias Current			1	3.5		1	3.5	μA
	T_{MIN}–T_{MAX}			6.5			6.5	μA
Input Offset Current			0.5	2		0.5	2	μA
	T_{MIN}–T_{MAX}			3			3	μA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$ V	74	80		74	80		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	58	62		65	68		dB
	T_{MIN}–T_{MAX}	54			56			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.5			1.5		pF
Input Common-Mode Voltage Range			±3.4			±3.4		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±2.8	±3.0		±2.8	±3.0		V
Output Current			50			50		mA
Output Resistance			0.2			0.2		Ω
Short Circuit Current			130			130		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			5.8	6.6		5.9	6.6	mA
	T_{MIN}–T_{MAX}			7.5			7.5	mA
Power Supply Rejection Ratio		72	78		72	78		dB

NOTES

[1]See Max Ratings and Theory of Operation sections of data sheet.

[2]Measured at $A_V = 50$.

[3]Measured with respect to the inverting input.

Specifications subject to change without notice.

ANALOG DEVICES

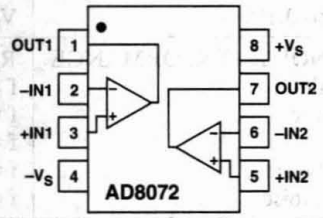
Low Cost Video Amplifiers

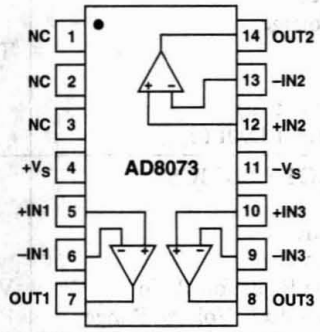
AD8072/AD8073

FEATURES
Very Low Cost
Good Video Specifications (R_L = 150 Ω)
Gain Flatness of 0.1 dB to 10 MHz
0.05% Differential Gain Error
0.1° Differential Phase Error
Low Power
3.5 mA/Amplifier Supply Current
Operates on Single +5 V to +12 V Supply
High Speed
100 MHz, –3 dB Bandwidth (G = +2)
500 V/μs Slew Rate
Fast Settling Time of 25 ns (0.1%)
Easy to Use
30 mA Output Current
Output Swing to 1.3 V of Rails on Single +5 V Supply

APPLICATIONS
Video Line Driver
Computer Video Plug-In Boards
RGB or S-Video Amplifier in Component Systems

FUNCTIONAL BLOCK DIAGRAMS





NC = NO CONNECT

PRODUCT DESCRIPTION

The AD8072 (dual) and AD8073 (triple) are low cost, current feedback amplifiers intended for high volume, cost sensitive applications. In addition to being low cost, these amplifiers deliver solid video performance into a 150 Ω load while consuming only 3.5 mA per amplifier of supply current. Furthermore, the AD8073 is three amplifiers in a single 14-pin narrow-body SOIC package. This makes it ideal for applications where small size is essential. Each amplifier's inputs and output are accessible providing added gain setting flexibility.

These devices provide 30 mA of output current per amplifier, and are optimized for driving one back terminated video load (150 Ω) each. These current feedback amplifiers feature gain flatness of 0.1 dB to 10 MHz while offering differential gain and phase error of 0.05% and 0.1°. This makes the AD8072 and AD8073 ideal for business and consumer video electronics.

Both will operate from a single +5 V to +12 V power supply. The outputs of each amplifier swing to within 1.3 volts of either supply rail to accommodate video signals on a single +5 V supply.

The high bandwidth of 100 MHz, 500 V/μs of slew rate, along with settling to 0.1% in 25 ns, make the AD8072 and AD8073 useful in many general purpose, high speed applications where a single +5 V or dual power supplies up to ±6 V are needed. The AD8072 is available in 8-pin plastic DIP and SOIC packages while the AD8073 is available in 14-pin plastic DIP and SOIC packages. Both operate over the commercial temperature range of 0°C to +70°C.

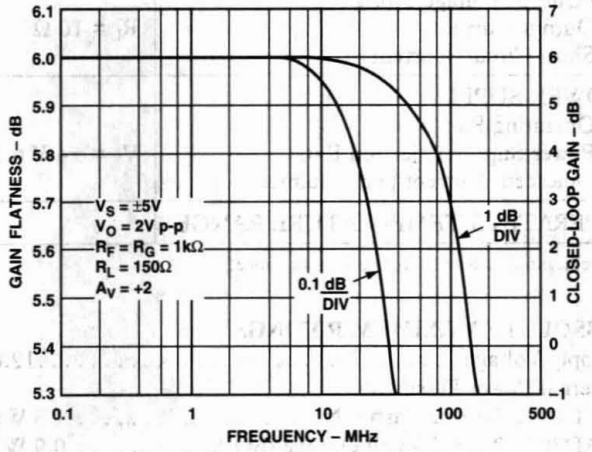


Figure 1. Large Signal Frequency Response

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD8072JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD8072JR	0°C to +70°C	8-Pin SOIC	SO-8
AD8072JR-REEL	0°C to +70°C	Reel 8-Pin SOIC	SO-8
AD8073JN	0°C to +70°C	14-Pin Plastic DIP	N-14
AD8073JR	0°C to +70°C	14-Pin Narrow SOIC	R-14
AD8073JR-REEL	0°C to +70°C	Reel 14-Pin SOIC	R-14

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD8072/AD8073–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ T_A = +25°C, V_S = ±5 V, R_L = 150 Ω, unless otherwise noted)

Parameter	Conditions	AD8072J/AD8073J Min	Typ	Max	Units
DYNAMIC PERFORMANCE	R_F = 1 kΩ				
–3 dB Bandwidth, Small Signal	No Peaking, G = +2	80	100		MHz
0.1 dB Bandwidth, Small Signal	No Peaking, G = +2	8	10		MHz
Slew Rate	V_O = 4 V Step		500		V/µs
Settling Time to 0.1%	V_O = 2 V Step		25		ns
DISTORTION/NOISE PERFORMANCE	R_F = 1 kΩ				
Differential Gain	f = 3.58 MHz, G = +2		0.05	0.15	%
Differential Phase	f = 3.58 MHz, G = +2		0.1	0.3	Degrees
Crosstalk	f = 5 MHz		60		dB
Input Voltage Noise	f = 10 kHz		3		$nV/\sqrt{Hz}$
Input Current Noise	f = 10 kHz (±I_{IN})		6		$pA/\sqrt{Hz}$
DC PERFORMANCE					
Transimpedance			0.3		MΩ
Input Offset Voltage			2	6	mV
	T_{MIN} to T_{MAX}			8	mV
Offset Drift			11		µV/°C
Input Bias Current (±)			4	12	µA
Input Bias Current Drift (±)			12		nA/°C
INPUT CHARACTERISTICS					
–Input Resistance			120		Ω
+Input Resistance			1		MΩ
Input Capacitance			1.6		pF
Common-Mode Rejection Ratio	V_{CM} = –3.8 V to +3.8 V		56		dB
Input Common-Mode Voltage Range			±3.8		V
OUTPUT CHARACTERISTICS					
+Output Voltage Swing		3	3.3		V
–Output Voltage Swing		2.25	3		V
Output Current	R_L = 10 Ω		30		mA
Short Circuit Current			80		mA
POWER SUPPLY					
Operating Range			±2.5 to ±6		V
Power Supply Rejection Ratio	V_S = ±4 V to ±6 V		70		dB
Quiescent Current per Amplifier			3.5	5	mA
OPERATING TEMPERATURE RANGE		0		+70	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
AD8072 8-Lead Plastic (N) . . . . . 1.3 Watts
AD8072 8-Lead Small Outline (SO-8) . . . . . 0.9 Watts
AD8073 14-Lead Plastic (N) . . . . . 1.6 Watts
AD8073 14-Lead Small Outline (R) . . . . . 1.0 Watts
Input Voltage (Common Mode) . . . . . ±V_S
Differential Input Voltage . . . . . ±1.25 V
Output Short Circuit Duration . . . . . Observe Power Derating Curves
Storage Temperature Range
N & R Packages . . . . . –65°C to +125°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 140°C/Watt
14-Pin Plastic Package: θ_{JA} = 75°C/Watt
14-Pin SOIC Package: θ_{JA} = 120°C/Watt

Low Cost 250 mA Output Single-Supply Amplifier

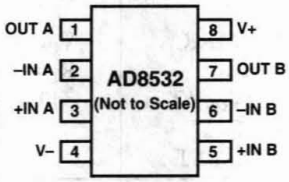
AD8532

FEATURES
Single-Supply Operation: 2.7 Volts to 6 Volts
High Output Current: ±250 mA
Low Supply Current: 1.4 mA
Wide Bandwidth: 3 MHz
Slew Rate: 5 V/μs
No Phase Reversal
Low Input Currents
Unity Gain Stable

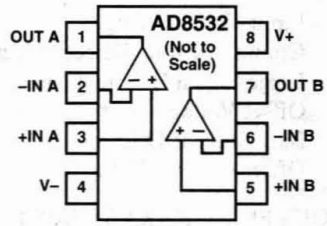
APPLICATIONS
Multimedia Audio
LCD Driver
ASIC Input or Output Amplifier
Headphone Driver

PIN CONFIGURATIONS

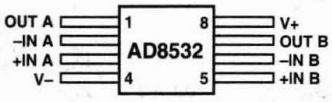
8-Lead Narrow Body SO
(R Suffix)



8-Lead Epoxy DIP
(N Suffix)



8-Lead TSSOP
(RU Suffix)



GENERAL DESCRIPTION

The AD8532 is a rail-to-rail input and output single-supply amplifier featuring 250 mA output drive current. This high output current makes the AD8532 excellent for driving either resistive or capacitive loads. AC performance is very good with 3 MHz bandwidth, 5 V/μs slew rate and low distortion. AD8532s are guaranteed to operate from a +3 volt single supply as well as a +5 volt supply.

The very low input bias currents enable the AD8532 to be used in integrators and diode amplification. Supply current is only 1.4 mA at 5 volts allowing low current applications to control high current loads.

Applications include audio amplification for computers, sound ports, sound cards and set-top boxes. AD8532s are also stable and capable of driving heavy capacitive loads, such as those found in LCDs.

The ability to swing rail-to-rail at the inputs and outputs enables designers to buffer CMOS DACs, ASICs or other wide output swing devices in single-supply systems.

The AD8532 is specified over the extended industrial (–40°C to +85°C) temperature range. It is available in 8-pin plastic DIPs, SO-8 and 8-lead TSSOP surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD8532AR	–40°C to +85°C	8-Pin SOIC	SO-8
AD8532AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD8532ARU[2]	–40°C to +85°C	8-Pin TSSOP	RU-8

NOTES
[1]For outline information see Package Information section.
[2]Available in 2,500 piece reels only.

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AD8532–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				25	mV
		$-40°C \le T_A \le +85°C$			30	mV
Input Bias Current	I_B			5	50	pA
		$-40°C \le T_A \le +85°C$			60	pA
Input Offset Current	I_{OS}			1	25	pA
		$-40°C \le T_A \le +85°C$			30	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	38	47		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 V to 4.5 V	20	60		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40°C \le T_A \le +85°C$		20		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA	4.9	4.94		V
		$-40°C \le T_A \le +85°C$	4.85			V
Output Voltage Low	V_{OL}	I_L = 10 mA		50	100	mV
		$-40°C \le T_A \le +85°C$			125	mV
Output Current	I_{OUT}			±250		mA
Closed Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		40		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 6 V	45	50		dB
Supply Current	I_{SY}	V_O = 0 V		1.4	2.5	mA
		$-40°C \le T_A \le +85°C$			3.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		5		V/µs
Full-Power Bandwidth	BW_p	1% Distortion		350		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	φo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		45		nV/√Hz
Voltage Noise Density	e_n	f = 10 kHz		30		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, V_{CM} = 1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 6 V	45	50		dB
Supply Current	I_{SY}	V_O = 0 V		1.2	2	mA
		$-40°C \le T_A \le +85°C$			2.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		3.5		V/µs
Settling Time	t_S	To 0.01%		1.4		µs
Gain Bandwidth Product	GBP			2.2		MHz
Phase Margin	φo			70		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 2 kΩ		65		dB

Specifications subject to change without notice.

Ultralow Distortion, Wide Bandwidth Voltage Feedback Op Amps

AD9631/AD9632

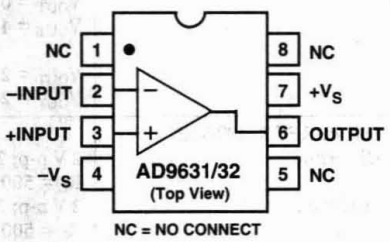
FEATURES

	AD9631, G = +1	AD9632, G = +2
Wide Bandwidth		
Small Signal	320 MHz	250 MHz
Large Signal (4 V p-p)	175 MHz	180 MHz

Ultralow Distortion (SFDR), Low Noise
–113 dBc typ @ 1 MHz
–95 dBc typ @ 5 MHz
–72 dBc typ @ 20 MHz
+46 dBm 3rd Order Intercept @ 25 MHz
7.0 nV/$\sqrt{\text{Hz}}$ Spectral Noise Density
High Speed
Slew Rate 1300 V/μs
Settling 16 ns to 0.01%, 2 V Step
±3 V to ±5 V Supply Operation
17 mA Supply Current

FUNCTIONAL BLOCK DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q), and SO (R) Packages



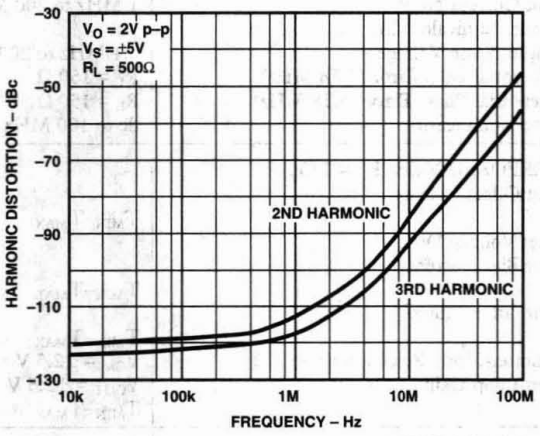


Figure 1. AD9631 Harmonic Distortion vs. Frequency, G = +1

PRODUCT DESCRIPTION

The AD9631 and AD9632 are very high speed and wide bandwidth amplifiers. They are an improved performance alternative to the AD9621 and AD9622. The AD9631 is unity gain stable. The AD9632 is stable at gains of two or greater. Utilizing a voltage feedback architecture, the AD9631/AD9632's exceptional settling time, bandwidth, and low distortion meet the requirements of many applications which previously depended on current feedback amplifiers. Its classical op amp structure works much more predictably in many designs.

A proprietary design architecture has produced an amplifier that combines many of the best characteristics of both current feedback and voltage feedback amplifiers. The AD9631 and AD9632 exhibit exceptionally fast and accurate pulse response (16 ns to 0.01%) as well as extremely wide small signal and large signal bandwidth and ultralow distortion. The AD9631 achieves –72 dBc at 20 MHz and 320 MHz small signal and 175 MHz large signal bandwidths.

These characteristics position the AD9631/AD9632 ideally for driving flash as well as high resolution ADCs. Additionally, the balanced high impedance inputs of the voltage feedback architecture allow maximum flexibility when designing active filters.

The AD9631 is offered in industrial (–40°C to +85°C) and military (–55°C to +125°C) temperature ranges and the AD9632 in industrial. Industrial versions are available in plastic DIP and SOIC; MIL versions are packaged in cerdip.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9631AN	–40°C to +85°C	Plastic DIP	N-8
AD9631AR	–40°C to +85°C	SOIC	R-8
AD9631(SMD)	–55°C to +125°C	Cerdip	Q-8
AD9631-EB		Evaluation Board	
AD9632AN	–40°C to +85°C	Plastic DIP	N-8
AD9632AR	–40°C to +85°C	SOIC	R-8
AD9632-EB		Evaluation Board	

*N = Plastic DIP; Q = Cerdip; R= SOIC (Small Outline Integrated Circuit). For outline information see Package Information section.

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AD9631/AD9632–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V; $R_{LOAD} = 100\ \Omega$; $A_V = 1$ (AD9631); $A_V = 2$ (AD9632), unless otherwise noted)

Parameter	Conditions	AD9631A Min	AD9631A Typ	AD9631A Max	AD9632A Min	AD9632A Typ	AD9632A Max	Units
DYNAMIC PERFORMANCE								
Bandwidth (–3 dB)								
Small Signal	$V_{OUT} \le 0.4$ V p-p	220	320		180	250		MHz
Large Signal[1]	$V_{OUT} = 4$ V p-p	150	175		155	180		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT} = 300$ mV p-p							
	9631, $R_F = 140\ \Omega$; 9632, $R_F = 425\ \Omega$		130			130		MHz
Slew Rate, Average +/–	$V_{OUT} = 4$ V Step	1000	1300		1200	1500		V/μs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step		1.2			1.4		ns
	$V_{OUT} = 4$ V Step		2.5			2.1		ns
Settling Time								
To 0.1%	$V_{OUT} = 2$ V Step		11			11		ns
To 0.01%	$V_{OUT} = 2$ V Step		16			16		ns
HARMONIC/NOISE PERFORMANCE								
2nd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–64	–57		–54	–47	dBc
	$R_L = 500\ \Omega$		–72	–65		–72	–65	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz, $R_L = 100\ \Omega$		–76	–69		–74	–67	dBc
	$R_L = 500\ \Omega$		–81	–74		–81	–74	dBc
3rd Order Intercept	25 MHz		+46			+41		dBm
Noise Figure	$R_S = 50\ \Omega$		18			14		dB
Input Voltage Noise	1 MHz to 200 MHz		7.0			4.3		$nV\sqrt{Hz}$
Input Current Noise	1 MHz to 200 MHz		2.5			2.0		$pA\sqrt{Hz}$
Average Equivalent Integrated Input Noise Voltage	0.1 MHz to 200 MHz		100			60		μV rms
Differential Gain Error (3.58 MHz)	$R_L = 150\ \Omega$		0.03	0.06		0.02	0.04	%
Differential Phase Error (3.58 MHz)	$R_L = 150\ \Omega$		0.02	0.04		0.02	0.04	Degree
Phase Nonlinearity	dc to 100 MHz		1.1			1.1		Degree
DC PERFORMANCE[2], $R_L = 150\ \Omega$								
Input Offset Voltage[3]			3	10		2	5	mV
	T_{MIN}–T_{MAX}			13			8	mV
Offset Voltage Drift			±10			±10		μV/°C
Input Bias Current			2	7		2	7	μA
	T_{MIN}–T_{MAX}			10			10	μA
Input Offset Current			0.1	3		0.1	3	μA
	T_{MIN}–T_{MAX}			5			5	μA
Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5$ V	70	90		70	90		dB
Open-Loop Gain	$V_{OUT} = \pm 2.5$ V	46	52		46	52		dB
	T_{MIN}–T_{MAX}	40			40			dB
INPUT CHARACTERISTICS								
Input Resistance			500			500		kΩ
Input Capacitance			1.2			1.2		pF
Input Common-Mode Voltage Range			±3.4			±3.4		V
OUTPUT CHARACTERISTICS								
Output Voltage Range, $R_L = 150\ \Omega$		±3.2	±3.9		±3.2	±3.9		V
Output Current			70			70		mA
Output Resistance			0.3			0.3		Ω
Short Circuit Current			240			240		mA
POWER SUPPLY								
Operating Range		±3.0	±5.0	±6.0	±3.0	±5.0	±6.0	V
Quiescent Current			17	18		16	17	mA
	T_{MIN}–T_{MAX}			21			20	mA
Power Supply Rejection Ratio	T_{MIN}–T_{MAX}	50	60		56	66		dB

NOTES
[1]See Max Ratings and Theory of Operation sections of data sheet.
[2]Measured at $A_V = 50$.
[3]Measured with respect to the inverting input.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... 12.6 V
Voltage Swing × Bandwidth Product ..... 550 V × MHz
Internal Power Dissipation[2]
Plastic Package (N) ..... 1.3 Watts
Small Outline Package (R) ..... 0.9 Watts
Input Voltage (Common Mode) ..... $\pm V_S$
Differential Input Voltage ..... ±1.2 V
Output Short Circuit Duration
..... Observe Power Derating Curves
Storage Temperature Range (N, R) ..... –65°C to +125°C
Operating Temperature Range (A Grade) ..... –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: $\theta_{JA} = 90$°C/Watt
8-Pin SOIC Package: $\theta_{JA} = 140$°C/Watt

ANALOG DEVICES

Closed-Loop High Speed Buffer

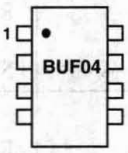
BUF04*

FEATURES
Bandwidth – 110 MHz
Slew Rate – 3000 V/μs
Low Offset Voltage – <1 mV
Very Low Noise – < 4 nV/√Hz
Low Supply Current – 8.5 mA Mux
Wide Supply Range – ±5 V to ±15 V
Drives Capacitive Loads
Pin Compatible with BUF03

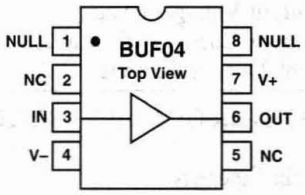
APPLICATIONS
Instrumentation Buffer
RF Buffer
Line Driver
High Speed Current Source
Op Amp Output Current Booster
High Performance Audio
High Speed AD/DA

FUNCTIONAL BLOCK DIAGRAMS

8-Lead Narrow-Body SO
(S Suffix)



Plastic DIP
8-Lead and Cerdip
(P, Z Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The BUF04 is a wideband, closed-loop buffer that combines state of the art dynamic performance with excellent dc performance. This combination enables designers to maximize system performance without any speed versus dc accuracy compromises.

Built on a high speed Complementary Bipolar (CB) process for better power performance ratio, the BUF04 consumes less than 8.5 mA operating from ±5 V or ±15 V supplies. With a 2000 V/μs min slew rate, and 100 MHz gain bandwidth product, the BUF04 is ideally suited for use in high speed applications where low power dissipation is critical.

Full ±10 V output swing over the extended temperature range along with outstanding ac performance and high loop gain accuracy makes the device useful in high speed data acquisition systems.

High slew rate and very low noise and THD, coupled with wide input and output dynamic range, make the BUF04 an excellent choice for video and high performance audio circuits.

The BUF04's inherent ability to drive capacitive loads over a wide voltage and temperature range makes it extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The BUF04 is specified over the extended industrial (–40°C to +85°C) and military (–55°C to +125°C) temperature range. BUF04s are available in plastic and ceramic DIP plus SO-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

***Patent pending.**

10

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
BUF04AZ/883	–55°C to +125°C	Cerdip	Q-8
BUF04GP	–40°C to +85°C	Plastic DIP	N-8
BUF04GS	–40°C to +85°C	SO	SO-8
BUF04GBC	+25°C	DICE	DICE

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

BUF04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.3	1	mV
Input Bias Current	I_B	V_{CM} = 0		0.7	5	µA
Input Voltage Range	V_{CM}			±13		V
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			30		µV/°C
Offset Null Range				±25		mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 150 Ω	±10.5	±11.1		V
Output Current – Continuous	I_{OUT}		±50	±65		mA
Peak Output Current	I_{OUTP}	Note 2		±80		mA
TRANSFER CHARACTERISTICS						
Gain	A_{VCL}	R_L = 2 kΩ	0.995	0.9985	1.005	V/V
Gain Linearity	NL	R_L = 1 kΩ, V_O = ±10 V		0.005		%
		R_L = 150 kΩ		0.008		%
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	76	93		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		6.9	8.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 70 pF	2000	3000		V/µs
Bandwidth	BW	–3 dB, C_L = 20 pF, R_L = ∞		110		MHz
Settling Time		V_{IN} = ±10 V Step to 0.1%		60		ns
Differential Phase		f = 3.58 MHz, R_L = 150 Ω		0.02		Degrees
		f = 4.43 MHz, R_L = 150 Ω		0.03		Degrees
Differential Gain		f = 3.58 MHz, R_L = 150 Ω		0.014		%
		f = 4.43 MHz, R_L = 150 Ω		0.008		%
Input Capacitance				3		pF
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		4		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		2		pA/√Hz

NOTE: For ±5 V specifications, request complete data sheet.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	V_S = ±15 V	1	mV max
	V_{OS}	V_S = ±5 V	2	mV max
Input Bias Current	I_B	V_{CM} = 0 V	5	µA max
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	76	dB
Output Voltage Range	V_O	R_L = 150 Ω	±10.5	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = 2 kΩ	8.5	mA max
Gain	A_{VCL}	V_O = ±10 V, R_L = 2 kΩ	1 ± 0.005	V/V

Specifications subject to change without notice.

ANALOG DEVICES

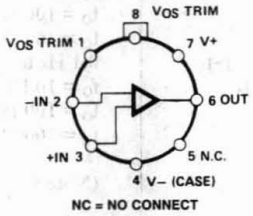
Ultralow Offset Voltage Operational Amplifier

OP07

FEATURES
- Low V_{OS}: 25 μV max
- Low V_{OS} Drift: 0.6 μV/°C max
- Ultra-Stable vs Time: 1.0 μV/Month max
- Low Noise: 0.6 μV p-p max
- Wide Input Voltage Range: ±14 V
- Wide Supply Voltage Range: ±3 V to ±18 V
- Fits 725, 108A/308A, 741, AD510 Sockets
- 125°C Temperature-Tested Dice
- Available in Die Form

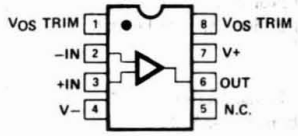
PIN CONNECTIONS

TO-99 (J Suffix)



NC = NO CONNECT

Epoxy Mini-DIP (P Suffix)
8-Pin Hermetic DIP (Z Suffix)
8-Pin SO (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP07 has very low input offset voltage (25 μV max for OP07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP07 also features low input bias current (±2 nA for OP07A) and high open-loop gain (300 V/mV for OP07A). The low offsets and high open-loop gain make the OP07 particularly useful for high-gain instrumentation applications.

The wide input voltage range of ±13 V minimum combined with high CMRR of 110 dB (OP07A) and high input impedance provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP07, even at high gain, combined with the freedom from external nulling have made the OP07 a new industry standard for instrumentation and military applications.

The OP07 is available in five standard performance grades. The OP07A and the OP07 are specified for operation over the full military range of –55°C to +125°C; the OP07E is specified for operation over the 0°C to +70°C range, and OP07C and D over the –40°C to +85°C temperature range.

The OP07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin mini-DIP, and in epoxy 8-pin mini-DIP. It is a direct replacement for 725, 108A, and OP05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP207, a dual OP07, is available for applications requiring close matching of two OP07 amplifiers. For improved specifications, see the OP77/OP177.

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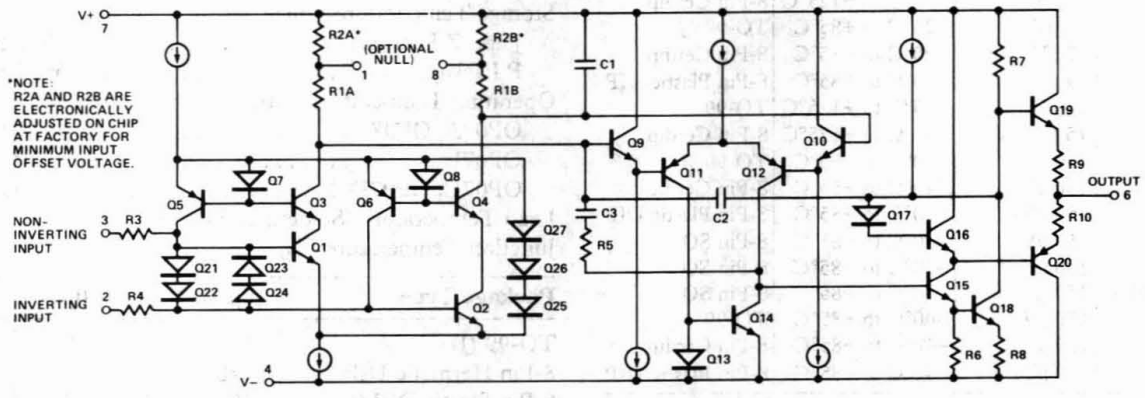


Figure 1. Simplified Schematic

OP07–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP07A Min	OP07A Typ	OP07A Max	OP07 Min	OP07 Typ	OP07 Max	Units
Input Offset Voltage	V_{OS}	(Note 1)		10	25		30	75	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 2)		0.2	1.0		0.2	1.0	µV/Month
Input Offset Current	I_{OS}			0.3	2.0		0.4	2.8	nA
Input Bias Current	I_B			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3]		0.35	0.6		0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[3]		10.3	18.0		10.3	18.0	nV/√Hz
		f_O = 100 Hz[3]		10.0	13.0		10.0	13.0	nV/√Hz
		f_O = 1000 Hz[3]		9.6	11.0		9.6	11.0	nV/√Hz
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz[3]		14	30		14	30	pA p-p
Input Noise Current Density	i_n	f_O = 10 Hz[3]		0.32	0.80		0.32	0.80	pA/√Hz
		f_O = 100 Hz[3]		0.14	0.23		0.14	0.23	pA/√Hz
		f_O = 1000 Hz[3]		0.12	0.17		0.12	0.17	pA/√Hz
Input Resistance—Differential-Mode	R_{IN}	(Note 4)	30	80		20	60		MΩ
Input Resistance—Common-Mode	R_{INCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	110	126		110	126		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		4	10		4	10	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	300	500		200	500		V/mV
		R_L ≥ 500 Ω, V_O = ±0.5 V, V_S = ±3 V[4]	150	400		150	400		V/mV
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±12.5	±13.0		±12.5	±13.0		V
		R_L ≥ 2 kΩ	±12.0	±12.8		±12.0	±12.8		V
		R_L ≥ 1 kΩ	±10.5	±12.0		±10.5	±12.0		V
Slew Rate	SR	R_L ≥ 2 kΩ[3]	0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1[3]	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	P_d	V_S = ±15 V, No Load		75	120		75	120	mW
		V_S = ±3 V, No Load		4	6		4	6	mW
Offset Adjustment Range		R_P = 20 kΩ		±4			±4		mV

NOTES
[1]OP07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
[2]Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. time over expended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µs—refer to typical performance curves. Parameter is sample tested.
[3]Sample tested.
[4]Guaranteed by design.

Specifications subject to change without notice.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
OP07AJ/883C	25 µV	–55°C to +125°C	TO-99
OP07AZ[3]	25 µV	–55°C to +125°C	8-Pin Cerdip
OP07EJ	75 µV	–25°C to +85°C	TO-99
OP07EZ	75 µV	–25°C to +85°C	8-Pin Cerdip
OP07EP	75 µV	–25°C to +85°C	8-Pin Plastic DIP
OP07J/883C	75 µV	–55°C to +125°C	TO-99
OP07Z[3]	75 µV	–55°C to +125°C	8-Pin Cerdip
OP07CJ	150 µV	–40°C to +85°C	TO-99
OP07CZ	150 µV	–40°C to +85°C	8-Pin Cerdip
OP07CP	150 µV	–40°C to +85°C	8-Pin Plastic DIP
OP07CS	150 µV	–40°C to +85°C	8-Pin SO
OP07CS-REEL	150 µV	–40°C to +85°C	8-Pin SO
OP07CS-REEL7[4]	150 µV	–40°C to +85°C	8-Pin SO
OP07DJ	150 µV	–40°C to +85°C	TO-99
OP07DZ	150 µV	–40°C to +85°C	8-Pin Cerdip
OP07DP	150 µV	–40°C to +85°C	8-Pin Plastic DIP

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[4]For availability and burn-in information on SO packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±22 V
Differential Input Voltage ..... ±30 V
Input Voltage[2] ..... ±22 V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  J and Z Packages ..... –65°C to +150°C
  P Package ..... –65°C to +125°C
Operating Temperature Range
  OP07A, OP07 ..... –55°C to +125°C
  OP07E ..... 0°C to +70°C
  OP07C, OP07D ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... +150°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ANALOG DEVICES

Low Noise, Precision Operational Amplifier

OP27

FEATURES

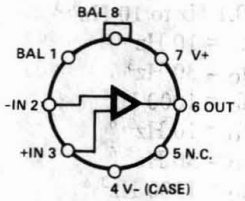
Low Noise
- **80 nV p-p (0.1 Hz to 10 Hz)**
- **3 nV/√Hz**

Low Drift: 0.2 μV/°C
High Speed
- **2.8 V/μs Slew Rate**
- **8 MHz Gain Bandwidth**

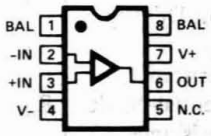
Low V_{OS}: 10 μV
Excellent CMRR: 126 dB at V_{CM} of ±11 V
High Open-Loop Gain: 1.8 Million
Fits 725, OP07, OP05, AD510, AD517, 5534A Sockets
Available in Die Form

PIN CONNECTIONS

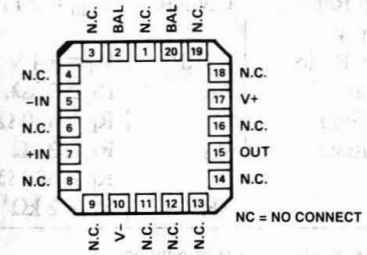
TO-99 (J Suffix)



8-Pin Hermetic DIP (Z Suffix)
Epoxy Mini-DIP (P Suffix)
8-Pin SO (S Suffix)



OP27BRC/883
LCC Package (RC Suffix)



GENERAL DESCRIPTION

The OP27 precision operational amplifier combines the low offset and drift of the OP07 with both high speed and low noise. Offsets down to 25 μV and drift of 0.6 μV/°C maximum make the OP27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5 nV/√Hz, at 10 Hz, a low 1/f noise corner frequency of 2.7 Hz, and high gain (1.8 million), allow accurate high gain amplification of low level signals. A gain-bandwidth product of 8 MHz and a 2.8 V/μs slew rate provides excellent dynamic accuracy in high speed data-acquisition systems.

A low input bias current of ±10 nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20 nA and 15 nA respectively.

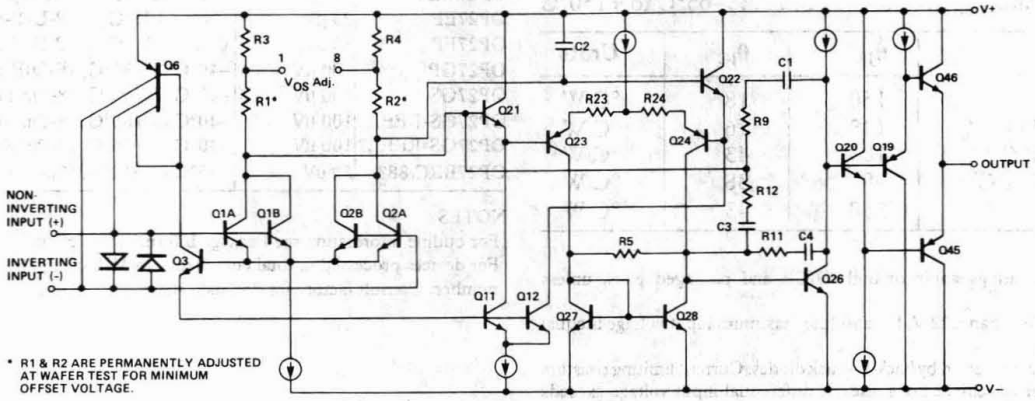
The output stage has good load driving capability. A guaranteed swing of ±10 V into 600 Ω and low output distortion make the OP27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120 dB. These characteristics, coupled with long-term drift of 0.2 μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low cost, high volume production of OP27 is achieved by using an on-chip Zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP27 provides excellent performance in low noise, high accuracy amplification of low level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP27 is a direct replacement for 725, OP06, OP07 and OP45 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.



Simplified Schematic

OP27–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP27A/E Min	OP27A/E Typ	OP27A/E Max	OP27B/F Min	OP27B/F Typ	OP27B/F Max	OP27C/G Min	OP27C/G Typ	OP27C/G Max	Units
Input Offset Voltage	V_{OS}	(Note 1)		10	25		20	60		30	100	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)		0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current	I_{OS}			7	35		9	50		12	75	nA
Input Bias Current	I_B			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3, 5]		0.08	0.18		0.08	0.18		0.09	0.25	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[3]		3.5	5.5		3.5	5.5		3.8	8.0	nV/√Hz
		f_O = 30 Hz[3]		3.1	4.5		3.1	4.5		3.3	5.6	nV/√Hz
		f_O = 1000 Hz[3]		3.0	3.8		3.0	3.8		3.2	4.5	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz[3, 6]		1.7	4.0		1.7	4.0		1.7		pA/√Hz
		f_O = 30 Hz[3, 6]		1.0	2.3		1.0	2.3		1.0		pA/√Hz
		f_O = 1000 Hz[3, 6]		0.4	0.6		0.4	0.6		0.4	0.6	pA/√Hz
Input Resistance Differential-Mode	R_{IN}	(Note 7)	1.3	6		0.94	5		0.7	4		MΩ
Input Resistance Common-Mode	R_{INCM}			3			2.5			2		GΩ
Input Voltage Range	IVR		±11.0	±12.3		±11.0	±12.3		±11.0	±12.3		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V		1	10		1	10		2	20	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	1000	1800		1000	1800		700	1500		
		R_L ≥ 600 Ω, V_O = ±10 V	800	1500		800	1500		600	1500		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12.0	±13.8		±12.0	±13.8		±11.5	±13.5		V
		R_L ≥ 600 Ω	±10.0	±11.5		±10.0	±11.5		±10.0	±11.5		V
Slew Rate	SR	R_L ≥ 2 kΩ[4]	1.7	2.8		1.7	2.8		1.7	2.8		V/µs

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±22 V
Input Voltage[2] ..... ±22 V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage[3] ..... ±0.7 V
Differential Input Current[3] ..... ±25 mA
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP27A, OP27B, OP27C (J, Z, RC) ..... –55°C to +125°C
OP27E, OP27F (J, Z) ..... –25°C to +85°C
OP27E, OP27F (P) ..... 0°C to +70°C
OP27G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]The OP27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current should be limited to 25 mA.
[4]θ_{JA} is specified for worst case mounting conditions i.e., θ_{JA} is specified for device in socket for TO, cerdip, plastic DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Description	Package Option[1]
OP27AJ[2]	25 µV	–55°C to +125°C	TO-99	H-08A
OP27EJ	25 µV	–25°C to +85°C	TO-99	H-08A
OP27BJ/883	60 µV	–55°C to +125°C	TO-99	H-08A
OP27FJ	60 µV	–25°C to +85°C	TO-99	H-08A
OP27GJ	100 µV	–40°C to +85°C	TO-99	H-08A
OP27AZ[2]	25 µV	–55°C to +125°C	Cerdip	Q-8
OP27EZ	25 µV	–25°C to +85°C	Cerdip	Q-8
OP27BZ	60 µV	–55°C to +125°C	Cerdip	Q-8
OP27FZ	60 µV	–25°C to +85°C	Cerdip	Q-8
OP27CZ	100 µV	–40°C to +85°C	Cerdip	Q-8
OP27GZ	100 µV	–40°C to +85°C	Cerdip	Q-8
OP27EP	25 µV	0°C to +70°C	P-DIP-8	N-8
OP27FP	60 µV	0°C to +70°C	P-DIP-8	N-8
OP27GP	100 µV	–40°C to +85°C	P-DIP-8	N-8
OP27GS	100 µV	–40°C to +85°C	8-Pin SO	SO-8
OP27GS-REEL	100 µV	–40°C to +85°C	8-Pin SO	SO-8
OP27GS-REEL7	100 µV	–40°C to +85°C	8-Pin SO	SO-8
OP27BRC/883	60 µV	–55°C to +125°C	20-Contact LCC	RC-20

NOTES
[1]For outline information see Package Information section.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

Low Noise, Precision High Speed Operational Amplifier ($A_{VCL} \geq 5$)

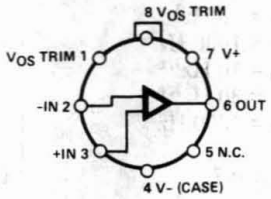
OP37

FEATURES

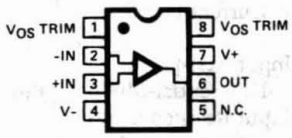
- **Low Noise**
  - **80 nV p-p (0.1 Hz to 10 Hz)**
  - **3 nV/√Hz @ 1 kHz**
- **Low Drift: 0.2 μV/°C**
- **High Speed**
  - **17 V/μs Slew Rate**
  - **63 MHz Gain Bandwidth**
- **Low Input Offset Voltage: 10 μV**
- **Excellent CMRR: 126 dB at V_{CM} of ±11 V**
- **High Open-Loop Gain: 1.8 Million**
- **Replaces 725, OP05, OP06, OP07, AD510, AD517, SE5534 in Gains > 5**
- **Available in Die Form**

PIN CONNECTIONS

TO-99 (J Suffix)



8-Pin Hermetic DIP (Z Suffix)
Epoxy Mini-DIP (P Suffix)
8-Pin SO (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP37 provides the same high performance as the OP27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17 V/μs and gain-bandwidth product to 63 MHz.

The OP37 provides the low offset and drift of the OP07 plus higher speed and lower noise. Offsets down to 25 μV and drift of 0.6 μV/°C maximum make the OP37 ideal for precision instrumentation applications. Exceptionally low noise (e_n = 3.5 nV/√Hz at 10 Hz), a low 1/f noise corner frequency of 2.7 Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low level signals.

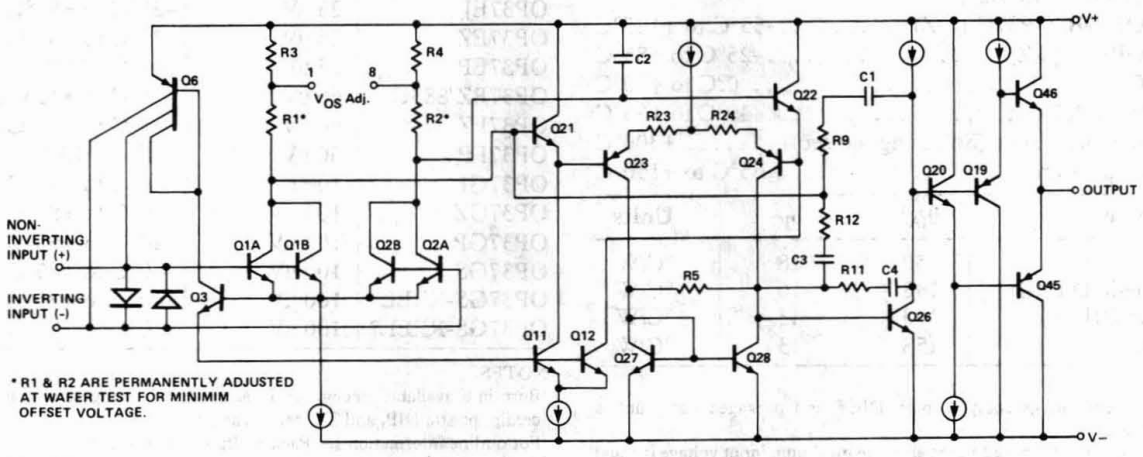
The low input bias current of ±10 nA and offset current of 7 nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to ±20 nA and 15 nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10 V into 600 Ω and low output distortion make the OP37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120 dB. These characteristics, coupled with long-term drift of 0.2 μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low cost, high volume production of the OP37 is achieved by using on-chip Zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP37 brings low noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.



Simplified Schematic

OP37–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37A/E Min	OP37A/E Typ	OP37A/E Max	OP37B/F Min	OP37B/F Typ	OP37B/F Max	OP37C/G Min	OP37C/G Typ	OP37C/G Max	Units
Input Offset Voltage	V_{OS}	(Note 1)		10	25		20	60		30	100	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)		0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current	I_{OS}			7	35		9	50		12	75	nA
Input Bias Current	I_B			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[3, 5]		0.08	0.18		0.08	0.18		0.09	0.25	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[3]		3.5	5.5		3.5	5.5		3.8	8.0	nV/√Hz
		f_O = 30 Hz[3]		3.1	4.5		3.1	4.5		3.3	5.6	nV/√Hz
		f_O = 1000 Hz[3]		3.0	3.8		3.0	3.8		3.2	4.5	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz[3, 6]		1.7	4.0		1.7	4.0		1.7		pA/√Hz
		f_O = 30 Hz[3, 6]		1.0	2.3		1.0	2.3		1.0		pA/√Hz
		f_O = 1000 Hz[3, 6]		0.4	0.6		0.4	0.6		0.4	0.6	pA/√Hz
Input Resistance Differential-Mode	R_{IN}	(Note 7)	1.3	6		0.94	5		0.7	4		MΩ
Input Resistance Common-Mode	R_{INCM}			3			2.5			2		GΩ
Input Voltage Range	IVR		±11.0	±12.3		±11.0	±12.3		±11.0	±12.3		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4 V to ±18 V		1	10		1	10		2	20	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	1000	1800		1000	1800		700	1500		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V	800	1500		800	1500		400	1500		V/mV
		R_L = 600 Ω, V_O = ±1 V, V_S = ±4 V[4]	250	700		250	700		200	500		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12.0	±13.8		±12.0	±13.8		±11.5	±13.5		V
		R_L ≥ 600 Ω	±10.0	±11.5		±10.0	±11.5		±10.0	±11.5		V
Slew Rate	SR	R_L ≥ 2 kΩ[4]	11	17		11	17		11	17		V/µs
Gain Bandwidth Prod.	GBW	f_O = 10 kHz[4]	45	63		45	63		45	63		MHz
		f_O = 1 MHz		40			40			40		MHz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Internal Voltage[2] . . . . . ±22 V
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage[3] . . . . . ±0.7 V
Differential Input Current[3] . . . . . ±25 mA
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range
OP37A, OP37B, OP37C (J, Z) . . . . . –55°C to +125°C
OP37E, OP37F (J, Z) . . . . . –25°C to +85°C
OP37E, OP37F (P) . . . . . 0°C to +70°C
OP37G (P, S, J, Z) . . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C
Junction Temperature . . . . . –65°C to +150°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged pans, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]The OP37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current should be limited to 25 mA.
[4]θ_{JA} is specified for worst case mounting conditions i.e., θ_{JA} is specified for device in socket for TO, cerdip, and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
OP37AJ/883C	25 µV	–55°C to +125°C	H-08A
OP37AZ[3]	25 µV	–55°C to +125°C	Q-8
OP37EJ	25 µV	–25°C to +85°C	H-08A
OP37EZ	25 µV	–25°C to +85°C	Q-8
OP37EP	25 µV	0°C to +70°C	N-8
OP37BZ/883C	60 µV	–55°C to +125°C	Q-8
OP37FZ	60 µV	–25°C to +85°C	Q-8
OP37FP	60 µV	0°C to +70°C	N-8
OP37GJ	100 µV	–40°C to +85°C	H-08A
OP37GZ	100 µV	–40°C to +85°C	Q-8
OP37GP	100 µV	–40°C to +85°C	N-8
OP37GS	100 µV	–40°C to +85°C	SO-8
OP37GS-REEL	100 µV	–40°C to +85°C	SO-8
OP37GS-REEL7	100 µV	–40°C to +85°C	SO-8

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

High Speed, Fast Settling Precision Operational Amplifier

OP42

FEATURES

Fast
- Slew Rate: 50 V/μs min
- Settling Time (0.01%): 1 μs max
- Gain-Bandwidth Product: 10 MHz typ

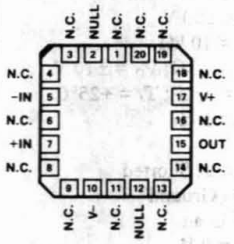
Precise
- Common-Mode Rejection: 88 dB min
- Open-Loop Gain: 500 V/mV min
- Offset Voltage: 750 μV max
- Bias Current: 200 pA max

Excellent Radiation Hardness

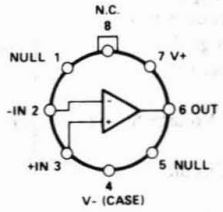
Available in Die Form

PIN CONNECTIONS

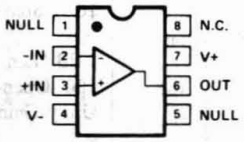
20-Contact LCC (RC Suffix)



TO-99 (J Suffix)



8-Pin Cerdip (Z Suffix), Epoxy Mini-DIP (P Suffix) and 8-Pin SO (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP42 is a fast precision JFET-input operational amplifier. Similar in speed to the OP17, the OP42 offers a symmetric 58 V/μs slew rate and is internally compensated for unity-gain operation. OP42 speed is achieved with a supply current of less than 6 mA. Unity-gain stability, a wide full-power bandwidth of 900 kHz, and a fast settling time of 800 ns to 0.01% make the OP42 an ideal output amplifier for fast digital-to-analog converters.

Equal attention was given to both speed and precision in the OP42 design. Its tight 750 μV maximum input offset voltage combined with well-controlled drift of less than 10 μV/°C eliminates the need for external nulling in many circuits. The OP42's common-mode rejection of 88 dB minimum over a ±11 V input voltage range is exceptional for a high speed amplifier. High CMR combined with a minimum 500 V/mV gain into 10 kΩ load ensures excellent linearity in both noninverting and inverting gain configurations. The low input bias and offset currents provided by the JFET input stage suit the OP42 for use in high speed sample and hold circuits, peak detectors, and log amplifiers. Excellent radiation hardness characteristics make the OP42 ideal for military and aerospace applications.

The OP42 conforms to the standard 741 pinout with nulling to V–. The OP42 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement. In circuits without nulling, the OP42 offers an upgrade for designs using the OP16, OP17, LT1022, LT1056, and HA2510.

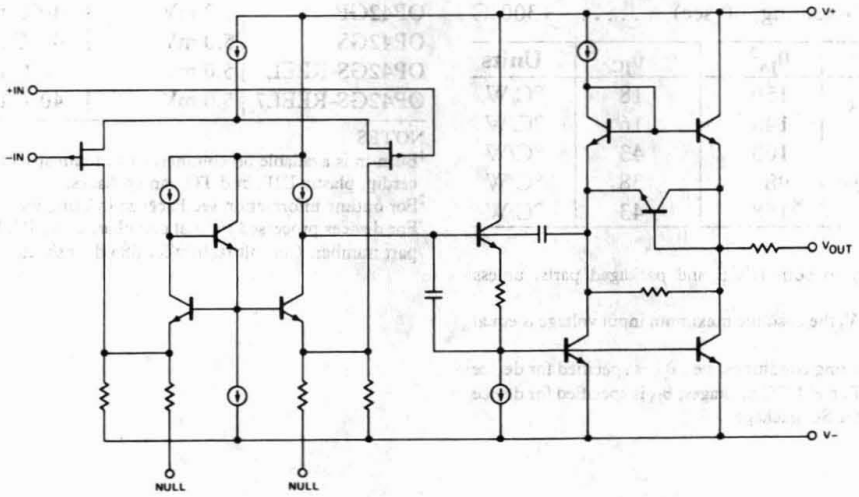


Figure 1. Simplified Schematic

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

OP42–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	OP42E Min	OP42E Typ	OP42E Max	OP42F Min	OP42F Typ	OP42F Max	OP42G Min	OP42G Typ	OP42G Max	Units
Offset Voltage	V_{OS}			0.3	0.75		0.4	1.5		1.5	5.0	mV
Input Bias Current	I_B	V_{CM} = 0 V; T_J = +25°C		80	200		130	250		130	250	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V; T_J = +25°C		4	40		6	50		6	50	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5		±11	+12.5		±11	+12.5		V
			±11	–12.0		±11	–12.0		±11	–12.0		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	88	98		80	92		80	92		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10 V to ±20 V		9	40		12	50		12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	500	900		500	900		500	900		V/mV
		R_L = 2 kΩ; V_O = ±10 V	200	260		200	260		200	260		
		R_L = 1 kΩ; T_J = +25°C	100	170		100	170		100	170		
Output Voltage Swing	V_O	R_L = 1 kΩ	±11.5	+12.5		±11.5	+12.5		±11.5	+12.5		V
			±11.5	–11.9		±11.5	–11.9		±11.5	–11.9		V
Short-Circuit		Output Shorted to Ground	±20	+33	±60	±20	+33	±60	±20	+33	±60	mA
			±20	–28	±60	±20	–28	±60	±20	–28	±60	mA
Supply Current	I_{SY}	No Load V_O = 0 V		5.1	6.0		5.1	6.5		5.1	6.5	mA
Slew Rate	SR		50	58		40	50		40	50		V/µs
Full-Power Bandwidth	BW_p	(Note 2)	750	900		600	800		600	800		kHz
Gain-Bandwidth Product	GBW	f_O = 10 kHz		10			10			10		MHz
Settling Time	t_S	10 V Step 0.01%[3]		0.8	1.0		0.9	1.2		0.9	1.2	µs
Overload Recovery Time	t_{OR}			700			700			700		ns
Phase Margin	ϕ_o	0 dB Gain		47			47			47		degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift		9			9			9		dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable[4]	100	300		100	300		100	300		pF

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±20 V
Input Voltage[2] ..... ±20 V
Differential Input Voltage[2] ..... 40 V
Output Short-Circuit Duration ..... Indefined
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range
OP42A (J, Z) ..... –55°C to +125°C
OP42E, F (J, Z) ..... –25°C to +85°C
OP42G ..... –40°C to +85°C
Junction Temperature ..... –65°C to +175°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package	θ_{JA}[3]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO-99, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
OP42AJ[3]	1.0 mV	–55°C to +125°C	TO-99
OP42AZ[3]	1.0 mV	–55°C to +125°C	Cerdip
OP42ARC/883	1.0 mV	–55°C to +125°C	LCC
OP42EJ	0.75 mV	–25°C to +85°C	TO-99
OP42EZ	0.75 mV	–25°C to +85°C	Cerdip
OP42FJ	1.5 mV	–25°C to +85°C	TO-99
OP42FZ	1.5 mV	–25°C to +85°C	Cerdip
OP42GP	5.0 mV	–40°C to +85°C	Plastic DIP
OP42GS	5.0 mV	–40°C to +85°C	SOIC
OP42GS-REEL	5.0 mV	–40°C to +85°C	SOIC
OP42GS-REEL7	5.0 mV	–40°C to +85°C	SOIC

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

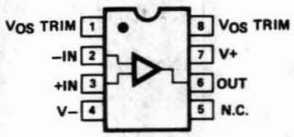
Next Generation OP07, Ultralow Offset Voltage Operational Amplifier

OP77

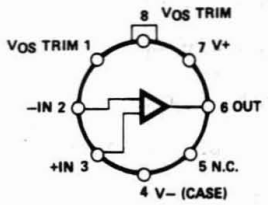
FEATURES
Outstanding Gain Linearity
Ultrahigh Gain: 5000 V/mV min
Low V_{OS} Over Temperature: 60 μV max
Excellent TCV_{OS}: 0.3 μV/°C max
High PSRR: 3 μV/V max
Low Power Consumption: 60 mW max
Fits OP07, 725, 108A/308A, 741 Sockets
Available in Die Form

PIN CONFIGURATIONS

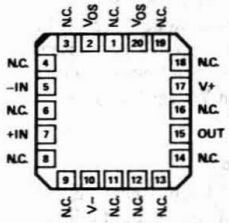
Epoxy Mini-DIP (P Suffix)
8-Pin Hermetic DIP (Z Suffix)
8-Pin SO (S Suffix)



TO-99 (J Suffix)



OP77BRC/883 LCC (RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP77 significantly advances the state-of-the-art in precision op amps. The OP77's outstanding gain of 10,000,000 or more is maintained over the full ±10 V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications. Low initial V_{OS} drift and rapid stabilization time, combined with only 50 mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3 μV/°C maximum and the low V_{OS} of 25 μV maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3 μV/V (110 dB) and CMRR of 1.0 μV/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP77 ideally suited for high-resolution instrumentation and other tight error budget systems.

This product is available in six standard grades and five standard packages: the TO-99 can, the 8-pin mini-DIP in ceramic, SO or epoxy, and the 20-contact LCC.

The OP77 is a direct or upgrade replacement for the OP07, 05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot. For higher precision performance refer to OP177.

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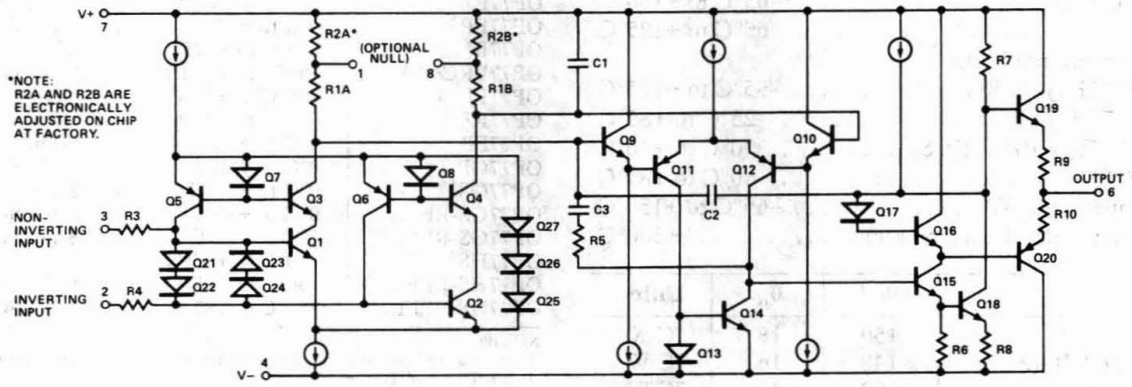


Figure 1. Simplified Schematic

OP77–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP77A Min	OP77A Typ	OP77A Max	OP77B Min	OP77B Typ	OP77B Max	Units
Input Offset Voltage	V_{OS}			10	25		20	60	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)		0.2			0.2		µV/Mo
Input Offset Current	I_{OS}			0.3	1.5		0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[2]		0.35	0.6		0.35	0.6	µV p-p
		f_O = 10 Hz[2]		10.3	18.0		10.3	18.0	µV p-p
Input Noise Voltage Density	e_n	f_O = 100 Hz[2]		10.0	13.0		10.0	13.0	V/√Hz
		f_O = 1000 Hz[2]		9.6	11.0		9.6	11.0	V/√Hz
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz[2]		14	30		14	30	pA p-p
		f_O = 10 Hz[2]		0.32	0.80		0.32	0.80	pA p-p
Input Noise Current Density	i_n	f_O = 100 Hz[2]		0.14	0.23		0.14	0.23	pA/√Hz
		f_O = 1000 Hz[2]		0.12	0.17		0.12	0.17	pA/√Hz
Input Resistance—Differential-Mode	R_{IN}	(Note 3)	26	45		18.5	45		MΩ
Input Resistance—Common-Mode	R_{INCM}			200			200		GΩ
Input Voltage Range	IVR		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V		0.1	1.0		0.1	1.0	µV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.7	3		0.7	3	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, VO = ±10 V	5000	12000		2000	8000		V/mV
Output Voltage Swing	V_O	R_L ≥ 10 kΩ	±13.5	±14.0		±13.5	±14.0		V
		R_L ≥ 2 kΩ	±12.5	±13.0		±12.5	±13.0		V
		R_L ≥ 1 kΩ	±12.0	±12.5		±12.0	±12.5		V
Slew Rate	SR	R_L ≥ 2 kΩ[2]	0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1[2]	0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O			60			60		Ω
		V_S = ±15 V, No Load		50	60		50	60	mW
Power Consumption	P_d	V_S = ±3 V, No Load		3.5	4.5		3.5	4.5	mW
Offset Adjustment Range		R_P = 20 kΩ		±3			±3		mV

NOTES
[1]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
[2]Sample tested.
[3]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Differential Input Voltage . . . . . ±30 V
Input Voltage[2] . . . . . ±22 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
J, Z, and RC Packages . . . . . –65°C to +150°C
P Package . . . . . –65°C to +125°C
Operating Temperature Range
OP77A, OP77B (J, Z, RC) . . . . . –55°C to +125°C
OP77E, OP77F (J, Z) . . . . . –25°C to +85°C
OP77E, OP77F, OP77G (P, S) . . . . . 0°C to +70°C
OP77H (P, S) . . . . . –40°C to +85°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE[1]

Model	Temperature Range	Package Option[2]
OP77AJ[3]	–55°C to +125°C	TO-99
OP77AZ[3]	–55°C to +125°C	8-Pin Cerdip
OP77EJ	–25°C to +85°C	TO-99
OP77EZ	–25°C to +85°C	8-Pin Cerdip
OP77EP	0°C to +70°C	8-Pin Plastic DIP
OP77BJ	–55°C to +125°C	TO-99
OP77BRC/883C	–55°C to +125°C	20-Contact LCC
OP77FJ	–25°C to +85°C	TO-99
OP77FZ	–25°C to +85°C	8-Pin Cerdip
OP77FP	0°C to +70°C	8-Pin Plastic DIP
OP77GP	0°C to +70°C	8-Pin Plastic DIP
OP77GS[4]	0°C to +70°C	8-Pin SO
OP77GS-REEL	0°C to +70°C	8-Pin SO
OP77GS-REEL7[4]	0°C to +70°C	8-Pin SO
OP77HS[4]	–40°C to +85°C	8-Pin SO
OP77HS-REEL	–40°C to +85°C	8-Pin SO
OP77HS-REEL7[4]	–40°C to +85°C	8-Pin SO

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in Cerdip, Plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[4]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

Low Power, High Precision Operational Amplifier

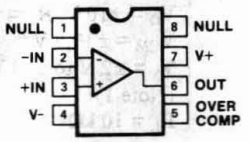
OP97

FEATURES

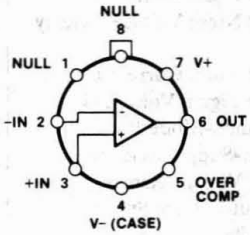
Low Supply Current: 600 μA max
OP07 Type Performance
Offset Voltage: 20 μV max
Offset Voltage Drift: 0.6 μV/°C max
Very Low Bias Current
+25°C: 100 pA max
–55°C to +125°C: 250 pA max
High Common-Mode Rejection: 114 dB min
Extended Industrial Temperature Range: –40°C to +85°C
Available in Die Form

PIN CONNECTIONS

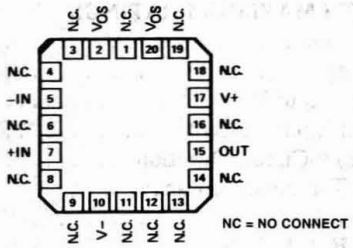
Epoxy Mini-DIP (P Suffix)
8-Pin Hermetic DIP
(Z Suffix)
8-Pin SO (S Suffix)



TO-99 (J Suffix)



OP97ARC/883 LCC
(RC Suffix)



GENERAL DESCRIPTION

The OP97 is a low power alternative to the industry-standard OP07 precision amplifier. The OP97 maintains the standards of performance set by the OP07 while utilizing only 600 μA supply current, less than 1/6 that of an OP07. Offset voltage is an ultra-low 25 μV, and drift over temperature is below 0.6 μV/°C. External offset trimming is not required in the majority of circuits.

Improvements have been made over OP07 specifications in several areas. Notable is bias current, which remains below 250 pA over the full military temperature range. The OP97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

Common-mode rejection and power-supply rejection are also improved with the OP97, at 114 dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from ±2.25 V to ±20 V and the OP97's minimal power requirements combine to make the OP97 a preferred device for portable and battery-powered instruments.

The OP97 conforms to the OP07 pinout, with the null potentiometer connected between Pins 1 and 8 with the wiper to V+. The OP97 will upgrade circuit designs using 725, OP05, OP07, OP12 and 1012-type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

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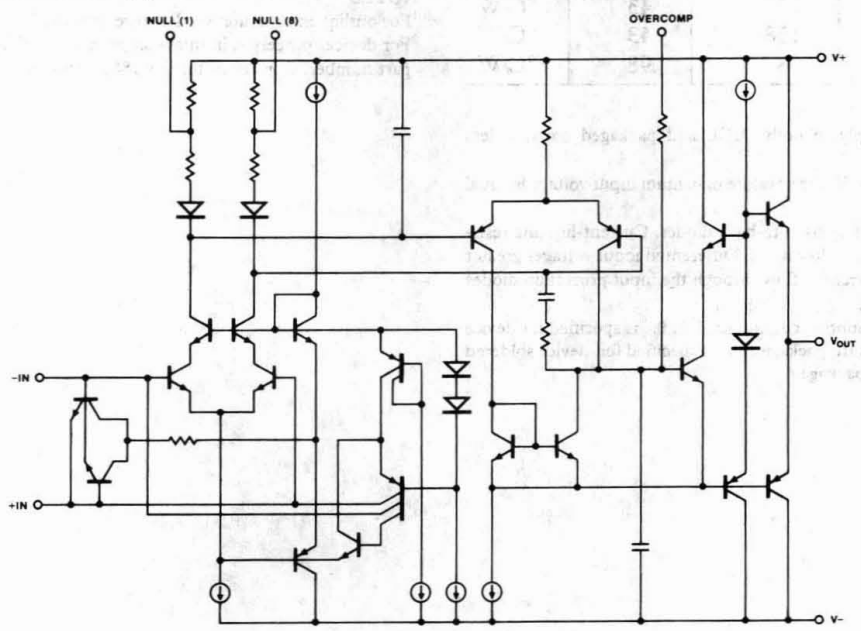


Figure 1. Simplified Schematic

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

OP97–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP97A/E Min	OP97A/E Typ	OP97A/E Max	OP97F Min	OP97F Typ	OP97F Max	Units
Input Offset Voltage	V_{OS}			10	25		30	75	µV
Long-Term Offset Voltage Stability	ΔV_{OS}/Time			0.3			0.3		µV/Month
Input Offset Current	I_{OS}			30	100		30	150	pA
Input Bias Current	I_B			±30	±100		±30	±150	pA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[2]		17	30		17	30	nV/√Hz
		f_O = 1000 Hz[3]		14	22		14	22	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		20			20		fA/√Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V; R_L = 2 kΩ	300	2000		200	2000		V/mV
Common-Mode Rejection	CMR	V_{CM} = ±13.5 V	114	132		110	132		dB
Power-Supply Rejection	PSR	V_S = ±2 V to ±20 V	114	132		110	132		dB
Input Voltage Range	IVR	(Note 1)	±13.5	±14.0		±13.5	±14.0		V
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		V
Slew Rate	SR		0.1	0.2		0.1	0.2		V/µs

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±20 V
Input Voltage[2] ..... ±20 V
Differential Input Voltage[3] ..... ±1 V
Differential Input Current[3] ..... ±10 mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
OP97A (J, Z, RC) ..... –55°C to +125°C
OP97E, F (J, P, Z, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W
20-Contact LCC (RC)	98	98	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3]The OP97's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1 V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.
[4]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
OP97AZ	–55°C to +125°C	8-Pin Cerdip
OP97ARC/883[2]	–55°C to +125°C	20-Contact LCC
OP97EJ	–40°C to +85°C	TO-99
OP97EZ	–40°C to +85°C	8-Pin Cerdip
OP97EP	–40°C to +85°C	8-Pin Plastic DIP
OP97FJ	–40°C to +85°C	TO-99
OP97FZ	–40°C to +85°C	8-Pin Cerdip
OP97FP	–40°C to +85°C	8-Pin Plastic DIP
OP97FS	–40°C to +85°C	8-Pin SOIC
OP97FS-REEL	–40°C to +85°C	8-Pin SOIC
OP97FS-REEL7	–40°C to +85°C	8-Pin SOIC

NOTES
[1]For outline information see Package Information section.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for /883 datasheet.

Low Noise, Low Drift Single-Supply Operational Amplifiers

OP113/OP213/OP413*

FEATURES
Single- or Dual-Supply Operation
Low Noise: 4.7 nV/√Hz @ 1 kHz
Wide Bandwidth: 3.4 MHz
Low Offset Voltage: 100 μV
Very Low Drift: 0.2 μV/°C
Unity Gain Stable
No Phase Reversal

APPLICATIONS
Digital Scales
Multimedia
Strain Gages
Battery Powered Instrumentation
Temperature Transducer Amplifier

GENERAL DESCRIPTION

The OP113 family dual operational amplifier features the lowest noise and drift of any single-supply amplifier. It has been designed for systems with internal calibration. Often these processor based systems are capable of calibrating corrections for offset and gain, but they cannot correct for temperature drifts and noise. Optimized for these parameters, the OP113 family can be used to take advantage of superior analog performance combined with digital correction. Many systems using internal calibration operate from unipolar supplies, usually either +5 volts or +12 volts. The OP113 family is designed to operate from single supplies from +4 volts to +36 volts, and to maintain its low noise and precision performance.

The OP113 family is specified for single +5 volt and dual ±15 volt operation over the XIND—extended industrial (–40°C to +85°C) temperature range. They are available in plastic and ceramic 8-pin DIPs, plus SOIC-8 surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

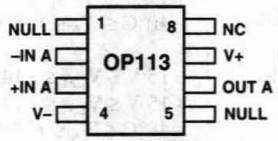
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP113EP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP113ES	–40°C to +85°C	8-Pin SOIC	SO-8
OP113FP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP113FS	–40°C to +85°C	8-Pin SOIC	SO-8
OP213EP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP213ES	–40°C to +85°C	8-Pin SOIC	SO-8
OP213FP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP213FS	–40°C to +85°C	8-Pin SOIC	SO-8
OP413EP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP413ES	–40°C to +85°C	16-Pin SOL	SOL-16
OP413FP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP413FS	–40°C to +85°C	16-Pin SOL	SOL-16

*For outline information see Package Information section.

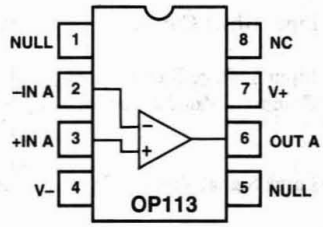
PIN CONNECTIONS

8-Lead Narrow-Body SO
(S Suffix)



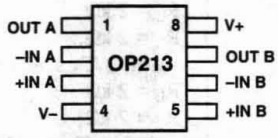
NC = NO CONNECT

8-Lead Epoxy DIP
(P Suffix)
8-Lead Ceramic DIP
(Z Suffix)



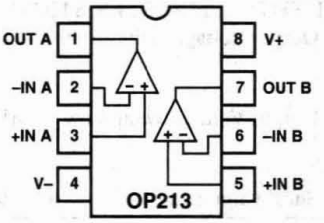
NC = NO CONNECT

8-Lead Narrow-Body SO
(Z Suffix)

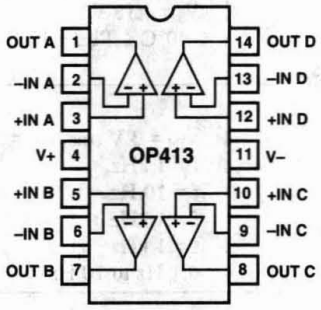


NC = NO CONNECT

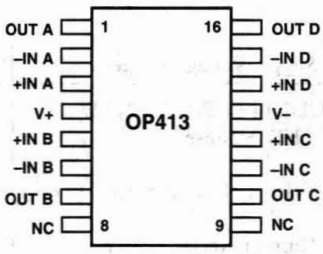
8-Lead Epoxy DIP
(P Suffix)
8-Lead Ceramic DIP
(S Suffix)



14-Lead Epoxy DIP
(P Suffix)
14-Lead Ceramic DIP
(Y Suffix)



16-Lead Narrow-Body SOL
(S Suffix)



NC = NO CONNECT

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*Protected by U.S. Patent No. 5,146,181.

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OP113/OP213/OP413–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	OP113E/OP413E Min	OP113E/OP413E Typ	OP113E/OP413E Max	OP113F/OP413F Min	OP113F/OP413F Typ	OP113F/OP413F Max	Units
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP113			75			150	µV
		–40°C ≤ T_A ≤ +85°C			125			225	µV
		OP213			100			250	µV
		–40°C ≤ T_A ≤ +85°C			150			325	µV
		OP413			125			275	µV
		–40°C ≤ T_A ≤ +85°C			175			350	µV
Input Bias Current	I_B	V_{CM} = 0 V,		240	600			600	nA
		–40°C ≤ T_A ≤ +85°C			700			700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V							
		–40°C ≤ T_A ≤ +85°C			50			50	nA
Input Voltage Range	V_{CM}		–15		+14	–15		+14	V
Common-Mode Rejection	CMR	–15 V ≤ V_{CM} ≤ +14 V	100	116		96			dB
		–15 V ≤ V_{CM} ≤ +14 V,							
		–40°C ≤ T_A ≤ +85°C	97	116		94			dB
Large Signal Voltage Gain	A_{VO}	OP113, OP213, R_L = 600 Ω,							
		–40°C ≤ T_A ≤ +85°C	1	2.4		1			V/µV
		OP413, R_L = 1 kΩ,							
		–40°C ≤ T_A ≤ +85°C	1	2.4		1			V/µV
		R_L = 2 kΩ,							
		–40°C ≤ T_A ≤ +85°C	2	8		2			V/µV
Long-Term Offset Voltage[1]	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	0.8			1.5	µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	R_L = 2 kΩ	+14			+14			V
		R_L = 2 kΩ,							
		–40°C ≤ T_A ≤ +85°C	+13.9			+13.9			V
Output Voltage Swing Low	V_{OL}	R_L = 2 kΩ			–14.5			–14.5	V
		R_L = 2 kΩ,							
		–40°C ≤ T_A ≤ +85°C			–14.5			–14.5	V
Short Circuit Limit	I_{SC}			±40			±40		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±18 V	103	120		100			dB
		V_S = ±2 V to ±18 V							
		–40°C ≤ T_A ≤ +85°C	100	120		97			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 0 V, R_L = ∞,							
		V_S = ±18 V			2			2	mA
		–40°C ≤ T_A ≤ +85°C			2.5			2.5	mA
Supply Voltage Range	V_S		+4		±18	+4		±18	V
AUDIO PERFORMANCE									
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ							
		f = 1 kHz,		0.0009			0.0009		%
Voltage Noise Density	e_n	f = 10 Hz		9			9		nV/√Hz
		f = 1 kHz		4.7			4.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4			0.4		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		120			120		nV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ	0.8	1.2		0.8	1.2		V/µs
Gain Bandwidth Product	GBP			3.4			3.4		MHz
Channel Separation		V_{OUT} = 10 V p-p							
		R_L = 2 kΩ, f = 1 kHz		105			105		dB
Settling Time	t_S	to 0.01%, 0 V to 10 V Step		9			9		µs

NOTES

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at 120°C, with an LTPD of 1.3.

[2]Guaranteed specifications, based on characterization data.

Specifications subject to change without notice.

15 MHz Rail-to-Rail Operational Amplifiers

OP162/OP262/OP462

FEATURES
Rail-to-Rail Output Swing
High Slew Rate: 13 V/μs
Wide Bandwidth: 15 MHz
Low Offset Voltage: 600 μV max
Fast Settling Time
Single-Supply Operation: +3 V to +12 V
Unity-Gain Stable
No Phase Inversion

APPLICATIONS
Portable Instrumentation
Flash ADC Amplifier
Wireless LANs
Direct Access Arrangement
Office Automation

GENERAL DESCRIPTION

The OP162, OP262, and OP462 are single, dual, and quad rail-to-rail output amplifiers with a unity gain bandwidth of 15 MHz. They are designed with greater output swings than standard high speed op amps so that they can be used in applications that require greater dynamic range or greater control than standard video amplifiers provide.

The OP162 family is specified over the extended industrial (–40°C to +125°C) temperature range. Both single and dual amplifiers are available in 8-pin plastic DIP and SO-8 surface mount packages. The OP462 is available in 14-pin plastic DIPs and narrow SO-14 packages. Consult the factory for availability of the OP462 in the 14-lead TSSOP packages.

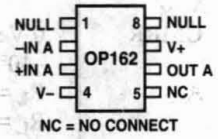
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP162GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP162GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP262GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP262GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP462GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP462GS	–40°C to +125°C	14-Pin SOIC	SO-14
OP462HRU	–40°C to +125°C	14-Pin TSSOP	RU-14

*For outline information see Package Information section.

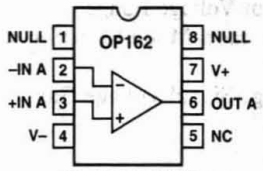
PIN CONFIGURATIONS

8-Lead Narrow-Body SO (S Suffix)



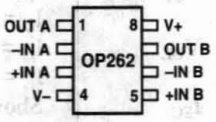
NC = NO CONNECT

8-Lead Epoxy DIP (P Suffix)

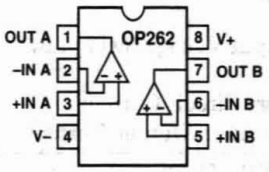


NC = NO CONNECT

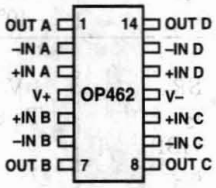
8-Lead Narrow-Body SO (S Suffix)



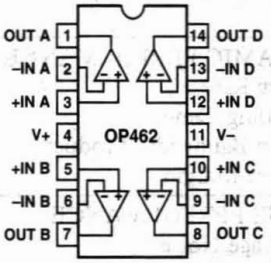
8-Lead Epoxy DIP (P Suffix)



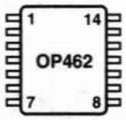
14-Lead Narrow-Body SO (S Suffix)



14-Lead Epoxy DI (P Suffix)



14-Lead TSSOP (RU Suffix)



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OP162/OP262/OP462–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G			600	µV
		–40°C ≤ T_A ≤ +125°C			800	µV
Offset Voltage	V_{OS}	OP462H, –40°C ≤ T_A ≤ +125°C			2	mV
Input Bias Current	I_B				600	nA
		–40°C ≤ T_A ≤ +125°C			650	nA
Input Offset Current	I_{OS}				±25	nA
		–40°C ≤ T_A ≤ +125°C			±40	nA
Input Voltage Range	V_{CM}		0		+4	V
Common-Mode Rejection	CMRR	0 V ≤ V_{CM} ≤ +4.0 V,				
		–40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ		30		V/mV
		R_L = 10 kΩ	65	88		V/mV
		R_L = 10 kΩ, –40°C ≤ T_A ≤ +125°C	40			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 1		1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C	4.95			V
		I_L = 5 mA	4.85			V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C			50	mV
		I_L = 5 mA			150	mV
Short Circuit Current	I_{SC}	Short to Ground		±80		mA
Maximum Output Current	I_{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +7 V,		120		dB
		–40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V		500	650	µA
		–40°C ≤ T_A ≤ +125°C			800	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	1 V < V_{OUT} < 4 V, R_L =10 kΩ		10		V/µs
Settling Time	t_S	To 0.01%		900		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	ϕ_m			62		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		10		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		pA/√Hz

Specifications subject to change without notice.

Bipolar/JFET, Audio Operational Amplifier

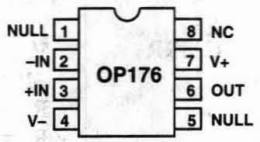
OP176*

FEATURES
Low Noise: 6 nV/√Hz
High Slew Rate: 25 V/μs
Wide Bandwidth: 10 MHz
Low Supply Current: 2.5 mA
Low Offset Voltage: 1 mV
Unity Gain Stable
SO-8 Package

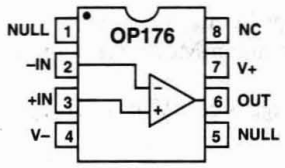
APPLICATIONS
Line Driver
Active Filters
Fast Amplifiers
Integrators

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)



8-Lead Epoxy DIP (P Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP176 is a low noise, high output drive op amp that features the Butler Amplifier front-end. This new front-end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals previous audio amplifiers, but at much lower supply currents.

Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than 200 μV. This allows the OP176 to be used in many dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP176 is specified over the extended industrial (–40°C to +85°C) temperature range. OP176s are available in both plastic DIP and SO-8 packages. SO-8 packages are available in 2500 piece reels. Many audio amplifiers are not offered in SO-8 surface mount packages for a variety of reasons, however, the OP176 was designed so that it would offer full performance in surface mount packaging.

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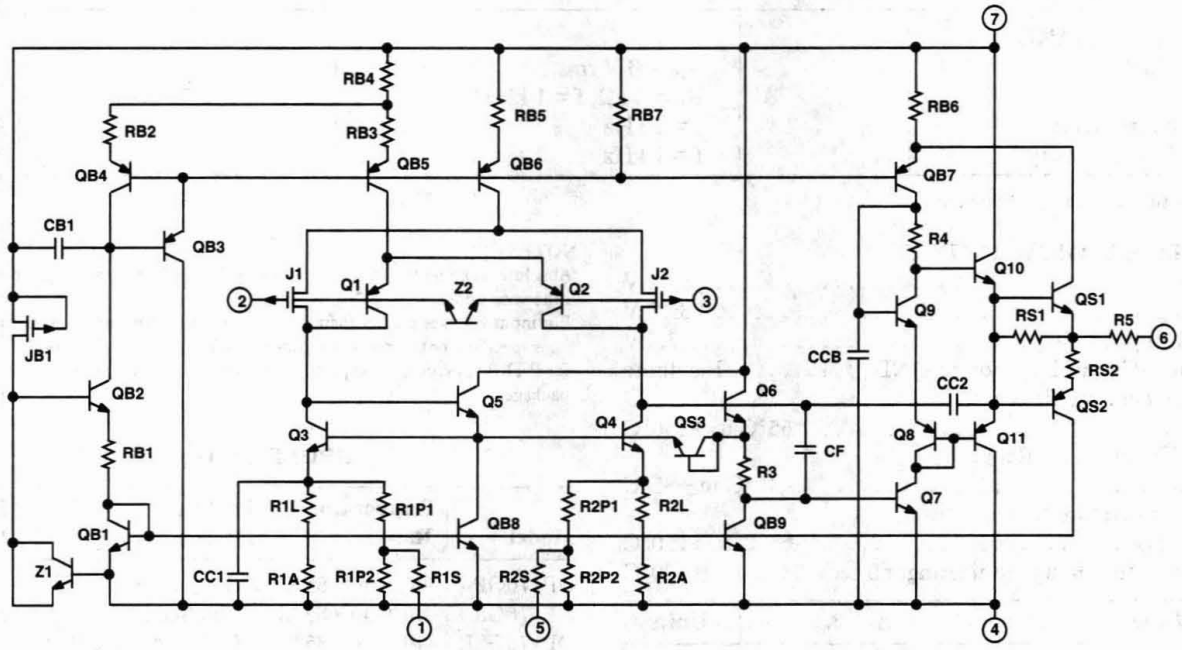
*Protected by U.S. Patent No. 5101126.



Simplified Schematic

OP176–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
Offset Voltage	V_{OS}	–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 0 V			350	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C			400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±50	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C			±100	nA
Input Voltage Range	V_{CM}		–10.5		+10.5	V
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V, –40°C ≤ T_A ≤ +85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	175			V/mV
		R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	–13.5		+13.5	V
		R_L = 600 Ω, V_S = ±18 V	–14.8		+14.8	V
Output Short Circuit Current	I_{SC}		±25	±50		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	86	108		dB
		–40°C ≤ T_A ≤ +85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C			2.5	mA
Supply Current	I_{SY}	V_S = ±22 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C			2.75	mA
Supply Voltage Range	V_S		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	25		V/µs
Gain Bandwidth Product	GBP			10		MHz
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz		0.001		%
Voltage Noise Density	e_n	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.5		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
OP176G . . . . . –40°C to +85°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For input voltages greater than ±7.5 V limit input current to less than 5 mA.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP176GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP176GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP176GSR	–40°C to +85°C	SO-8 Reel, 2500 Pieces	
OP176GBC	+25°C	DICE	

*For outline information see Package Information section.

ANALOG DEVICES

Ultraprecision Operational Amplifier

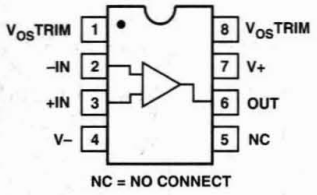
OP177

FEATURES

Ultralow Offset Voltage:
T_A = +25°C: 10 μV max
–55°C ≤ T_A ≤ +125°C: 20 μV max
Outstanding Offset Voltage Drift: 0.1 μV/°C max
Excellent Open-Loop Gain and Gain Linearity:
12 V/μV typ
CMRR: 130 dB min
PSRR: 120 dB min
Low Supply Current: 2.0 mA max
Fits Industry Standard Precision Op Amp Sockets (OP07/OP77)

PIN CONNECTIONS

Epoxy Mini-DIP
(P Suffix)
8-Pin Hermetic DIP
(Z-Suffix)
8-Pin SO
(S-Suffix)



GENERAL DESCRIPTION

The OP177 features the highest precision performance of any op amp currently available. Offset voltage of the OP177 is only 10 μV max at room temperature and 20 μV max over the full military temperature range of –55°C to +125°C. The ultralow V_{OS} of the OP177, combines with its exceptional offset voltage drift (TCV_{OS}) of 0.1 μV/°C max, to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP177's open-loop gain of 12 V/μV is maintained over the full ±10 V output range. CMRR of 130 dB min, PSRR of 120 dB min, and maximum supply current of 2 mA are just a few examples of the excellent performance of this operational amplifier. The OP177's combination of outstanding specifications insure accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

The OP177 is offered in both the –55°C to +125°C military, and the –40°C to +85°C extended industrial temperature ranges. This product is available in 8-pin ceramic and epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO) and the Leadless Chip Carrier (LCC) packages.

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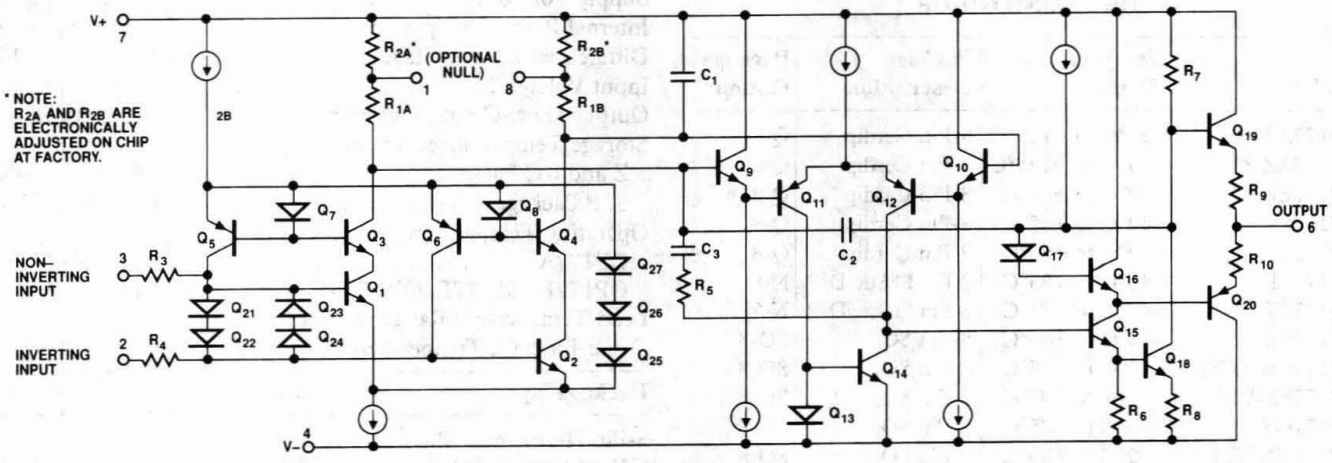


Figure 1. Simplified Schematic

OP177–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	OP177E Min	OP177E Typ	OP177E Max	OP177F Min	OP177F Typ	OP177F Max	OP177G Min	OP177G Typ	OP177G Max	Units
Input Offset Voltage	V_{OS}			4	10		10	25		20	60	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)		0.2			0.3			0.4		µV/Mo
Input Offset Current	I_{OS}			0.3	1.0		0.3	1.5		0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.0	1.5	–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_n	f_o = 1 Hz to 100 Hz[2]		118	150		118	150		118	150	nV rms
Input Noise Current	i_n	f_o = 1 Hz to 100 Hz[2]		3	8		3	8		3	8	pA rms
Input Resistance Differential-Mode	R_{IN}	(Note 3)	26	45		26	45		18.5	45		MΩ
Input Resistance Common-Mode	R_{INCM}			200			200			200		GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13 V	130	140		130	140		115	140		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V	120	125		115	125		110	120		dB
Large Signal Voltage Gain	A_{VO}	$R_L \geq 2$ kΩ, V_O = ±10 V[5]	5000	12000		5000	12000		2000	6000		V/mV
Output Voltage Swing	V_O	$R_L \geq 10$ kΩ	±13.5	±14.0		±13.5	±14.0		±13.5	±14.0		V
		$R_L \geq 2$ kΩ	±12.5	±13.0		±12.5	±13.0		±12.5	±13.0		V
		$R_L \geq 1$ kΩ	±12.0	±12.5		±12.0	±12.5		±12.0	±12.5		V
Slew Rate	SR	$R_L \geq 2$ kΩ[2]	0.1	0.3		0.1	0.3		0.1	0.3		V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1[2]	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open-Loop Output Resistance	R_O			60			60			60		Ω
Power Consumption	P_D	V_S = ±15 V, No Load		50	60		50	60		50	60	mW
		V_S = ±3 V, No Load		3.5	4.5		3.5	4.5		3.5	4.5	mW
Supply Current	I_{SY}	V_S = ±15 V, No Load		1.6	2.0		1.6	2.0		1.6	2.0	mA
Offset Adjustment Range		R_P = 20 kΩ		±3			±3			±3		mV

NOTES

[1]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0 µV.

[2]Sample tested.

[3]Guaranteed by design.

[4]Guaranteed by CMRR test condition.

[5]To insure high open-loop gain throughout the ±10 V output range, A_{VO} is tested at –10 V ≤ V_O ≤ 0 V, 0 V ≤ V_O ≤ +10 V, and –10 V ≤ V_O ≤ +10 V.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP177AZ	–55°C to +125°C	8-Pin Cerdip	Q-8
OP177AZ/883C	–55°C to +125°C	8-Pin Cerdip	Q-8
OP177EZ	–40°C to +85°C	8-Pin Cerdip	Q-8
OP177FZ	–40°C to +85°C	8-Pin Cerdip	Q-8
OP177GZ	–40°C to +85°C	8-Pin Cerdip	Q-8
OP177FP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP177GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP177FS	–40°C to +85°C	8-Pin SO	SO-8
OP177FS-REEL	–40°C to +85°C	8-Pin SO	SO-8
OP177FS-REEL7	–40°C to +85°C	8-Pin SO	SO-8
OP177GS	–40°C to +85°C	8-Pin SO	SO-8
OP177GS-REEL	–40°C to +85°C	8-Pin SO	SO-8
OP177GS-REEL7	–40°C to +85°C	8-Pin SO	SO-8

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22 V
Internal Power Dissipation[1] . . . . . 500 mW
Differential Input Voltage . . . . . ±30 V
Input Voltage . . . . . ±22 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Z and RC Packages . . . . . –65°C to +150°C
  S, P Package . . . . . –65°C to +125°C
Operating Temperature Range
  OP177A . . . . . –55°C to +125°C
  OP177E, OP177F, OP177G . . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C
DICE Junction Temperature (T_J) . . . . . –65°C to +150°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES

[1]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

5 MHz Single-Supply Operational Amplifiers

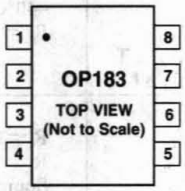
OP183/OP283

FEATURES
Single-Supply – +3 Volts to +36 Volts
Wide Bandwidth – 5 MHz
Low Offset Voltage – <1 mV
High Slew Rate – 10 V/μs
Low Noise – 10 nV/√Hz
Unity-Gain Stable
Input and Output Range Includes GND
No Phase Reversal

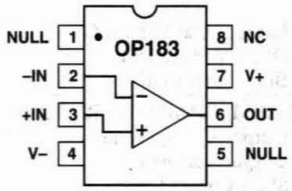
APPLICATIONS
Multimedia
Telecom
ADC Buffers
Wide Band Filters
Microphone Preamplifiers

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)

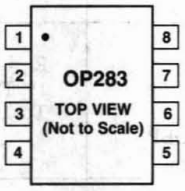


8-Lead Epoxy DIP (P Suffix)

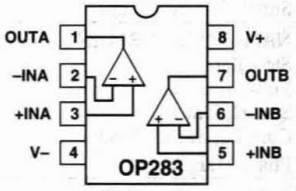


NC = NO CONNECT

8-Lead Narrow-Body SO (S Suffix)



8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

The OP183 is a single-supply, 5 MHz bandwidth amplifier with slew rates of 10 V/μs. The OP283 is a dual version. Both can operate from voltages as low as 3 volts and up to 36 volts. This combination of slew rate and bandwidth yields excellent single-supply ac performance making them ideally suited for telcom and multimedia audio applications.

In addition to its ac characteristics, the OP183 family provides good dc performance with guaranteed 1 mV offset. Noise is a respectable 10 nV/√Hz. Supply current is only 1.2 mA per amplifier.

These amplifiers are well suited for single-supply applications that require moderate bandwidths even when used in high gain configurations. This makes them useful in filters and instrumentation. Their output drive capability and very wide full power bandwidth make them a good choice for multimedia headphone drivers or microphone input amplifiers.

The OP183 and OP283 are available in 8-pin plastic DIP and SO-8 surface mount packages. They are specified over the extended industrial (–40°C to +85°C) temperature range.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP183GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP183GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP283GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP283GS	–40°C to +85°C	8-Pin SOIC	SO-8

*For outline information see Package Information section.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Input Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±7 V
Output Short-Circuit Duration to GND ..... Indefinite
Storage Temperature Range
P, S Package ..... –65°C to +150°C
Operating Temperature Range
OP183/OP283G ..... –40°C to +85°C
Junction Temperature Range
P, S Package ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 Sec) ..... +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±7 V, the absolute maximum input voltage is equal to the supply voltage. Maximum input current should not exceed 2 mA.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC packages.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

OP183/OP283–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		0.025	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,		350	600	nA
		−40°C ≤ T_A ≤ +85°C		430	750	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V, V_{OUT} = 2.5 V,				nA
		−40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.5 V				
		−40°C ≤ T_A ≤ +85°C	70	104		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 3.8 V	100			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			−1.6		nA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	+4.0	4.22		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		50	75	mV
Short Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +4 V to +6 V,				
		−40°C ≤ T_A ≤ +85°C	70	104		dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V,				
		−40°C ≤ T_A ≤ +85°C		1.2	1.5	mA
Supply Voltage Range	V_S		+3		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	5	10		V/µs
Full-Power Bandwidth	BWp	1% Distortion		>50		kHz
Settling Time	t_S	To 0.01%		1.5		µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			46		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 2.5 V		10		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		0.3	1.0	mV
		−40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,		350	600	nA
		−40°C ≤ T_A ≤ +85°C			750	nA
Input Offset Current	I_{OS}	V_{CM} = 1.5 V, V_{OUT} = 1.5 V,				
		−40°C ≤ T_A ≤ +85°C		11	±50	nA
Input Voltage Range			0		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.5 V,				
		−40°C ≤ T_A ≤ +85°C	70	103		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.2 ≤ V_O ≤ 1.8 V	100	260		V/mV
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to GND	+2.0	2.25		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to GND		90	125	mV
Short Circuit Limit	I_{SC}	Source		25		mA
		Sink		30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.5 V to +3.5 V,				
		−40°C ≤ T_A ≤ +85°C	60	113		dB
Supply Current/Amplifier	I_{SY}	−40°C ≤ T_A ≤ +85°C, V_O = 1.5 V		1.2	1.5	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			5		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz, V_{CM} = 1.5 V		10		nV/√Hz

Specifications subject to change without notice.

Precision Rail-to-Rail Input & Output Operational Amplifiers

OP184/OP284/OP484

FEATURES
Single-Supply Operation
Wide Bandwidth: 4 MHz
Low Offset Voltage: 65 μV
Unity-Gain Stable
High Slew Rate: 4.0 V/μs
Low Noise: 3.9 nV/√Hz

APPLICATIONS
Battery Powered Instrumentation
Power Supply Control and Protection
Telecom
DAC Output Amplifier
ADC Input Buffer

GENERAL DESCRIPTION

The OP184/OP284/OP484 are single, dual and quad single-supply, 4 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from +3 to +36 (or ±1.5 to ±18) volts and will function with a single supply as low as +1.5 volts.

These amplifiers are superb for single applications requiring both ac and precision dc performance. The combination of bandwidth, low noise and precision makes the OP184/OP284/OP484 useful in a wide variety of applications, including filters and instrumentation.

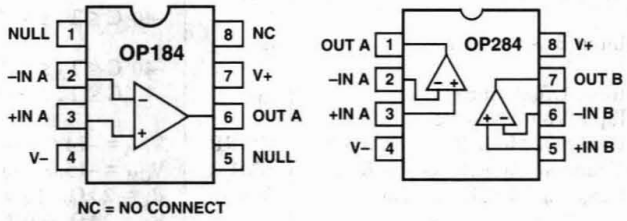
Other applications for these amplifiers include portable telecom equipment, power supply control and protection, and as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

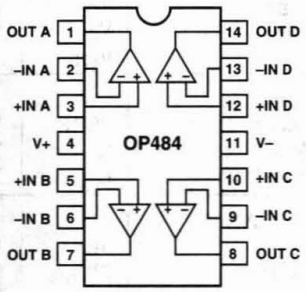
The OP184/OP284/OP484 are specified over the HOT extended industrial (–40°C to +125°C) temperature range. The single and dual OP284 are available in 8-pin plastic DIP plus SO surface mount packages. The quad OP484 is available in 14-pin plastic DIPs and 14-lead narrow-body SO packages.

PIN CONFIGURATIONS

8-Lead Epoxy DIP (P Suffix)
8-Lead SO (S Suffix)



14-Lead Epoxy DIP (P Suffix)
14-Lead Narrow-Body SO (S Suffix)



10

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP184EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP184ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP184ES-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP184ES-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP184FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP184FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP184FS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP184FS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP284EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP284ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP284ES-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP284ES-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP284FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP284FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP284FS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP284FS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP484EP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP484ES	–40°C to +125°C	14-Pin SOIC	SO-14
OP484ES-REEL	–40°C to +125°C	14-Pin SOIC	SO-14
OP484FP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP484FS	–40°C to +125°C	14-Pin SOIC	SO-14
OP484FS-REEL	–40°C to +125°C	14-Pin SOIC	SO-14

*For outline information see Package Information section.

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OP184/OP284/OP484–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, V_{CM} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage "184/284E" Grade	V_{OS}	Note 1			100	µV
		–40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage "184/284F" Grade	V_{OS}				175	µV
		–40°C ≤ T_A ≤ +125°C			375	µV
Offset Voltage "484E" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage "484F" Grade	V_{OS}				250	µV
		–40°C ≤ T_A ≤ +125°C			500	µV
Input Bias Current	I_B			80	300	nA
		–40°C ≤ T_A ≤ +125°C			500	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			–15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –14.0 V to +14.0 V, –40°C ≤ T_A ≤ +125°C	86	90		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15.0 V to +15.0 V	80			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, –10 V ≤ V_O ≤ +10 V	150	1000		V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +125°C	75			V/mV
Offset Voltage Drift "E" Grade	$\Delta V_{OS}/\Delta T$			0.2	2.00	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	+14.8			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			–14.875	V
Output Current	I_{OUT}		±10			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18 V, –40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, –40°C ≤ T_A ≤ +125°C			1.75	mA
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, –40°C ≤ T_A ≤ +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.0		V/µs
Full-Power Bandwidth	BW_p	1% Distortion, R_L = 2 kΩ, V_O = 29 V p-p		35		kHz
Setting Time	t_S	To 0.01%, 10 V Step		4		µs
Gain Bandwidth Product	GBP			4.25		MHz
Phase Margin	Øo			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 100 Hz		0.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage "284E" Grade	V_{OS}	Note 1			65	µV
		–40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage "284F" Grade	V_{OS}				125	µV
		–40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage "484E" Grade	V_{OS}				75	µV
		–40°C ≤ T_A ≤ +125°C			175	µV
Offset Voltage "484F" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			450	µV
Input Bias Current	I_B			60	300	nA
		–40°C ≤ T_A ≤ +125°C			500	nA
Input Offset Current	I_{OS}			2	50	nA
		–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	60			dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.0 V to 4.0 V, –40°C ≤ T_A ≤ +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 1 V ≤ V_O ≤ 4 V	50	240		V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +125°C	25			V/mV

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

Micropower Single-Supply Rail-to-Rail Input/Output Op Amps

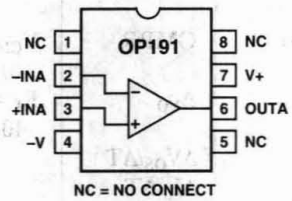
OP191/OP291/OP491

FEATURES
Single-Supply Operation: 2.7 V to 12 V
Wide Input Voltage Range
Rail-to-Rail Output Swing
Low Supply Current: 300 μA/Amp
Wide Bandwidth: 3 MHz
Slew Rate: 0.5 V/μs
Low Offset Voltage: 700 μV
No Phase Reversal

APPLICATIONS
Industrial Process Control
Battery Powered Instrumentation
Power Supply Control and Protection
Telecom
Remote Sensors
Low Voltage Strain Gage Amplifiers
DAC Output Amplifier

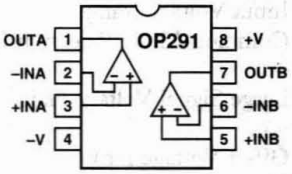
PIN CONFIGURATIONS

8-Lead Narrow-Body SO (S Suffix)
8-Lead Epoxy DIP (P Suffix)

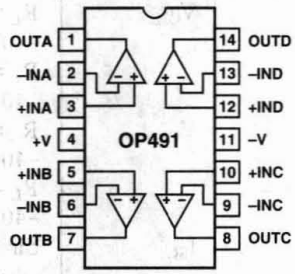


NC = NO CONNECT

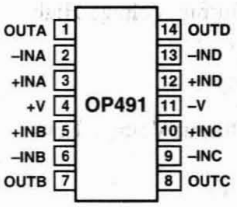
8-Lead Epoxy DIP (P Suffix)
8-Lead Narrow-Body SO (S Suffix)



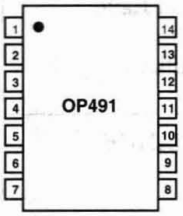
14-Lead Epoxy DIP (P Suffix)



14-Lead SO (S Suffix)



14-Lead TSSOP (RU Suffix)



GENERAL DESCRIPTION

The OP191, OP291 and OP491 are single, dual and quad micropower, single-supply, 3 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. All are guaranteed to operate from a 3 volt single supply as well as ±5 volt dual supplies.

Fabricated on Analog Devices' CBCMOS process, the OP191 family has a unique input stage that allows the input voltage to safely extend 10 volts beyond either supply without any phase inversion or latch-up. The output voltage swings to within millivolts of the supplies and continues to sink or source current all the way to the supplies.

Applications for these amplifiers include portable telecom equipment, power supply control and protection, and interface for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

The OP191/OP291/OP491 are specified over the extended industrial (–40°C to +125°C) temperature range. The OP191 single and OP291 dual amplifiers are available in 8-pin plastic DIPs and SO surface mount packages. The OP491 quad is available in 14-pin DIPs and narrow 14-pin SO packages. Consult factory for OP491 TSSOP availability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP191GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP191GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP191GS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP191GS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP191GBC	+25°C	DICE	
OP291GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP291GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP291GS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP291GS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP291GBC	+25°C	DICE	
OP491GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP491GS	–40°C to +125°C	14-Pin SOIC	SO-14
OP491GS-REEL	–40°C to +125°C	14-Pin SOIC	SO-14
OP491HRU-REEL	–40°C to +125°C	14-Pin TSSOP	RU-14
OP491GBC	+25°C	DICE	

*For outline information see Package Information section.

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OP191/OP291/OP491–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = 0.1 V, V_O = 1.4 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage OP191G	V_{OS}			80	500	µV
		$-40 \le T_A \le +125°C$			1	mV
OP291G/OP491G	V_{OS}			80	700	µV
		$-40 \le T_A \le +125°C$			1.25	mV
Input Bias Current	I_B			30	50	nA
		$-40 \le T_A \le +125°C$			70	nA
Input Offset Current	I_{OS}			0.1	8	nA
		$-40 \le T_A \le +125°C$			16	nA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.9 V	70	90		dB
		$-40 \le T_A \le +125°C$	65	87		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ , V_O = 0.3 V to 2.7 V	25	70		V/mV
		$-40 \le T_A \le +125°C$		50		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1.1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			100		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.95	2.99		V
		–40°C to +125°C	2.90	2.98		V
		R_L = 2 kΩ to GND	2.8	2.9		V
		–40°C to +125°C	2.70	2.8		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		4.5	10	mV
		–40°C to +125°C			35	mV
		R_L = 2 kΩ to V+		40	75	mV
		–40°C to +125°C			130	mV
Short Circuit Limit	I_{SC}	Sink/Source	±8.75	±13.5		mA
		–40°C to +125°C	±6.0	±10.5		mA
Open Loop Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	80	110		dB
		$-40°C \le T_A \le +125°C$	75	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		200	350	µA
		$-40°C \le T_A \le +125°C$		330	480	µA
DYNAMIC PERFORMANCE						
Slew Rate	+SR	R_L = 10 kΩ		0.4		V/µs
Slew Rate	–SR	R_L = 10 kΩ		0.4		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		1.2		kHz
Settling Time	t_S	To 0.01%		22		µs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_O			45		Degrees
Channel Separation	CS	f = 1 kHz, R_L = 10 kΩ		145		dB
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		35		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.8		$pA/\sqrt{Hz}$

Specifications subject to change without notice.

Precision, Micropower Operational Amplifiers

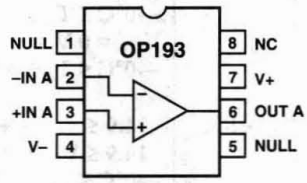
OP193/OP293/OP493*

FEATURES
Operates from +1.7 V to ±18 V
Low Supply Current: 15 μA/Amplifier
Low Offset Voltage: 75 μV
Outputs Sink and Source: ±8 mA
No Phase Reversal
Single or Dual Supply Operation
High Open-Loop Gain: 600 V/mV
Unity-Gain Stable

APPLICATIONS
Digital Scales
Strain Gages
Portable Medical Equipment
Battery Powered Instrumentation
Temperature Transducer Amplifier

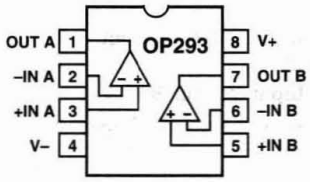
PIN CONFIGURATIONS

8-Lead Epoxy DIP (P Suffix) 8-Lead SO (S Suffix)

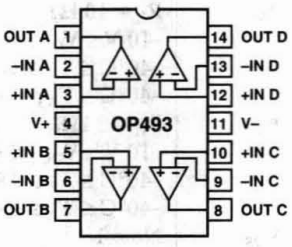


NC = NO CONNECT

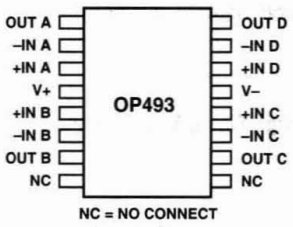
8-Lead Epoxy DIP (P Suffix) 8-Lead SO (S Suffix)



14-Lead Epoxy DIP (P Suffix)



16-Lead Wide Body SOL (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP193 family of single-supply operational amplifiers features a combination of high precision, low supply current and the ability to operate at low voltages. For high performance in single supply systems the input and output ranges include ground, and the outputs swing from the negative rail to within 600 mV of the positive supply. For low voltage operation the OP193 family can operate down to 1.7 volts or ±0.85 volts.

The combination of high accuracy and low power operation make the OP193 family useful for battery powered equipment. Its low current drain and low voltage operation allow it to continue performing long after other amplifiers have ceased functioning either because of battery drain or headroom.

The OP193 family is specified for single +2 volt through dual ±15 volt operation over the HOT (–40°C to +125°C) temperature range. They are available in plastic DIPs, plus SOIC surface mount packages.

***Patent pending.**

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Input Voltage[2] ..... ±18 V
Differential Input Voltage[2] ..... ±18 V
Output Short-Circuit Duration to Gnd ..... Indefinite
Storage Temperature Range
P, S Package ..... –65°C to +150°C
Operating Temperature Range
OP193/OP293/OP493E, F ..... –40°C to +125°C
Junction Temperature Range
P, S Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

[2]For supply voltages less than ±18 V, the input voltage is limited to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC package.

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP193EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP193ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP193ES-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP193ES-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP193FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP193FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP193FS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP193FS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP193GBC	+25°C	DICE	
OP293EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP293ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP293ES-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP293ES-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP293FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP293FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP293FS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP293FS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP293GBC	+25°C	DICE	
OP493EP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP493ES	–40°C to +125°C	16-Pin SOL	SOL-16
OP493ES-REEL	–40°C to +125°C	16-Pin SOL	SOL-16
OP493FP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP493FS	–40°C to +125°C	16-Pin SOL	SOL-16
OP493FS-REEL	–40°C to +125°C	16-Pin SOL	SOL-16
OP493GBC	+25°C	DICE	

*For outline information see Package Information section.

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OP193/OP293/OP493–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	"E" Grade Min	"E" Grade Typ	"E" Grade Max	"F" Grade Min	"F" Grade Typ	"F" Grade Max	Units
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	OP193			75			150	µV
		OP193, –40°C ≤ T_A ≤ +125°C			175			250	µV
		OP293			100			250	µV
		OP293, –40°C ≤ T_A ≤ +125°C			200			350	µV
		OP493			125			275	µV
		OP493, –40°C ≤ T_A ≤ +125°C			225			375	µV
Input Bias Current	I_B	V_{CM} = 0 V,							
		–40°C ≤ T_A ≤ +125°C			15			20	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V,							
		–40°C ≤ T_A ≤ +125°C			2			4	nA
Input Voltage Range	V_{CM}		–14.9		+13.5	–14.9		+13.5	V
Common-Mode Rejection	CMRR	–14.9 ≤ V_{CM} ≤ +14 V	100	116		97	116		dB
		–14.9 ≤ V_{CM} ≤ +14 V,							
		–40°C ≤ T_A ≤ +125°C	97			94			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,							
		–10 V ≤ V_{OUT} ≤ +10 V	500			500			V/mV
		–40°C ≤ T_A ≤ +85°C	300			300			V/mV
		–40°C ≤ T_A ≤ +125°C		300			300		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ,							
		–10 V ≤ V_{OUT} ≤ +10 V	350			350			V/mV
		–40°C ≤ T_A ≤ +85°C	200			200			V/mV
		–40°C ≤ T_A ≤ +125°C		150			150		V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ,							
		–10 V ≤ V_{OUT} ≤ +10 V	200			200			V/mV
		–40°C ≤ T_A ≤ +85°C	125			125			V/mV
		–40°C ≤ T_A ≤ +125°C		100			100		V/mV
Long Term Offset Voltage	V_{OS}	Note 1			150			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		0.2	1.75				µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage Swing High	V_{OH}	I_L = 1 mA	+14.1	14.2		+14.1	14.2		V
		I_L = 1 mA,							
		–40°C ≤ T_A ≤ +125°C	+14.0			+14.0			V
		I_L = 5 mA	+13.9	14.1		+13.9	14.1		V
Output Voltage Swing Low	V_{OL}	I_L = –1 mA		–14.7	–14.6		–14.7	–14.6	V
		I_L = –1 mA,							
		–40°C ≤ T_A ≤ +125°C			–14.4			–14.4	V
		I_L = –5 mA		14.2	–14.1		14.2	–14.1	V
Short Circuit Current	I_{SC}			±25			±25		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±18 V	100	120		97	120		dB
		V_S = ±1.5 V to ±18 V,							
		–40°C ≤ T_A ≤ +125°C	97			94			dB
Supply Current/Amplifier	I_{SY}	–40°C ≤ T_A ≤ +125°C, R_L = ∞							
		V_{OUT} = 0 V, V_S = ±18 V			30			30	µA
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		65			65		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		3			3		µV p-p
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		15			15		V/ms
Gain Bandwidth Product	GBP			35			35		kHz
Channel Separation		V_{OUT} = 10 V p-p,							
		R_L = 2 kΩ, f = 1 kHz		120			120		dB

NOTES

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2]Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

Micropower, Rail-to-Rail Input and Output Operational Amplifiers

OP196/OP296/OP496

FEATURES

Rail-to-Rail Input and Output Swing
Low Power: 60 μA/Amplifier
Gain Bandwidth Product: 450 kHz
Single-Supply Operation: +3 V to +12 V
Low Offset Voltage: 300 μV max
High Open-Loop Gain: 500 V/mV
Unity-Gain Stable
No Phase Reversal

APPLICATIONS

Battery Monitoring
Sensor Conditioners
Portable Power Supply Control
Portable Instrumentation

GENERAL DESCRIPTION

The OP196 family of CBCMOS operational amplifiers features micropower operation and rail-to-rail input and output ranges.

The extremely low power requirements and guaranteed operation from +3 V to +12 V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 26 nV/$\sqrt{\text{Hz}}$ voltage noise density, recommends them for battery-powered audio applications. Capacitive loads to 200 pF are handled without oscillation.

The OP196/OP296/OP496 are specified over the HOT extended industrial (–40°C to +125°C) temperature range. +3 V operation is specified over the 0°C to +125°C temperature range.

The single OP196 and the dual OP296 are available in 8-pin plastic DIP and SO-8 surface mount packages. The quad OP496 is available in 14-pin plastic DIP and narrow SO-14 surface mount packages. Check factory for availability of the OP296 and OP496 in TSSOP packages.

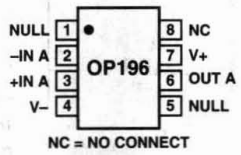
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP196GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP196GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP296GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP296GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP296HRU	–40°C to +125°C	8-Pin TSSOP	RU-8
OP296GBC	+25°C	DICE	
OP496GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP496GS	–40°C to +125°C	14-Pin SOIC	SO-14
OP496HRU	–40°C to +125°C	14-Pin TSSOP	RU-14
OP496GBC	+25°C	DICE	

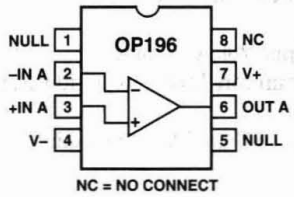
*For outline information see Package Information section.

PIN CONFIGURATIONS

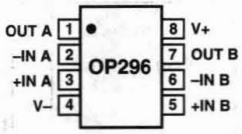
8-Lead Narrow-Body SO (S Suffix)



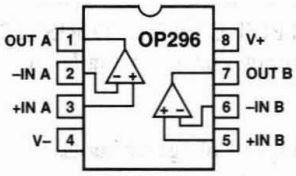
8-Lead Epoxy DIP (P Suffix)



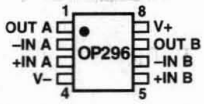
8-Lead Narrow-Body SO (S Suffix)



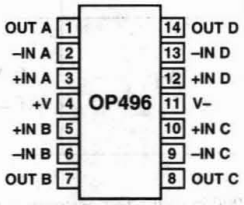
8-Lead Epoxy DIP (P Suffix)



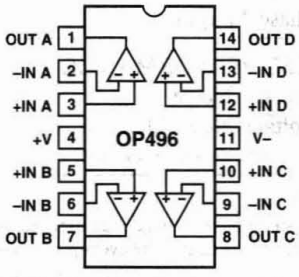
8-Lead TSSOP (RU Suffix)



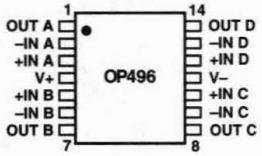
14-Lead Narrow-Body SO (S Suffix)



14-Lead Epoxy DIP (P Suffix)



14-Lead TSSOP (RU Suffix)



10

OP196/OP296/OP496–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP196G, OP296G, OP496G		35	300	µV
		–40°C ≤ T_A ≤ +125°C			650	µV
		OP296H, OP496H			800	µV
		–40°C ≤ T_A ≤ +125°C			1.2	mV
Input Bias Current	I_B	–40°C ≤ T_A ≤ +125°C		±10	±35	nA
Input Offset Current	I_{OS}			±1.5	±5	nA
		–40°C ≤ T_A ≤ +125°C			±15	nA
Input Voltage Range	V_{CM}		0		+5.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5.0 V,				
		–40°C ≤ T_A ≤ +125°C	65			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,				
		0.30 V ≤ V_{OUT} ≤ 4.7 V,				
		–40°C ≤ T_A ≤ +125°C	150	200		V/mV
Long-Term Offset Voltage	V_{OS}	G Grade, Note 1			550	µV
		H Grade, Note 1			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	G Grade, Note 2		1.5		µV/°C
		H Grade, Note 2		2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 µA	4.85	4.92		V
		I_L = 1 mA	4.30	4.56		V
		I_L = 2 mA		4.1		V
Output Voltage Swing Low	V_{OL}	I_L = –100 µA		36	70	mV
		I_L = –1 mA		350	450	mV
		I_L = –2 mA		750		mV
Output Current	I_{OUT}			±4		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±2.5 V ≤ V_S ≤ ±6 V,				
		–40°C ≤ T_A ≤ +125°C	85			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞			60	µA
		–40°C ≤ T_A ≤ +125°C		45	80	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =100 kΩ		0.3		V/µs
Gain Bandwidth Product	GBP			350		kHz
Phase Margin	$ø_m$			47		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		26		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.19		pA/√Hz

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2]Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ANALOG DEVICES

Dual Low Offset, Low Power Operational Amplifier

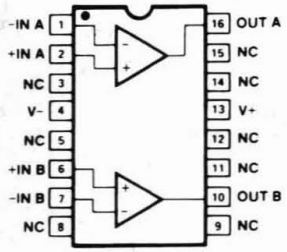
OP200

FEATURES

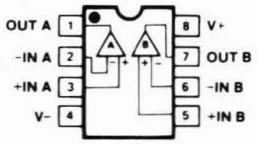
Low Input Offset Voltage: 75 μV max
Low Offset Voltage Drift,
Over −55°C ≤ T_A ≤ +125°C: 0.5 μV/°C max
Low Supply Current (Per Amplifier): 725 μA max
High Open-Loop Gain: 5000 V/mV min
Low Input Bias Current: 2 nA max
Low Noise Voltage Density: 11 nV/√Hz at 1 kHz
Stable With Large Capacitive Loads: 10 nF typ
Pin Compatible to OP14, OP221, LM158, MC1458/1558, and LT1013 With Improved Performance
Available in Die Form

PIN CONFIGURATIONS

16-Pin SOL (S Suffix)



Epoxy Mini-DIP (P Suffix)
8-Pin Hermetic DIP (Z Suffix)



GENERAL DESCRIPTION

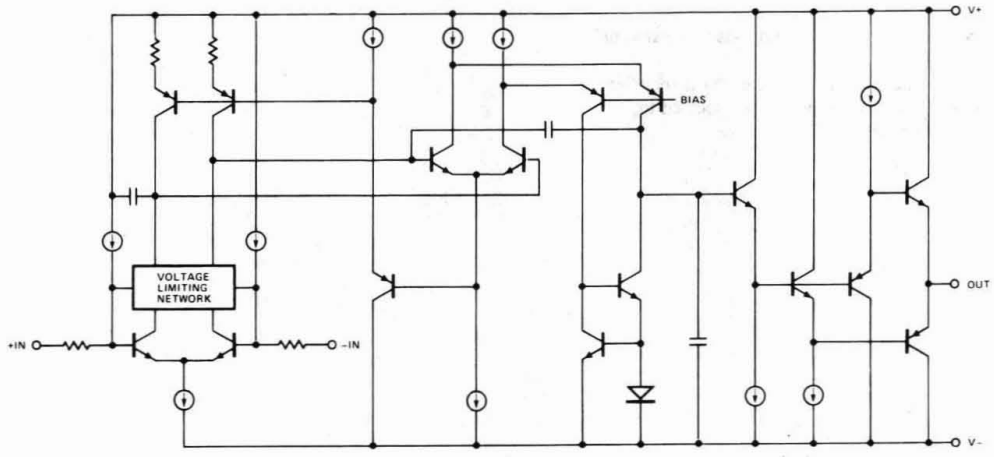
The OP200 is the first monolithic dual operational amplifier to offer OP77 type precision performance. Available in the industry standard 8-pin pinout, the OP200 combines precision performance with the space and cost savings offered by a dual amplifier.

The OP200 features an extremely low input offset voltage of less than 75 μV with a drift below 0.5 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP200 exceeds 5,000,000 into a 10 kΩ load; input bias current is under 2 nA; CMR is over 120 dB and PSRR below 1.8 μV/V. On-chip Zener-zap trimming is used to achieve the extremely low input offset voltage of the OP200 and eliminates the need for offset nulling.

Power consumption of the OP200 is very low, with each amplifier drawing less than 725 μA of supply current. The total current drawn by the dual OP200 is less than one-half that of a single OP07, yet the OP200 offers significant improvements over this industry standard op amp. The voltage noise density of the OP200, 11 nV/√Hz at 1 kHz, is half that of most competitive devices.

The OP200 is pin compatible with the OP14, OP221, LM158, MC1458/1558, and LT1013 and can be used to upgrade systems using these devices. The OP200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP400.



Simplified Schematic (One of Two Amplifiers Is Shown.)

OP200–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A/E Min	OP200A/E Typ	OP200A/E Max	OP200F Min	OP200F Typ	OP200F Max	OP200G Min	OP200G Typ	OP200G Max	Units
INPUT CHARACTERISTICS												
Input Offset Voltage	V_{OS}			25	75		50	150		80	200	µV
Long-Term Input Voltage Stability				0.1			0.1			0.1		µV/mo
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.05	1.0		0.05	2.0		0.05	3.5	nA
Input Bias Current	I_B	V_{CM} = 0 V		0.1	2.0		0.1	4.0		0.1	5.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[1]		22	36		22	36		22		nV/√Hz
	e_n	f_O = 1000 Hz[1]		11	18		11	18		11		nV/√Hz
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz		15			15			15		pA p-p
Input Noise Current Density	i_n	f_O = 10 Hz		0.4			0.4			0.4		pA√Hz
Input Resistance Differential Mode	R_{IN}			10			10			10		MΩ
Input Resistance Common-Mode	R_{INCM}			125			125			125		GΩ
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V										
		R_L = 10 kΩ	5000	12000		3000	7000		3000	7000		V/mV
		R_L = 2 kΩ	2000	3700		1500	3200		1500	3200		V/mV

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±20 V
Differential Input Voltage ..... ±30 V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, S, Z-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP200A ..... –55°C to +125°C
OP200E, OP200F ..... –40°C to +85°C
OP200G ..... –40°C to +85°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for Cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
OP200AZ[2]	–55°C to +125°C	8-Pin Cerdip	Q-8
OP200EZ	–40°C to +85°C	8-Pin Cerdip	Q-8
OP200FZ	–40°C to +85°C	8-Pin Cerdip	Q-8
OP200GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP200GS[3]	–40°C to +85°C	16-Pin SOL	R-16
OP200GS-REEL	–40°C to +85°C	16-Pin SOL	R-16

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages. For outline information see Package Information section.
[2]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO package, contact your local sales office.

Dual, Precision JFET High Speed Operational Amplifier

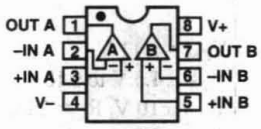
OP249

FEATURES
- Fast Slew Rate: 22 V/μs typ
- Settling Time (0.01%): 1.2 μs max
- Offset Voltage: 300 μV max
- High Open-Loop Gain: 1000 V/mV min
- Low Total Harmonic Distortion: 0.002% typ
- Improved Replacement for AD712, LT1057, OP215, TL072, and MC34082
- Available in Die Form

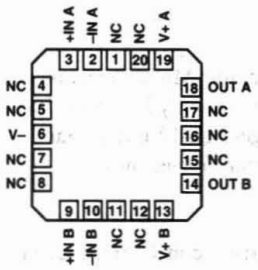
APPLICATIONS
- Output Amplifier for Fast D/As
- Signal Processing
- Instrumentation Amplifiers
- Fast Sample/Holds
- Active Filters
- Low Distortion Audio Amplifiers
- Input Buffer for A/D Converters
- Servo Controllers

PIN CONNECTIONS

8-Pin Cerdip (Z Suffix)
8-Pin Epoxy Mini-DIP (P Suffix)

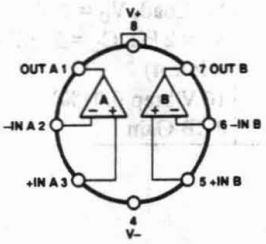


20-Contact LCC (RC Suffix)

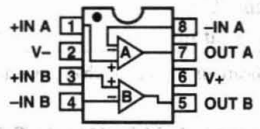


NC = NO CONNECT

TO-99 (J Suffix)



8-Pin SO (S Suffix)



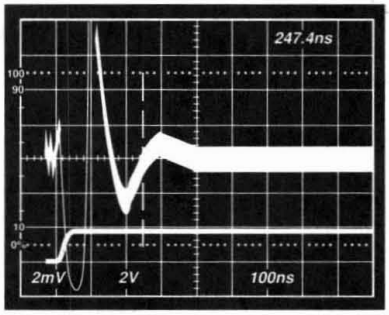
GENERAL DESCRIPTION

The OP249 is a high speed, precision dual JFET op amp, similar to the popular single op amp, the OP42. The OP249 outperforms available dual amplifiers by providing superior speed with excellent dc performance. Ultrahigh open-loop gain (1 kV/mV minimum), low offset voltage, and superb gain linearity, makes the OP249 the industry's first true precision, dual high speed amplifier.

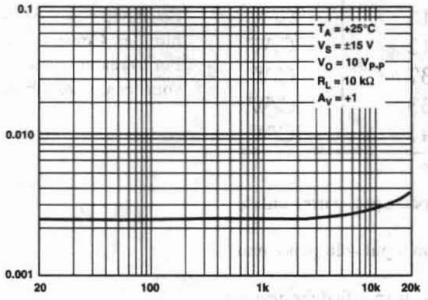
With a slew rate of 22 V/μs typical, and a fast settling time of less than 1.2 μs maximum to 0.01%, the OP249 is an ideal choice for high speed bipolar D/A and A/D converter applications. The excellent dc performance of the OP249 allows the full accuracy of high resolution CMOS D/As to be realized.

Symmetrical slew rate, even when driving large loads, such as 600 Ω, or 200 pF of capacitance, and ultralow distortion, make the OP249 ideal for professional audio applications, active filters, high speed integrators, servo systems, and buffer amplifiers.

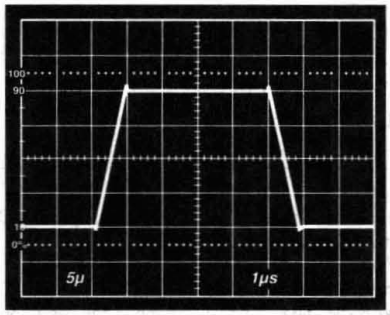
The OP249 provides significant performance upgrades to the TL072, AD712, OP215, MC34082 and the LT1057.



Fast Settling (0.01%)



Low Distortion A_V = +1, R_L = 10 kΩ



Excellent Output Drive, R_L = 600 Ω

OP249–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP249A Min	OP249A Typ	OP249A Max	OP249E Min	OP249E Typ	OP249E Max	OP249F Min	OP249F Typ	OP249F Max	Units
Offset Voltage	V_{OS}			0.2	0.5		0.1	0.3		0.2	0.7	mV
Long Term Offset Voltage	V_{OS}	(Note 1)			0.8			0.6			1.0	mV
Offset Stability				1.5			1.5			1.5		µV/Month
Input Bias Current	I_B	V_{CM} = 0 V, T_J = +25°C		30	75		20	50		30	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V, T_J = +25°C		6	25		4	15		6	25	pA
Input Voltage Range	IVR	(Note 2)		+12.5			+12.5			+12.5		V
			±11			±11			±11			V
				–12.5			–12.5			–12.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	80	90		86	95		80	90		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		12	31.6		9	31.6		12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	1000	1400		1000	1400		500	1200		V/mV
Output Voltage Swing	V_O	R_L = 2 kΩ		+12.5			+12.5			+12.5		V
			±12.0			±12.0			±12.0			V
				–12.5			–12.5			–12.5		V
Short-Circuit Current Limit	I_{SC}	Output Shorted to		+36			+36			+36		mA
		Ground	±20		±50	±20		±50	±20		±50	mA
				–33			–33			–33		mA
Supply Current	I_{SY}	No Load, V_O = 0 V		5.6	7.0		5.6	7.0		5.6	7.0	mA
Slew Rate	SR	R_L = 2 kΩ, C_L = 50 pF	18	22		18	22		18	22		V/µs
Gain-Bandwidth Product	GBW	(Note 4)	3.5	4.7		3.5	4.7		3.5	4.7		MHz
Settling Time	t_S	10 V Step 0.01%[3]		0.9	1.2		0.9	1.2		0.9	1.2	µs
Phase Margin	θ_0	0 dB Gain		55			55			55		Degrees

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Input Voltage[2] ..... ±18 V
Differential Input Voltage[2] ..... 36 V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range
  OP249A (J, Z, RC) ..... –55°C to +125°C
  OP249E, F (J, Z) ..... –40°C to +85°C
  OP249G (P, S) ..... –40°C to +85°C
Junction Temperature
  OP249 (J, Z, RC) ..... –65°C to +175°C
  OP249 (P, S) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE[1]

Model	Temperature Range	Package Option[2]
OP249AZ[3]	–55°C to +125°C	8-Pin Cerdip
OP249ARC/883	–55°C to +125°C	20-Contact LCC
OP249EJ	–40°C to +85°C	TO-99
OP249FZ	–40°C to +85°C	8-Pin Cerdip
OP249GP	–40°C to +85°C	8-Pin Plastic DIP
OP249GS[4]	–40°C to +85°C	8-Pin SO
OP249GS-REEL	–40°C to +85°C	8-Pin SO
OP249GS-REEL7	–40°C to +85°C	8-Pin SO

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[4]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

Dual Very Low Noise Precision Operational Amplifier

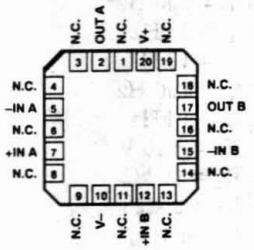
OP270

FEATURES

Very Low Noise: 5 nV/√Hz @ 1 kHz max
Excellent Input Offset Voltage: 75 μV max
Low Offset Voltage Drift: 1 μV/°C max
Very High Gain: 1500 V/mV min
Outstanding CMR: 106 dB min
Slew Rate: 2.4 V/μs typ
Gain-Bandwidth Product: 5 MHz typ
Industry Standard 8-Pin Dual Pinout
Available In Die Form

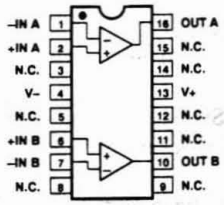
PIN CONFIGURATIONS

20-Pin LCC (RC Suffix)



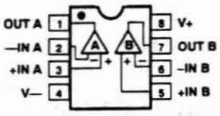
NC = NO CONNECT

16-Pin SOL (S Suffix)



NC = NO CONNECT

Epoxy Mini-DIP (P Suffix)
8-Pin Hermetic DIP (Z Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP270 is a high performance monolithic dual operational amplifier with exceptionally low voltage noise, 5 nV/√Hz at 1 kHz max, offering comparable performance to PMI's industry standard OP27.

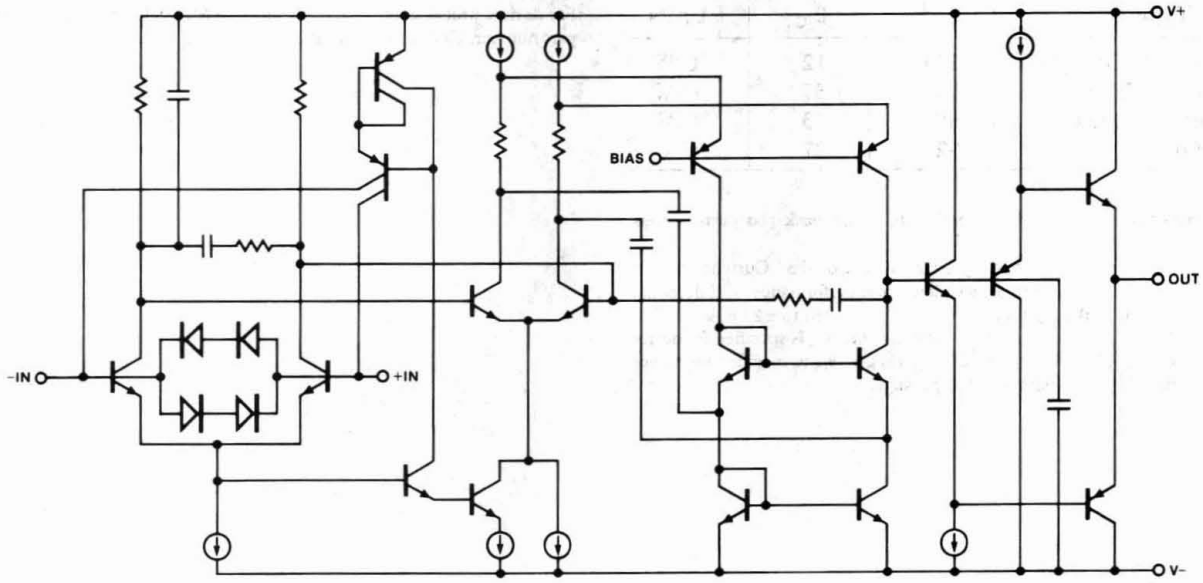
The OP270 features an input offset voltage below 75 μV and an offset drift under 1 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP270 is over 1,500,000 into a 10 kΩ load ensuring excellent gain accuracy and linearity, even in high gain applications. Input bias current is under 20 nA which reduces errors due to signal source resistance. The OP270's CMR of over 106 dB and PSRR of less than 3.2 μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the dual OP270 is one-third less than two OP27s, a significant advantage for power conscious applications. The OP270 is unity-gain stable with a gain-bandwidth product of 5 MHz and a slew rate of 2.4 V/μs.

The OP270 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, dual buffers, and low noise active filters.

The OP270 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, SE5532/A, RM4558 and HA5102 dual op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP271, with a slew rate of 8 V/μs, is recommended. For a quad op amp, see the OP470.

10



Simplified Schematic (One of Two Amplifiers Is Shown)

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

OP270–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}			10	75		20	150		50	250	µV
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	10		3	15		5	20	nA
Input Bias Current	I_B	V_{CM} = 0 V		5	20		10	40		15	60	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[1]		80	200		80	200		80		nV p-p
Input Noise	e_n	f_O = 10 Hz[2]		3.6	6.5		3.6	6.5		3.6		nV/√Hz
Voltage Density		f_O = 100 Hz[2]		3.2	5.5		3.2	5.5		3.2		nV/√Hz
		f_O = 1 kHz[2]		3.2	5.0		3.2	5.0		3.2		nV/√Hz
Input Noise	i_n	f_O = 10 Hz		1.1			1.1			1.1		pA/√Hz
Current Density		f_O = 100 Hz		0.7			0.7			0.7		pA/√Hz
		f_O = 1 kHz		0.6			0.6			0.6		pA/√Hz
Large-Signal	A_{VO}	V_O = ±10 V										
Voltage Gain		R_L = 10 kΩ	1500	2300		1000	1700		750	1500		V/mV
		R_L = 2 kΩ	750	1200		500	900		350	700		V/mV
Input Voltage Range	IVR	(Note 3)	±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	106	125		100	120		90	110		dB
Power Supply												
Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.56	3.2		1.0	5.6		1.5	6	µV/V
Slew Rate	SR		1.7	2.4		1.7	2.4		1.7	2.4		V/µs

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±1.0 V
Differential Input Current[2] ..... ±25 mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, S, Z Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP270A ..... –55°C to +125°C
OP270E, OP270F, OP270G ..... –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The OP270's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±10 V, the input current should be limited to ±25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, plastic DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[1]
OP270AZ[2]	75 µV	–55°C to +125°C	Q-8
OP270EZ	75 µV	–40°C to +85°C	Q-8
OP270FZ	150 µV	–40°C to +85°C	Q-8
OP270GP	250 µV	–40°C to +85°C	N-16
OP270GS	250 µV	–40°C to +85°C	R-16
OP207GS-REEL	250 µV	–40°C to +85°C	R-16
OP270ARC/883C	75 µV	–55°C to +125°C	E-20A

NOTES
[1]For outline information see Package Information section.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

ANALOG DEVICES

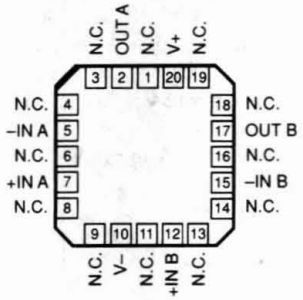
High Speed, Dual Operational Amplifier

OP271

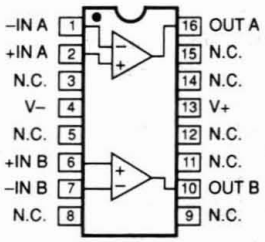
FEATURES
Excellent Speed: 8.5 V/μs typ
Fast Settling (0.01%): 2 μs typ
Unity-Gain Stable
High Gain-Bandwidth: 5 MHz typ
Low Input Offset Voltage: 200 μV max
Low Offset Voltage Drift: 2 μV/°C max
High Gain: 400 V/mV min
Outstanding CMR: 106 dB min
Industry Standard 8-Pin Dual Pinout
Available in Die Form

PIN CONNECTIONS

LCC (RC Suffix)

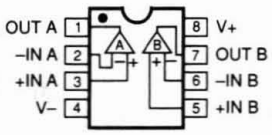


16-Pin SOL (S Suffix)



NC = NO CONNECT

Epoxy Mini-DIP (P Suffix)
8-Pin Hermetic DIP (Z Suffix)



GENERAL DESCRIPTION

The OP271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5 V/μs typical, and fast settling time, 2 μs typical to 0.01%. The OP271 has a gain bandwidth of 5 MHz with a high phase margin of 62°.

Input offset voltage of the OP271 is under 200 μV with input offset voltage drift below 2 μV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10 kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 20 nA limiting errors due to source resistance. The OP271's outstanding CMR, over 106 dB, and low PSRR, under 5.6 μV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP271 exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

The OP271 offers outstanding dc and ac matching between channels. This is especially valuable for applications such as multiple gain blocks, high speed instrumentation and amplifiers, buffers and active filters.

The OP271 conforms to the industry standard 8-pin dual op amp pinout. It is pin compatible with the TL072, TL082, LF412, and 1458/1558 dual op amps and can be used to significantly improve systems using these devices.

For applications requiring lower voltage noise, see the OP270. For a quad version of the OP271, see the OP471.

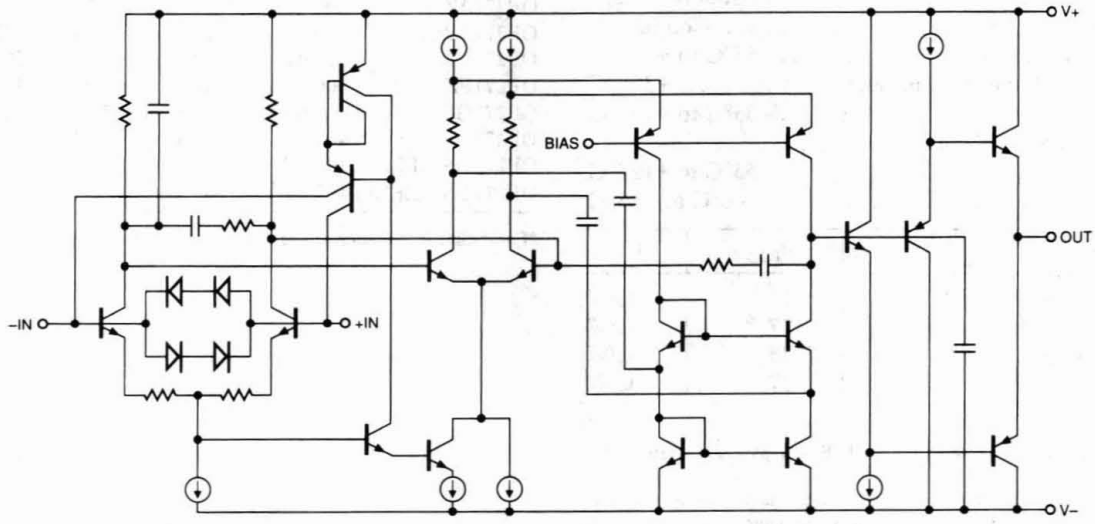


Figure 1. Simplified Schematic (One of the Two Amplifiers Is Shown.)

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OP271–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	OP271A/E Min	OP271A/E Typ	OP271A/E Max	OP271F Min	OP271F Typ	OP271F Max	OP271G Min	OP271G Typ	OP271G Max	Units
Input Offset Voltage	V_{OS}			75	200		150	300		200	400	µV
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	10		4	15		7	20	nA
Input Bias Current	I_B	V_{CM} = 0 V		4	20		6	40		12	60	nA
Input Noise Voltage Density	e_n	f_O = 1 kHz		7.6			7.6			7.6		nV/√Hz
Large-Signal		V_O = ±10 V										
Voltage	A_{VO}	R_L = 10 kΩ	400	650		300	500		250	400		V/mV
Gain		R_L = 2 kΩ	300	500		200	300		175	250		V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	106	120		100	115		90	105		dB
Power Supply												
Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.6	3.2		1.8	5.6		2.4	7.0	µV/V
Slew Rate	SR		5.5	8.5		5.5	8.5		5.5	8.5		V/µs
Phase Margin	$ø_m$	A_V = +1		62			62			62		Degree
Supply Current												
(All Amplifiers)	I_{SY}	No Load		4.5	6.5		4.5	6.5		4.5	6.5	mA
Gain Bandwidth Product	GBW			5			5			5		MHz
Channel Separation	CS	V_O = 20 V p-p										
		f_O = 10 Hz[2]	125	175		125	175			175		dB
Input Capacitance	C_{IN}			3			3			3		pF
Input Resistance												
Differential-Mode	R_{IN}			0.4			0.4			0.4		MΩ
Input Resistance												
Common-Mode	R_{INCM}			20			20			20		GΩ
Settling Time	t_S	A_V = +1, 10 V Step										
		to 0.01%		2			2			2		µs

NOTES
[1]Guaranteed by CMR test.
[2]Guaranteed but not 100% tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±1.0 V
Differential Input Current[2] ..... ±25 mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP271A ..... –55°C to +125°C
OP271E, OP271F, OP271G ..... –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	92	27	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The OP271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If different voltage exceeds ±1.0 V, the input current should be limited to 25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

Model	V_{OS} max T_A = +25°C	Temperature Range	Package Option*
OP271AZ	200 µV	–55°C to +125°C	8-Pin Cerdip
OP271ARC/883	200 µV	–55°C to +125°C	20-Contact LCC
OP271EZ	200 µV	–40°C to +85°C	8-Pin Cerdip
OP271FZ	300 µV	–40°C to +85°C	8-Pin Cerdip
OP271GP	400 µV	–40°C to +85°C	8-Pin Plastic DIP
OP271GS	400 µV	–40°C to +85°C	16-Pin SOL
OP271GS-REEL	400 µV	–40°C to +85°C	16-Pin SOL
OP271GS-REEL7	400 µV	–40°C to +85°C	16-Pin SOL

*For outline information see Package Information section.

Dual Bipolar/JFET, Audio Operational Amplifier

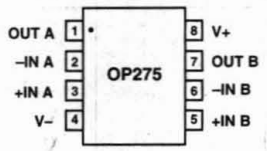
OP275*

FEATURES
Excellent Sonic Characteristics
Low Noise: 6 nV/√Hz
Low Distortion: 0.0006%
High Slew Rate: 22 V/μs
Wide Bandwidth: 9 MHz
Low Supply Current: 5 mA
Low Offset Voltage: 1 mV
Low Offset Current: 2 nA
Unity Gain Stable
SOIC-8 Package

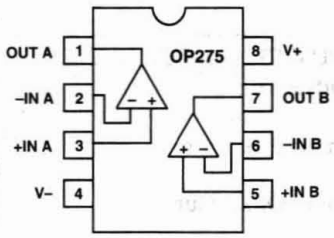
APPLICATIONS
High Performance Audio
Active Filters
Fast Amplifiers
Integrators

PIN CONNECTIONS

8-Lead Narrow-Body SO (S Suffix)



8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

The OP275 is the first amplifier to feature the Butler Amplifier front-end. This new front-end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals that of previous audio amplifiers, but at much lower supply currents.

A very low l/f corner of below 6 Hz maintains a flat noise density response. Whether noise is measured at either 30 Hz or 1 kHz, it is only 6 nV/√Hz. The JFET portion of the input stage gives the OP275 its high slew rates to keep distortion low, even when large output swings are required, and the 22 V/μs slew rate of the OP275 is the fastest of any standard audio amplifier. Best of all, this low noise and high speed are accomplished using less than 5 mA of supply current, lower than any standard audio amplifier.

Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than 200 μV. This allows the OP275 to be used in many dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP275 is specified over the extended industrial (–40°C to +85°C) temperature range. OP275s are available in both plastic DIP and SOIC-8 packages. SOIC-8 packages are available in 2500 piece reels. Many audio amplifiers are not offered in SOIC-8 surface mount packages for a variety of reasons; however, the OP275 was designed so that it would offer full performance in surface mount packaging.

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ORDERING GUIDE

Model	Temperature Range	Package Option*
OP275GP	–40°C to +85°C	8-Pin Plastic DIP
OP275GS	–40°C to +85°C	8-Pin SOIC
OP275GSR	–40°C to +85°C	SO-8 Reel, 2500 pcs.
OP275GBC	+25°C	DICE

*For outline information see Package Information section.

*Protected by U.S. Patent No. 5,101,126.

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OP275–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
THD + Noise		V_{in} = 3 V rms, R_L = 2 kΩ, f = 1 kHz		0.006		%
Voltage Noise Density	e_n	f = 30 Hz		7		nV/√Hz
		f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.5		pA/√Hz
Headroom		THD + Noise ≤ 0.01%, R_L = 2 kΩ, V_S = ±18 V		>12.9		dBu
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
		–40°C ≤ T_A ≤ +85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 0 V		100	350	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C		100	400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2	50	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C		2	100	nA
Input Voltage Range	V_{CM}		–10.5		+10.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10.5 V, –40°C ≤ T_A ≤ +85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	175			V/mV
		R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	–13.5	±13.9	+13.5	V
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	–13	±13.9	+13	V
		R_L = 600 Ω, V_S = ±18 V			–16/+14	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	85	111		dB
		V_S = ±4.5 V to ±18 V, –40°C ≤ T_A ≤ +85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C		4	5	mA
		V_S = ±22 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C			5.5	mA
Supply Voltage Range	V_S		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	22		V/µs
Full-Power Bandwidth	BW_P					kHz
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	$ø_m$			62		Degrees
Overshoot Factor		V_{IN} = 100 mV, A_V = +1, R_L = 600 Ω, C_L = 100 pF		10		%

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±22 V
Input Voltage[2] ..... ±22 V
Differential Input Voltage ..... ±7.5 V
Output Short-Circuit Duration to GND[3] ..... Indefinite
Storage Temperature Range
P, S Package ..... –65°C to +150°C
Operating Temperature Range
OP275G ..... –40°C to +85°C
Junction Temperature Range
P, S Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages greater than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]Shorts to either supply may destroy the device. See data sheet for full details.
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

Rail-to-Rail High Output Current Operational Amplifier

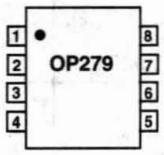
OP279

FEATURES
Rail-to-Rail Inputs and Outputs
High Output Current: ±80 mA
Single Supply: +5 V to +12 V
Wide Bandwidth: 5 MHz
High Slew Rate: 3 V/μs
Low Distortion: 0.01%
Unity-Gain Stable
No Phase Reversal
Short Circuit Protected
Drives Capacitive Loads: 10 nF

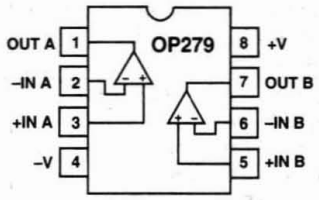
APPLICATIONS
Multimedia
Telecom
DAA Transformer Driver
LCD Driver
Low Voltage Servo Control

FUNCTIONAL BLOCK DIAGRAM

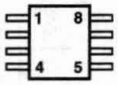
8-Lead Narrow Body SO (SO-8)



8-Lead Epoxy DIP (N-8)



8-Lead TSSOP (RU Suffix)



OP279

PIN ROTATION IS THE SAME FOR ALL PACKAGES.

GENERAL DESCRIPTION

The OP279 is a dual rail-to-rail, high output current, single-supply amplifier. It is designed for low voltage applications that require either current or capacitive load drive capability. The OP279 can sink and source currents of ±80 mA (typ) and is stable with capacitive loads to 10 nF.

Applications that benefit from the OP279's high output current include driving headphones, displays, transformers, and power transistors. The powerful output is combined with a unique input stage that maintains very low distortion with wide common-mode range, even in single supply designs.

The OP279 can be used as a buffer to provide much greater drive capability than can usually be provided by CMOS outputs. CMOS ASICs and DACs often have outputs that can swing to both the positive supply and ground, but are incapable of driving greater than a few milliamps.

Bandwidth is typically 5 MHz and the slew rate is 3 V/μs, making these amplifiers well suited for single supply applications that require audio bandwidths when used in high gain configurations. Operation is guaranteed from voltages as low as 4.5 V, up to 12 V.

When using the OP279 in +5 volt systems, very good audio performance can be attained. THD is below 0.01% with a 600 Ω load, and noise is a respectable 21 nV/√Hz. Supply current is less than 3.5 mA per amplifier.

The OP279 is available in 8-pin plastic DIP and SO-8 surface mount packages. They are specified over the industrial (–40°C to +85°C) temperature range.

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP279GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP279GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP279HRU	–40°C to +85°C	8-Pin TSSOP	RU-8

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +16 V
Input Voltage . . . . . +16 V
Differential Input Voltage[1] . . . . . ±1 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
P, S, RU Package . . . . . –65°C to +150°C
Operating Temperature Range
OP279G, H . . . . . –40°C to +85°C
Junction Temperature Range
P, S, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
8-Lead TSSOP	240	43	°C/W

NOTES
[1]The inputs are clamped with back-to-back diodes. If the differential input voltage exceeds 1 volt, the input current should be limited to 5 mA.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, packages; θ_{JA} is specified for device soldered in circuit board for SOIC packages.

OP279–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 2.5 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	V_{OUT} = 2.5 V			4	mV
Input Bias Current	I_B	V_{OUT} = 2.5 V, T_A = +25°C			±300	nA
Input Bias Current	I_B	V_{OUT} = 2.5 V			±600	nA
Input Offset Current	I_{OS}	V_{OUT} = 2.5 V, T_A = +25°C			±50	nA
Input Offset Current	I_{OS}	V_{OUT} = 2.5 V			±100	nA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	56	66		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3.5 V	70			dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, 0.3 V ≤ V_{OUT} ≤ 4.7 V	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink, T_A = +25°C			75	mV
Output Voltage Low	V_{OL}	I_L = 10 mA Sink			100	mV
Short Circuit Limit	I_{SC}		±45	±80		mA
Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		22		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +4.5 V to +12 V	76	88		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V		2.6	3.5	mA
Supply Voltage Range	V_S		+4.5		+12	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 kΩ, 1 nF		3		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			60		Degrees
Capacitive Load Drive		No Oscillation		10		nF
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD			0.01		%
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz

ELECTRICAL SPECIFICATIONS (@ V_S = ±5.0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				4	mV
Input Bias Current	I_B	T_A = +25°C			±300	nA
Input Bias Current	I_B				±600	nA
Input Offset Current	I_{OS}	T_A = +25°C			±50	nA
Input Offset Current	I_{OS}				±100	nA
Input Voltage Range	V_{CM}		–5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –5 V to +5 V	60	66		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, –4.7 V ≤ V_{OUT} ≤ 4.7 V, T_A = +25°C	20			V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, –4.7 V ≤ V_{OUT} ≤ 4.7 V	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink			–4.85	V
Short Circuit Limit	I_{SC}		±50	±80		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		22		Ω
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_S = ±6 V, V_{OUT} = 0 V		2	3.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 kΩ, 1 nF		3		V/µs
Full-Power Bandwidth	BW_P	1% Distortion				kHz
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			69		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
Current Noise Density	i_n			1		pA/√Hz

Specifications subject to change without notice.

Dual/Quad Low Power, High Speed JFET Operational Amplifiers

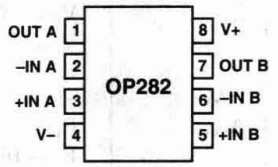
OP282/OP482

FEATURES
High Slew Rate: 9 V/μs
Wide Bandwidth: 4 MHz
Low Supply Current: 250 μA/Amplifier
Low Offset Voltage: 3 mV
Low Bias Current: 100 pA
Fast Settling Time
Common-Mode Range Includes V+
Unity Gain Stable

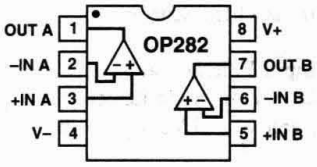
APPLICATIONS
Active Filters
Fast Amplifiers
Integrators
Supply Current Monitoring

PIN CONNECTIONS

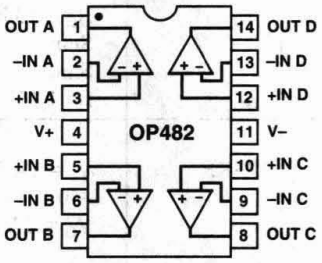
8-Lead Narrow-Body SOIC (S Suffix)



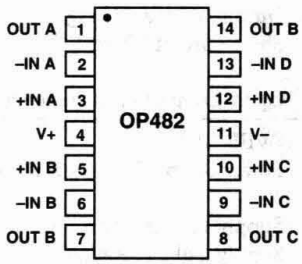
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SOIC (S Suffix)



GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. Slew rate exceeds 7 V/μs with supply current under 250 μA per amplifier. These unity gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 insures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

With a wide output swing, within 1.5 volts of each supply, low power consumption and high slew rate, the OP282/OP482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. Both dual and quad amplifiers are available in plastic and ceramic DIP plus SOIC surface mount packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP282GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP282GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP482GP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP482GS	–40°C to +85°C	14-Pin SOIC	SO-14

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
OP282A, OP482A . . . . . –55°C to +125°C
OP282G, OP482G . . . . . –40°C to +85°C
Junction Temperature Range
P, S Packages . . . . . –65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

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OP282/OP482–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP282		0.2	3	mV
		OP282, $-40 \le T_A \le +85°C$			4.5	mV
Offset Voltage	V_{OS}	OP482		0.2	4	mV
		OP482, $-40 \le T_A \le +85°C$			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V, Note 1			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V, Note 1			250	pA
Input Voltage Range			–11		+15	V
Common-Mode Rejection	CMR	$-11 V \le V_{CM} \le +15 V$, $-40 \le T_A \le +85°C$	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, $-40 \le T_A \le +85°C$	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	–13.5	±13.9	13.5	V
Short Circuit Limit	I_{SC}	Source	3	10		mA
		Sink	–8	–12		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, $-40 \le T_A \le +85°C$		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, $40 \le T_A \le +85°C$		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$Ø_O$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

NOTE
[1]The input bias and offset currents are tested at $T_A = T_J$ = +85°C. Bias and offset currents are guaranteed but not tested at –40°C.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	OP282	3	mV max
Offset Voltage	V_{OS}	OP482	4	mV max
Input Bias Current	I_B	V_{CM} = 0 V	100	pA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	50	pA max
Input Voltage Range[1]			–11, +15	V min/max
Common-Mode Rejection	CMRR	$-11 V \le V_{CM} \le +15 V$	70	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	316	µV/V
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	±13.5	V min
Supply Current/Amplifier	I_{SY}	V_O = 0 V, $R_L = \infty$	250	µA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

Specifications subject to change without notice.

Dual, 9 MHz Precision Operational Amplifier

OP285*

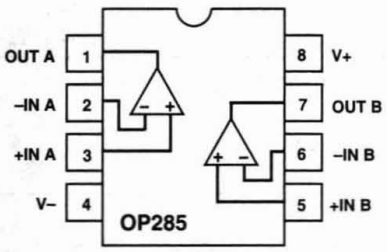
FEATURES
Low Offset Voltage: 250 μV
Low Noise: 6 nV/√Hz
Low Distortion: 0.0006%
High Slew Rate: 22 V/μs
Wide Bandwidth: 9 MHz
Low Supply Current: 5 mA
Low Offset Current: 2 nA
Unity-Gain Stable
SO-8 Package

APPLICATIONS
High Performance Audio
Active Filters
Fast Amplifiers
Integrators

PIN CONNECTIONS

8-Lead Narrow-Body SO
(S Suffix)

8-Lead Epoxy DIP
(P Suffix)



GENERAL DESCRIPTION

The OP285 is a precision high speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP285 offers the slew rate and low power of a JFET amplifier combined with the precision, low noise and low drift of a bipolar amplifier. Input offset voltage is laser-trimmed and guaranteed less than 250 μV. This makes the OP285 useful in dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry. Slew rates of 22 V/μs and a bandwidth of 9 MHz make the OP285 one of the most accurate medium speed amplifiers available.

The combination of low noise, speed and accuracy can be used to build high speed instrumentation systems. Circuits such as instrumentation amplifiers, ramp generators, bi-quad filters and dc coupled audio systems are all practical with the OP285.

For applications that require long term stability, the OP285 has a guaranteed maximum long term drift specification.

The OP285 is specified over the XIND—extended industrial—(–40°C to +85°C) temperature range. OP285s are available in 8-pin plastic DIP and SOIC-8 surface mount packages.

***Protected by U.S. Patent No. 510116.**

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP285GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP285GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP285GS-REEL	–40°C to +85°C	SO-8 Reel, 2500 pcs.	
OP285GS-REEL7	–40°C to +85°C	SO-8 7" Reel 1000 pcs.	

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to Gnd[3] . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
OP285G . . . . . –40°C to +85°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±7.5 V, the absolute maximum input voltage is equal to the supply voltage.
[3]Shorts to either supply may destroy the device. See data sheet for full details.
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

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OP285–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			35	250	µV
Offset Voltage	V_{OS}	–40°C ≤ T_A ≤ +85°C			600	µV
Input Bias Current	I_B	V_{CM} = 0 V		100	350	nA
Input Bias Current	I_B	V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C			400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2	±50	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C		2	±100	nA
Input Voltage Range	V_{CM}		–10.5		+10.5	V
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V, –40°C ≤ T_A ≤ +85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	175			V/mV
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
Common-Mode Input Capacitance				7.5		pF
Differential Input Capacitance				3.7		pF
Long Term Offset Voltage	ΔV_{OS}	Note 1			300	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	–13.5	±13.9	+13.5	V
Output Voltage Swing	V_O	R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	–13	±13.9	+13	V
		R_L = 600 Ω, V_S = ±18 V		–16/+14		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	85	111		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, –40°C ≤ T_A ≤ +85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C		4	5	mA
Supply Current	I_{SY}	V_S = ±22 V, V_O = 0 V, R_L = ∞, –40°C ≤ T_A ≤ +85°C			5.5	mA
Supply Voltage Range	VS		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	22		V/µs
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	θo			62		Degrees
Settling Time	t_S	To 0.1%, 10 V Step		625		ns
Settling Time	t_S	To 0.01%, 10 V Step		750		ns
Distortion		A_V = +1, V_{OUT} = 8.5 V p-p, f = 1 kHz, R_L = 2 kΩ		–104		dB
Voltage Noise Density	e_n	f = 30 Hz		7		nV/√Hz
Voltage Noise Density	e_n	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.9		pA/√Hz
Headroom		THD + Noise ≤ 0.01%, R_L = 2 kΩ, V_S = ±18 V		>12.9		dBu

NOTE

[1]Long term offset voltage is guaranteed by a 1000 hour life test performed on three independent wafer lots at +125 °C, with an LTPD of 1.3.

Specifications subject to change without notice.

ANALOG DEVICES

Dual/Quad Rail-to-Rail Operational Amplifiers

OP295/OP495

FEATURES
Rail-to-Rail Output Swing
Single-Supply Operation: +3 V to +36 V
Low Offset Voltage: 300 μV
Gain Bandwidth Product: 75 kHz
High Open-Loop Gain: 1000 V/mV
Unity-Gain Stable
Low Supply Current/Per Amplifier: 150 μA max

APPLICATIONS
Battery Operated Instrumentation
Servo Amplifiers
Actuator Drives
Sensor Conditioners
Power Supply Control

GENERAL DESCRIPTION

Rail-to-rail output swing combined with dc accuracy are the key features of the OP495 quad and OP295 dual CBCMOS operational amplifiers. By using a bipolar front end, lower noise and higher accuracy than that of CMOS designs has been achieved. Both input and output ranges include the negative supply, providing the user "zero-in/zero-out" capability. For users of 3.3 volt systems such as lithium batteries, the OP295/OP495 is specified for three volt operation.

Maximum offset voltage is specified at 300 μV for +5 volt operation, and the open-loop gain is a minimum of 1000 V/mV. This yields performance that can be used to implement high accuracy systems, even in single supply designs.

The ability to swing rail-to-rail and supply +15 mA to the load makes the OP295/OP495 an ideal driver for power transistors and "H" bridges. This allows designs to achieve higher efficiencies and to transfer more power to the load than previously possible without the use of discrete components. For applications that require driving inductive loads, such as transformers, increases in efficiency are also possible. Stability while driving capacitive loads is another benefit of this design over CMOS rail-to-rail amplifiers. This is useful for driving coax cable or large FET transistors. The OP295/OP495 is stable with loads in excess of 300 pF.

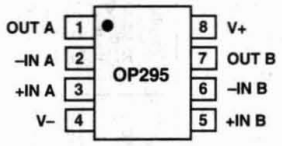
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP295GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP295GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP295GS-REEL	–40°C to +125°C	8-Pin SOIC	SO-8
OP295GS-REEL7	–40°C to +125°C	8-Pin SOIC	SO-8
OP295GBC	+25°C	DICE	
OP495GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP495GS	–40°C to +125°C	16-Pin SOL	R-16
OP495GS-REEL	–40°C to +125°C	16-Pin SOL	R-16
OP495GBC	+25°C	DICE	

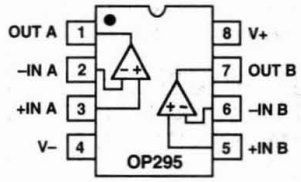
*For outline information see Package Information section.

PIN CONNECTIONS

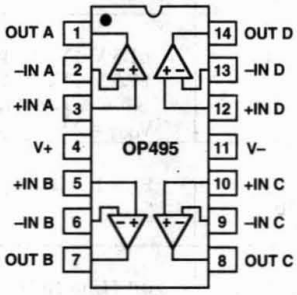
8-Lead Narrow-Body SO (S Suffix)



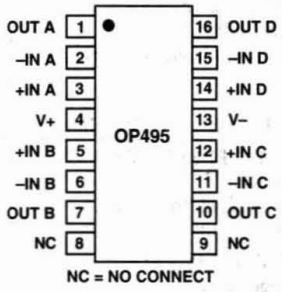
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



16-Lead SO (300 Mil) (S Suffix)



The OP295 and OP495 are specified over the extended industrial (–40°C to +125°C) temperature range. OP295s are available in 8-pin plastic and ceramic DIP plus SO-8 surface mount packages. OP495s are available in 14-pin plastic and SO-16 surface mount packages. Contact your local sales office for MIL-STD-883 data sheet.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2]. . . . . +36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
OP295G, OP495G . . . . . –40°C to +125°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
16-Pin SO (S)	98	30	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ± 18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC package.

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OP295/OP495–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	300	µV
		–40°C ≤ T_A ≤ +125°C			800	µV
Input Bias Current	I_B			8	20	nA
		–40°C ≤ T_A ≤ +125°C			30	nA
Input Offset Current	I_{OS}			±1	±3	nA
		–40°C ≤ T_A ≤ +125°C			±5	nA
Input Voltage Range	V_{CM}		0		+4.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 4.0 V, –40°C ≤ T_A ≤ +125°C	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, 0.005 ≤ V_{OUT} ≤ 4.0 V	1000	10,000		V/mV
		R_L = 10 kΩ, –40°C ≤ T_A ≤ +125°C	500			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1	5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ to GND	4.98	5.0		V
		R_L = 10 kΩ to GND	4.90	4.94		V
		I_{OUT} = 1 mA, –40°C ≤ T_A ≤ +125°C		4.7		V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ to GND		0.7	2	mV
		R_L = 10 kΩ to GND		0.7	2	mV
		I_{OUT} = 1 mA, –40°C ≤ T_A ≤ +125°C		90		mV
Output Current	I_{OUT}		±11	±18		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
		±1.5 V ≤ V_S ≤ ±15 V, –40°C ≤ T_A ≤ +125°C	85			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞, –40°C ≤ T_A ≤ +125°C			150	µA
DYNAMIC PERFORMANCE						
Skew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			86		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		51		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, V_{CM} = +1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			30	500	µV
Input Bias Current	I_B			8	20	nA
Input Offset Current	I_{OS}			±1	±3	nA
Input Voltage Range	V_{CM}		0		+2.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 2.0 V, –40°C ≤ T_A ≤ +125°C	90	110		dB
Large Voltage Gain	A_{VO}	R_L = 10 kΩ		750		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 10 kΩ to GND	2.9			V
Output Voltage Swing Low	V_{OL}	R_L = 10 kΩ to GND		0.7	2	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±15 V	90	110		dB
		±1.5 V ≤ V_S ≤ ±15 V, –40°C ≤ T_A ≤ +125°C	85			dB
Supply Current Per Amplifier	I_{SY}	V_{OUT} = 1.5 V, R_L = ∞, –40°C ≤ T_A ≤ +125°C			150	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/µs
Gain Bandwidth Product	GBP			75		kHz
Phase Margin	θ_O			85		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		1.6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		53		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.1		pA/√Hz

Specifications subject to change without notice.

ANALOG DEVICES

Dual Low Bias Current Precision Operational Amplifier

OP297

FEATURES

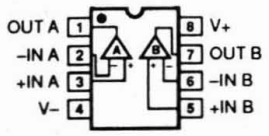
Precision Performance in Standard SO-8 Pinout
Low Offset Voltage: 50 μV max
Low Offset Voltage Drift: 0.6 μV/°C max
Very Low Bias Current:
+25°C (100 pA max)
–55°C to +125°C (450 pA max)
Very High Open-Loop Gain (2000 V/mV min)
Low Supply Current (Per Amplifier): 625 μA max
Operates From ±2 V to ±20 V Supplies
High Common-Mode Rejection: 120 dB min
Pin Compatible to LT1013, AD706, AD708, OP221, LM158, and MC1458/1558 with Improved Performance

APPLICATIONS

Strain Gauge and Bridge Amplifiers
High Stability Thermocouple Amplifiers
Instrumentation Amplifiers
Photo-Current Monitors
High-Gain Linearity Amplifiers
Long-Term Integrators/Filters
Sample-and-Hold Amplifiers
Peak Detectors
Logarithmic Amplifiers
Battery-Powered Systems

PIN CONNECTIONS

Plastic Epoxy-DIP (P Suffix)
8-Pin Cerdip (Z Suffix)
8-Pin Narrow Body SOIC (S Suffix)



GENERAL DESCRIPTION

The OP297 is the first dual op amp to pack precision performance into the space-saving, industry standard 8-pin SO package. Its combination of precision with low power and extremely low input bias current makes the dual OP297 useful in a wide variety of applications.

Precision performance of the OP297 includes very low offset, under 50 μV, and low drift, below 0.6 μV/°C. Open-loop gain exceeds 2000 V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP297's common-mode rejection of over 120 dB. The OP297's power supply rejection of over 120 dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP297 is under 625 μA per amplifier and it can operate with supply voltages as low as ±2 V.

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ORDERING GUIDE[1]

Model	Temperature Range	Package Description	Package Option[1]
OP297AZ	–55°C to +125°C	8-Pin Cerdip	Q-8
OP297EZ	–40°C to +85°C	8-Pin Cerdip	Q-8
OP297EP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP297FP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP297FS	–40°C to +85°C	8-Pin SO	SO-8
OP297FS-REEL	–40°C to +85°C	8-Pin SO	SO-8
OP297FS-REEL7	–40°C to +85°C	8-Pin SO	SO-8
OP297GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP297GS	–40°C to +85°C	8-Pin SO	SO-8
OP297GS-REEL	–40°C to +85°C	8-Pin SO	SO-8
OP297GS-REEL7[2]	–40°C to +85°C	8-Pin SO	SO-8

NOTES
[1]Burn-in is available on extended industrial temperature range parts in cerdip, and plastic DIP packages. For outline information see Package Information section.
[2]For availability and burn-in information on SO packages, contact your local sales office.

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OP297–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP297A/E Min	OP297A/E Typ	OP297A/E Max	OP297F Min	OP297F Typ	OP297F Max	OP297G Min	OP297G Typ	OP297G Max	Units
Input Offset Voltage	V_{OS}			25	50		50	100		80	200	µV
Long-Term Input Voltage Stability				0.1			0.1			0.1		µV/mo
Input Offset Current	I_{OS}	V_{CM} = 0 V		20	100		35	150		50	200	pA
Input Bias Current	I_B	V_{CM} = 0 V		20	±100		35	±150		50	±200	pA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz		20			20			20		nV/√Hz
	e_n	f_O = 1000 Hz		17			17			17		nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		20			20			20		fA√Hz
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common-Mode	R_{INCM}			500			500			500		GΩ
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V, R_L = 2 kΩ	2000	4000		1500	3200		1200	3200		V/mV
Input Voltage Range	IVR	(Note 1)	±13	±14		±13	±14		±13	±14		V
Common-Mode Rejection	CMR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
Power Supply Rejection	PSR	V_S = ±2 V to ±20 V	120	130		114	125		114	125		dB
Output Voltage Swing	V_O	R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		V
	V_O	R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7		V
Supply Current Per Amplifier	I_{SY}	No Load		525	625		525	625		525	625	µA
Supply Voltage	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µs
Gain Bandwidth Product	GBWP	A_V = +1		500			500			500		kHz
Channel Separation	CS	V_O = 20 V p–p, f_O = 10 Hz		150			150			150		dB
Input Capacitance	C_{IN}			3			3			3		pF

NOTES
[1]Guaranteed by CMR test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±20 V
Input Voltage[2] . . . . . ±20 V
Differential Input Voltage[2] . . . . . 40 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Z Package . . . . . –65°C to +175°C
  P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
  OP297A (Z) . . . . . –55°C to +125°C
  OP297E, F (Z) . . . . . –40°C to +85°C
  OP297F, G (P, S) . . . . . –40°C to +85°C
Junction Temperature
  Z Package . . . . . –65°C to +175°C
  P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP, packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ANALOG DEVICES

Quad Low Offset, Low Power Operational Amplifier

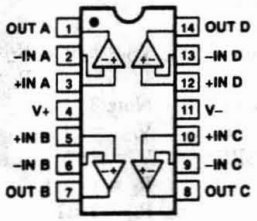
OP400

FEATURES

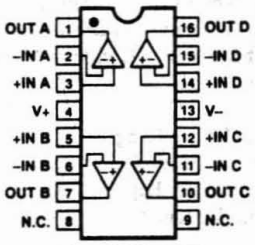
Low Input Offset Voltage: 150 μV max
Low Offset Voltage Drift,
Over –55°C to +125°C: 1.2 μV/°C max
Low Supply Current (Per Amplifier): 725 μA max
High Open-Loop Gain: 5000 V/mV min
Input Bias Current: 3 nA max
Low Noise Voltage Density: 11 nV/√Hz @ 1 kHz
Stable With Large Capacitive Loads: 10 nF typ
Pin Compatible to OP11, LM148, HA4741, RM4156, and LT1014 with Improved Performance
Available in Die Form

PIN CONNECTIONS

14-Pin Hermetic DIP (Y Suffix)
14-Pin Plastic DIP (P Suffix)

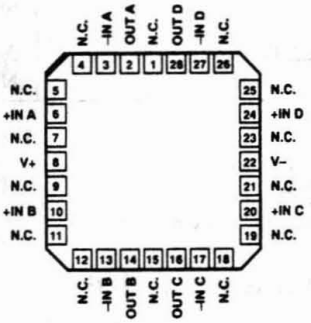


16-Pin SOL (S Suffix)



NC = NO CONNECT

28-Lead LCC (TC Suffix)



GENERAL DESCRIPTION

The OP400 is the first monolithic quad operational amplifier that features OP77 type performance. Precision performance no longer has to be sacrificed to obtain the space and cost savings offered by quad amplifiers.

The OP400 features an extremely low input offset voltage of less than 150 μV with a drift of under 1.2 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP400 is over 5,000,000 into a 10 kΩ load; input bias current is under 3 nA; CMR is above 120 dB and PSRR below 1.8 μV/V. On-chip Zener-zap trimming is used to achieve the low input offset voltage of the OP400 and eliminates the need for offset nulling. (The OP400 conforms to the industry standard quad pinout which does not have null terminals.)

The OP400 features low power consumption, drawing less than 725 μA per amplifier. The total current drawn by this quad amplifier is less than that of a single OP07, yet the OP400 offers significant improvements over this industry standard op amp. Voltage noise density of the OP400 is a low 11 nV/√Hz at 10 Hz which is half that of most competitive devices.

The OP400 is pin compatible with the OP11, LM148, HA4741, RM4156, and LT1014 operational amplifiers and can be used to upgrade systems using these devices. The OP400 is an ideal choice for applications requiring multiple precision operational amplifiers and where low power consumption is critical.

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ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
OP400AY[3]	150 mV	–55°C to +125°C	14-Pin Cerdip
OP400ATC/883	150 mV	–55°C to +125°C	28-Contact LCC
OP400EY	150 mV	–25°C to +85°C	14-Pin Cerdip
OP400FY	230 mV	–25°C to +85°C	14-Pin Cerdip
OP400GP	300 mV	0°C to +70°C	14-Pin Plastic DIP
OP400GS[4]	300 mV	0°C to +70°C	16-Pin SOL
OP400GS-REEL	300 mV	0°C to +70°C	16-Pin SOL
OP400HP	300 mV	–40°C to +85°C	14-Pin Plastic DIP
OP400HS[4]	300 mV	–40°C to +85°C	16-Pin SOL
OP400HS-REEL	300 mV	–40°C to +85°C	16-Pin SOL

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip and plastic DIP packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[4]For available and burn-in information on SO and PLCC packages, contact your local sales office.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

OP400–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP400A/E Min	OP400A/E Typ	OP400A/E Max	OP400F Min	OP400F Typ	OP400F Max	OP400G/H Min	OP400G/H Typ	OP400G/H Max	Units
Input Offset Voltage	V_{OS}			40	150		60	230		80	300	µV
Long-Term Input Voltage Stability				0.1			0.1			0.1		µV/mo
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.1	1.0		0.1	2.0		0.1	3.5	nA
Input Bias Current	I_B	V_{CM} = 0 V		0.75	3.0		0.75	6.0		0.75	7.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5			0.5		µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[1]		22	36		22	36		22		nV/√Hz
		f_O = 1000 Hz[1]		11	18		11	18		11		nV/√Hz
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz		15			15			15		pA p-p
Input Noise Current Density	i_n	f_O = 10 Hz		0.6			0.6			0.6		pA/√Hz
Input Resistance Differential Mode	R_{IN}			10			10			10		MΩ
Input Resistance Common Mode	R_{INCM}			200			200			200		GΩ
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V; R_L = 10 kΩ	5000	12000		3000	7000		3000	7000		V/mV
		R_L = 2 kΩ	2000	3500		1500	3000		1500	3000		V/mV
Input Voltage Range	IVR	Note 3	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	120	140		115	140		110	135		dB
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.1	1.8		0.1	3.2		0.2	5.6	µV/V
Output Voltage Swing	V_O	R_L = 10 kΩ	±12	±12.6		±12	±12.6		±12	±12.6		V
		R_L = 2 kΩ	±11	±12.2		±11	±12.2		±11	±12.2		V
Supply Current Per Amplifier	I_{SY}	No Load		600	725		600	725		600	725	µA
Slew Rate	SR		0.1	0.15		0.1	0.15		0.1	0.15		V/µs
Gain Bandwidth Product	GBWP	A_V = +1		500			500			500		kHz
Channel Separation	CS	V_O = 20 V p-p f_O = 10 Hz[2]	123	135		123	135		123	135		dB
Input Capacitance	C_{IN}			3.2			3.2			3.2		pF
Capacitive Load Stability		A_V = +1 No Oscillations		10			10			10		nF

NOTES
[1]Sample tested
[2]Guaranteed but not 100% tested.
[3]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[2]

Supply Voltage ..... ±20 V
Differential Input Voltage ..... ±30 V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP400A ..... –55°C to +125°C
OP400E, OP400F ..... –25°C to +85°C
OP400G ..... 0°C to +70°C
OP400H ..... –40°C to +85°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.
[2]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

Quad Precision, High Speed Operational Amplifier

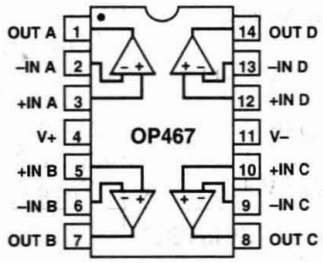
OP467

FEATURES
- High Slew Rate – 170 V/μs
- Wide Bandwidth – 28 MHz
- Fast Settling Time – <200 ns to 0.01%
- Low Offset Voltage – <500 μV
- Unity-Gain Stable
- Low Voltage Operation ±5 V to ±15 V
- Low Supply Current – <10 mA
- Drives Capacitive Loads

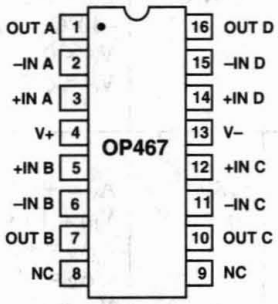
APPLICATIONS
- High Speed Image Display Drivers
- High Frequency Active Filters
- Fast Instrumentation Amplifiers
- High Speed Detectors
- Integrators
- Photo Diode Preamps

PIN CONNECTIONS

14-Lead Ceramic DIP (Y Suffix) and 14-Lead Epoxy DIP (P Suffix)

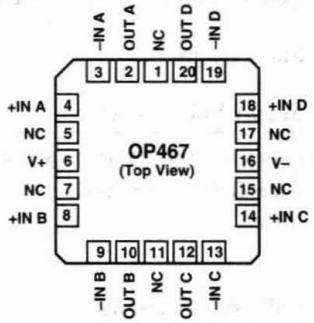


16-Lead SOL (S Suffix)



NC = NO CONNECT

20-Position Chip Carrier (RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP467 is a quad, high speed, precision operational amplifier. It offers the performance of a high speed op amp combined with the advantages of a precision operational amplifier all in a single package. The OP467 is an ideal choice for applications where, traditionally, more than one op amp was used to achieve this level of speed and precision.

The OP467's internal compensation ensures stable unity-gain operation, and it can drive large capacitive loads without oscillation. With a gain bandwidth product of 28 MHz driving a 30 pF load, output slew rate in excess of 170 V/μs, and settling time to 0.01% in less than 200 ns, the OP467 provides excellent dynamic accuracy in high speed data-acquisition systems. The channel-to-channel separation is typically 60 dB at 10 MHz.

The dc performance of OP467 includes less than 0.5 mV of offset, voltage noise density below 6 nV/√Hz and total supply current under 10 mA. Common-mode rejection and power supply rejection ratios are typically 85 dB. PSRR is maintained to better than 40 dB with input frequencies as high as 1 MHz. The low offset and drift plus high speed and low noise, make the OP467 usable in applications such as high speed detectors and instrumentation.

The OP467 is specified for operation from ±5 V to ±15 V over the extended industrial temperature range (–40°C to +85°C) and is available in 14-pin plastic and ceramic DIP, plus SOL-16 and 20-lead LCC surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP467AY/883	–55°C to +125°C	14-Pin Cerdip	Q-14
OP467ARC/883	–55°C to +125°C	20-Contact LCC	E-20A
OP467GP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP467GS	–40°C to +85°C	16-Pin SOL	R-16
OP467GBC	+25°C	DICE	

*For outline information see Package Information section.

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OP467–SPECIFICATIONS[1]

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	0.5	mV
		–40°C ≤ T_A ≤ +85°C			1	mV
Input Bias Current	I_B	V_{CM} = 0 V		150	600	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C		150	700	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		10	100	nA
		V_{CM} = 0 V, –40°C ≤ T_A ≤ +85°C		10	150	nA
Common-Mode Rejection	CMR	V_{CM} = ±12V	80	90		dB
	CMR	V_{CM} = ±12 V, –40°C ≤ T_A ≤ +85°C	80	88		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	86		dB
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	77.5			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			0.2		pA/°C
Long Term Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2			750	µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13.0	±13.5		V
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +85°C	±12.9	±13.12		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V_S = ±18 V	96	120		dB
		–40°C ≤ T_A ≤ +85°C	86	115		dB
Supply Current	I_{SY}	V_O = 0 V		8	10	mA
		V_O = 0 V, –40°C ≤ T_A ≤ +85°C			13	mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	A_V = +1, C_L = 30 pF		28		MHz
Slew Rate	SR	V_{IN} = 10 V Step, R_L = 2 kΩ, C_L = 30 pF				
		A_V = +1	125	170		V/µs
		A_V = –1		350		V/µs
Full-Power Bandwidth	BW_p	V_{IN} = 10 V Step		2.7		MHz
Settling Time	t_S	To 0.01%, V_{IN} = 10 V Step		200		ns
Phase Margin	θ_0			45		Degrees
Input Capacitance						
Common Mode				2.0		pF
Differential				1.0		pF
NOISE PERFORMANCE						
Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		8		pA/√Hz

NOTES

[1]For ±5 V specifications, request complete data sheet.

[2]Long Term Offset Voltage Drift is guaranteed by 1000 hrs. Life test performed on three independent wafer lots at +125 °C, with an LTPD of 1.3.

Specifications subject to change without notice.

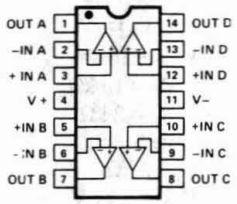
Very Low Noise Quad Operational Amplifier

OP470

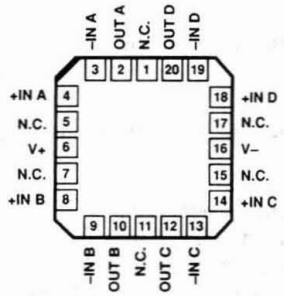
FEATURES
Very Low Noise: 5 nV/√Hz @ 1 kHz max
Excellent Input Offset Voltage: 0.4 mV max
Low Offset Voltage Drift: 2 μV/°C max
Very High Gain: 1000 V/mV min
Outstanding CMR: 110 dB min
Slew Rate: 2 V/μs typ
Gain-Bandwidth Product: 6 MHz typ
Industry Standard Quad Pinout
Available in Die Form

PIN CONNECTIONS

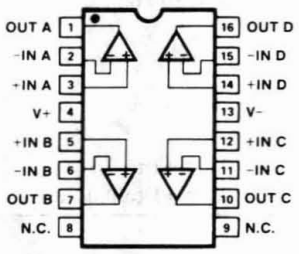
14-Pin Hermetic DIP (Y Suffix)
14-Pin Plastic Mini-DIP (P Suffix)



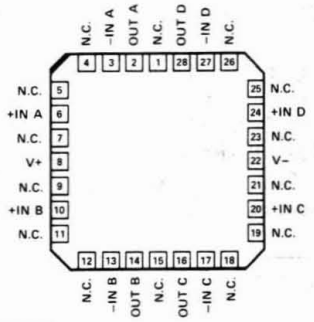
20-Lead LCC (RC Suffix)



16-Pin SOL (S Suffix)



28-Lead LCC (TC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP470 is a high performance monolithic quad operational amplifier with exceptionally low voltage noise, 5 nV/√Hz @ 1 kHz max, offering comparable performance to PMI's industry standard OP27.

The OP470 features an input offset voltage below 0.4 mV, excellent for a quad op amp, and an offset drift under 2 μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP470 is over 1,000,000 into a 10 kΩ load insuring excellent gain accuracy and linearity, even in high gain applications. Input bias current is under 25 nA which reduces errors due to signal source resistance. The OP470's CMR of over 110 dB and PSRR of less than 1.8 μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP470 is half that of four OP27s, a significant advantage for power conscious applications. The OP470 is unity-gain stable with a gain-bandwidth product of 6 MHz and a slew rate of 2 V/μs.

The OP470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, quad buffers, and low noise active filters.

The OP470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP471, with a slew rate of 8 V/μs, is recommended.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
OP470ARC/883C	400 μV	–55°C to +125°C	20-Lead LCC[3]
OP470AY[3]	400 μV	–55°C to +125°C	14-Pin Cerdip
OP470ATC/883C	400 μV	–55°C to +125°C	28-Lead LCC[3]
OP470EY	400 μV	–25°C to +85°C	14-Pin Cerdip
OP470FY	800 μV	–25°C to +85°C	14-Pin Cerdip
OP470GP	1000 μV	–40°C to +85°C	14-Pin Plastic DIP
OP470GS[4]	1000 μV	–40°C to +85°C	16-Pin SOL
OP470GS-REEL	1000 μV	–40°C to +85°C	16-Pin SOL

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip and plastic DIP packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[4]For availability and burn-in information on SO packages, contact your local sales office.

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OP470–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP470A/E Min	OP470A/E Typ	OP470A/E Max	OP470F Min	OP470F Typ	OP470F Max	OP470G Min	OP470G Typ	OP470G Max	Units
Input Offset Voltage	V_{OS}			0.1	0.4		0.2	0.8		0.4	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0 V		3	10		6	20		12	30	nA
Input Bias Current	I_B	V_{CM} = 0 V		6	25		15	50		25	60	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[1]		80	200		80	200		80	200	nV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[2]		3.8	6.5		3.8	6.5		3.8	6.5	nV/√Hz
		f_O = 100 Hz[2]		3.3	5.5		3.3	5.5		3.3	5.5	nV/√Hz
		f_O = 1 kHz[2]		3.2	5.0		3.2	5.0		3.2	5.0	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		1.7			1.7			1.7		pA/√Hz
		f_O = 100 Hz		0.7			0.7			0.7		pA/√Hz
		f_O = 1 kHz		0.4			0.4			0.4		pA/√Hz
Large-Signal Voltage Gain		V_O = ±10 V										
	A_{VO}	R_L = 10 kΩ	1000	2300		800	1700		800	1700		V/mV
		R_L = 2 kΩ	500	1200		400	900		400	900		V/mV
Input Voltage Range	IVR	Note 3	±11	±12		±11	±12		±11	±12		V
Output Voltage Swing	V_O	$R_L \geq 2$ kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	110	125		100	120		100	120		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.56	1.8		1.0	5.6		1.0	5.6	µV/V
Slew Rate	SR		1.4	2		1.4	2		1.4	2		V/µs
Supply Current (All Amplifiers)	I_{SY}	No Load		9	11		9	11		9	11	mA
Gain Bandwidth Product	GBW	A_V = +10		6			6			6		MHz
Channel Separation	CS	V_O = 20 V p-p,										
		f_O = 10 Hz[1]	125	155		125	155		125	155		dB
Input Capacitance	C_{IN}			2			2			2		pF
Input Resistance												
Differential-Mode	R_{IN}			0.4			0.4			0.4		MΩ
Input Resistance												
Common-Mode	R_{INCM}			11			11			11		GΩ
Settling Time	t_S	A_V = +1 to 0.1%		5.5			5.5			5.5		µs
		A_V = +1 to 0.01%		6.0			6.0			6.0		µs

NOTES
[1]Guaranteed but not 100% tested.
[2]Sample tested.
[3]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±1.0 V
Differential Input Current[2] ..... ±25 mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y Packages ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP470A ..... –55°C to +125°C
OP470E, OP470F ..... –25°C to +85°C
OP470G ..... –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The OP470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

High Speed, Low Noise Quad Operational Amplifier

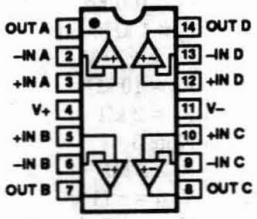
OP471

FEATURES

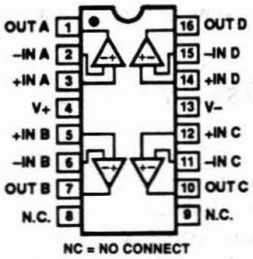
- Excellent Speed: 8 V/μs typ
- Low Noise: 11 nV/√Hz @ 1 kHz max
- Unity Gain Stable
- High Gain Bandwidth: 6.5 MHz typ
- Low Input Offset Voltage: 0.8 mV max
- Low Offset Voltage Drift: 4 μV/°C max
- High Gain: 500 V/mV min
- Outstanding CMR: 105 dB min
- Industry Standard Quad Pinout
- Available in Die Form

PIN CONNECTIONS

14-Pin Hermetic DIP (Y Suffix)
14-Pin Plastic DIP (P Suffix)

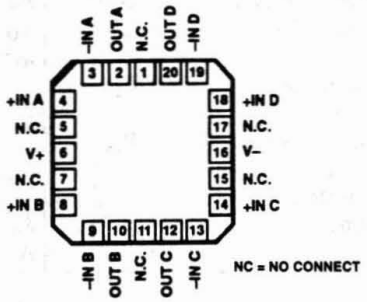


16-Pin SOL (S Suffix)



NC = NO CONNECT

20-Lead LCC (RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The OP471 is a monolithic quad op amp featuring low noise, 11 nV/√Hz max @ 1 kHz, excellent speed, 8 V/μs typical, a gain-bandwidth of 6.5 MHz, and unity-gain stability.

The OP471 has an input offset voltage under 0.8 mV and an input offset voltage drift below 4 μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP471 is over 500,000 into a 10 kΩ load insuring outstanding gain accuracy and linearity. The input bias current is under 25 nA limiting errors due to signal source resistance. The OP471's CMR of over 105 dB and PSRR of under 5.6 μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, quad buffers and low noise active filters.

The OP471 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP11, LM148/149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP470, with a voltage density of 5 nV/√Hz max @ 1 kHz, is recommended.

ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Option[2]
OP471AY[3]	800 μV	–55°C to +125°C	14-Pin Cerdip
OP471ARC/883	800 μV	–55°C to +125°C	20-Lead LCC
OP471EY	800 μV	–25°C to +85°C	14-Pin Cerdip
OP471FY	1500 μV	–25°C to +85°C	14-Pin Cerdip
OP471GP	1800 μV	–40°C to +85°C	14-Pin Plastic DIP
OP471GS[4]	1800 μV	–40°C to +85°C	16-Pin SOL

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip and plastic DIP packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[4]For availability and burn-in information on SO package, contact your local sales office.

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OP471–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP471A/E Min	OP471A/E Typ	OP471A/E Max	OP471F Min	OP471F Typ	OP471F Max	OP471G Min	OP471G Typ	OP471G Max	Units
Input Offset Voltage	V_{OS}			0.25	0.8		0.5	1.5		1.0	1.8	mV
Input Offset Current	I_{OS}	V_{CM} = 0 V		4	10		7	20		12	30	nA
Input Bias Current	I_B	V_{CM} = 0 V		7	25		15	50		25	60	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz[1]		250	500		250	500		250	500	nV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[2]		9	16		9	16		9	16	nV/√Hz
		f_O = 100 Hz[2]		7	12		7	12		7	12	nV/√Hz
		f_O = 1 kHz[2]		6.5	11		6.5	11		6.5	11	nV/√Hz
Input Noise Current Density	i_n	f_O = 10 Hz		1.7			1.7			1.7		pA/√Hz
		f_O = 100 Hz		0.7			0.7			0.7		pA/√Hz
		f_O = 1 kHz		0.4			0.4			0.4		pA/√Hz
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V										
		R_L = 10 kΩ	500	700		300	500		300	500		V/mV
		R_L = 2 kΩ	350	550		175	275		175	275		V/mV
Input Voltage Range	IVR	Note 3	±11	±12		±11	±12		±11	±12		V
Output Voltage Swing	V_O	$R_L \geq 2$ kΩ	±12	±13		±12	±13		±12	±13		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	105	120		95	115		95	115		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		1	5.6		5.6	17.8		5.6	17.8	µV/V
Slew Rate	SR		6.5	8		6.5	8		6.5	8		V/µs
Supply Current (All Amplifiers)	I_{SY}	No Load		9.2	11		9.2	11		9.2	11	mA
Gain Bandwidth Product	GBW	A_V = +10		6.5			6.5			6.5		MHz
Channel Separation	CS	V_O = 20 V p-p,										
		f_O = 10 Hz[1]	125	150		125	150		125	150		dB
Input Capacitance	C_{IN}			2.6			2.6			2.6		pF
Input Resistance Differential-Mode	R_{IN}			1.1			1.1			1.1		MΩ
Input Resistance Common-Mode	R_{INCM}			11			11			11		GΩ
Settling Time	t_S	A_V = +1 to 0.1%		4.5			4.5			4.5		µs
		A_V = +1 to 0.01%		7.5			7.5			7.5		µs

NOTES
[1]Guaranteed but not 100% tested.
[2]Sample tested.
[3]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Differential Input Voltage[2] ..... ±1.0 V
Differential Input Current[2] ..... ±25 mW
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, Y Packages ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP471A ..... –55°C to +125°C
OP471E, OP471F ..... –25°C to +85°C
OP471G ..... –40°C to +85°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
TO-99 (J)	xxx	xx	°C/W
8-Pin Hermetic DIP (Z)	x	x	°C/W
8-Pin Plastic DIP (P)	x	x	°C/W
20-Contact LCC (RC, TC)	x	x	°C/W
8-Pin SO (S)	x	x	°C/W
20-Contact PLCC (PC)	x	x	°C/W
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]The OP471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0 V, the input current should be limited to ±25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

Precision Picoampere Input Current Quad Operational Amplifier

OP497

FEATURES

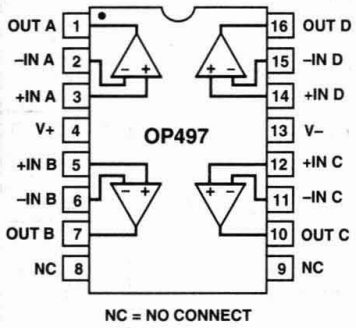
Low Offset Voltage: 50 μV max
Low Offset Voltage Drift: 0.5 μV/°C max
Very Low Bias Current
+25°C: 100 pA max
–55°C to +125°C: 450 pA max
Very High Open-Loop Gain: 2000 V/mV min
Low Supply Current (per Amplifier): 625 μA max
Operates from ±2 V to ±20 V Supplies
High Common-Mode Rejection: 120 dB min

APPLICATIONS

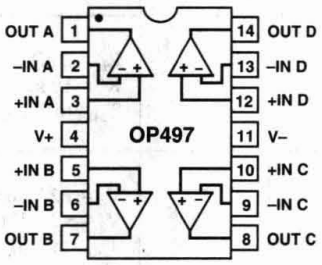
Strain Gage and Bridge Amplifiers
High Stability Thermocouple Amplifiers
Instrumentation Amplifiers
Photo-Current Monitors
High Gain Linearity Amplifiers
Long-Term Integrators/Filters
Sample-and-Hold Amplifiers
Peak Detectors
Logarithmic Amplifiers
Battery-Powered Systems

PIN CONNECTIONS

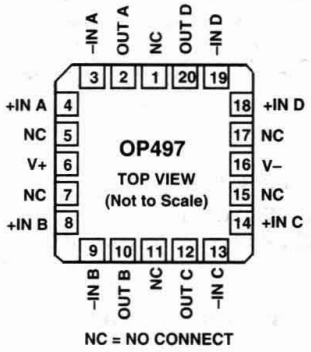
16-Lead Wide Body SOIC
(S Suffix)



14-Lead Plastic DIP
(P Suffix)
14-Lead Ceramic DIP
(Y Suffix)



20-Position Chip Carrier
(RC Suffix)



GENERAL DESCRIPTION

The OP497 is a quad op amp with precision performance in the space saving, industry standard 16-pin SOIC package. Its combination of exceptional precision with low power and extremely low input bias current makes the quad OP497 useful in a wide variety of applications.

Precision performance of the OP497 includes very low offset, under 50 μV, and low drift, below 0.5 μV/°C. Open-loop gain exceeds 2000 V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP497's common-mode rejection of over 120 dB. The OP497's power supply rejection of over 120 dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP497 is under 625 μA per amplifier, and it can operate with supply voltages as low as ±2 V.

The OP497 utilizes a superbeta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP497 is under 100 pA at 25°C and is under 450 pA over the military temperature range.

Combining precision, low power and low bias current, the OP497 is ideal for a number of applications including instrumentation amplifiers, log amplifiers, photodiode preamplifiers and long-term integrators. For a single device see the OP97, for a dual see the OP297.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
OP497AY	–55°C to +125°C	14-Pin Cerdip	Q-14
OP497BY/883C	–55°C to +125°C	14-Pin Cerdip	Q-14
OP497CY	–55°C to +125°C	14-Pin Cerdip	Q-14
OP497BRC/883	–55°C to +125°C	20-Contact LCC	E-20A
OP497FY	–40°C to +85°C	14-Pin Cerdip	Q-14
OP497FP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP497FS	–40°C to +85°C	16-Pin SOIC	R-16
OP497GP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP497GS	–40°C to +85°C	16-Pin SOIC	R-16
OP497GS-REEL	–40°C to +85°C	16-Pin SOIC	R-16

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

OP497–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	A Min	A Typ	A Max	B/F Min	B/F Typ	B/F Max	C/G Min	C/G Typ	C/G Max	Units
INPUT CHARACTERISTICS												
Offset Voltage	V_{OS}			20	50		40	75		80	150	µV
		–40°C < T_A < +85°C					70	150		120	250	
		–55°C < T_A < +125°C		40	100		80	150		140	300	
Average Input Offset Voltage Drift	TCV_{OS}	T_{MIN} to T_{MAX}		0.2	0.5		0.4	1.0		0.6	1.5	µV/°C
Long Term Input Offset Voltage Stability				0.1			0.1			0.1		µV/Mo
Input Bias Current	I_B	V_{CM} = 0 V		30	100		40	150		60	200	pA
		–40°C < T_A < +85°C					60	200		80	300	
		–55°C < T_A < +125°C		80	450		110	600		130	600	
Average Input Bias Current Drift	TC_{IB}	–40°C < T_A < +85°C					0.3			0.3		
		–55°C < T_A < +125°C		0.5			0.7			0.7		pA/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		15	100		30	150		50	200	pA
		–40°C < T_A < +85°C					50	200		80	300	
		–55°C < T_A < +125°C		35	400		60	600		90	600	
Average Input Offset Current Drift	T_CI_{OS}			0.2			0.3			0.4		pA/°C
Input Voltage Range[1]	IVR		±13	±14		±13	±14		±13	±14		V
		T_{MIN} to T_{MAX}	±13	±13.5		±13	±13.5		±13	±13.5		
Common-Mode Rejection	CMR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
		T_{MIN} to T_{MAX}	114	130		108	120		108	120		
Large Signal Voltage Gain	A_{VO}	V_O = +10 V, R_L = 2 kΩ	2000	6000		1500	4000		1200	4000		V/mV
		–40°C ≤ T_A ≤ +85°C				800	2000		800	2000		
		–55°C ≤ T_A ≤ +125°C	1200	4000		1000	3000		800	3000		
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common Mode	R_{INCM}			500			500			500		GΩ
Input Capacitance	C_{IN}			3			3			3		pF
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7		V
		R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		
		T_{MIN} to T_{MAX}, R_L = 10 kΩ	±13	±13.5		±13	±13.5		±13	±13.5		
Short Circuit	I_{SC}			±25			±25			±25		mA
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±20 V	120	140		114	135		114	135		dB
		V_S = ±2.5 V to ±20 V										
		T_{MIN} to T_{MAX}	114	130		108	120		108	120		
Supply Current (per Amplifier)	I_{SY}	No Load		525	625		525	625		525	625	µA
		T_{MIN} to T_{MAX}		580	750		580	750		580	750	
Supply Voltage Range	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
		T_{MIN} to T_{MAX}	±2.5		±20	±2.5		±20	±2.5		±20	
DYNAMIC PERFORMANCE												
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µs
Gain Bandwidth Product	GBW			500			500			500		kHz
Channel Separation	CS	V_O = 20 V p-p, f_O = 10 Hz		150			150			150		dB
NOISE PERFORMANCE												
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3			0.3			0.3		µV p-p
Voltage Noise Density	e_n = 10 Hz			17			17			17		nV/√Hz
	e_n = 1 kHz			15			15			15		nV/√Hz
Current Noise Density	i_n = 10 Hz			20			20			20		fA/√Hz

NOTES

[1]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±20 V
Input Voltage[2] . . . . . ±20 V
Differential Input Voltage[2] . . . . . 40 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Y, RC Package . . . . . –65°C to +175°C
  P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
  OP497A, B, C (Y) . . . . . –55°C to +125°C
  OP497F, G (Y) . . . . . –40°C to +85°C
  OP497F, G (P, S) . . . . . –40°C to +85°C
Junction Temperature
  Y, RC Package . . . . . –65°C to +175°C
  P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}	θ_{JC}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	33	°C/W
16-Pin SOIC (S)	92	23	°C/W

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References–Selection Guides

Single Output

Model	Nominal Output Voltage Volts	Initial Calibration mV	Ref Drift ppm/°C	Noise 0.1 Hz to 10 Hz µV p-p	Long Term Stability/ 1000 Hrs µV	I_Q mA	I_{OUT} mA	# Pins	Page No.	Comments	Fax-code
AD1580	1.225	1–10	50–100	5	NS	50 µA	NA	2	11–21	Two Terminal, SOT-23	1963
AD589	1.235	15	10–100	5	NS	5	NA	2	11–13	Two Terminal	1185
REF191	+2.048	2–10	5–25	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761
REF03G	+2.5	15	50	6	NS	1.4	10	8	11–27	Low Cost	1757
REF43	+2.5	5–30	10–25	10	1 ppm/Mon	0.6	20	8/20	11–29		1762
AD580J	+2.5	10–75	10–85	60	250	2	10	3	*		1176
AD680J	+2.5	50–100	20–25	10	63	0.250	10	8	11–15	Low Power	1231
AD1403A	+2.5	5–25	25	NS	NS	1.50		8	*		1058
AD1403	+2.5	25	40	NS	NS	1.5	10	8	*		1058
REF192	+2.5	2–10	5–25	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761
AD780	+2.5–3	1–5	3–7	4	20	1	±10	8	11–19	Very Low Noise, Pin Strap +2.5 or +3.0 V	1355
AD586	+5	2–25	2–20	4	75	3	±10	8	11–7	Can Be Used at –5 V	1182
REF02	+5	5–100	8.5–250	1	NS	1.4	10	8	11–25		1756
AD587	+10	5–10	5–20	4	150	4	±10	8	11–9	Can Be Used at –10 V	1183
AD581	+10	5–30	5–30	50	250	1	10	3	*		1177
REF01	+10	30–100	8.5–65	30	NS	1.4	10	8	11–23		1755
REF193	+3	10	25	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761
REF196	+3.3	10	25	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761
REF198	+4.5	2–10	4–8	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761
REF194	+4.5	2–10	5–25	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761
REF195	+5	2–10	5–25	50	NS	45 µA	30	8	11–31	Low Dropout & Power	1761

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Model	# of Buffer Amps	Output Voltage Option Volts	Initial Calibration Error ±mV	PPM Grades ppm	Tracking Error ±mV	Noise 0.1 Hz to 10 Hz μV p-p	Long Term Stability/ 1000 Hrs ppm	I_Q mA	I_{OUT} mA	# Pins	Page No.	Fax-code
AD588	2					6	15	10	10	16	11–11	1184
		+10	5	1.5, 3, 4, 6								
		+5	5	1.5, 3, 4, 6								
		±5	5	1.5, 3, 4, 6	1.5							
		–5	5	1.5, 3, 4, 6								
		–10	5	1.5, 3, 4, 6								
AD688	2	+10	2, 5	3, 6		6	15	12	10	16	11–17	1234
		±10	2, 5	3, 6	3							
		–10	2, 5	3, 6								
AD584	1	+10	5–30	15, 30		50	25	1	10	8	11–5	1180
		+7.5	4–20	15, 30								
		+5	3–15	15, 30								
		+2.5	2.5–7.5	15, 30								

Pin Programmable Precision Voltage Reference

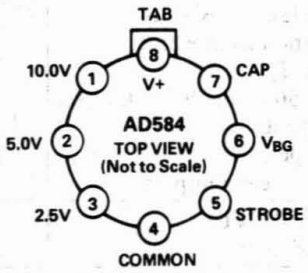
AD584*

FEATURES

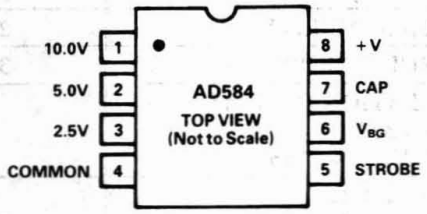
Four Programmable Output Voltages:
10.000 V, 7.500 V, 5.000 V, 2.500 V
Laser-Trimmed to High Accuracies
No External Components Required
Trimmed Temperature Coefficient:
5 ppm/°C max, 0°C to +70°C (AD584L)
15 ppm/°C max, –55°C to +125°C (AD584T)
Zero Output Strobe Terminal Provided
Two Terminal Negative Reference Capability (5 V & Above)
Output Sources or Sinks Current
Low Quiescent Current: 1.0 mA max
10 mA Current Output Capability
MIL-STD-883 Compliant Versions Available

PIN CONFIGURATIONS

8-Pin TO-99



8-Pin DIP



GENERAL DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000 V, 7.500 V, 5.000 V and 2.500 V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100 μA. In the "on" state the total supply current is typically 750 μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14-bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K and L are specified for operation from 0°C to +70°C; the AD584S and T are specified for the –55°C to +125°C range. All grades are packaged in a hermetically sealed eight-terminal TO-99 metal can; the AD584 J and K are also available in an 8-pin plastic DIP.

***Protected by U.S. Patent No. 3,887,863; RE 30,586**

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25 mV from 0°C to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10 V, 7.5 V and 5 V outputs).
5. The AD584 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD584/883B data sheet for detailed specifications.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD584—SPECIFICATIONS (@ V_{IN} = +15 V and 25°C)

Model	AD584J			AD584K			AD584L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal Outputs of:										
10.000 V			±30			±10			±5	mV
7.500 V			±20			±8			±4	mV
5.000 V			±15			±6			±3	mV
2.500 V			±7.5			±3.5			±2.5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C Value, T_{MIN} to T_{MAX}[2]										
10.000 V, 7.500 V, 5.000 V Outputs			30			15			5	ppm/°C
2.500 V Output			30			15			10	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE (0.1 Hz to 10 Hz)		50			50			50		µV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
15 V ≤ V_{IN} ≤ 30 V			0.002			0.002			0.002	%/V
(V_{OUT} +2.5 V) ≤ V_{IN} ≤ 15 V			0.005			0.005			0.005	%/V
LOAD REGULATION										
0 ≤ I_{OUT} ≤ 5 mA, All Outputs		20	50		20	50		20	50	ppm/mA
OUTPUT CURRENT										
V_{IN} ≥ V_{OUT} +2.5 V										
Source @ +25°C	10			10			10			mA
Source T_{MIN} to T_{MAX}	5			5			5			mA
Sink T_{MIN} to T_{MAX}	5			5			5			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	–65		+175	–65		+175	–65		+175	°C
PACKAGE OPTION[3]										
TO-99 (H-08A)	AD584JH			AD584KH			AD584LH			
Plastic (N-8)	AD584JN			AD584KN						

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]H = Hermetic Metal Can; N = Plastic DIP. For outline information see Package Information section.

Specifications subject to change without notice.

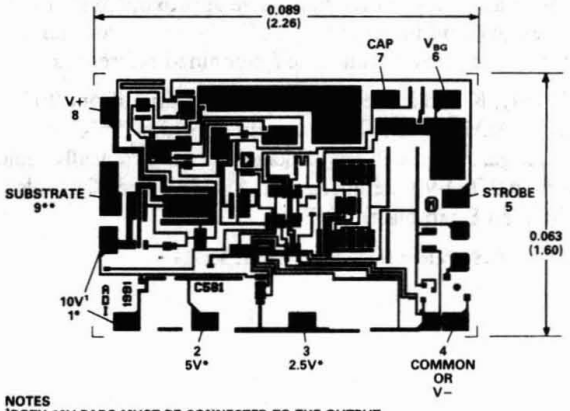
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Input Voltage V_{IN} to Ground ..... 40 V
Power Dissipation @ +25°C ..... 600 mW
Operating Junction Temperature Range ....–55°C to +125°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Thermal Resistance
Junction-to-Ambient (H-08A) ..... 150°C/W

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



NOTES
¹BOTH 10V PADS MUST BE CONNECTED TO THE OUTPUT.
*INTERCONNECTIONS REQUIRED; SEE PIN DESIGNATIONS FOR INFORMATION.
**NOT BROUGHT OUT IN PACKAGE DEVICE.
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8-PIN METAL PACKAGE.

ANALOG DEVICES

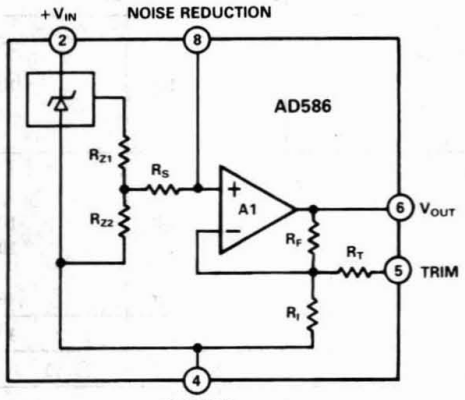
High Precision 5 V Reference

AD586

FEATURES

Laser Trimmed to High Accuracy:
5.000 V ±2.0 mV (M Grade)
Trimmed Temperature Coefficient:
2 ppm/°C max, 0°C to +70°C (M Grade)
5 ppm/°C max, –40°C to +85°C (B & L Grades)
10 ppm/°C max, –55°C to +125°C (T Grade)
Low Noise, 100 nV/$\sqrt{Hz}$
Noise Reduction Capability
Output Trim Capability
MIL-STD-883 Compliant Versions Available
Industrial Temperature Range SOICs Available
Output Capable of Sourcing or Sinking 10 mA

FUNCTIONAL BLOCK DIAGRAM



NOTE: PINS 1, 3 & 7 ARE INTERNAL TEST POINTS. MAKE NO CONNECTIONS TO THESE POINTS.

PRODUCT DESCRIPTION

The AD586 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD586 provides outstanding performance at low cost.

The AD586 offers much higher performance than most other 5 V references. Because the AD586 uses an industry standard pinout, many systems can be upgraded instantly with the AD586. The buried Zener approach to reference design provides lower noise and drift than bandgap voltage references. The AD586 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD586 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD586J, K, L and M are specified for operation from 0°C to +70°C, the AD586A and B are specified for –40°C to +85°C operation, and the AD586S and T are specified for –55°C to +125°C operation. The AD586J, K, L and M are available in an 8-pin plastic DIP. The AD586J, K, L, A and B are available in an 8-pin plastic surface mount small outline (SO) package. The AD586J, K, L, S and T are available in an 8-pin cerdip package.

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ORDERING GUIDE

Model[1]	Initial Error	Temperature Coefficient	Temperature Range	Package Option[2]
AD586JN	20 mV	25 ppm/°C	0°C to +70°C	N-8
AD586JQ	20 mV	25 ppm/°C	0°C to +70°C	Q-8
AD586JR	20 mV	25 ppm/°C	0°C to +70°C	SO-8
AD586KN	5 mV	15 ppm/°C	0°C to +70°C	N-8
AD586KQ	5 mV	15 ppm/°C	0°C to +70°C	Q-8
AD586KR	5 mV	15 ppm/°C	0°C to +70°C	SO-8
AD586LN	2.5 mV	5 ppm/°C	0°C to +70°C	N-8
AD586LR	2.5 mV	5 ppm/°C	0°C to +70°C	SO-8
AD586MN	2 mV	2 ppm/°C	0°C to +70°C	N-8
AD586AR	5 mV	15 ppm/°C	–40°C to +85°C	SO-8
AD586BR	2.5 mV	5 ppm/°C	–40°C to +85°C	SO-8
AD586LQ	2.5 mV	5 ppm/°C	0°C to +70°C	Q-8
AD586SQ	10 mV	20 ppm/°C	–55°C to +125°C	Q-8
AD586TQ	2.5 mV	10 ppm/°C	–55°C to +125°C	Q-8
AD586JCHIPS	20 mV	25 ppm/°C	0°C to +70°C	

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD586/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip; SO = Small Outline IC (SOIC). For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD586—SPECIFICATIONS (@ T_A = +25°C, V_{IN} = +15 V unless otherwise noted)

Model	AD586J Min	Typ	Max	AD586K/A Min	Typ	Max	AD586L/B Min	Typ	Max	AD586M Min	Typ	Max	AD586S Min	Typ	Max	AD586T Min	Typ	Max	Units
Output Voltage	4.980		5.020	4.995		5.005	4.9975		5.0025	4.998		5.002	4.990		5.010	4.9975		5.0025	V
Output Voltage Drift[1]																			
0°C to +70°C			25			15			5			2							ppm/°C
–55°C to +125°C															20			10	
Gain Adjustment	+6			+6			+6			+6			+6			+6			%
	–2			–2			–2			–2			–2			–2			
Line Regulation[1]																			
10.8 V < +V_{IN} < 36 V																			
T_{MIN} to T_{MAX}			100			100			100			100							±μV/V
11.4 V < +V_{IN} < 36 V																			
T_{MIN} to T_{MAX}															150			150	
Load Regulation[1]																			
Sourcing 0 < I_{OUT} < 10 mA																			
25°C			100			100			100			100			150			150	μV/mA
T_{MIN} to T_{MAX}			100			100			100			100			150			150	
Sinking –10 < I_{OUT} < 0 mA																			
25°C			400			400			400			400			400			400	
Quiescent Current		2	3		2	3		2	3		2	3		2	3		2	3	mA
Power Consumption		30			30			30			30			30			30		mW
Output Noise																			
0.1 Hz to 10 Hz		4			4			4			4			4			4		μV p-p
Spectral Density, 100 Hz		100			100			100			100			100			100		nV/√Hz
Long-Term Stability		15			15			15			15			15			15		ppm/1000 Hr
Short-Circuit Current-to-Ground		45	60		45	60		45	60		45	60		45	60		45	60	mA
Temperature Range																			
Specified Performance[2]	0		+70	0		+70	0		+70	0		+70	–55		+125	–55		+125	°C
				–40		+85	–40		+85										
Operating Performance[3]	–40		+85	–40		+85	–40		+85	–40		+85	–55		+125	–55		+125	

NOTES
[1]Maximum output voltage drift is guaranteed for all packages and grades. Cerdip packaged parts are also 100°C production tested.
[2]Lower row shows specified performance for A and B grades.
[3]The operating temperature range is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

Specifications subject to change without notice.

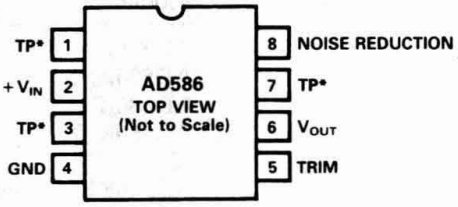
Specifications in boldface are rested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground ..... 36 V
Power Dissipation (25°C) ..... 500 mW
Storage Temperature ..... –65°C to +150°C
Lead Temp (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
θ_{JC} ..... 22°C/W
θ_{JA} ..... 110°C/W
Output Protection: Output safe for indefinite short to ground or V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM
(Top View)



*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

ANALOG DEVICES

High Precision 10 V Reference

AD587

FEATURES

Laser Trimmed to High Accuracy:
10.000 V ±5 mV (L and U Grades)
Trimmed Temperature Coefficient:
5 ppm/°C max, (L and U Grades)
Noise Reduction Capability
Low Quiescent Current: 4 mA max
Output Trim Capability
MIL-STD-883 Compliant Versions Available

PRODUCT DESCRIPTION

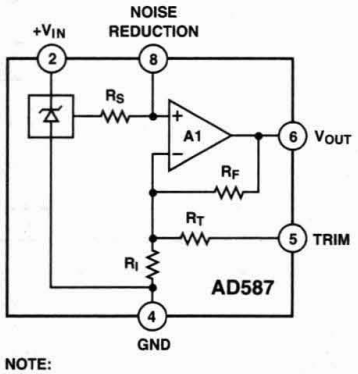
The AD587 represents a major advance in the state-of-the-art in monolithic voltage references. Using a proprietary ion-implanted buried Zener diode and laser wafer trimming of high stability thin-film resistors, the AD587 provides outstanding performance at low cost.

The AD587 offers much higher performance than most other 10 V references. Because the AD587 uses an industry standard pinout, many systems can be upgraded instantly with the AD587. The buried Zener approach to reference design provides lower noise and drift than bandgap voltage references. The AD587 offers a noise reduction pin which can be used to further reduce the noise level generated by the buried Zener.

The AD587 is recommended for use as a reference for 8-, 10-, 12-, 14- or 16-bit D/A converters which require an external precision reference. The device is also ideal for successive approximation or integrating A/D converters with up to 14 bits of accuracy and, in general, can offer better performance than the standard on-chip references.

The AD587J, K and L are specified for operation from 0°C to +70°C, and the AD587S, T and U are specified for –55°C to +125°C operation. All grades are available in 8-pin cerdip. The J and K versions are also available in an 8-pin Small Outline IC (SOIC) package for surface mount applications, while the J, K and L grades also come in an 8-pin plastic package.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
PINS 1,3 AND 7 ARE INTERNAL TEST POINTS.
NO CONNECTIONS TO THESE POINTS.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficients results in very low errors over temperature without the use of external components. The AD587L has a maximum deviation from 10.000 V of ±8.5 mV between 0°C and +70°C, and the AD587U guarantees ±14 mV maximum total error between –55°C and +125°C.
2. For applications requiring higher precision, an optional fine trim connection is provided.
3. Any system using an industry standard pinout 10 volt reference can be upgraded instantly with the AD587.
4. Output noise of the AD587 is very low, typically 4 µV p-p. A noise reduction pin is provided for additional noise filtering using an external capacitor.
5. The AD587 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD587/883B data sheet for detailed specifications.

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ORDERING GUIDE

Model[1]	Initial Error	Temperature Coefficient	Temperature Range	Package Options[2]
AD587JQ	10 mV	20 ppm/°C	0°C to +70°C	Q-8
AD587JR	10 mV	20 ppm/°C	0°C to +70°C	SO-8
AD587JN	10 mV	20 ppm/°C	0°C to +70°C	N-8
AD587KQ	5 mV	10 ppm/°C	0°C to +70°C	Q-8
AD587KR	5 mV	10 ppm/°C	0°C to +70°C	SO-8
AD587KN	5 mV	10 ppm/°C	0°C to +70°C	N-8
AD587LQ	5 mV	5 ppm/°C	0°C to +70°C	Q-8
AD587LN	5 mV	5 ppm/°C	0°C to +70°C	N-8
AD587SQ	10 mV	20 ppm/°C	–55°C to +125°C	Q-8
AD587TQ	10 mV	10 ppm/°C	–55°C to +125°C	Q-8
AD587UQ	5 mV	5 ppm/°C	–55°C to +125°C	Q-8
AD587JCHIPS	10 mV	20 ppm/°C	0°C to +70°C	

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD587/883B data sheet.
[2]N = Plastic DIP; Q = Cerdip; SO = SOIC. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD587—SPECIFICATIONS (T_A = +25°C, V_{IN} = +15 V unless otherwise noted)

Model	AD587J/S			AD587K/T			AD587L/U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE	9.990		10.010	9.995		10.005	9.995		10.005	V
OUTPUT VOLTAGE DRIFT[1]										
0°C to +70°C			20			10			5	ppm/°C
−55°C to +125°C			20			10			5	
GAIN ADJUSTMENT	+3			+3			+3			%
	−1			−1			−1			
LINE REGULATION[1]										
13.5 V ≤ + V_{IN} ≤ 36 V										
T_{MIN} to T_{MAX}			100			100			100	±µV/V
LOAD REGULATION[1]										
Sourcing 0 < I_{OUT} < 10 mA										
T_{MIN} to T_{MAX}			100			100			100	±µV/mA
Sourcing −10 < I_{OUT} < 0 mA[2]										
T_{MIN} to T_{MAX}			100			100			100	
QUIESCENT CURRENT		2	4		2	4		2	4	mA
POWER DISSIPATION		30			30			30		mW
OUTPUT NOISE										
0.1 Hz to 10 Hz		4			4			4		µV p-p
Spectral Density, 100 Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY		15			15			15		±ppm/1000 Hr.
SHORT-CIRCUIT CURRENT-TO-GROUND		30	50		30	50		30	50	mA
SHORT-CIRCUIT CURRENT-TO-V_{IN}		30	50		30	50		30	50	mA
TEMPERATURE RANGE										
Specified Performance (J, K, L)	0		+70	0		+70	0		+70	°C
Operating Performance (J, K, L)[3]	−40		+85	−40		+85	−40		+85	
Specified Performance (S, T, U)	−55		+125	−55		+125	−55		+125	
Operating Performance (S, T, U)[3]	−55		+125	−55		+125	−55		+125	

NOTES

[1]Spec is guaranteed for all packages and grades. Cerdip packaged parts are 100% production test.

[2]Load Regulation (Sinking) specification for SOIC (R) package is ±200 µV/mA.

[3]The operating temperature ranged is defined as the temperatures extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

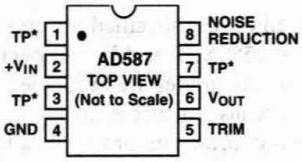
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground ..... 36 V
Power Dissipation (+25°C) ..... 500 mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
θ_{JC} ..... 22°C/W
θ_{JA} ..... 110°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

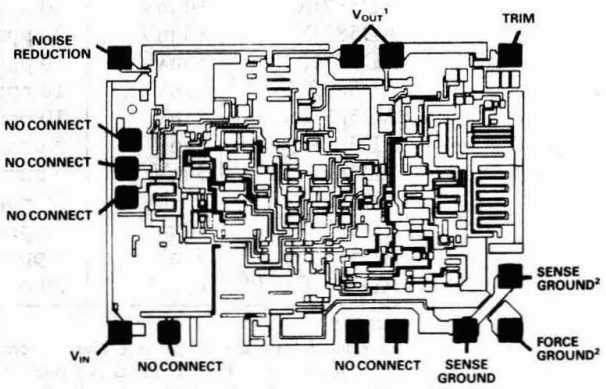
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

DIE LAYOUT



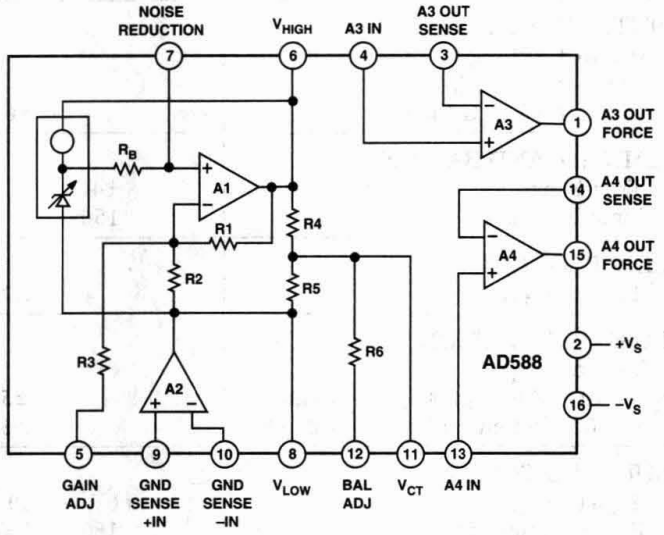
ANALOG DEVICES

High Precision Voltage Reference

AD588*

FEATURES
Low Drift: 1.5 ppm/°C
Low Initial Error: 1 mV
Pin-Programmable Output
+10 V, +5 V, ±5 V Tracking, –5 V, –10 V
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine-Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. Low initial error and low temperature drift give the AD588 absolute accuracy performance previously not available in monolithic form. The AD588 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift trimming of high stability thin-film resistors to provide outstanding performance at low cost.

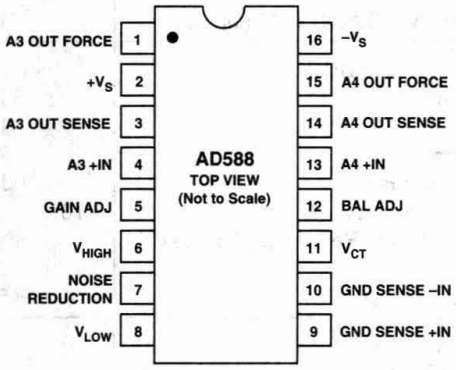
The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift to maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads, delivering the full accuracy of the AD588 where it is required in the application circuit.

The low initial error allows the AD588 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 in conjunction autocalibration software.

The AD588 is available in seven versions. The AD588 JQ and KQ grades are packaged in a 16-pin cerdip and are specified for 0°C to +70°C operation. AD588AQ and BQ grades are packaged in a 16-pin cerdip and are specified for the –25°C to +85°C industrial temperature range. The ceramic AD588SQ and TQ grades are specified for the full military/aerospace temperature range. For military surface mount applications, the AD588SE and TE grades are also available in 20-pin LCC packages.

***Covered by Patent Number 4,644,253.**

PIN CONFIGURATION



ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range	Package Option[2]
AD588AQ	3 mV	3 ppm/°C	–25°C to +85°C	Cerdip (Q-16)
AD588BQ	1 mV	1.5 ppm/°C	–25°C to +85°C[3]	Cerdip (Q-16)
AD588SQ	5 mV	6 ppm/°C	–55°C to +125°C	Cerdip (Q-16)
AD588TQ	3 mV	4 ppm/°C	–55°C to +125°C	Cerdip (Q-16)
AD588JQ	3 mV	3 ppm/°C	0°C to +70°C	Cerdip (Q-16)
AD588KQ	1 mV	1.5 ppm/°C	0°C to +70°C	Cerdip (Q-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD588/883B.
[2]For outline information see Package Information section.
[3]Temperature coefficient specified from 0°C to +70°C.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD588—SPECIFICATIONS (typical @ + 25°C, +10 V output, V_S = ±15 V unless otherwise noted[1])

	AD588SQ			AD588JQ/AQ/TQ			AD588KQ/BQ			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR										
+10 V, –10 V Outputs	–5		+5	–3		+3	–1		+1	mV
+5 V, –5 V Outputs	–5		+5	–3		+3	–1		+1	mV
±5 V TRACKING MODE										
Symmetry Error	–1.5		+1.5	–1.5		+1.5	–0.75		+0.75	mV
OUTPUT VOLTAGE DRIFT										
0°C to +70°C (J, K, B)				–3	±2	+3	–1.5		+1.5	ppm/°C
–25°C to +85°C (A, B)				–3		+3	–3		+3	ppm/°C
–55°C to +125°C (S, T)	–6		+6	–4		+4				ppm/°C
GAIN ADJ AND BAL ADJ[2]										
Trim Range		±4			±4			±4		mV
Input Resistance		150			150			150		kΩ
LINE REGULATION										
T_{MIN} to T_{MAX}[3]			±200			±200			±200	µV/V
LOAD REGULATION										
T_{MIN} to T_{MAX}										
+10 V Output, 0 < I_{OUT} < 10 mA			±50			±50			±50	µV/mA
–10 V Output, –10 < I_{OUT} < 0 mA			±50			±50			±50	µV/mA
SUPPLY CURRENT										
T_{MIN} to T_{MAX}		6	10		6	10		6	10	mA
Power Dissipation		180	300		180	300		180	300	mW
OUTPUT NOISE (Any Output)										
0.1 Hz to 10 Hz		6			6			6		µV p-p
Spectral Density, 100 Hz		100			100			100		nV/√Hz
LONG-TERM STABILITY (@ +25°C)		15			15			15		ppm/1000 hr
BUFFER AMPLIFIERS										
Offset Voltage		100			100			10		µV
Offset Voltage Drift		1			1			1		µV/°C
Bias Current		20			20			20		nA
Open Loop Gain		110			110			110		dB
Output Current A3, A4	–10		+10	–10		+10	–10		+10	mA
Common-Mode Rejection (A3, A4)										
V_{CM} = 1 V p-p		100			100			100		dB
Short-Circuit Current		50			50			50		mA
TEMPERATURE RANGE										
Specified Performance										
J, K Grades				0		+70	0		+70	°C
A, B Grades				–25		+85	–25		+85	°C
S, T Grades	–55		+125	–55		+125				°C

NOTES

[1]Output — Configuration
+10 V — Figure 2a
–10 V — Figure 2c
+5 V, –5 V, ±5 V — Figure 2b

Specifications tested using +10 V configuration unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Conditions:

+10 V Output	$-V_S$ = –15 V, 13.5 V ≤ $+V_S$ ≤ 18 V
–10 V Output	–18 V ≤ $-V_S$ ≤ –13.5 V, $+V_S$ = 15 V
±5 V Output	$+V_S$ = +18 V, $-V_S$ = –18 V
	$+V_S$ = +10.8 V, $-V_S$ = –10.8 V

Specifications subject to change without notice

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$ ..... 36 V
Power Dissipation (+25°C)
Q Package ..... 600 mW
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C
Package Thermal Resistance
Q (θ_{JA}/θ_{JC}) ..... 90/25°C/W
Output Protection: All Outputs Safe If Shorted to Ground

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Two-Terminal IC 1.2 V Reference

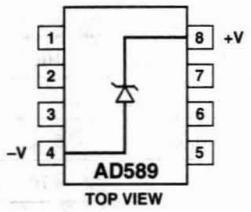
AD589

FEATURES

Superior Replacement for Other 1.2 V References
Wide Operating Range: 50 μA to 5 mA
Low Power: 60 μW Total P_D at 50 μA
Low Temperature Coefficient:
10 ppm/°C max, 0°C to +70°C (AD589M)
25 ppm/°C max, –55°C to +125°C (AD589U)
Two-Terminal "Zener" Operation
Low Output Impedance: 0.6 Ω
No Frequency Compensation Required
Low Cost
MIL-STD-883 Compliant Versions Available

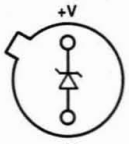
FUNCTIONAL BLOCK DIAGRAMS

SOIC (SO-8)



TOP VIEW

Metal Can (H-02A)



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23 V output voltage for input currents between 50 μA and 5.0 mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC Zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0°C to +70°C operation, while the S, T, and U grades are rated for the full –55°C to +125°C temperature range. All grades are available in a metal can (H-02A) package. The AD589J is also available in an 8-pin SOIC package.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6 Ω and temperature coefficients as low as 10 ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50 μA (60 μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589 is an exact replacement for other 1.2 V references, offering superior temperature performance and reduced sensitivity to capacitive loading.
6. The AD589 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD589/883B data sheet for detailed specifications.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD589–SPECIFICATIONS (typical @ I_{IN} = 500 µA and T_A = +25°C unless otherwise noted)

Model	AD589JH/JR			AD589KH			AD589LH			AD589MH			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50 µA–5 mA)			5			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	2		0.6	2		0.6	2		0.6	2	Ω
RMS NOISE VOLTAGE 10 Hz < f < 10 kHz		5			5			5			5		µV
TEMPERATURE COEFFICIENT[1]			100			**50**			25			**10**	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25			25		µs
OPERATING CURRENT[2]	**0.05**		5	**0.05**		5	**0.05**		5	**0.05**		5	mA
OPERATING TEMPERATURE	0		+70	0		+70	0		+70	0		+70	°C
PACKAGE OPTION[3] Metal Can (H-02A) SOIC (R-8)	AD589JH AD589JR			AD589KH			AD589LH			AD589MH			

Model	AD589SH			AD589TH			AD589UH			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE, T_A = +25°C	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	**1.200**	1.235	**1.250**	V
OUTPUT VOLTAGE CHANGE vs. CURRENT (50 µA–5 mA)			5			5			5	mV
DYNAMIC OUTPUT IMPEDANCE		0.6	2		0.6	2		0.6	2	Ω
RMS NOISE VOLTAGE 10 Hz < f < 10 kHz		5			5			5		µV
TEMPERATURE COEFFICIENT[1]			**100**			**50**			**25**	ppm/°C
TURN-ON SETTLING TIME TO 0.1%		25			25			25		µs
OPERATING CURRENT[2]	**0.05**		5	**0.05**		5	**0.05**		5	mA
OPERATING TEMPERATURE	–55		+125	–55		+125	–25		+125	°C
PACKAGE OPTION[3] Metal Can (H-02A) SOIC (SO-8)	AD589SH AD589JR			AD589TH			AD589UH			

NOTES

[1]See the following page for explanation of temperature coefficient measurement method.

[2]Optimum performance is obtained at currents below 500 µA. For current operation below 200 µA, stray shunt capacitances should be limited to 20 pF or increased to 1µF. If strays can not be avoided, operation at 500 µA and a shunt capacitor of at least 1000 pF are recommended.

[3]H = Hermetic Metal Can; SO = SOIC. For outline information see Package Information section.

Specifications shown in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

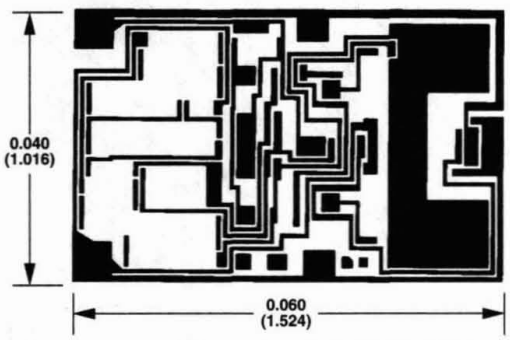
ABSOLUTE MAXIMUM RATINGS

Current ..... 10 mA
Reverse Current ..... 10 mA
Power Dissipation[1] ..... 125 mW
Storage Temperature ..... –65°C to +175°C
Operating Junction Temperature Range ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

NOTE

[1]Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and θ_{JA} = 400 = C/W.

AD589 CHIP DIMENSIONS AND PAD LAYOUT



THE AD589 IS AVAILABLE IN CHIP FORM WITH FULLY TESTED AND GUARANTEED SPECIFICATIONS. CONSULT FACTORY FOR AVAILABLE GRADES AND PRICING.

ANALOG DEVICES

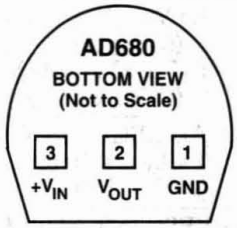
Low Power, Low Cost 2.5 V Reference

AD680*

FEATURES
Low Quiescent Current: 250 μA max
Laser Trimmed to High Accuracy:
2.5 V ±5 mV max (AN, AR Grade)
Trimmed Temperature Coefficient:
20 ppm/°C max (AN, AR Grade)
Low Noise: 8 μV p-p from 0.1 Hz to 10 Hz
250 nV/√Hz Wideband
Temperature Output Pin (N, R Packages)
Available in Three Package Styles:
8-Pin Plastic DIP, 8-Pin SOIC and 3-Pin TO-92

CONNECTION DIAGRAMS

NC = NO CONNECT



*TP DENOTES FACTORY TEST POINT. NO CONNECTIONS SHOULD BE MADE TO THESE PINS.

PRODUCT DESCRIPTION

The AD680 is a bandgap voltage reference which provides a fixed 2.5 V output from inputs between 4.5 V and 36 V. The architecture of the AD680 enables the reference to be operated at a very low quiescent current while still realizing excellent dc characteristics and noise performance. Trimming of the high stability thin-film resistors is performed for initial accuracy and temperature coefficient, resulting in low errors over temperature.

The precision dc characteristics of the AD680 make it ideal for use as a reference for D/A converters which require an external precision reference. The device is also ideal for A/D converters and, in general, can offer better performance than the standard on-chip references.

Based upon the low quiescent current of the AD680, which rivals that of many incomplete two-terminal references, the AD680 is recommended for low power applications such as hand-held battery equipment.

A temperature output pin is provided on the 8-pin package versions of the AD680. The temperature output pin provides an output voltage that varies linearly with temperature and allows the AD680 to be configured as a temperature transducer while providing a stable 2.5 V output.

The AD680 is available in five grades. The AD680AN is specified for operation from –40°C to +85°C, while the AD680JN is specified for 0°C to +70°C operation. Both the AD680AN and AD680JN are available in 8-pin plastic DIP packages. The AD680AR is specified for operation from –40°C to +85°C, while the AD680JR is specified for 0°C to +70°C operation. Both are available in an 8-pin Small Outline IC (SOIC) package. The AD680JT is specified for 0°C to +70°C operation and is available in a 3-pin TO-92 package.

***Protected by U.S. Patent Nos. 4,902,959; 4,250,445 and 4,857,862.**

PRODUCT HIGHLIGHTS

1. The AD680 bandgap reference operates on a very low quiescent current which rivals that of many two-terminal references. This makes the complete, higher accuracy AD680 ideal for use in power sensitive applications.
2. Laser trimming of both initial accuracy and temperature coefficients results in low errors over temperature without the use of external components. The AD680AN and AD680AR have a maximum variation of 6.25 mV between –40°C and +85°C.
3. The AD680 noise is low, typically 8 μV p-p from 0.1 Hz to 10 Hz. Spectral density is also low, typically 250 nV/√Hz.
4. The temperature output pin on the 8-pin package versions enables the AD680 to be configured as a temperature transducer.
5. Plastic DIP packaging provides machine insertability, while SOIC packaging provides surface mount capability. TO-92 packaging offers a cost effective alternative to two-terminal references, offering a complete solution in the same package in which two-terminal references are usually found.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD680–SPECIFICATIONS (T_A = +25°C, V_{IN} = +5 V, unless otherwise noted)

Model	AD680AN/AR Min	AD680AN/AR Typ	AD680AN/AR Max	AD680JN/JR Min	AD680JN/JR Typ	AD680JN/JR Max	AD680JT Min	AD680JT Typ	AD680JT Max	Units
OUTPUT VOLTAGE	**2.495**		**2.505**	**2.490**		**2.510**	**2.490**		**2.510**	V
OUTPUT VOLTAGE DRIFT[1]										
0°C to +70°C		10			10	25		10	30	ppm/°C
–40°C to +85°C			20		25			25		
LINE REGULATION										
4.5 V ≤ +V_{IN} ≤ 15 V			40			*			*	µV/V
(@ T_{MIN} to T_{MAX})			40			*			*	
15 V ≤ +V_{IN} ≤ 36 V			40			*			*	
(@ T_{MIN} to T_{MAX})			40			*			*	
LOAD REGULATION										
0 < I_{OUT} < 10 mA		80	100		*	*		*	*	µV/mA
(@ T_{MIN} to T_{MAX})		80	100		*	*		*	*	
QUIESCENT CURRENT		195	**250**		*	*		*	*	µA
(@ T_{MIN} to T_{MAX})			280			*			*	
POWER DISSIPATION		1	**1.25**		*	*		*	*	mW
OUTPUT NOISE										
0.1 Hz to 10 Hz		8	10		*	*		*	*	mV p-p
Spectral Density, 100 Hz		250			*			*		nV/√Hz
CAPACITIVE LOAD			50			*			*	nF
LONG TERM STABILITY		25			*			*		ppm/1000 hr
SHORT CIRCUIT CURRENT TO GROUND		25	50		*	*		*	*	mA
TEMPERATURE PIN										
Voltage Output @ +25°C	540	596	660	*	*	*				mV
Temperature Sensitivity		2			*					mV/°C
Output Current	–5		+5	*		*				µA
Output Resistance		12			*					kΩ
TEMPERATURE RANGE										
Specified Performance	–40		+85	0		+70	0		+70	°C
Operating Performance[2]	–40		+85	–40		+85	–40		+85	

NOTES

[1]Maximum output voltage drift is guaranteed for all packages.

[2]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

*Same as AD680AN/AR specification.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final eleetrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground ..... 36 V
Power Dissipation (25°C) ..... 500 mW
Storage Temperature ..... –65°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Package Thermal Resistance
θ_{JA} (All Packages) ..... 120°C/W
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Initial Error mV	Temperature Coeff. ppm/°C	Temperature Range	Package Description	Package Option*
AD680JN	10	25	0°C to +70°C	Plastic	N-8
AD680JR	10	25	0°C to +70°C	SOIC	SO-8
AD680JT	10	30	0°C to +70°C	TO-92	TO-92
AD680AN	5	20	–40°C to +85°C	Plastic	N-8
AD680AR	5	20	–40°C to +85°C	SOIC	SO-8

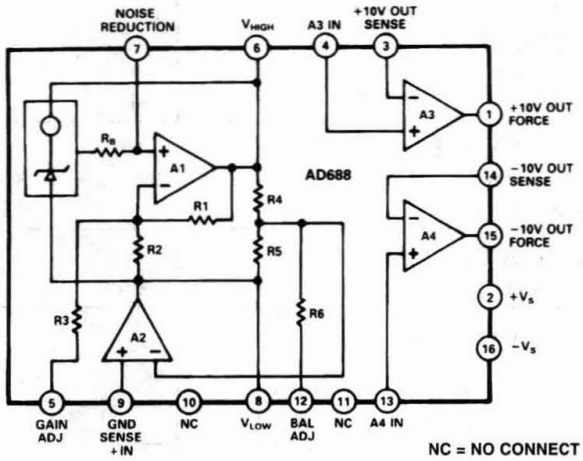
*N = Plastic DIP Package; SO = SOIC Package; T = TO-92 Package. For outline information see Package Information section.

High Precision ±10 V Reference

AD688*

FEATURES
±10 V Tracking Outputs
Kelvin Connections
Low Tracking Error – 1.5 mV
Low Initial Error – 2.0 mV
Low Drift – 1.5 ppm/°C
Low Noise – 6 μV p-p
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine Insertable DIP Packaging
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD688 is a high precision ±10 V tracking reference. Low tracking error, low initial error and low temperature drift give the AD688 reference absolute ±10 V accuracy performance previously unavailable in monolithic form. The AD688 uses a proprietary ion-implanted buried Zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

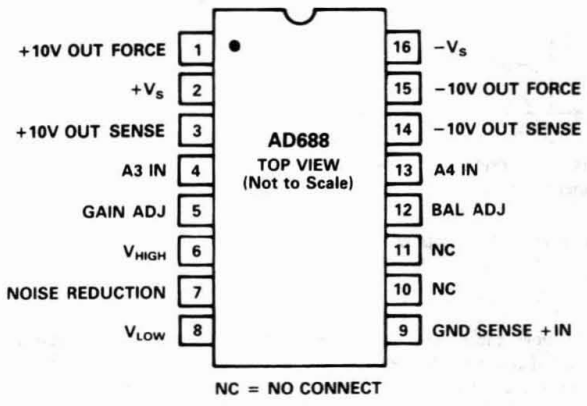
The AD688 includes the basic reference cell and three additional amplifiers. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high current loads, delivering the full accuracy of the AD688 where it is required in the application circuit.

The low initial error allows the AD688 to be used as a system reference in precision measurement applications requiring 12-bit absolute accuracy. In such systems, the AD688 can provide a known voltage for system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD688 and calibration software.

The AD688 is available in three versions. The AD688AQ and BQ grades are packaged in 16-pin cerdip (0.3") packages and are specified for operation from –40°C to +85°C. The AD688SQ grade is specified for operation from –55°C to +125°C.

***Covered by Patent Number 4,644,253.**

PIN CONFIGURATION



ORDERING GUIDE

Part Number[1]	Initial Error	Temperature Coefficient	Temperature Range – °C	Package Option[2]
AD688AQ	5 mV	3 ppm/°C	–40 to +85	Q-16
AD688BQ	2 mV	3 ppm/°C	–40 to +85*	Q-16
AD688SQ	5 mV	6 ppm/°C	–55 to +125	Q-16

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the *Analog Devices Military Products Databook* or current AD688/883B data sheet.
[2]Q = Cerdip. For outline information see Package Information section.
*Temperature coefficient specified from 0°C to +70°C.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD688–SPECIFICATIONS (typical @ +25°C, +10 V output, V_S = ±15 V unless otherwise noted[1])

	AD688AQ/SQ			AD688BQ			
	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR							
+10 V, –10 V Outputs	**–5**		**+5**	**–2**		**+2**	mV
±10 V TRACKING ERROR	**–3**		**+3**	**–1.5**		**+1.5**	mV
OUTPUT VOLTAGE DRIFT							
+10 V, –10 V Outputs							
0°C to +70°C (A, B)		±2		**–1.5**		**+1.5**	ppm/°C
–40°C to +85°C (A, B)	**–3**		**+3**	**–3**		**+3**	ppm/°C
–55°C to +125°C (S)	**–6**		**+6**				ppm/°C
GAIN ADJ AND BAL ADJ[2]							
Trim Range		±5			±5		mV
Input Resistance		150			150		kΩ
LINE REGULATION							
T_{MIN} to T_{MAX}[3]	**–200**		**+200**	**–200**		**+200**	µV/V
LOAD REGULATION							
T_{MIN} to T_{MAX}							
+10 V Output, $0<I_{OUT}<10$ mA			**±50**			**±50**	µV/mA
–10 V Output, $-10<I_{OUT}<0$ mA			**±50**			**±50**	µV/mA
SUPPLY CURRENT							
T_{MIN} to T_{MAX}		9	**12**		9	**12**	mA
Power Dissipation		270	360		270	360	mW
OUTPUT NOISE (ANY OUTPUT)							
0.1 Hz to 10 Hz		6			6		µV p-p
Spectral Density, 100 Hz		140			140		$nV\sqrt{Hz}$
LONG TERM STABILITY (@ +25°C)		15			15		ppm/1000 hours
BUFFER AMPLIFIERS							
Offset Voltage		100			100		µV
Offset Voltage Drift		1			1		µV/°C
Bias Current		20			20		nA
Open Loop Gain		110			110		dB
Output Current A3, A4	**–10**		**+10**	**–10**		**+10**	mA
Common Mode Rejection (A3, A4)							
V_{CM} = 1 V p-p		100			100		dB
Short-Circuit Current		50			50		mA
TEMPERATURE RANGE							
Specified Performance							
A, B Grades	–40		+85	–40		+85	°C
S Grade	–55		+125				°C

NOTES

[1]See Figure 2a for output configuration. Specifications tested using +10 V output unless otherwise indicated.

[2]Gain and balance adjustments guaranteed capable of trimming output voltage error and symmetry error to zero.

[3]Test Condition: $+V_S$ = +18 V, $-V_S$ = –18 V; $+V_S$ = +13.5 V, V_S = –13 .5 V.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to $-V_S$ ..... 36 V

Power Dissipation (+25°C)

Q Package ..... 600 mW

Storage Temperature ..... –65°C to +150°C

Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Package Thermal Resistance

Q (θ_{JA}/θ_{JC}) ..... 120/35°C/W

Output Protection: All outputs safe if shorted to ground

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

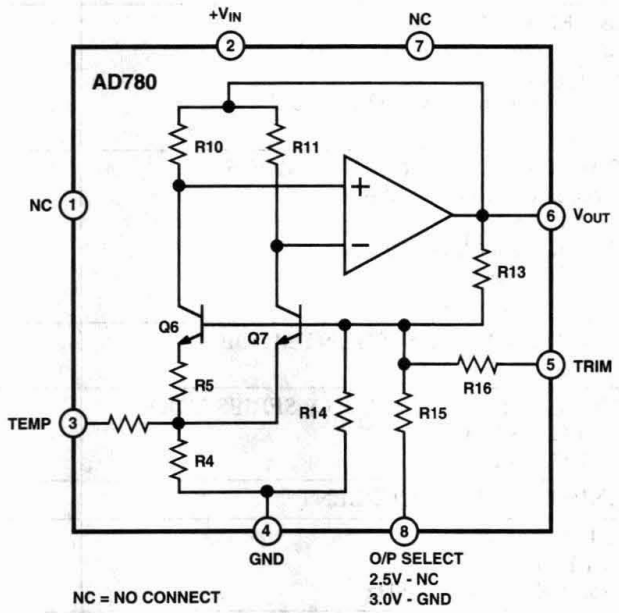
2.5 V/3.0 V High Precision Reference

AD780

FEATURES

Pin-Programmable 2.5 V or 3.0 V Output
Ultralow Drift: 3 ppm/°C max
High Accuracy: 2.5 V or 3.0 V ± 1 mV max
Low Noise: 100 nV/√Hz
Noise Reduction Capability
Low Quiescent Current: 1 mA max
Output Trim Capability
Plug-In Upgrade for Present References
Temperature Output Pin
Series or Shunt Mode Operation (±2.5 V, ±3.0 V)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD780 is an ultrahigh precision bandgap reference voltage which provides a 2.5 V or 3.0 V output from inputs between 4.0 V and 36 V. Low initial error and temperature drift combined with low output noise and the ability to drive any value of capacitance make the AD780 the ideal choice for enhancing the performance of high resolution ADCs and DACs and for any general purpose precision reference application. A unique low headroom design facilitates a 3.0 V output from a 5.0 V ± 10% input, providing a 20% boost to the dynamic range of an ADC, over performance with existing 2.5 V references.

The AD780 can be used to source or sink up to 10 mA and can be used in series or shunt mode, thus allowing positive or negative output voltages without external components. This makes it suitable for virtually any high performance reference application. Unlike some competing references, the AD780 has no "region of possible instability." The part is stable under all load conditions when a 1 µF bypass capacitor is used on the supply.

A temperature output pin is provided on the AD780. This provides an output voltage that varies linearly with temperature, allowing the AD780 to be configured as a temperature transducer while providing a stable 2.5 V or 3.0 V output.

The AD780 is a pin-compatible performance upgrade for the LT1019(A)–2.5 and the AD680. The latter is targeted toward low power applications.

The AD780 is available in two grades in plastic DIP, SOIC and cerdip packages. The AD780AN, AD780AR, AD780BN and AD780BR are specified for operation from –40°C to +85°C. The AD780SQ and AD780SQ/883B are specified for –55°C to +125°C operation.

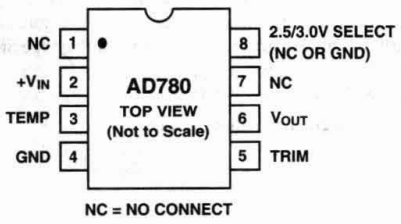
ORDERING GUIDE

Model	Initial Error	Temperature Coefficient	Temperature Range	Package Options*
AD780AN	5 mV	7 ppm/°C	–40°C to +85°C	N-8
AD780AR	5 mV	7 ppm/°C	–40°C to +85°C	SO-8
AD780BN	1 mV	3 ppm/°C	–40°C to +85°C	N-8
AD780BR	1 mV	3 ppm/°C	–40°C to +85°C	SO-8
AD780SQ	5 mV	20 ppm/°C	–55°C to +125°C	Q-8
AD780SQ/883B	5 mV	20 ppm/°C	–55°C to +125°C	Q-8

*For outline information see Package Information section.

PIN CONFIGURATION

8-Pin Plastic DIP, SOIC and Cerdip Packages



AD780—SPECIFICATIONS (T_A = +25°C, V_{IN} = +5 V unless otherwise noted)

Parameter	AD780AN/AR/SQ Min	Typ	Max	AD780BN/BR Min	Typ	Max	Units
OUTPUT VOLTAGE							
2.5 V Out	2.495		2.505	2.499		2.501	Volts
3.0 V Out	2.995		3.005	2.999		3.001	Volts
OUTPUT VOLTAGE DRIFT[1]							
–40°C to +85°C			7			3	ppm/°C
–55°C to +125°C			20				ppm/°C
LINE REGULATION							
2.5 V Output, 4 V ≤ +V_{IN} ≤ 36 V							
T_{MIN} to T_{MAX}			10			*	µV/V
3.0 V Output, 4.5 V ≤ +V_{IN} ≤ 36 V							
T_{MIN} to T_{MAX}			10			*	µV/V
LOAD REGULATION, SERIES MODE							
Sourcing 0 < I_{OUT} < 10 mA			50			*	µV/mA
T_{MIN} to T_{MAX}			75			*	µV/mA
Sinking –10 < I_{OUT} < 0 mA			75			*	µV/mA
–40°C to +85°C			75			*	µV/mA
–55°C to +125°C			150			*	µV/mA
LOAD REGULATION, SHUNT MODE							
I < I_{SHUNT} < 10 mA			75			*	µV/mA
QUIESCENT CURRENT, 2.5 V SERIES MODE[2]							
–40°C to +85°C		0.75	1.0		*	*	mA
–55°C to +125°C		0.8	1.3		*	*	mA
MINIMUM SHUNT CURRENT		0.7	1.0		*	*	mA
OUTPUT NOISE							
0.1 Hz to 10 Hz		4			*	*	µV p-p
Spectral Density, 100 Hz		100			*	*	nV/√Hz
LONG TERM STABILITY[3]		20			*		±ppm/1000 Hr
TRIM RANGE	4.0			*			±%
TEMPERATURE PIN							
Voltage Output @ 25°C	500	560	620	*	*	*	mV
Temperature Sensitivity		1.9			*		mV/°C
Output Resistance		3			*		kΩ
SHORT CIRCUIT CURRENT TO GROUND		30			*		mA
TEMPERATURE RANGE							
Specified Performance (A, B)	–40		+85	*		*	°C
Operating Performance (A, B)[4]	–55		+125	*		*	°C
Specified Performance (S)	–55		+125	*		*	°C
Operating Performance (S)	–55		+125	*		*	°C

NOTES

[1]Maximum output voltage drift is guaranteed for all packages.

[2]3.0 V mode typically adds 100 µA to the quiescent current. Also, Iq increases by 2 µA/V above an input voltage of 5 V.

[3]The long term stability specification is noncumulative. The drift in subsequent 1000 hr. periods is significantly lower than in the first 1000 hr. period.

[4]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

*Same as AD780AN/AR/SQ specification.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{IN} to Ground . . . . . 36 V
Trim Pin to Ground . . . . . 36 V
Temp Pin to Ground . . . . . 36 V
Power Dissipation (25°C) . . . . . 500 mW
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.
ESD Classification . . . . . Class 1 (1000 V)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational specification is not implied. Exposure to absolute maximum specifications for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD780 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

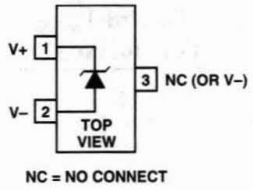
1.2 V Micropower, Precision Shunt Voltage Reference

AD1580

FEATURES
Wide Operating Range: 50 μA–10 mA
Initial Accuracy: ±0.1% max
Temperature Drift: ±50 ppm/°C max
Output Impedance: 0.5 Ω max
Wideband Noise (10 Hz–10 kHz): 20 μV rms
Operating Temperature Range: –40°C to +85°C
High ESD Rating
4 kV Human Body Model
400 V Machine Model
Compact, Surface-Mount, SOT-23 Package

PIN CONFIGURATION

SOT-23 Package



NC = NO CONNECT

GENERAL DESCRIPTION

The AD1580 is a low cost, two-terminal (shunt), precision bandgap reference. It provides an accurate 1.225 V output for input currents between 50 μA and 10 mA.

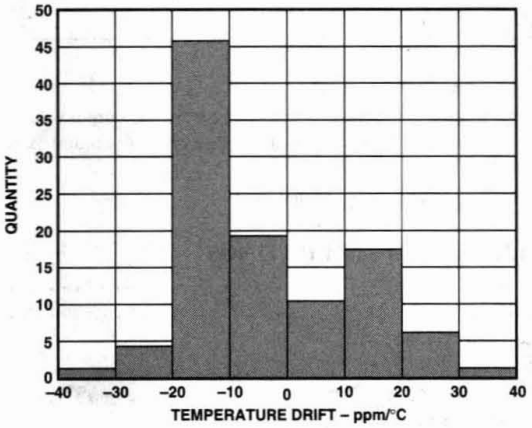
The AD1580's superior accuracy and stability is made possible by the precise matching and thermal tracking of on-chip components. Proprietary curvature correction design techniques have been used to minimize the nonlinearities in the voltage output temperature characteristics. The AD1580 is stable with any value of capacitive load.

The low minimum operating current makes the AD1580 ideal for use in battery powered 3 V or 5 V systems. However, the wide operating current range means that the AD1580 is extremely versatile and suitable for use in a wide variety of high current applications.

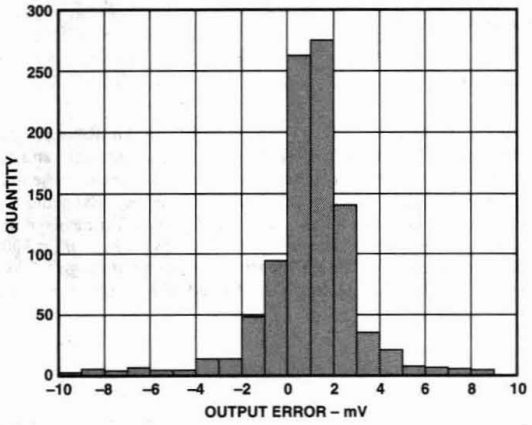
The AD1580 is available in two grades, A and B, both of which are provided in an SOT-23 package, the smallest surface mount package available on the market. Both grades are specified over the industrial temperature range of –40°C to +85°C.

TARGET APPLICATIONS

1. Portable, Battery-Powered Equipment:
   Cellular Phones, Notebook Computers, PDAs, GPS and DMM.
2. Computer Workstations
   Suitable for use with a wide range of video RAMDACs.
3. Smart Industrial Transmitters
4. PCMCIA Cards.
5. Automotive.
6. 3 V/5 V 8–12-Bit Data Converters.



Reverse Voltage Temperature Drift Distribution



Reverse Voltage Error Distribution

11

AD1580–SPECIFICATIONS (@ T_A = +25°C, I_{IN} = 100 µA, unless otherwise noted)

Model	AD1580A			AD1580B			Units
	Min	Typ	Max	Min	Typ	Max	
Reverse Voltage Output	1.215	1.225	1.235	1.224	1.225	1.226	V
Reverse Voltage Temperature Drift –40°C to +85°C			100			50	ppm/°C
Minimum Operating Current, T_{MIN} to T_{MAX}			50			50	µA
Reverse Voltage Change with Reverse Current 50 µA < I_{IN} < 10 mA, T_{MIN} to T_{MAX} 50 µA < I_{IN} < 1 mA, T_{MIN} to T_{MAX}		2.5 0.5	5		2.5 0.5	5	mV mV
Dynamic Output Impedance ($\Delta V_R/\Delta I_R$) I_{IN} = 1 mA ±100 µA (f = 120 Hz)		0.4	1		0.4	0.5	Ω
OUTPUT NOISE RMS Noise Voltage: 10 Hz to 10 kHz Low Frequency Noise Voltage: 0.1 Hz to 10 Hz		20 5			20 5		µV rms µV p-p
Turn-On Settling Time to 0.1%[1]		5			5		µs
Output Voltage Hysteresis[2]		80			80		µV
Temperature Range Specified Performance, T_{MIN} to T_{MAX} Operating Range[3]	 –40 –55		 +85 +125	 –40 –55		 +85 +125	 °C °C

NOTES

[1]Measured with no load capacitor.

[2]Output hysteresis is defined as the change in the +25°C output voltage after a temperature excursion to +85°C and then to –40°C.

[3]The operating temperature range is defined as the temperature extremes at which the device will continue to function. Parts may deviate from their specified performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Reverse Current ..... 25 mA
Forward Current ..... 20 mA
Internal Power Dissipation[2]
SOT-23 (RT) ..... 0.3 Watts
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
AD1580/RT ..... –55°C to +125°C
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD Susceptibility[3]
Human Body Model ..... 4 kV
Machine Model ..... 400 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air at +25°C: SOT-23 Package: θ_{JA} = 300°C/Watt.

[3]The human body model is a 100 pF capacitor discharged through 1.5 kΩ. For the machine model, a 200 pF capacitor is discharged directly into the device.

ORDERING GUIDE

Model	Initial Output Error	Temperature Coefficient	Package Option[1]
AD1580ART	10 mV	100 ppm/°C	SOT-23
AD1580ART-REEL[2]	10 mV	100 ppm/°C	SOT-23
AD1580ART-REEL7[3]	10 mV	100 ppm/°C	SOT-23
AD1580BRT	1 mV	50 ppm/°C	SOT-23
AD1580BRT-REEL[2]	1 mV	50 ppm/°C	SOT-23
AD1580BRT-REEL7[3]	1 mV	50 ppm/°C	SOT-23

NOTES

[1]For outline information see Package Information section.

[2]Provided on a 13-inch reel containing 7,000 pieces.

[3]Provided on a 7-inch reel containing 2,000 pieces.

PACKAGE BRANDING INFORMATION

Four marking fields identify the device generic, grade, and date of processing. The first field is the product identifier. A "0" identifies the generic as the AD1580. The second field indicates the device grade; "A" or "B." In the third field a numeral or letter indicates a calendar year; "5" for 1995, "A" for 2001. In the fourth field, letters A-Z represent a two week window within the calendar year; starting with "A" for the first two weeks of January.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1580 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

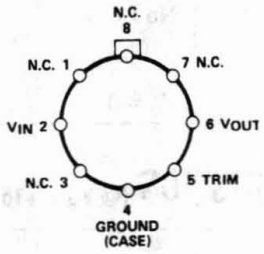
+10 V Precision Voltage Reference

REF01

FEATURES
10 Volt Output: ±0.3%
Adjustment Range: ±3%
Excellent Temperature Stability: 3 ppm/°C
Low Noise: 20 μV p-p
Low Supply Current: 1.4 mA max
Wide Input Voltage Range: 13 V to 33 V
High Load-Driving Capability: 20 mA
No External Components
Short-Circuit Proof
MIL-STD-883 Screening Available

PIN CONNECTIONS

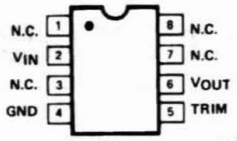
TO-99
(J Suffix)



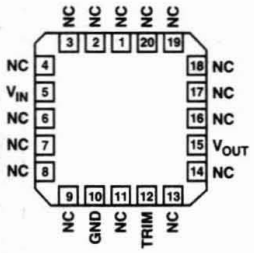
Epoxy Mini-DIP
(P Suffix)

8-Pin Hermetic DIP
(Z Suffix)

8-Pin SO
(S Suffix)



20-Terminal LCC
(RC Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The REF01 precision voltage reference provides a stable +10 V output which can be adjusted over at ±3% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 12 V to 40 V, low current drain of 1 mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For guaranteed long-term drift see the REF10 data sheet.

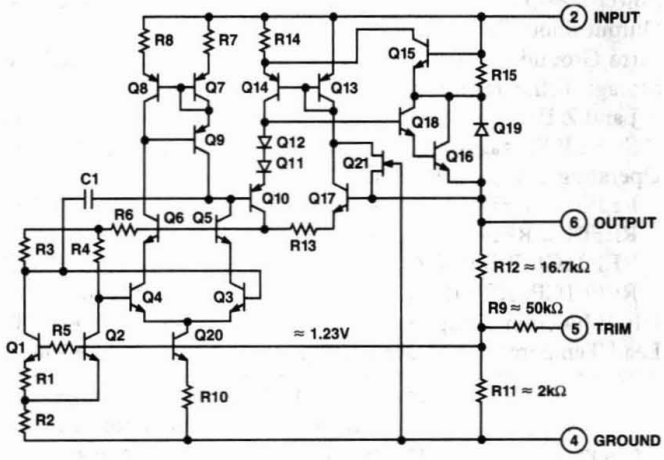


Figure 1. Simplified Schematic

ORDERING GUIDE[1]

Model	ΔV_O max (T_A = +25°C)	Temperature Range	Package Option[2]
REF01AJ[3]	±30 mV	–55°C to +125°C	TO-99
REF01AZ[3]	±30 mV	–55°C to +125°C	8-Pin Cerdip
REF01EJ	±30 mV	0°C to +70°C	TO-99
REF01EZ	±30 mV	0°C to +70°C	8-Pin Cerdip
REF01J[3]	±50 mV	–55°C to +125°C	TO-99
REF01HJ	±50 mV	0°C to +70°C	TO-99
REF01HZ	±50 mV	0°C to +70°C	8-Pin Cerdip
REF01HP	±50 mV	0°C to +70°C	8-Pin Plastic DIP
REF01CJ	±100 mV	0°C to +70°C	TO-99
REF01CZ	±100 mV	0°C to +70°C	8-Pin Cerdip
REF01CP	±100 mV	–40°C to +85°C	8-Pin Plastic DIP
REF01CP	±100 mV	–40°C to +85°C	8-Pin Plastic DIP
REF01CS	±100 mV	–40°C to +85°C	8-Pin SO
REF01RC /883	±50 mV	–55°C to +125°C	20-Pin LCC

NOTES
[1]All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883.
[2]For outline information see Package Information section.
[3]Also available with MIL-STD-883 processing. To order add/883 as a suffix to the part number.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

REF01–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{IN} = +15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	REF01A/E Min	REF01A/E Typ	REF01A/E Max	REF01H Min	REF01H Typ	REF01H Max	Units
Output Voltage	V_O	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{TRIM}	R_P = 10 kΩ	±3.0	±3.3		±3.0	±3.3		%
Output Voltage Range	e_n p-p	0.1 Hz to 10 Hz[6]		20	30		20	30	µV p-p
Line Regulation[4]		V_{IN} = 13 V to 33 V		0.006	0.010		0.006	0.010	%/V
Load Regulation[4]		I_L = 0 to 10 mA		0.005	0.008		0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To ±0.1% of final value		5			5		µs
Quiescent Supply Current	I_{SY}	No Load		1.0	1.4		1.0	1.4	mA
Load Current	I_L		10	21		10	21		mA
Sink Current	I_S		–0.3	–0.5		–0.3	–0.5		mA
Short-Circuit Current	I_{SC}	V_O = 0		30			30		mA

ELECTRICAL CHARACTERISTICS (@ V_{IN} = +15 V, –55°C ≤ T_A ≤ +125°C and I_L = 0 mA, unless otherwise noted.)

Parameter	Symbol	Conditions	REF01A/E Min	REF01A/E Typ	REF01A/E Max	REF01H Min	REF01H Typ	REF01H Max	Units
Output Voltage Change with Temperature[1, 2]	ΔV_{OT}	0°C ≤ T_A ≤ +70°C		0.02	0.06		0.07	0.17	%
		–55°C ≤ T_A ≤ +125°C		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	Note 3		3.0	8.5		10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_P = 10 kΩ		0.7			0.7		ppm/%
Line Regulation		0°C ≤ T_A ≤ +70°C		0.007	0.012		0.007	0.012	%/V
(V_{IN} = 13 V to 33 V)[4]		–55°C ≤ T_A ≤ +125°C		0.009	0.015		0.009	0.015	%/V
Load Regulation		0°C ≤ T_A ≤ +70°C		0.006	0.010		0.007	0.012	%/mA
(I_L = 0 to 8 mA)[4]		–55°C ≤ T_A ≤ +125°C		0.007	0.012		0.009	0.015	%/mA

NOTES

[1]ΔV_{OT} is defined as the absolute difference between the maximum output voltage over the specified temperature range expressed as a percentage of 10 V:

[2]ΔV_{OT} specification applies trimmed to +10.000 V or untrimmed.

[3]TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O\ (0°C \text{ to } +70°C) = \frac{\Delta V_{OT}\ (0°C \text{ to } +70°C)}{70°C}$$

and

$$TCV_O\ (-55°C \text{ to } +125°C) = \frac{\Delta V_{OT}\ (-55°C \text{ to } +125°C)}{180°C}$$

[4]Line and Load Regulation specifications include the effect of self heating.

[5]Guaranteed by design.

[6]Sampled tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage
- REF01, A, E, H, All DICE ..... 40 V
- REF01C ..... 30 V

Power Dissipation[2] ..... 500 mW

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J and Z Packages ..... –65°C to +150°C
- S and P Packages ..... –65°C to +125°C

Operating Temperature Range
- REF01A, REF01 ..... –55°C to +70°C
- REF01E, REF01H
- REF01CJ, REF01CZ ..... 0°C to +70°C
- REF01CP, REF01CS ..... –40°C to +85°C

DICE Junction Temperature (T_J) ..... –65°C to +150°C

Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1 mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7 mW/°C
8-Pin Plastic DIP (P)	36°C	5.6 mW/°C

NOTES

[1]Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

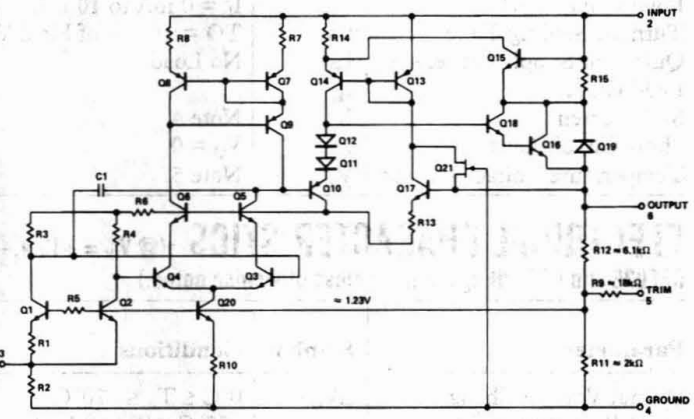
[2]See table for maximum ambient temperature rating and derating factor.

+5 V Precision Voltage Reference/Temperature Transducer

REF02

FEATURES
5 Volt Output: ±0.3% max
Temperature Voltage Output: 2.1 mV/°C
Adjustment Range: ±3% min
Excellent Temperature Stability: 8.5 ppm/°C max
Low Noise: 15 μV p-p max
Low Supply Current: 1.4 mA max
Wide Input Voltage Range: 7 V to 40 V
High Load-Driving Capacity: 20 mA
No External Components
Short-Circuit Proof
MIL-STD-883 Screening Available
Available in Die Form

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The REF02 precision voltage reference provides a stable +5 V output which can be adjusted over a ±6% range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7 V to 40 V, low current drain of 1 mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF02 is enhanced by its use as a monolithic temperature transducer. For +10 V references, see the REF01 and REF10 data sheets.

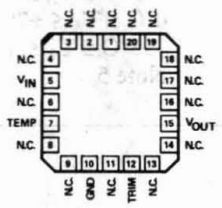
ORDERING GUIDE[1]

Model	V_{OS} max (T_A = +25°C)	Temperature Range	Package Options[2]
REF02AJ[3]	±15 mV	–65°C to +125°C	TO-99
REF02AZ[3]	±15 mV	–65°C to +125°C	8-Pin Cerdip
REF02EJ	±15 mV	0°C to +70°C	TO-99
REF02EZ	±15 mV	0°C to +70°C	8-Pin Cerdip
REF02J[3]	±25 mV	–65°C to +125°C	TO-99
REF02Z[3]	±25 mV	–65°C to +125°C	8-Pin Cerdip
REF02RC/883	±25 mV	–65°C to +125°C	20-Contact LCC
REF02HJ	±25 mV	0°C to +70°C	TO-99
REF02HZ	±25 mV	0°C to +70°C	8-Pin Cerdip
REF02HP	±25 mV	0°C to +70°C	8-Pin Plastic DIP
REF02CJ	±50 mV	0°C to +70°C	TO-99
REF02CZ	±50 mV	0°C to +70°C	8-Pin Cerdip
REF02CP	±50 mV	–40°C to +85°C	8-Pin Plastic DIP
REF02CS[4]	±50 mV	–40°C to +85°C	8-Pin SO
REF02DP	±100 mV	0°C to +70°C	8-Pin Plastic DIP

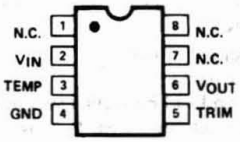
NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[4]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

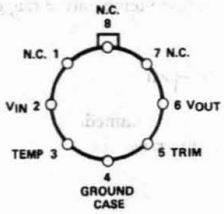
REF02RC/883 LCC
(RC Suffix)



8-Pin Hermetic DIP
(Z Suffix)
Epoxy Mini-DIP
(P Suffix)
8-Pin SO
(S Suffix)



TO-99
(J Suffix)



NC = NO CONNECT

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REF02–SPECIFICATIONS[1]

ELECTRICAL CHARACTERISTICS (@ V_{IN} = +15 V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	REF02A/E Min	REF02A/E Typ	REF02A/E Max	REF02H Min	REF02H Typ	REF02H Max	Units
Output Voltage	V_O	I_L = 0	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{TRIM}	R_P = 10 kΩ	±3	±6		±3	±6		%
Output Voltage Noise	e_n p-p	0.1 Hz to 10 Hz[2]		10	15		10	15	µV p-p
Line Regulation[3]		V_{IN} = 8 V to 33 V		0.006	0.010		0.006	0.010	%/V
Load Regulation[3]		I_L = 0 mA to 10 mA		0.005	0.010		0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	TO = ±0.1% of Final Value		5			5		µs
Quiescent Supply Current	I_{SY}	No Load		1.0	1.4		1.0	1.4	mA
Load Current	I_L		10	21		10	21		mA
Sink Current	I_S	Note 4	–0.3	–0.5		–0.3	–.5		mA
Short-Circuit Current	I_{SC}	V_O = 0		30			30		mA
Temperature Voltage Output	V_T	Note 5		630			630		mV

ELECTRICAL CHARACTERISTICS (@ V_{IN} = +15 V, –55°C ≤ T_A ≤ +25°C for REF02A and REF02, 0°C ≤ T_A ≤ +70°C for REF02E and REF02H, I_L = 0 mA, unless otherwise noted.)

Parameter	Symbol	Conditions	REF02A/E Min	REF02A/E Typ	REF02A/E Max	REF02H Min	REF02H Typ	REF02H Max	Units
Output Voltage Change with Temperature[6, 7]	ΔV_{OT}	0°C ≤ T_A ≤ –70°C		0.02	0.06		0.07	0.17	%
		–55°C ≤ T_A ≤ +125°C		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	Note 8		3	8.5		10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_P = 10 kΩ		0.7			0.7		ppm/%
Line Regulation[3]		0°C ≤ T_A ≤ +70°C		0.007	0.012		0.007	0.012	%/V
(V_{IN} = 8 to 33 V)		–55°C ≤ T_A ≤ +125°C		0.009	0.015		0.009	0.015	%/V
Load Regulation[3]		0°C ≤ T_A ≤ +70°C		0.006	0.010		0.007	0.012	%/mA
(I_L = 0 to 8 mA)		–55°C ≤ T_A ≤ +125°C		0.007	0.012		0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	Note 5		2.1			2.1		mV/°C

NOTES
[1]Guaranteed by design.
[2]Sample tested.
[3]Line and Load Regulation specifications include the effect of self heating.
[4]During sink current test the driver meets the output voltage specified.
[5]Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.
[6]ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5 V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

[7]ΔV_{OT} specification applies trimmed to +5.000 V or untrimmed.
[8]TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage
- REF02A, E, H, RC, All DICE ..... 40 V
- REF02C, D ..... 30 V

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range
- J, RC, and Z Packages ..... –65°C to +150°C
- P Package ..... –65°C to +125°C

Operating Temperature Range
- REF02A, REF02, REF02RC ..... –65°C to +125°C
- REF02E, REF02H ..... 0°C to +70°C
- REF02CJ, CZ, REF02D ..... 0°C to +70°C
- REF02CP, CS ..... –40°C to +85°C

Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W
20-Contact LCC (RC, TC)	120	40	°C/W
8-Pin SO (S)	160	44	°C/W
20-Contact PLCC (PC)	80	39	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

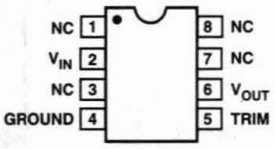
+2.5 V Precision Voltage Reference

REF03

FEATURES
+2.5 Volt Output: ±0.6% max
Wide Input Voltage Range: 4.5 V to 33 V
Supply Current: 1.4 mA max
Output Voltage Tempco: 50 ppm/°C max
Line Regulation: 50 ppm/V max
Load Regulation: 100 ppm/mA max
Extended Industrial Temp Range: –40°C to +85°C
Low Cost

PIN CONNECTION

8-Pin Plastic DIP (P Suffix)
8-Pin SO (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The REF03 precision voltage reference provides a stable +2.5 V output, with minimal change for variations in supply voltage, ambient temperature or loading conditions. Single-supply operation over an input voltage range of +4.5 V to +33 V with a current drain of 1 mA and good temperature stability is achieved using an improved bandgap design. Primarily targeted at price-sensitive applications, the REF03 is available in plastic mini-DIPs and surface-mountable small outline plastic packages. For improved performance or –55°C/125°C operation, see the REF43 data sheet.

ORDERING GUIDE[1]

Model	Temperature Range	Package Options[2]
REF03GP	–40°C to +85°C	8-Pin Plastic DIP
REF03GS[3]	–40°C to +85°C	8-Pin SO

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in plastic DIP.
[2]For outline information see Package Information section.
[3]For availability and burn-in information on SO packages, contact your local sales office.

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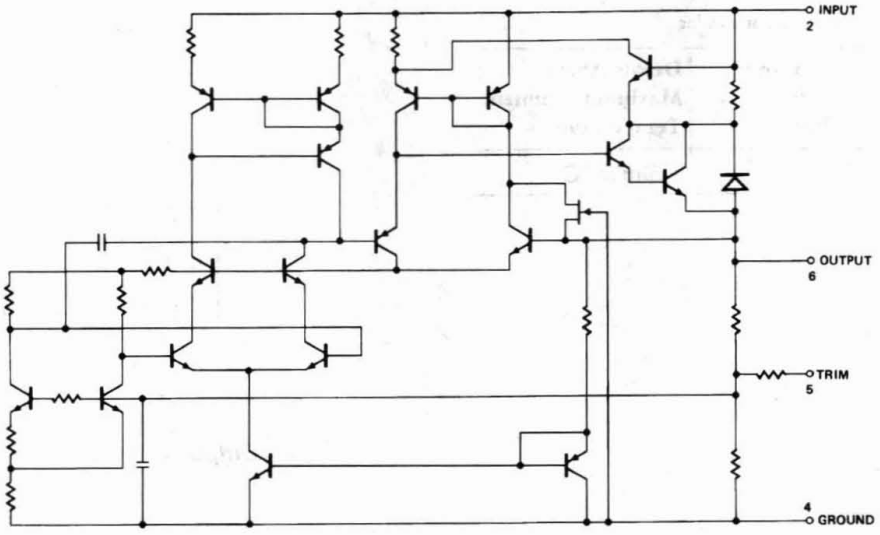


Figure 1. Simplified Schematic

REF03–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{IN} = +15 V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	REF03G Min	REF03G Typ	REF03G Max	Units
Output Voltage	V_O	No Load	2.485	2.500	2.515	V
Output Voltage Tolerance		No Load		0.2	0.6	%
Output Voltage Temperature Coefficient	TCV_O	Note 1		10	50	ppm/°C
Line Regulation		V_{IN} = +4.5 V to +33 V		20	50	ppm/V
				0.002	0.005	%/V
Load Regulation		I_L = 0 mA to 10 mA		60	100	ppm/mA
				0.006	0.010	%/mA
Load Current (Sourcing)	I_L		10	21		mA
Load Current (Sinking)	I_S		–0.3	–0.5		mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground		24		mA
Quiescent Supply Current	I_{SY}	No Load		1.0	1.4	mA
Turn-On Settling Time	t_{ON}	To ±0.1% of Final Value		5		µs
Output Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		6		µV p-p
Output Adjustment Range	ΔV_{TRIM}	R_{POT} = 10 kΩ	±6	±11		%
Input Voltage Range			4.5	15	33	V

NOTE
[1]TCV_O is measured by the endpoint method, and is equal to $\left|\frac{V(85°C) - V(-40°C)}{(2.5 \times 10^{-6})\ (125°C)}\right|$ in ppm/°C.

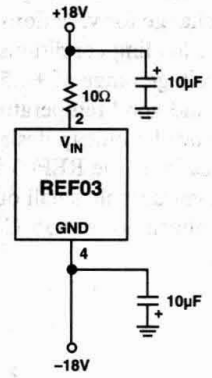
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

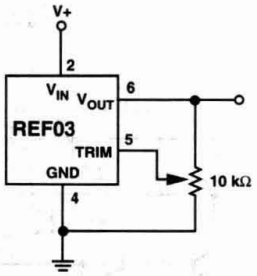
Supply Voltage . . . . . 40 V
Internal Power Dissipation[2] . . . . . 500 mW
Output Short-Circuit Duration . . . . . Indefinite
Operating Temperature Range
REF03G (P, S) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +175°C
Junction Temperature Range . . . . . –65°C to +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]See table for maximum ambient temperature and rating.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
8-Pin Plastic DIP (P)	62°C	5.6 mW/°C



Burn-In Circuit



Output Voltage Trim Method

+2.5 V Low-Power Precision Voltage Reference

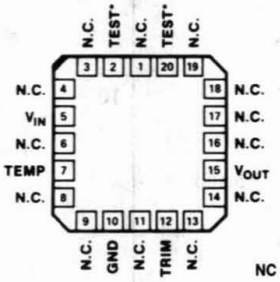
REF43

FEATURES

+2.5 Volt Output: ±0.05% max
Low Temperature Coefficient: 10 ppm/°C max
Excellent Regulation
Load Regulation: 20 ppm/mA max
Line Regulation: 2 ppm/V max
Supply Current: 450 µA max
Temperature Voltage Output: +1.9 mV/°C
Operating Voltage Range: +4.5 V to +40 V
Extended Industrial Temp Range: –40°C to +85°C

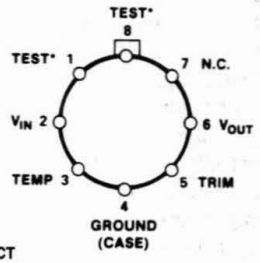
PIN CONNECTIONS

REF43BRC/883
20-Contact LCC
(RC Suffix)

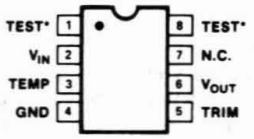


NC = NO CONNECT

TO-99
(J Suffix)



8-Pin Cerdip (Z Suffix)
8-Pin Plastic DIP (P Suffix)
8-Pin SO (S Suffix)



*RESERVED FOR FACTORY TESTING.
MAKE NO ELECTRICAL CONNECTION TO THESE PINS.

GENERAL DESCRIPTION

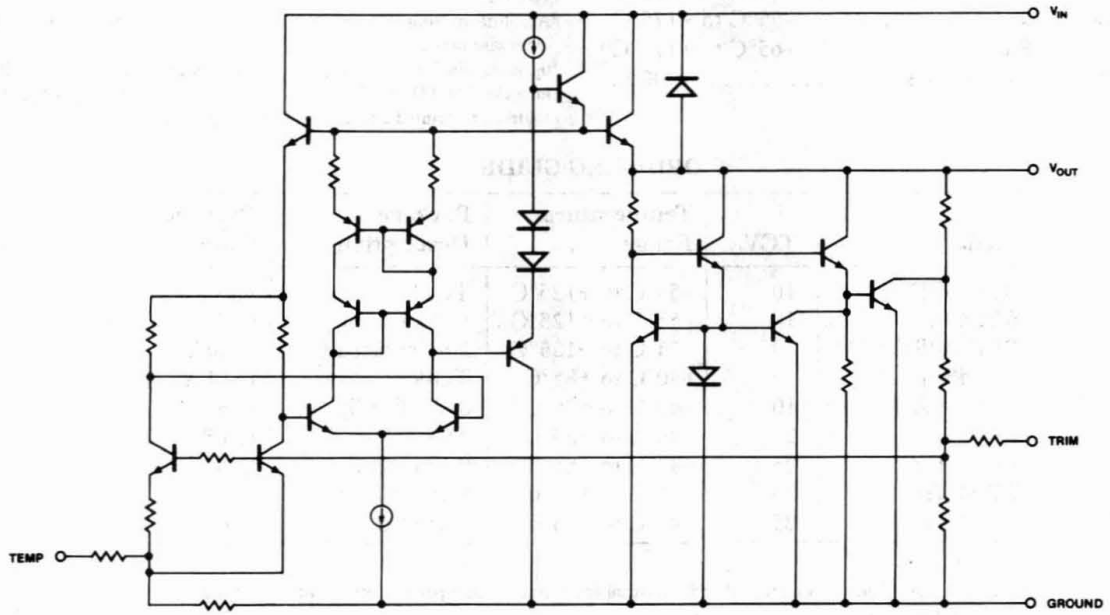
The REF43 is a low power precision reference providing a stable +2.5 V output independent of variations in supply voltage, load conditions or ambient temperature. It is suitable as a reference level for 8-, 10- and 12-bit data acquisition systems, or wherever a stable, known voltage is required.

Tight output tolerances and low thermal drift are assured by Zener-zap trimming of both output voltage and its temperature coefficient. A unique curvature correction circuit reduces the thermal curvature which is characteristic of many previous bandgap references.

The REF43 may be operated with supply voltages from +4.5 V to +40 V. The output voltage changes by less than 178 µV from one extreme of supply voltage to the other. With only 450 µA maximum quiescent current, the REF43 is ideally suited to applications where power dissipation must be minimized, as in precision battery-powered equipment. The low supply current minimizes drift due to self-heating after power-up.

A temperature output provides a means of determining system ambient temperature. Applications of the REF43 include A/D and D/A conversion, 4-20 mA transmitter/receiver operation, log amplifiers, and power-supply regulators.

For a low cost 2.5 V reference available in small-outline packages consult the REF03 data sheet.



Simplified Schematic

REF43–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{IN} = +5 V, I_L = 0 mA, T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Conditions	REF43B Min	REF43B Typ	REF43B Max	REF43F Min	REF43F Typ	REF43F Max	REF43G Min	REF43G Typ	REF43G Max	Units
Output Voltage Tolerance		No Load		0.04	0.1		0.02	0.06		0.04	0.1	%
Output Voltage	V_O	No Load	2.4975	2.5000	2.5025	2.4985	2.5000	2.5015	2.4975	2.5000	2.5025	V
Output Voltage Noise	e_n rms	10 Hz–1 kHz (Note 1)		7	10		7	10		7	10	µV rms
Line Regulation		V_{IN} = +4.5 V–+40 V		0.8	2		0.8	2		0.8	2	ppm/V
Load Regulation		I_L = 0 mA–10 mA		14	20		14	20		14	20	ppm/mA
Quiescent Supply Current	I_{SY}	No Load		340	450		340	450		340	450	µA
Load Current (Sourcing)	I_L	(Note 2)	10	20		10	20		10	20		mA
Load Current (Sinking)	I_S	(Note 3)		–1.2			–1.2			–12		mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground		60			60			60		mA
Temperature Voltage Output	V_{TEMP}			567			567			567		mV
V_{OUT} Adjust Range				±95			±95			±95		mV
Long-Term Output Drift	ΔV_O/Time	(Note 4)		1			1			1		ppm/month

NOTES
[1]Guaranteed but not tested.
[2]Guaranteed by load regulation test.
[3]Output remains within 2.5 V ± 2.5 mV.
[4]Calculated from accelerated life tests at T_A = 150°C. Activation energy = 0.7 eV.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 40 V
Internal Power Dissipation[2] . . . . . 500 mW
Output Short-Circuit Duration . . . . . Indefinite
Operating Temperature Range
REF43B (J, Z) . . . . . –55°C to +125°C
REF43F (J, Z) . . . . . –40°C to +85°C
REF43G (J, Z, P, S) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +175°C
Junction Temperature Range . . . . . –65°C to +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, cerdip, P-DIP, and LCC packages: θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE[1]

Model	TCV_O	Temperature Range	Package Description	Package Option[2]
REF43BJ[3]	10	–55°C to +125°C	TO-99	H-08A
REF43BZ[3]	10	–55°C to +125°C	8-Pin Cerdip	Q-8
REF43BRC/883[3]	10	–55°C to +125°C	20-Contact LCC	E-20A
REF43FJ	10	–40°C to +85°C	TO-99	H-08A
REF43FZ	10	–40°C to +85°C	8-Pin Cerdip	Q-8
REF43GJ	25	–40°C to +85°C	TO-99	H-08A
REF43GZ	25	–40°C to +85°C	8-Pin Cerdip	Q-8
REF43GP	25	–40°C to +85°C	8-Pin P-DIP	N-8
REF43GS	25	–40°C to +85°C	8-Pin SO	SO-8

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For outline information see Package Information section.
[3]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

Precision Micropower, Low Dropout, Voltage References

REF19x Series*

FEATURES
Initial Accuracy: ±2 mV max
Temperature Coefficient: 5 ppm/°C max
Low Supply Current: 45 μA max
Sleep Mode: 15 μA max
Low Dropout Voltage
Load Regulation: 4 ppm/mA
Line Regulation: 4 ppm/V
High Output Current: 30 mA
Short Circuit Protection

APPLICATIONS
Portable Instrumentation
A-to-D and D-to-A Converters
Smart Sensors
Solar Powered Applications
Loop Current Powered Instrumentations

GENERAL DESCRIPTION
REF19x series precision bandgap voltage references utilize a patented temperature drift curvature correction circuit and laser trimming of highly stable thin-film resistors to achieve a very low temperature coefficient and a high initial accuracy.

The REF19x series are micropower, Low Dropout Voltage (LDV) devices providing a stable output voltage from supplies as low as 100 mV above the output voltage and consuming less than 45 μA of supply current. In sleep mode, which is enabled by applying a low TTL or CMOS level to the sleep pin, the output is turned off and supply current is further reduced to less than 15 μA.

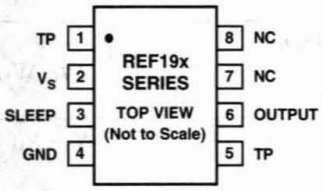
The REF19x series references are specified over the extended industrial temperature range (–40°C to +85°C) with typical performance specifications over –40°C to +125°C for applications such as automotive.

All electrical grades are available in 8-pin SOIC; the PDIP and TSSOP are only available in the lowest electrical grade. Products are also available in die form.

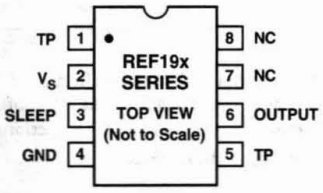
*Protected by U.S. Patent 5291122.

PIN CONFIGURATIONS

8-Lead Narrow-Body SO and TSSOP (S Suffix and RU Suffix)



8-Lead Epoxy DIP (P Suffix)



NC = NO CONNECT
TP PINS ARE FACTORY TEST POINTS
NO USER CONNECTION

Table I.

Part Number	Nominal Output Voltage (V)
REF191	2.048
REF192	2.50
REF193	3.00
REF194	4.50
REF195	5.00
REF196	3.30
REF198	4.096

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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
REF19xGP	–40°C to +85°C	8-Pin Plastic DIP[2]	N-8
REF19xES[3]	–40°C to +85°C	8-Pin SOIC	SO-8
REF19xFS[3]	–40°C to +85°C	8-Pin SOIC	SO-8
REF19xGS	–40°C to +85°C	8-Pin SOIC	SO-8
REF19xGRU	–40°C to +85°C	8-Pin TSSOP	TSSOP-8
REF19xGBC	+25°C	DICE	

NOTES
[1]For outline information see Package Information section.
[2]8-pin plastic DIP only available in "G" grade.
[3]REF193 and REF196 are available in "G" grade only.

REF191–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = 3.3 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
INITIAL ACCURACY[1]						
"E" Grade	V_O	I_{OUT} = 0 mA	2.046	2.048	2.050	V
"F" Grade			2.043		2.053	V
"G" Grade			2.038		2.058	V
LINE REGULATION[2]						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
"F & G" Grades				4	8	ppm/V
LOAD REGULATION[2]						
"E" Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 ≤ I_{OUT} ≤ 30 mA		4	10	ppm/mA
"F & G" Grades				6	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.0 V, I_{LOAD} = 2 mA			0.95	V
		V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 25 mA			1.55	V
LONG-TERM STABILITY[3]	ΔV_O	1000 Hours @ +125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		20		μV p-p

NOTES
[1]Initial accuracy includes temperature hysteresis effect.
[2]Line and load regulation specifications include the effect of self-heating.
[3]Long-term drift is guaranteed by 1000 hours life test performed on three independent wafer lots at +125°C, with an LTPD of 1.3.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = 3.3 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
TEMPERATURE COEFFICIENT[1, 2]						
"E" Grade	TCV_O/°C	I_{OUT} = 0 mA		2	5	ppm/°C
"F" Grade				5	10	ppm/°C
"G" Grade[3]				10	25	ppm/°C
LINE REGULATION[4]						
"E" Grade	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
"F & G" Grades				10	20	ppm/V
LOAD REGULATION[4]						
"E" Grade	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 ≤ I_{OUT} ≤ 25 mA		5	15	ppm/mA
"F & G" Grades				10	20	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.0 V, I_{LOAD} = 2 mA			0.95	V
		V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 25 mA			1.55	V
SLEEP PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				–8	μA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				–8	μA
SUPPLY CURRENT		No Load			45	μA
Sleep Mode		No Load			15	μA

NOTES
[1]For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.
[2]TCV_O is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C.

$$TCV_O = (V\,max - V\,min)/V_O\,(T_{MAX} - T_{MIN}).$$

[3]Guaranteed by characterization.
[4]Line and load regulation specifications include the effect of self-heating.
Specifications subject to change without notice.

Sample/Track-Hold Amplifiers
Contents

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Sample/Track-Hold Amplifiers–Selection Guides

±1 V Input Range

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate mV/µs max	# Pins	Page No.	Comments	Fax-code
AD9100	0.01	0.023	0.8	<0.001	6000	20/28	12–7	14-Bit Accurate, 23 ns to 0.01%	1457
AD9101	0.1	0.007	0.5	<0.001	9000	20/28	12–9	12-Bit Accurate, 7 ns to 0.01%	1458

±3 V Input Range

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate mV/µs max	# Pins	Page No.	Comments	Fax-code
AD783	0.01	0.375	15	0.01	1	8	12–5	Single	1361
SMP04	0.01	7.0	NS	NS	0.025	16	12–11	Quad	1773
SMP08	0.1	7.0	NS	NS	0.02	16	12–13	Octal, 1 Input, 8 Outputs	1774
SMP18	0.01	3.5	NS	NS	0.04	16	12–15	Octal, 1 Input, 8 Outputs	1777

±5 V Input Range

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate mV/µs max	# Pins	Page No.	Comments	Fax-code
AD781	0.01	0.7	25	0.05	1	8	*	Single	1356
AD684	0.01	1.0	20	0.1	1	16	*	Quad	1233

±10 V Input Range

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate mV/µs max	# Pins	Page No.	Comments	Fax-code
AD585	0.01	3.0	35	0.5	1	14/18	12–3	With On-Chip Hold Cap	1181

*Product not recommended for new designs; for complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

High Speed, Precision Sample-and-Hold Amplifier

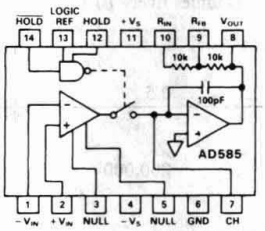
AD585

FEATURES
3.0 μs Acquisition Time to ±0.01% max
Low Droop Rate: 1.0 mV/ms max
Sample/Hold Offset Step: 3 mV max
Aperture Jitter: 0.5 ns
Extended Temperature Range: –55°C to +125°C
Internal Hold Capacitor
Internal Application Resistors
±12 V or ±15 V Operation
Available in Surface Mount

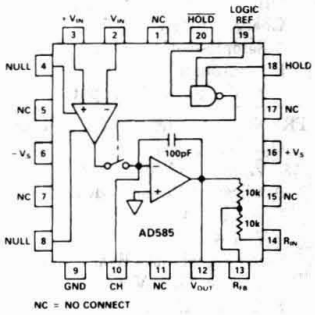
APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM

DIP



LCC/PLCC Package



PRODUCT DESCRIPTION

The AD585 is a complete monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultralow leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and matched applications resistors have been provided for high precision and applications flexibility.

The performance of the AD585 makes it ideal for high speed 10- and 12-bit data acquisition systems, where fast acquisition time, low sample-to-hold offset, and low droop are critical. The AD585 can acquire a signal to ±0.01% in 3 μs maximum, and then hold that signal with a maximum sample-to-hold offset of 3 mV and less than 1 mV/ms droop, using the on-chip hold capacitor. If lower droop is required, it is possible to add a larger external hold capacitor.

The high speed analog switch used in the AD585 exhibits aperture jitter of 0.5 ns, enabling the device to sample full scale (20 V peak-to-peak) signals at frequencies up to 78 kHz with 12-bit precision.

The AD585 can be used with any user-defined feedback network to provide any desired gain in the sample mode. On-chip precision thin-film resistors can be used to provide gains of +1, –1, or +2. Output impedance in the hold mode is sufficiently low to maintain an accurate output signal even when driving the dynamic load presented by a successive-approximation A/D converter. However, the output is protected against damage from accidental short circuits.

The control signal for the HOLD command can be either active high or active low. The differential HOLD signal is compatible with all logic families, if a suitable reference level is provided. An on-chip TTL reference level is provided for TTL compatibility.

The AD585 is available in three performance grades. The JP grade is specified for the 0°C to +70°C commercial temperature range and packaged in a 20-pin PLCC. The AQ grade is specified for the –25°C to +85°C industrial temperature range and is packaged in a 14-pin cerdip. The SQ and SE grades are specified for the –55°C to +125°C military temperature range and are packaged in a 14-pin cerdip and 20-pin LCC.

PRODUCT HIGHLIGHTS

1. The fast acquisition time (3 μs) and low aperture jitter (0.5 ns) make it the first choice for very high speed data acquisition systems.
2. The droop rate is only 1.0 mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
3. The low charge transfer of the analog switch keeps sample-to-hold offset below 3 mV with the on-chip 100 pF hold capacitor, eliminating the trade-off between acquisition time and S/H offset required with other SHAs.
4. The AD585 has internal pretrimmed application resistors for applications versatility.
5. The AD585 is complete with an internal hold capacitor for ease of use. Capacitance can be added externally to reduce the droop rate when long hold times and high accuracy are required.
6. The AD585 is recommended for use with 10- and 12-bit successive-approximation A/D converters such as AD573, AD574A, AD674A, AD7572 and AD7672.
7. The AD585 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD585/883B data sheet for detailed specifications.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD585—SPECIFICATIONS (typical @ +25°C and V_S = ±12 V or ±15 V, and C_H = Internal, A = +1, $\overline{HOLD}$ active unless otherwise noted)

Model	AD585J			AD585A			AD585S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SAMPLE/HOLD CHARACTERISTICS										
Acquisition Time, 10 V Step to 0.01%			3			3			3	µs
20 V Step to 0.01%			5			5			5	µs
Aperture Time, 20 V p-p Input, $\overline{HOLD}$ 0 V		35			35			35		ns
Aperture Jitter, 20 V p-p Input, $\overline{HOLD}$ 0 V		0.5			0.5			0.5		ns
Settling Time, 20 V p-p Input, $\overline{HOLD}$ 0 V, to 0.01%		0.5			0.5			0.5		µs
Droop Rate			1			1			1	mV/ms
Droop Rate T_{MIN} to T_{MAX}		Doubles Every 10°C			Double Every 10°C			Doubles Every 10°C		
Charge Transfer			0.3			0.3			0.3	pC
Sample-to-Hold Offset	–3		3	–3		3	–3		3	mV
Feedthrough 20 V p-p, 10 kHz Input		0.5			0.5			0.5		mV
TRANSFER CHARACTERISTICS[1]										
Open Loop Gain V_{OUT} = 20 V p-p, R_L = 2k		200,000			200,000			200,000		V/V
Application Resistor Mismatch			0.3			0.3			0.3	%
Common-Mode Rejection V_{CM} = ±10 V	80			80			80			dB
Small Signal Gain Bandwidth V_{OUT} = 100 mV p-p		2.0			2.0			2.0		MHz
Full Power Bandwidth V_{OUT} = 20 V p-p		160			160			160		kHz
Slew Rate V_{OUT} = 20 V p-p		10			10			10		V/µs
Output Resistance (Sample Mode) I_{OUT} = ±10 mA			0.05			0.05			0.05	Ω
Output Short Circuit Current		50			50			50		mA
Output Short Circuit Duration		Indefinite			Indefinite			Indefinite		
ANALOG INPUT CHARACTERISTICS										
Offset Voltage			5			2			2	mV
Offset Voltage, T_{MIN} to T_{MAX}			6			3			3	mV
Bias Current			2			2			2	nA
Bias Current, T_{MIN} to T_{MAX}			5			5		20	50[2]	nA
Input Capacitance, f = 1 MHz		10			10			10		pF
Input Resistance, Sample or Hold 20 V p-p Input, A = +1		10^{12}			10^{12}			10^{12}		Ω
DIGITAL INPUT CHARACTERISTICS										
TTL Reference Output	1.2	1.4	1.6	1.2	1.4	1.6	1.2	1.4	1.6	V
Logic Input High Voltage T_{MIN} to T_{MAX}	2.0			2.0			2.0			V
Logic Input Low Voltage T_{MIN} to T_{MAX}			0.8			0.8			0.7	V
Logic Input Current (Either Input)			50			50			50	µA
POWER SUPPLY CHARACTERISTICS										
Operating Voltage Range	+5, –10.8		±18	+5, –10.8		±18	+5, –10.8		±18	V
Supply Current, R_L = ∞	6		10	6		10	6		10	mA
Power Supply Rejection, Sample Mode	70			70			70			dB
TEMPERATURE RANGE										
Specified Performance	0		+70	–25		+85	–55		+125	°C
PACKAGE OPTIONS[3,4]										
Cerdip (Q-14)					AD585AQ			AD585SQ		
LCC (E-20A)								AD585SE		
PLCC (P-20A)		AD585JP								

NOTES

[1]Maximum input signal is the minimum supply minus a headroom voltage of 2.5 V.

[2]Not tested at –55°C.

[3]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

[4]For AD585/883B specifications, refer to Analog Devices Military Products Databook.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supplies ($+V_S$, $-V_S$) . . . . . ±18 V
Logic Inputs . . . . . $\pm V_S$
Analog Inputs . . . . . $\pm V_S$
R_{IN}, R_{FB} Pins . . . . . $\pm V_S$
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering) . . . . . 300°C
Output Short Circuit to Ground . . . . . Indefinite
TTL Logic Reference Short Circuit to Ground . . . . . Indefinite

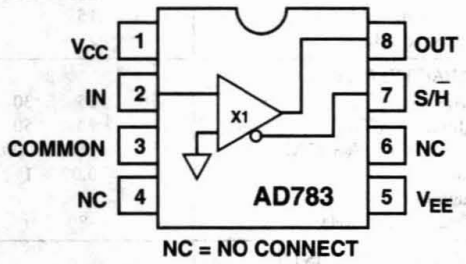
Complete Very High Speed Sample-and-Hold Amplifier

AD783*

FEATURES

Acquisition Time to 0.01%: 250 ns Typical
Low Power Dissipation: 95 mW
Low Droop Rate: 0.02 μV/μs
Fully Specified and Tested Hold Mode Distortion
Total Harmonic Distortion: –85 dB
Aperture Jitter: 50 ps Maximum
Internal Hold Capacitor
Self-Correcting Architecture
8-Pin Mini Cerdip and SOIC Packages

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD783 is a high speed, monolithic sample-and-hold amplifier (SHA). The AD783 offers a typical acquisition time of 250 ns to 0.01%. The AD783 is specified and tested for hold mode total harmonic distortion with input frequencies up to 100 kHz. The AD783 is configured as a unity gain amplifier and uses a patented self-correcting architecture that minimizes hold mode errors and ensures accuracy over temperature. The AD783 is self-contained and requires no external components or adjustments.

The AD783 retains the held value with a droop rate of 0.02 μV/μs. Excellent linearity and hold mode dc and dynamic performance make the AD783 ideal for high speed 12- and 14-bit analog-to-digital converters.

The AD783 is manufactured on Analog Devices' ABCMOS process which merges high performance, low noise bipolar circuitry with low power CMOS to provide an accurate, high speed, low power SHA.

The J grade device is specified for operation from 0°C to +70°C and the A grade from –40°C to +85°C. The J and A grades are available in 8-pin cerdip and SOIC packages. The military temperature range version is specified for operation from –55°C to +125°C and is available in an 8-pin cerdip package. For details refer to the *Analog Devices Military Products Databook* or AD783/883B data sheet.

***Protected by U.S. Patent Number 4,962,325.**

ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Options[2]
AD783JQ	0°C to +70°C	8-Pin Cerdip	Q-8
AD783AQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD783JR	0°C to +70°C	8-Pin SOIC	R-8
AD783AR	–40°C to +85°C	8-Pin SOIC	R-8

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD783/883B data sheet.
[2]Q = Cerdip, R = SOIC. For outline information see Package Information section.

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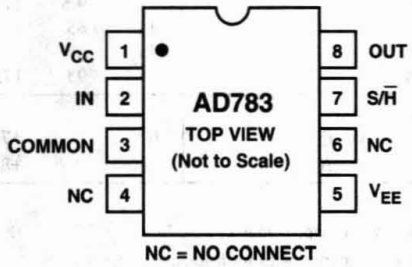
PIN CONFIGURATION



To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD783–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = –5 V ± 5%, C_L = pF, unless otherwise noted)

Parameter	AD783J/A Min	Typ	Max	Units
SAMPLING CHARACTERISTICS				
Acquisition Time				
5 V Step to 0.01%		250	375	ns
5 V Step to 0.1%		200	350	ns
Small Signal Bandwidth		15		MHz
Full Power Bandwidth		2		MHz
HOLD CHARACTERISTICS				
Effective Aperture Delay (+25°C)	–30	15	30	ns
Aperture Jitter (+25°C)		20	50	ps
Hold Settling (to 1 mV, +25°C)		150	200	ns
Droop Rate		0.02	1	µV/µs
Feedthrough (+25°C)				
(V_{IN} = ±2.5 V, 500 kHz)		–80		dB
ACCURACY CHARACTERISTICS[1]				
Hold Mode Offset	–5	0	+5	mV
Hold Mode Offset Drift		10		µV/°C
Sample Mode Offset		50	200	mV
Nonlinearity		±0.005		% FS
Gain Error		±0.03	±0.1	% FS
OUTPUT CHARACTERISTICS				
Output Drive Current	–5		+5	mA
Output Resistance, DC		0.3	0.6	Ω
Total Output Noise (DC to 5 MHz)		150		µV rms
Sampled DC Uncertainty		85		µV rms
Hold Mode Noise (DC to 5 MHz)		125		µV rms
Short Circuit Current				
Source			20	mA
Sink			13	mA
INPUT CHARACTERISTICS				
Input Voltage Range	–2.5		+2.5	V
Bias Current		100	250	nA
Input Impedance		10		MΩ
Input Capacitance		2		pF
DIGITAL CHARACTERISTICS				
Input Voltage Low			0.8	V
Input Voltage High	2.0			V
Input Current High (V_{IN} = 5 V)		2	10	µA
POWER SUPPLY CHARACTERISTICS				
Operating Voltage Range	±4.75	±5	±5.25	V
Supply Current		9.5	17	mA
+PSRR (+5 V ± 5%)	45	65		dB
–PSRR (–5 V ± 5%)	45	65		dB
Power Consumption		95	175	mW
TEMPERATURE RANGE				
Specified Performance (J)	0		+70	°C
(A)	–40		+85	°C

NOTES
[1]Specified and tested over an input range of ±2.5 V.
Specifications subject to change without notice.

HOLD MODE AC SPECIFICATIONS

(T_{MIN} to T_{MAX} with V_{CC} = +5 V ± 5%, V_{EE} = –5 V ± 5%, C_L = 50 pF, unless otherwise noted)[1]

Parameter	AD783J/A Min	Typ	Max	Units
TOTAL HARMONIC DISTORTION				
f_{IN} = 100 kHz		–85	–80	dB
f_{IN} = 500 kHz		–72		dB
SIGNAL-TO-NOISE AND DISTORTION				
f_{IN} = 100 kHz		77		dB
f_{IN} = 500 kHz		70		dB
INTERMODULATION DISTORTION				
(F1 = 99 kHz, F2 = 100 kHz)				
Second Order Products		–80		dB
Third Order Products		–85		dB

NOTES
[1]f_{IN} amplitude = 0 dB and f_{SAMPLE} = 300 kHz unless otherwise indicated.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Spec	With Respect to	Min	Max	Units
V_{CC}	COM	–0.5	+6.5	V
V_{EE}	COM	–6.5	+0.5	V
Analog Input	COM	–6.5	+6.5	V
Digital Input	COM	–0.5	+6.5	V
Output Short Circuit to Ground, V_{CC}, or V_{EE}		Indefinite		
Maximum Junction Temperature			+175	°C
Storage		–65	+150	°C
Lead Temperature (10 sec max)			+300	°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

ANALOG DEVICES

Ultrahigh Speed Monolithic Track-and-Hold

AD9100*

FEATURES

Excellent Hold Mode Distortion into 250 Ω
–88 dB @ 30 MSPS (2.3 MHz V_{IN})
–83 dB @ 30 MSPS (12.1 MHz V_{IN})
–74 dB @ 30 MSPS (19.7 MHz V_{IN})
16 ns Acquisition Time to 0.01%
<1 ps Aperture Jitter
250 MHz Tracking Bandwidth
83 dB Feedthrough Rejection @ 20 MHz
3.3 nV/√Hz Spectral Noise Density
MIL-STD-Compliant Versions Available

APPLICATIONS

A/D Conversion
Direct IF Sampling
Imaging/FLIR Systems
Peak Detectors
Radar/EW/ECM
Spectrum Analysis
CCD ATE

GENERAL DESCRIPTION

The AD9100 is a monolithic track-and-hold amplifier which sets a new standard for high speed and high dynamic range applications. It is fabricated in a mature high speed complementary bipolar process. In addition to innovative design topologies, a custom package is utilized to minimize parasitics and optimize dynamic performance.

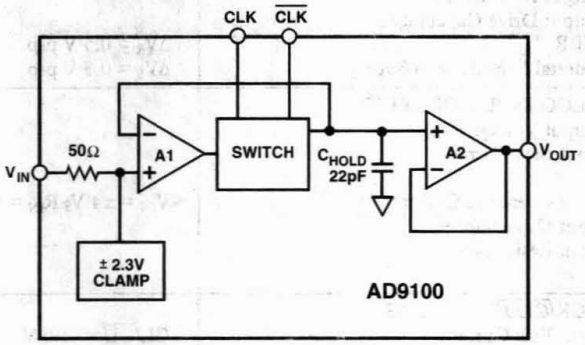
Acquisition time (hold to track) is 13 ns to 0.1% accuracy, and 16 ns to 0.01%. The AD9100 boasts superlative hold-mode frequency domain performance; when sampling at 30 MSPS hold mode distortion is less than 83 dBfs for analog frequencies up to 12 MHz; and –74 dBfs at 20 MHz. The AD9100 can also drive capacitive loads up to 100 pF with little degradation in acquisition time; it is therefore well suited to drive 8- and 10-bit flash converters at clock speeds to 50 MSPS. With a spectral noise density of 3.3 nV/√Hz and feedthrough rejection of 83 dB at 20 MHz, the AD9100 is well suited to enhance the dynamic range of many 8- to 16-bit systems.

The AD9100 is "user friendly" and easy to apply: (1) it requires +5 V/–5.2 V power supplies; (2) the hold capacitor and switch power supply decoupling capacitors are built into the DIP package; (3) the encode clock is differential ECL to minimize clock jitter; (4) the input resistance is typically 800 kΩ; (5) the analog input is internally clamped to prevent damage from voltage transients.

The AD9100 is available in a 20-lead side-brazed "skinny DIP" package and a 28-lead LCC package. Commercial, industrial, and military temperature grade parts are available. Consult the factory for information about the availability of 883-qualified devices.

***Patent pending.**

FUNCTIONAL BLOCK DIAGRAM

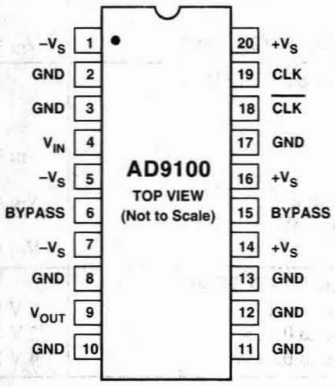


ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±6 V
Continuous Output Current . . . . . 70 mA
Analog Input Voltage[2] . . . . . ±5 V
Operating Temperature Range (Case)
AD9100JD . . . . . 0°C to +70°C
AD9100AD/AE . . . . . –25°C to +85°C
AD9100SD/SE . . . . . –55°C to +125°C
Junction Temperature . . . . . +175°C
Storage Temperature . . . . . –65°C to +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Analog input voltage should not exceed $\pm V_S$.

AD9100 PINOUTS



ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD9100JD	0°C to +70°C	Ceramic DIP	D-28
AD9100AD	–40°C to +85°C	Ceramic DIP	D-28
AD9100AE	–40°C to +85°C	Ceramic LCC	E-28A
AD9100SD	–55°C to +125°C	Ceramic DIP	D-28
AD9100SE	–55°C to +125°C	Ceramic LCC	E-28A

NOTES
[1]Consult factory about availability of parts screened to MIL-STD-883.
[2] For outline information see Package Information section.

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AD9100–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V; $R_{LOAD} = 100\ \Omega$; $R_{IN} = 50\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9100AE/SE/JD/AD/SD[1] Min	Typ	Max	Units
DC ACCURACY							
Gain	$\Delta V_{IN} = 2$ V	Full	VI	0.989	0.994		V/V
Offset	$V_{IN} = 0$ V	Full	VI	–5	±1	+5	mV
Output Resistance		25°C	V		0.4		Ω
Output Drive Capability		Full	VI	±40	±60		mA
PSRR	$\Delta V_S = 0.5$ V p-p	Full	VI	48	55		dB
Pedestal Sensitivity to Supply	$\Delta V_S = 0.5$ V p-p	Full	VI		0.9	3	mV/V
ANALOG INPUT/OUTPUT							
Output Voltage Range		Full	VI	+2	±2.2	–2	V
Input Bias Current		25°C	VI	–8	±3	+8	µA
		Full	VI	–16		+16	µA
Input Overdrive Current[2]	$V_{IN} = \pm 4$ V; $R_{IN} = 50\ \Omega$	25°C	V		±22		mA
Input Capacitance		25°C	V		1.2		pF
Input Resistance		25°C, T_{MAX}	VI	350	800		kΩ
		T_{MIN}	VI	200			kΩ
CLOCK/$\overline{\text{CLOCK}}$ INPUTS							
Input Bias Current	CL/$\overline{\text{CL}}$ = –1.0 V	Full	VI		4	5	mA
Input Low Voltage (V_{IL})		Full	VI	–1.8		–1.5	V
Input High Voltage (V_{IH})		Full	VI	–1.0		–0.8	V
TRACK MODE DYNAMICS							
Bandwidth (–3 dB)	$V_{OUT} \le 0.4$ V p-p	Full	IV	150	250		MHz
Slew Rate	4 V Step	25°C	IV	550	850		V/µs
	4 V Step	Full	IV	500			V/µs
Overdrive Recovery Time[2] (to 0.1%)	$V_{IN} = \pm 4$ V to 0 V	25°C	V		21		ns
2nd Harm. Dist. (20 MHz, 2 V p-p)		Full	V		–65		dBc
3rd Harm. Dist. (20 MHz, 2 V p-p)		Full	V		–75		dBc
Integrated Output Noise (1-200 MHz)		25°C	V		45		µV
RMS Spectral Noise @ 10 MHz		25°C	V		3.3		nV/$\sqrt{\text{Hz}}$
HOLD MODE DYNAMICS							
Worst Harmonic (2.3 MHz, 30 MSPS)	$V_{OUT} = 2$ V p-p	25°C	V		–83		dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p-p	25°C	IV		–80	–72	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p-p	T_{MAX}	IV			–70	dBfs
Worst Harmonic (12.1 MHz, 30 MSPS)	$V_{OUT} = 2$ V p-p	T_{MIN}	IV		–77	–68	dBfs
Worst Harmonic (19.7 MHz, 30 MSPS)	$V_{OUT} = 2$ V p-p	25°C	V		–74		dBfs
Hold Noise[3]		25°C	V		300 × t_H		V/s rms
Droop Rate[4]	$V_{IN} = 0$ V	25°C	VI		1	6	±mV/µs
		T_{MIN}	VI		7	40	±mV/µs
		T_{MAX}	VI		5	30	±mV/µs
Feedthrough Rejection (20 MHz)	$V_{IN} = 2$ V p-p	Full	V		83		dB
TRACK-TO-HOLD SWITCHING							
Aperture Delay		25°C	V		+800		ps
Aperture Jitter		25°C	V		<1		ps
Pedestal Offset	$V_{IN} = 0$ V	25°C	VI	–5	±1	+5	mV
		Full	VI	–10		+10	mV
Transient Amplitude	$V_{IN} = 0$ V	Full	V		±6		mV
Settling Time to 1 mV		Full	IV		7	10	ns
Glitch Product	$V_{IN} = 0$ V	25°C	V		15		pV-s
HOLD-TO-TRACK SWITCHING							
Acquisition Time to 0.1%	2 V Step	25°C	V		13		ns
Acquisition Time to 0.01%	2 V Step	Full	IV		16	23	ns
Acquisition Time to 0.01%	4 V Step	25°C	V		20		ns
POWER SUPPLY							
Power Dissipation		Full	VI		1.05	1.25	W
$+V_S$ Current		Full	VI		96	118	mA
$-V_S$ Current		Full	VI		116	132	mA

NOTES

[1]AD9100JD: 0°C to +70°C. AD9100AD: –40°C to +85°C. AD9100SD: –55°C to +125°C. DIP $\theta_{JA} = 38$°C/W; this is valid with the device mounted flush to a grounded 2 oz copper clad board with 16 sq inches of surface area and no air flow. LCC $\theta_{JA} = 48$°C/W.

[2]The input to the AD9100 is internally clamped at ±2.3 V. The internal input series resistance is nominally 50 Ω.

[3]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 6 µV (300 V/s × 20 ns). This value must be combined with the track mode noise to obtain total noise.

[4]Min and max droop rates are based on the military temperature range (–55°C to +125°C). Refer to the "Droop Rate vs Temperature" chart for min/max limits over the commercial and industrial ranges.

Specifications subject to change without notice.

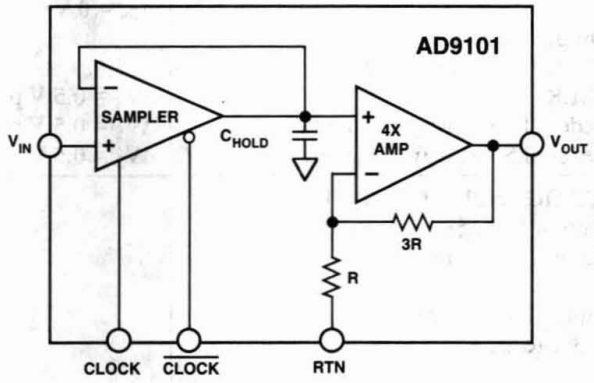
125 MSPS Monolithic Sampling Amplifier

AD9101

FEATURES
350 MHz Sampling Bandwidth
125 MHz Sampling Rate
Excellent Hold Mode Distortion
–75 dB @ 50 MSPS (25 MHz V_{IN})
–57 dB @ 125 MSPS (50 MHz V_{IN})
7 ns Acquisition Time to 0.1%
<1 ps Aperture Jitter
66 dB Feedthrough Rejection @ 50 MHz
3.3 nV/$\sqrt{Hz}$ Spectral Noise Density

APPLICATIONS
Direct IF Sampling
Digital Sampling Oscilloscopes
HDTV Cameras
Peak Detectors
Radar/EW/ECM
Spectrum Analysis
Test Equipment/CCD Testers
DDS DAC Deglitcher

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9101 is an extremely accurate, general purpose, high speed sampling amplifier. Its fast and accurate acquisition speed allows for a wide range of frequency vs. resolution performance. The AD9101 is capable of 8 to 12 bits of accuracy at clock rates of 125 MSPS or 50 MSPS, respectively. This level of performance makes it an ideal driver for almost all 8- to 12-bit A/D encoders on the market today.

In effect, the AD9101 is a track-and-hold with a post amplifier. This configuration allows the front end sampler to operate at relatively low signal amplitudes. This results in dramatic improvement in both track and hold mode distortion while keeping power low.

The gain-of-four output amplifier has been optimized for fast and accurate large signal step settling characteristics even when heavily loaded. This amplifier's fast Settling Time Linearity (STL) characteristic causes the amplifier to be transparent to the low signal level distortion of the sampler. When sampled, output distortion levels reflect only the distortion performance of the sampler.

Dramatic SNR and distortion improvements can be realized when using the AD9101 with high speed flash converters. Flash converters generally have excellent linearity at dc and low frequencies. However, as signal slew rate increases, their performance degrades due to the internal comparators' aperture delay variations and finite gain bandwidth product.

The benefits of using a track-and-hold ahead of a flash converter have been well known for many years. However, before the AD9101, there was no track-and-hold amplifier with sufficient bandwidth and linearity to markedly increase the dynamic performance of such flashes as the AD9002, AD9012, AD9020, and AD9060.

A new application made possible by the AD9101 is direct IF-to-digital conversion. Utilizing the Nyquist principle, the IF frequency can be rejected, and the baseband signal can be recovered. As an example, a 40 MHz IF is modulated by a 10 MHz bandwidth signal. By sampling at 25 MSPS, the signal of interest is detected.

The AD9101 is offered in commercial and military temperature ranges. Commercial versions include the AD9101AR in plastic SOIC and AD9101AE in ceramic LCC. Military devices are available in ceramic LCC. Contact the factory for availability of versions in DIP and/or military versions.

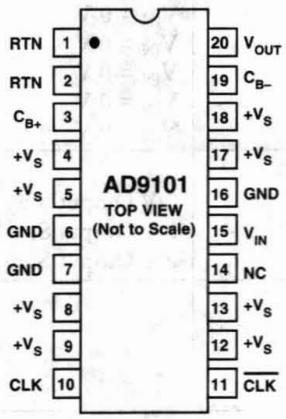
ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option*
AD9101AR	–40°C to +85°C	Plastic SOIC	R-20
AD9101AE	–40°C to +85°C	LCC	E-20A
AD9101SE	–55°C to +125°C	LCC	E-20A

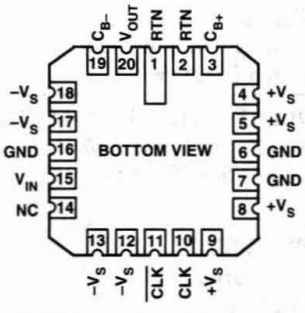
*For outline information see Package Information section.

PIN CONFIGURATIONS

20-Pin SOIC



20-Pin Ceramic LCC



NC=NO CONNECT

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AD9101–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V, $-V_S$ = –5.2 V, R_{LOAD} = 100 Ω, R_{IN} = 50 Ω, unless otherwise noted.)

Parameter	Conditions	Temp	Min	Typ	Max	Units
DC ACCURACY						
Gain	ΔV_{IN} = 0.5 V	25°C	3.93	4	4.07	V/V
	ΔV_{IN} = 0.5 V	Full	3.9		4.1	V/V
Offset	V_{IN} = 0 V	25°C		±3	±10	mV
	V_{IN} = 0 V	Full			+15	mV
Output Resistance		25°C		0.4		Ω
Output Drive Capability		Full	±60	±70		mA
PSRR	ΔV_S = 0.5 V p-p	25°C	37	43		dB
Pedestal Sensitivity to Supply	ΔV_S = 0.5 V p-p	Full		4		mV/V
Pedestal Sensitivity to Supply	ΔV_S = 0.5 V p-p	Full		8		mV/V
ANALOG INPUT/OUTPUT						
Output Voltage Range		Full	±2.4	±2.7		V
Input Bias Current		25°C		±5	±15	μA
		Full			±20	μA
Input Capacitance		25°C		2		pF
Input Resistance		25°C–T_{MAX}	30	125		kΩ
		T_{MIN}	25			kΩ
CLOCK/$\overline{\text{CLOCK}}$ INPUTS						
Input Bias Current	CL/$\overline{\text{CL}}$ = –1.0 V	Full		3	3.6	mA
Input Low Voltage (V_{IL})	V_{IN} = 0.5 V p-p	Full	–1.8		–1.5	V
Input High Voltage (V_{IH})	V_{IN} = 0.5 V p-p	Full	–1.0		–0.8	V
TRACK MODE DYNAMICS						
Bandwidth (–3 dB)	V_{OUT} = 1 V p-p	Full	160	250		MHz
Slew Rate	4 V Output Step	Full	1300	1800		V/μs
Overdrive Recovery Time (to 0.1%)	V_{IN} = ±1 V to 0 V	25°C		55		ns
Integrated Output Noise	(5 MHz–200 MHz)	25°C		210		μV
RMS Spectral Noise @ 10 MHz		25°C		3.3		nV/$\sqrt{\text{Hz}}$
HOLD MODE DYNAMICS						
Worst Harmonic (23 MHz, 50 MSPS)	V_{OUT} = 2 V p-p	25°C		–75		dBFS
Worst Harmonic (48 MHz, 100 MSPS)	V_{OUT} = 2 V p-p	25°C		–62	–57	dBFS
Worst Harmonic (48 MHz, 100 MSPS)	V_{OUT} = 2 V p-p	Full (Ind.)			–53	dBFS
Worst Harmonic (48 MHz, 100 MSPS)	V_{OUT} = 2 V p-p	Full (Mil.)			–51	dBFS
Worst Harmonic (48 MHz, 125 MSPS)	V_{OUT} = 2 V p-p	25°C		–57		dBFS
Sampling Bandwidth (–3 dB)	V_{IN} = 0.5 V p-p	25°C		350		MHz
Hold Noise (RMS)		Full		150 × t_H		mV/s
Droop Rate		25°C		±5	±18	mV/μs
		Full			±40	mV/μs
Feedthrough Rejection (50 MHz)	V_{OUT} = 2 V p-p	Full		–66		dB
TRACK-TO-HOLD SWITCHING						
Aperture Delay		25°C		–250		ps
Aperture Jitter		25°C		<1		ps rms
Pedestal Offset	V_{IN} = 0 V	25°C		±5	±20	mV
	V_{IN} = 0 V	Full			±35	mV
Transient Amplitude	V_{IN} = 0 V	Full		8		mV
Settling Time to 4 mV	V_{IN} = 0 V	Full		4		ns
Glitch Product	V_{IN} = 0 V	25°C		20		pV-s
HOLD-TO-TRACK SWITCHING						
Acquisition Time to 0.1%	2 V Output Step	25°C		7		ns
Acquisition Time to 0.01%	2 V Output Step	25°C		11	14	ns
	2 V Output Step	Full			16	ns
POWER SUPPLY						
$+V_S$ Current		Full		55	70	mA
$-V_S$ Current		Full		59	73	mA
Power Dissipation		Full		570	715	mW

Specifications subject to change without notice.

ANALOG DEVICES

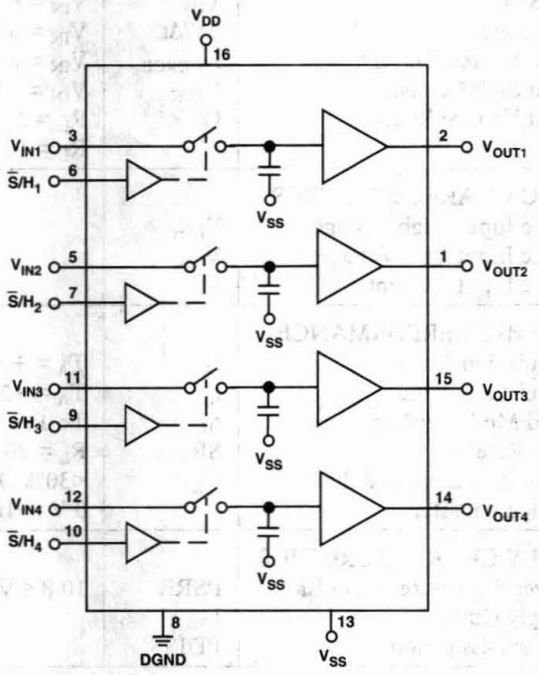
CMOS Quad Sample-and-Hold Amplifier

SMP04

FEATURES
- Four Independent Sample-and-Holds
- Internal Hold Capacitors
- High Accuracy: 12-Bit
- Very Low Droop Rate (2 mV/s typ)
- Output Buffers Stable for $C_L \leq 500$ pF
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Applications
- Monolithic Low Power CMOS Design

APPLICATIONS
- Signal Processing Systems
- Multichannel Data Acquisition Systems
- Automatic Test Equipment
- Medical and Analytical Instrumentation
- Event Analysis
- DAC Deglitching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

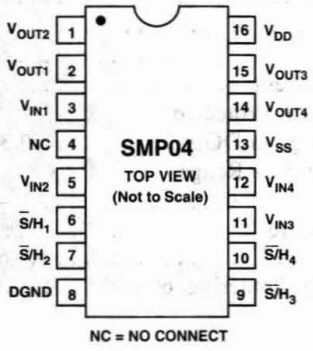
The SMP04 is a monolithic quad sample-and-hold; it has four internal precision buffer amplifiers and internal hold capacitors. It is manufactured in ADI's advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate and fast acquisition time required by data acquisition and signal processing systems. The device can acquire an 8-bit input signal to ±1/2 LSB in less than seven microseconds. The SMP04 can operate from single or dual power supplies with TTL/CMOS logic compatibility. Its output swing includes the negative supply.

The SMP04 is ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more can be used with a single or multiple DACs to provide multiple setpoints within a system.

The SMP04 offers significant cost and size reduction over equivalent module or discrete designs. It is available in a 16-pin hermetic or plastic DIP and surface mount SOIC packages. It is specified over the extended industrial temperature range of 0°C to +85°C.

PIN CONNECTIONS

16-Pin Cerdip
(Q Suffix)
16-Pin Plastic DIP
(P Suffix)
16-Pin SO
(S Suffix)



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SMP04EQ	–40°C to +85°C	Cerdip-16	Q-16
SMP04EP	–40°C to +85°C	PDIP-16	N-16
SMP04ES	–40°C to +85°C	SO-16	R-16A

*For outline information see Package Information section.

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SMP04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +12.0 V, V_{SS} = DGND = 0 V, R_L = No Load, T_A = Operating Temperature Range specified in Absolute Maximum Ratings, unless otherwise noted.)

Parameter	Symbol	Conditions	SMP04 Min	SMP04 Typ	SMP04 Max	Units
Linearity Error				0.01		%
Buffer Offset Voltage	V_{OS}	V_{IN} = 6 V	–10	±2.5	+10	mV
Hold Step	V_{HS}	V_{IN} = 6 V		1	±4	mV
Droop Rate	$\Delta V/\Delta t$	V_{IN} = 6 V, T_A = +25°C		2	25	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 6 V[1]	0.5			mA
Output Voltage Range	OVR	R_L = 20 kΩ	0.06		10.0	V
		R_L = 10 kΩ	0.06		9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}			0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_A	T_A = +25°C, 0 V to 10 V Step to 0.1%		7		µs
Acquisition Time	t_A	T_A = +25°C, 0 V to 10 V Step to 0.01%		9		µs
Hold Mode Settling Time	t_H	To 1 mV		1		µs
Slew Rate	SR	R_L = 20 kΩ[3]	3	4		V/µs
Capacitive Load Stability	C_L	<30% Overshoot		500		pF
Analog Crosstalk		0 V to 10 V Step		–80		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8 ≤ V_{DD} ≤ 13.2 V	60	75		dB
Supply Current	I_{DD}			4	7	mA
Power Dissipation	PDISS				84	mW

NOTES
[1]Outputs are capable of sinking and sourcing over 20 mA but linearity and offset are guaranteed at specified load levels.
[2]All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[3]Slew rate is measured in the sample mode with a 0 V to 10 V step from 20% to 80%.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... –0.3 V, 17 V
V_{DD} to V_{SS} ..... –0.7 V, 17 V
V_{LOGIC} to DGND ..... –0.3 V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20 mA
(Not Short-Circuit Protected)
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} +0.3 V
Operating Temperature Range
EQ, EP, ES ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
16-Pin Cerdip (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SO (S)	92	27	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and function operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.

Octal Sample-and-Hold with Multiplexed Input

SMP08*

FEATURES
Internal Hold Capacitors
Low Droop Rate
TTL/CMOS Compatible Logic Inputs
Single or Dual Supply Operation
Break-Before-Make Channel Addressing
Compatible With CD4051 Pinout
Low Cost

APPLICATIONS
Multiple Path Timing Deskew for A.T.E.
Memory Programmers
Mass Flow/Process Control Systems
Multichannel Data Acquisition Systems
Robotics and Control Systems
Medical and Analytical Instrumentation
Event Analysis
Stage Lighting Control

GENERAL DESCRIPTION

The SMP08 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP08 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than 7 microseconds. The SMP08's output swing includes the negative supply in both single and dual supply operation.

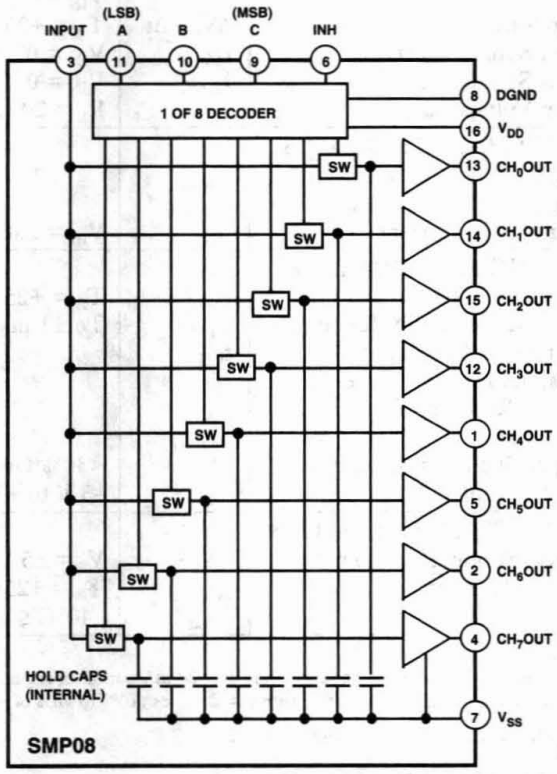
The SMP08 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP08 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP08 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP08s can be used with single or multiple DACs to provide multiple set points within a system.

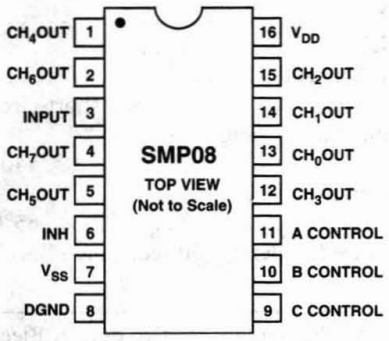
The SMP08 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP, or surface-mount SOIC package.

***Manufactured under the following U.S. patent: 4,739,281**

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTION



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ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SMP08FQ	–40°C to +85°C	Cerdip	Q-16
SMP08FP	–40°C to +85°C	Plastic DIP	N-16
SMP08FS	–40°C to +85°C	SO-16	R-16A

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

SMP08–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5 V, V_{SS} = –5 V, DGND = 0 V, R_L = No Load, T_A = –40°C to +85°C for SMP08F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		–3 V ≤ V_{IN} ≤ +3 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C		2.5	10	mV
		–40°C ≤ T_A ≤ +85°C		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 0 V, T_A = +25°C to +85°C		2.8	4	mV
		V_{IN} = 0 V, T_A = –40°C			5	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0 V		2	20	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	–3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, –3 V to +3 V to 0.1%		3.6		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate	SR			3		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		–3 V to +3 V Step		–72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±6 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		4	7.5	mA
		–40°C ≤ T_A ≤ +85°C		5	9.5	

NOTES

[1]Outputs are capable of sinking and sourcing over 20 mA but offset is guaranteed at specified load levels.

[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND ..... –0.3 V, 17 V
V_{DD} to V_{SS} ..... –0.3 V, 17 V
V_{LOGIC} to DGND ..... –0.3 V, V_{DD}
V_{IN} to DGND ..... V_{SS}, V_{DD}
V_{OUT} to DGND ..... V_{SS}, V_{DD}
Analog Output Current ..... ±20 mA
(Not short-circuit protected)
Operating Temperature Range
FP, FS ..... –40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	27	°C/W

NOTES

[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SMP08 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

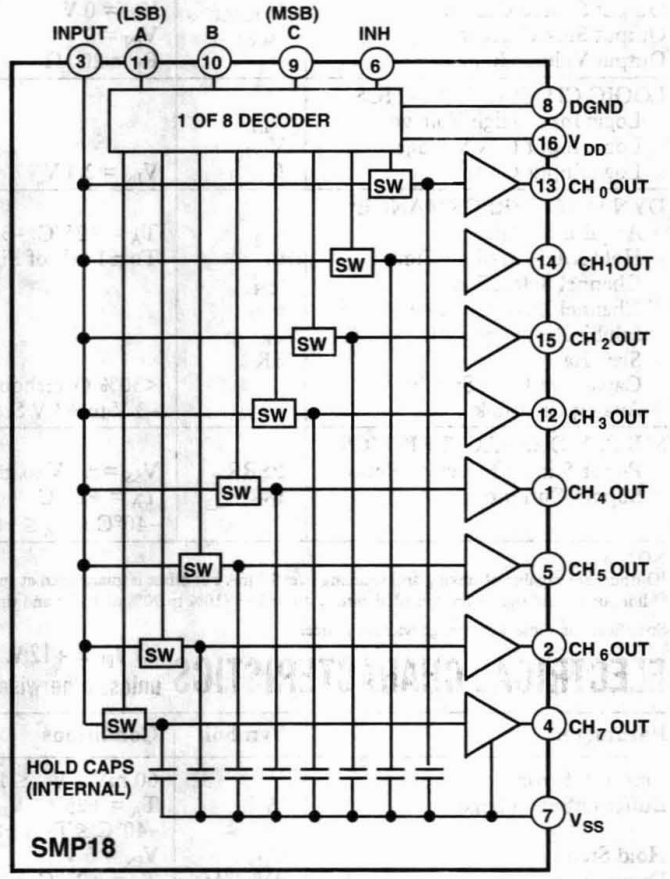
Octal Sample-and-Hold with Multiplexed Input

SMP18

FEATURES
- High Speed Version of SMP08
- Internal Hold Capacitors
- Low Droop Rate
- TTL/CMOS Compatible Logic Inputs
- Single or Dual Supply Operation
- Break-Before-Make Channel Addressing
- Compatible With CD4051 Pinout
- Low Cost

APPLICATIONS
- Multiple Path Timing Deskew for A.T.E.
- Memory Programmers
- Mass Flow/Process Control Systems
- Multichannel Data Acquisition Systems
- Robotics and Control Systems
- Medical and Analytical Instrumentation
- Event Analysis
- Stage Lighting Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

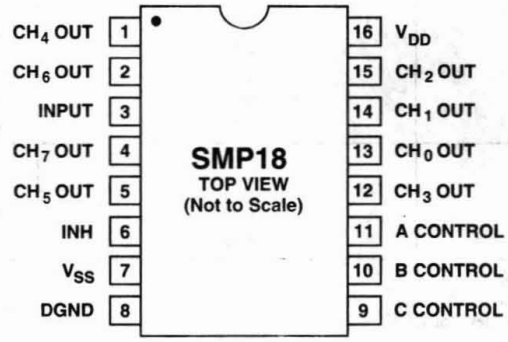
The SMP18 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP18 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than 2.5 microseconds. The SMP18's output swing includes the negative supply in both single and dual supply operation.

The SMP18 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP18 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP18 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP18s can be used with single or multiple DACs to provide multiple set points within a system.

The SMP18 offers significant cost and size reduction over discrete designs. It is available in a 16-pin plastic DIP or narrow body SO-16 surface-mount SOIC package. The SMP18 is a higher speed direct replacement for the SMP08.

PIN CONNECTION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SMP18FP	–40°C to +85°C	Plastic DIP	N-16
SMP18FRU	–40°C to +85°C	TSSOP-16	RU-16
SMP18FS	–40°C to +85°C	SO-16	R-16A

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

SMP18–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V, V_{SS} = –5 V, DGND = 0 V, R_L = No Load, T_A = –40°C to +85°C for SMP18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		–3 V ≤ V_{IN} ≤ +3 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 0 V		2.5	10	mV
		–40°C ≤ T_A ≤ +85°C, V_{IN} = 0 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 0 V		4	8	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	–3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, –3 V to +3 V to 0.1%		3.5		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate	SR			6		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		–3 V to +3 V Step		–72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_{SS} = ±5 V to ±6 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		5.5	7.5	mA
		–40°C ≤ T_A ≤ +85°C		7.5	9.5	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +12 V, V_{SS} = 0 V, DGND = 0 V, R_L = No Load, T_A = –40°C to +85°C for SMP18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Limits
Linearity Error		60 mV ≤ V_{IN} ≤ 10 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 6 V		2.5	10	mV
		–40°C ≤ T_A ≤ +85°C, V_{IN} = 6 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 6 V		4	8	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 6 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	0.06		10.0	V
		R_L = 10 kΩ	0.06		9.5	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10 V to 0.1%		2.5		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate[3]	SR			7		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		0 to 10 V Step		–72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	10.8 V ≤ V_{DD} ≤ 13.2 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		6.0	8.0	mA
		–40°C ≤ T_A ≤ +85°C		8.0	10.0	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[3]Slew rate is measured in the sample mode with a 0 to 10 V step from 20% to 80%.

Specifications subject to change without notice.

Variable Gain Amplifiers
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Variable Gain Amplifiers–Selection Guides

Single

Model	V_{SS} Volts	I_{DD} mA	I_{DD} mA	Range dB	–3 dB BW MHz	Input Spectral Noise nV/√Hz	Input Resistance Ohms	Slew Rate V/µs	Accuracy +25°C %	I3P dB	1 dB Comp @ 10 MHz	Grade Temp Range 0°C to +70°C	Grade Temp Range –40°C to +85°C	# Pins	Page No.	Comments	Fax-code
AD603	±5	17	20	–11–+31	90	1.4	100	275	±1	NS	NS		A	8	13–5	Pin Programmable Gain Ranges	1195

Duals

Model	V_{SS} Volts	I_{DD} mA	I_{DD} mA	Range dB	–3 dB BW MHz	Input Spectral Noise nV/√Hz	Input Resistance Ohms	Slew Rate V/µs	Accuracy +25°C %	I3P dB	1 dB Comp @ 10 MHz	Grade Temp Range 0°C to +70°C	Grade Temp Range –40°C to +85°C	# Pins	Page No.	Comments	Fax-code
AD600	±5	12.5	14	0–+40	35	1.4	100	275	1.5	ns	ns	J		16	13–3		1193
AD600									0.5	ns	ns		A	16	13–3		1193
AD602	±5	12.5	14	–10–+30	35	1.4	100	275	1.5	ns	ns	J		16	13–3		1193
AD602									0.5	ns	ns		A	16	13–3		1193
AD604	±5	31	31	0–+48	40	0.8	300 k		0.5	TBD	TBD	J		24	13–7	With Powerdown, Pin Programmable Gain Ranges, Preamp	1959
AD605	+5	19		–14–+34	40	1.8	200		0.5	–6			A	16	13–9		1941
AD605				0–+40											13–9		1941
				+9–+51	9			9									

Dual, Low Noise, Wideband Variable Gain Amplifiers

AD600/AD602*

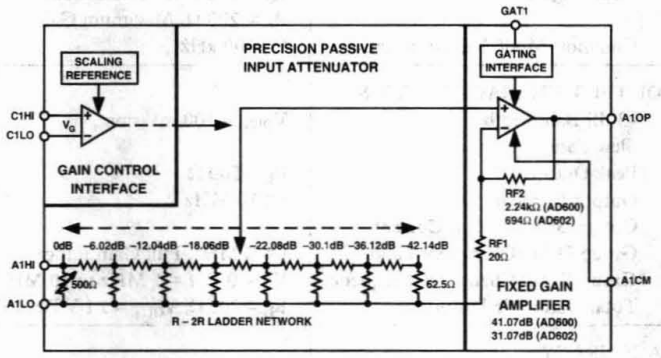
FEATURES

Two Channels with Independent Gain Control
"Linear in dB" Gain Response
Two Gain Ranges:
AD600: 0 dB to +40 dB
AD602: –10 dB to +30 dB
Accurate Absolute Gain: ±0.3 dB
Low Input Noise: 1.4 nV/√Hz
Low Distortion: –60 dBc THD at ±1 V Output
High Bandwidth: DC to 35 MHz (–3 dB)
Stable Group Delay: ±2 ns
Low Power: 125 mW (max) per Amplifier
Signal Gating Function for Each Amplifier
Drives High Speed A/D Converters
MIL-STD-883 Compliant and DESC Versions Available

APPLICATIONS

Ultrasound and Sonar Time-Gain Control
High Performance Audio and RF AGC Systems
Signal Measurement

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD600 and AD602 dual channel, low noise variable gain amplifiers are optimized for use in ultrasound imaging systems, but are applicable to any application requiring very precise gain, low noise and distortion, and wide bandwidth. Each independent channel provides a gain of 0 dB to +40 dB in the AD600 and –10 dB to +30 dB in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio at the output. However, both products have the same 1.4 nV/√Hz input noise spectral density. The decibel gain is directly proportional to the control voltage, is accurately calibrated, and is supply- and temperature-stable.

To achieve the difficult performance objectives, a proprietary circuit form—the X-AMP®—has been developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to –42.14 dB followed by a high speed fixed gain amplifier. In this way, the amplifier never has to cope with large inputs, and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a seven-stage R-2R ladder network having an input resistance of 100 Ω, laser-trimmed to ±2%. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting control function is linear in dB.

The gain-control interfaces are fully differential, providing an input resistance of ~15 MΩ and a scale factor of 32 dB/V (that is, 31.25 mV/dB) defined by an internal voltage reference. The response time of this interface is less than 1 µs. Each channel also has an independent gating facility that optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL and CMOS compatible.

X-AMP is a registered trademark of Analog Devices, Inc.
*Patented.

The maximum gain of the AD600 is 41.07 dB, and that of the AD602 is 31.07 dB; the –3 dB bandwidth of both models is nominally 35 MHz, essentially independent of the gain. The signal-to-noise ratio (SNR) for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is flat within ±0.5 dB from 100 kHz to 10 MHz; over this frequency range the group delay varies by less than ±2 ns at all gain settings.

Each amplifier channel can drive 100 Ω load impedances with low distortion. For example, the peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load. For a 200 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically –60 dBc.

The AD600J and AD602J are specified for operation from 0°C to +70°C, and are available in both 16-pin plastic DIP (N) and 16-pin SOIC (R). The AD600A and AD602A are specified for operation from –40°C to +85°C and are available in both 16-pin cerdip (Q) and 16-pin SOIC (R).

The AD600S and AD602S are specified for operation from –55°C to +125°C and are available in a 16-pin cerdip (Q) package and are MIL-STD-883 compliant. The AD600S and AD602S are also available under DESC SMD 5962-94572.

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ORDERING GUIDE

Model	Gain Range	Temperature Range	Package Option[1]
AD600AQ	0 dB to +40 dB	–40°C to +85°C	Q-16
AD600AR	0 dB to +40 dB	–40°C to +85°C	R-16
AD602AQ	–10 dB to +30 dB	–40°C to +85°C	Q-16
AD602AR	–10 dB to +30 dB	–40°C to +85°C	R-16
AD600JN	0 dB to +40 dB	0°C to +70°C	N-16
AD600JR	0 dB to +40 dB	0°C to +70°C	R-16
AD602JN	–10 dB to +30 dB	0°C to +70°C	N-16
AD602JR	–10 dB to +30 dB	0°C to +70°C	R-16
AD600SQ/883B[2]	0 dB to +40 dB	–55°C to +150°C	Q-16
AD602SQ/883B[3]	–10 dB to +30 dB	–55°C to +150°C	Q-16

NOTES
[1]N = Plastic DIP; Q= Cerdip; R= Small Outline IC (SOIC). For outline information see Package Information section.
[2]Refer to AD600/AD602 Military data sheet. Also available as 5962-9457201MPA.
[3]Refer to AD600/AD602 Military data sheet. Also available as 5962-9457202MPA.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD600/AD602—SPECIFICATIONS (Each amplifier section, at T_A = +25°C, V_S = ±5 V, –625 mV ≤ V_G ≤ +625 mV, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted. Specifications for AD600 and AD602 are identical unless otherwise noted.)

Parameter	Conditions	AD600J/AD602J Min	AD600J/AD602J Typ	AD600J/AD602J Max	AD600A/AD602A Min	AD600A/AD602A Typ	AD600A/AD602A Max	Units
INPUT CHARACTERISTICS								
Input Resistance	Pins 2 to 3; Pins 6 to 7	**98**	100	**102**	**95**	100	**105**	Ω
Input Capacitance			2			2		pF
Input Noise Spectral Density[1]			1.4			1.4		nV/√Hz
Noise Figure	R_S = 50 Ω, Maximum Gain		5.3			5.3		dB
	R_S = 200 Ω, Maximum Gain		2			2		dB
Common-Mode Rejection Ratio	f = 100 kHz		30			30		dB
OUTPUT CHARACTERISTICS								
–3 dB Bandwidth	V_{OUT} = 100 mV rms		35			35		MHz
Slew Rate			275			275		V/µs
Peak Output[2]	$R_L \geq$ 500 Ω	±2.5	±3		±2.5	±3		V
Output Impedance	f ≤ 10 MHz		2			2		Ω
Output Short-Circuit Current			50			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2			±2		ns
Group Delay Change vs. Frequency	V_G = 0 V, f = 1 MHz to 10 MHz		±2			±2		ns
Total Harmonic Distortion	R_L = 200 Ω, V_{OUT} = ±1 V Peak, Rpd = 1 kΩ		–60			–60		dBc
ACCURACY								
AD600								
Gain Error	0 dB to 3 dB Gain	**0**	+0.5	**+1**	**–0.5**	+0.5	**+1.5**	dB
	3 dB to 37 dB Gain	**–0.5**	±0.2	**+0.5**	**–1.0**	±0.2	**+1.0**	dB
	37 dB to 40 dB Gain	**–1**	–0.5	**0**	**–1.5**	–0.5	**+0.5**	dB
Maximum Output Offset Voltage[3]	V_G = –625 mV to +625 mV		10	**50**		10	**65**	mV
Output Offset Variation	V_G = –625 mV to +625 mV		10	**50**		10	**65**	mV
AD602								
Gain Error	–10 dB to –7 dB Gain	**0**	+0.5	**+1**	**–0.5**	+0.5	**+1.5**	dB
	–7 dB to 27 dB Gain	**–0.5**	±0.2	**+0.5**	**–1.0**	±0.2	**+1.0**	dB
	27 dB to 30 dB Gain	**–1**	–0.5	**0**	**–1.5**	–0.5	**+0.5**	dB
Maximum Output Offset Voltage[3]	V_G = –625 mV to +625 mV		5	**30**		10	**45**	mV
Output Offset Variation	V_G = –625 mV to +625 mV		5	**30**		10	**45**	mV
GAIN CONTROL INTERFACE								
Gain Scaling Factor	3 dB to 37 dB (AD600); –7 dB to 27 dB (AD602)	**31.7**	32	**32.3**	**30.5**	32	**33.5**	dB/V
Common-Mode Range		–0.75		2.5	–0.75		2.5	V
Input Bias Current			0.35	1		0.35	1	µA
Input Offset Current			10	50		10	50	nA
Differential Input Resistance	Pins 1 to 16; Pins 8 to 9		15			15		MΩ
Response Rate	Full 40 dB Gain Change		40			40		dB/µs
SIGNAL GATING INTERFACE								
Logic Input "LO" (Output ON)				0.8			0.8	V
Logic Input "HI" (Output OFF)		2.4			2.4			V
Response Time	ON to OFF, OFF to ON		0.3			0.3		µs
Input Resistance	Pins 4 to 3; Pins 5 to 6		30			30		kΩ
Output Gated OFF								
Output Offset Voltage			±10	**±100**		±10	**±400**	mV
Output Noise Spectral Density			65			65		nV/√Hz
Signal Feedthrough @ 1 MHz								
AD600			–80			–80		dB
AD602			–70			–70		dB
POWER SUPPLY								
Specified Operating Range		±4.75		±5.25	±4.75		±5.25	V
Quiescent Current			11	**12.5**		22	**28**	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD600 is X113; thus an input offset of only 100 µV becomes an 11.3 mV output offset. In the AD602, the amplifier's gain is X35.7; thus, an input offset of 100 µV becomes a 3.57 mV output offset.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ANALOG DEVICES

Low Noise, 90 MHz Variable-Gain Amplifier

AD603*

FEATURES
"Linear in dB" Gain Control
Pin Programmable Gain Ranges
–11 dB to +31 dB with 90 MHz Bandwidth
+9 dB to +51 dB with 9 MHz Bandwidth
Any Intermediate Range, e.g., –1 dB to +41 dB with 30 MHz Bandwidth
Bandwidth Independent of Variable Gain
1.3 nV/$\sqrt{\text{Hz}}$ Input Noise Spectral Density
±0.5 dB Typical Gain Accuracy
MIL-STD-883 Compliant and DESC Versions Available

APPLICATIONS
RF/IF AGC Amplifier
Video Gain Control
A/D Range Extension
Signal Measurement

PRODUCT DESCRIPTION

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems. It provides accurate, pin selectable gains of –11 dB to +31 dB with a bandwidth of 90 MHz or +9 dB to +51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3 nV/$\sqrt{\text{Hz}}$ and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is "linear in dB," accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain-control voltage of only 1 V to span the central 40 dB of the gain range. An over- and under-range of 1 dB is provided whatever the selected range. The gain-control response time is less than 1 µs for a 40 dB change.

The differential gain-control interface allows the use of either differential or single-ended positive or negative control voltages. Several of these amplifiers may be cascaded and their gain-control gains offset to optimize the system S/N ratio.

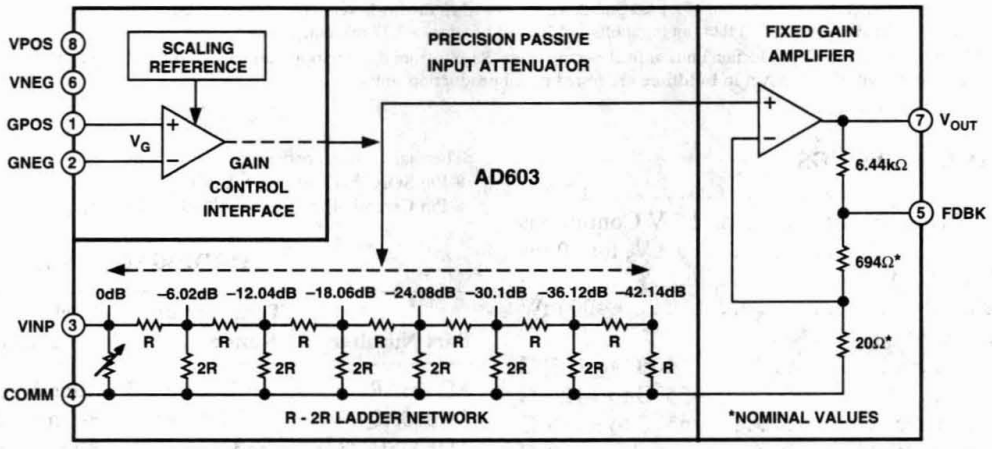
The AD603 can drive a load impedance as low as 100 Ω with low distortion. For a 500 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically –60 dBc. The peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load.

The AD603 uses a proprietary circuit topology—the X-AMP®. The X-AMP comprises a variable attenuator of 0 dB to –42.14 dB followed by a fixed-gain amplifier. Because of the attenuator, the amplifier never has to cope with large inputs and can use negative feedback to define its (fixed) gain and dynamic performance. The attenuator has an input resistance of 100 Ω, laser trimmed to ±3%, and comprises a seven-stage R-2R ladder network, resulting in an attenuation between tap points of 6.021 dB. A proprietary interpolation technique provides a continuous gain-control function which is linear in dB.

The AD603A is specified for operation from –40°C to +85°C and is available in both 8-pin SOIC (R) and 8-pin ceramic DIP (Q). The AD603S is specified for operation from –55°C to +125°C and is available in an 8-pin ceramic DIP (Q). The AD603 is also available under DESC SMD 5962-94572.

***Patented.**
X-AMP is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



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AD603–SPECIFICATIONS (@ T_A = +25°C, V_S = ±5 V, –500 mV ≤ V_G ≤ +500 mV, –10 dB to +30 dB Gain Range, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted.)

Model / Parameter	Conditions	AD603 Min	AD603 Typ	AD603 Max	Units
INPUT CHARACTERISTICS					
Input Resistance	Pins 3 to 4	97	100	**103**	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]	Input Short Circuited		1.3		$nV/\sqrt{Hz}$
Noise Figure	f = 10 MHz, Gain = max, R_S = 10 Ω		8.8		dB
1 dB Compression Point	f = 10 MHz, Gain = max, R_S = 10 Ω		–11		dBm
Peak Input Voltage			±1.4	±2	V
OUTPUT CHARACTERISTICS					
–3 dB Bandwidth	V_{OUT} = 100 mV rms		90		MHz
Slew Rate	R_L ≥ 500 Ω		275		V/µs
Peak Output[2]	R_L ≥ 500 Ω	±2.5	±3.0		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 MHz to 10 MHz		±2		ns
Differential Gain			0.2		%
Differential Phase			0.2		Degree
Total Harmonic Distortion	f = 10 MHz, V_{OUT} = 1 V rms		–60		dBc
3rd Order Intercept	f = 40 MHz, Gain = max, R_S = 50 Ω		15		dBm
ACCURACY					
Gain Accuracy	–500 mV ≤ V_G ≤ +500 mV		±0.5	**±1**	dB
T_{MIN} to T_{MAX}				±1.5	
Output Offset Voltage[3]	V_G = 0 V			**20**	mV
T_{MIN} to T_{MAX}				30	
Output Offset Variation vs. V_G	–500 mV ≤ V_G ≤ +500 mV			**20**	mV
T_{MIN} to T_{MAX}				30	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor		**39.4**	40	**40.6**	dB/V
T_{MIN} to T_{MAX}		38		42	dB/V
Common-Mode Range		–1.2		+2.0	V
Input Bias Current			200		nA
Input Offset Current			10		nA
Differential Input Resistance	Pins 1 to 2		50		MΩ
Response Rate	Full 40 dB Gain Change		40		dB/µs
POWER SUPPLY					
Specified Operating Range		±4.75		±5.25	V
Quiescent Current			12.5	**17**	mA
T_{MIN} to T_{MAX}				20	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD603 is ×35.7; thus, an input offset of 100 µV becomes a 3.57 mV output offset.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ±V_S . . . . . ±7.5 V
Internal Voltage VINP (Pin 3) . . . . . ±2 V Continuous
. . . . . ±V_S for 10 ms
GNEG, GPOS (Pins 1, 2) . . . . . ±V_S
Internal Power Dissipation[2] . . . . . 400 mW
Operating Temperature Range
AD603A . . . . . –40°C to +85°C
AD603S . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:
8-Pin SOIC Package: θ_{JA} = 155°C/Watt, θ_{JC} = 33°C/Watt
8-Pin Ceramic Package; θ_{JA} = 140°C/Watt, θ_{JC} = 15°C/Watt

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option[1]
AD603AR	–40°C to +85°C	8-Pin SOIC	R-8
AD603AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD603SQ/883B[2]	–55°C to +125°C	8-Pin Ceramic DIP	Q-8

NOTES

[1]R = SOIC; Q = Cerdip. For outline information see Package Information section.

[2]Refer to AD603 Military data sheet. Also available as 5962-9457203MPA.

Dual, Ultralow Noise Variable Gain Amplifier

AD604

FEATURES

Ultralow Input Noise at Maximum Gain:
0.80 nV/√Hz, 3.0 pA/√Hz
Two Independent Linear-in-dB Channels
Absolute Gain Range per Channel Programmable:
0 dB to +48 dB (Preamp Gain = +14 dB), through
+6 dB to +54 dB (Preamp Gain = +20 dB)
±0.5 dB Gain Accuracy
Bandwidth: DC to 40 MHz (–3 dB)
300 kΩ Input Resistance
Variable Gain Scaling: 20 dB/V through 40 dB/V
Stable Gain with Temperature and Supply Variations
Single-Ended Unipolar Gain Control
Power Shutdown at Lower End of Gain Control
Can Drive AD9040/AD9050 A/D Converters Directly

APPLICATIONS

Ultrasound and Sonar Time-Gain Control
High Performance AGC Systems
Signal Measurement

PRODUCT DESCRIPTION

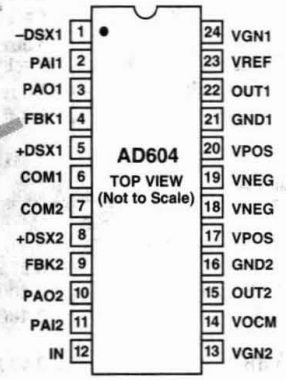
The AD604 is an ultralow noise, very accurate, dual channel, linear-in-dB variable gain amplifier (VGA) optimized for any application requiring low noise, wide bandwidth variable gain control. Each channel of the AD604 provides a 300 kΩ input resistance and unipolar gain control for ease of use. User determined gain ranges, gain scaling (dB/V) and channel-to-channel gain scale tracking further optimizes application performance.

Each independent channel of the AD604 provides a gain range of 48 dB which can be optimized for the application by programming the preamplifier with a single resistor. The linear-in-dB gain response of the AD604 can be described by the equation: $G\,(dB) = (Gain\ Scaling\ (dB/V)) \times VGN\ (V) + ((Pre\text{-}Amp\ Gain\ (dB)) - 19\ dB)$. Preamplifier gains between 5 and 10 (+14 dB and +20 dB) provide overall gain ranges per channel of 0 dB through +48 dB and +6 dB through +54 dB. The two channels of the AD604 can be cascaded to provide greater levels of gain range by bypassing the 2nd channels preamplifier. The AD604 provides access to the output of the preamplifier allowing for external filtering between the preamplifier and the differential attenuator stage.

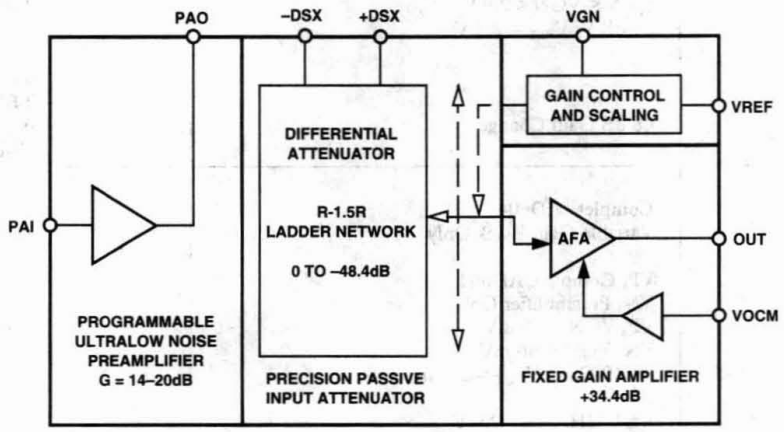
The gain control interface provides an input resistance of approximately 50 MΩ and scale factors from 20 dB/V to 30 dB/V for a V_{REF} input voltage of 2.5 V to 1.67 V respectively. Note that scale factors up to 40 dB are achievable with reduced accuracy in the absolute value of V_{REF}.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



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AD604—SPECIFICATIONS (Each amplifier channel at T_A = +25°C, V_S = ±5 V, R_S = 50 Ω, R_L = 500 Ω, C_L = 5 pF, 0.5 V ≤ V_G ≤ 2.5 V (Scaling = 20 dB/V), 0 dB to +48 dB gain range (Preamplifier Gain = +14 dB), unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance			300		kΩ
Input Capacitance			8.5		pF
Input Bias Current			–27		mA
Peak Input Voltage	Preamp Gain = +14 dB		±400		mV
	Preamp Gain = +20 dB		±200		mV
Input Voltage Noise	V_G = 2.9 V, R_S = 0 Ω				
	Preamp Gain = +14 dB		0.80		nV/√Hz
	Preamp Gain = +20 dB		0.73		nV/√Hz
Input Current Noise	Independent of Gain		3.0		pA/√Hz
Noise Figure	R_S = 50 Ω, f = 1 MHz, VGN = 2.9 V		2.3		dB
	R_S = 200 Ω, f =1 MHz, VGN = 2.9 V		1.1		dB
OUTPUT CHARACTERISTICS					
–3 dB Bandwidth Constant with Gain			40		MHz
Slew Rate	V_G = 1.5 V, Output = 1 V Step		170		V/µs
Output Signal Range	R_L ≥ 500 Ω		2.5 ± 1.5		V
Output Impedance	f = 10 MHz		2		Ω
Output Short-Circuit Current			±40		mA
Harmonic Distortion	V_G = 1 V, V_{OUT} = 1 V p-p				
HD2	f = 1 MHz		–52		dBc
HD3	f = 1 MHz		–67		dBc
HD2	f = 10 MHz		–50		dBc
HD3	f = 10 MHz		–42		dBc
Two-Tone Intermodulation	VGN = 2.9 V, V_{OUT} = 1 V p-p				
Distortion (IMD)	f = 1 MHz		–74		dBc
	f = 10 MHz		–71		dBc
3rd Order Intercept	f = 10 MHz, V_G = 2.9 V, V_{OUT} = 1 V p-p, Input Referred		–14		dBm
1 dB Compression Point	f = 1 MHz, Max Gain, Output Referred		+11		dBm
Channel-to-Channel Crosstalk	V_{OUT} = 1 V p-p, F = 1 MHz				
	Ch #1: VGN = 2.9 V, Inputs Shorted		–38		dB
	Ch #2: VGN = 1.5 V (Mid Gain)		–58		dB
Group Delay	1 MHz < f < 10 MHz, Full Gain Range		10		ns
VOCM Input Resistance			TBD		kΩ
ACCURACY					
Absolute Gain Error					
0 dB to +2.5 dB	0.275 V < VGN < 0.400 V	–0.5	+0.75	+2	dB
+2.5 dB to +42.5 dB	0.400 V < VGN < 2.400 V	–0.5	±0.2	+0.5	dB
+42.5 dB to +48 dB	2.400 V < VGN < 2.675 V	–3.0	–1.25	+0.5	dB
Gain Scaling Error					
+2.5 dB to +42.5 dB	0.400 V < VGN < 2.400 V	–0.30	0	+0.30	dB
Output Offset Voltage	V_{REF} = 2.500 V, V_{OCM} = 2.500 V		±10		mV max
GAIN CONTROL INTERFACE					
Gain Scaling Factor	V_{REF} = 2.5 V		20		dB/V
	V_{REF} = 1.67 V		30		dB/V
Gain Range	0.1 V < VGN < 2.9 V		0 to +48		dB
Input Voltage (VGN) Range	20 dB/V, V_{REF} = 2.5 V		0.1 to 2.9		V
Input Bias Current			–0.4		µA
Input Resistance			50		MΩ
Input Capacitance			TBD		pF
Response Time	48 dB Gain Change		0.5		µs
V_{REF} Input Resistance			TBD		kΩ
POWER SUPPLY					
Specified Operating Range	Complete AD604		±5		V
	Variable Gain Block Only		+5		V
Power Dissipation			220		mW
Quiescent Supply Current	VP, Complete AD604		32		mA
	VN, Preamplifier Only		12		mA
Powered Down	VP, VGN < 50 mV		1.9		mA
	VN, VGN < 50 mV		150		µA
Power-Up Response Time	48 dB Gain, V_{OUT} = 2 V p-p		1		µs
Power-Down Response Time			400		ns
Supply Rejection, from V_{POS}	f = 1 MHz, V_G = 2.9 V		TBD		dB
from V_{NEG}	f = 1 MHz, V_G = 2.9 V		TBD		dB

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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Dual, Low Noise, Single-Supply Variable Gain Amplifier

AD605

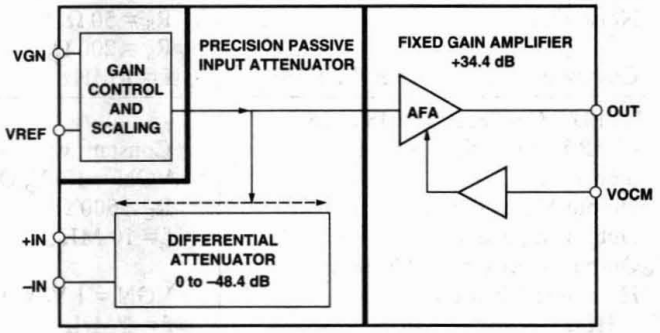
FEATURES

Two Independent Linear-in-dB Channels
Input Noise at Maximum Gain: 1.8 nV/√Hz, 2.2 pA/√Hz
Bandwidth: DC to 40 MHz (–3 dB)
Differential Input
Absolute Gain Range Programmable:
–14 dB to +34 dB (FBO Shorted to OUT), through
0 dB to +48 dB (FBO Open)
Variable Gain Scaling: 20 dB/V through 40 dB/V
Stable Gain with Temperature and Supply Variations
Single-Ended Unipolar Gain Control
Output Common-Mode Independently Set
Power Shutdown at Lower End of Gain Control
Single +5 V Supply
Low Power: 90 mW/Channel
Drives A/D Converters Directly

APPLICATIONS

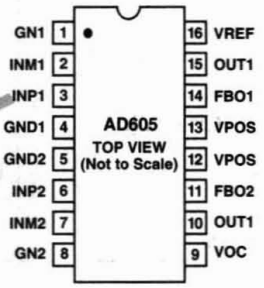
Ultrasound and Sonar Time-Gain Control
High Performance AGC Systems
Signal Measurement

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

16 Pin Package for Dual Channel AD605



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD605 is a very accurate, low noise, dual channel, linear-in-dB variable gain amplifier, which is optimized for any application requiring high performance, wide bandwidth variable gain control. Operating from a single +5 V supply, the AD605 provides differential inputs and unipolar gain control resulting in ease of use. Added flexibility is achieved with a user determined gain range and an external reference input which provides user determined gain scaling (dB/V) and gain scale tracking between multiple channels.

The high performance linear-in-dB response of the AD605 is achieved with the differential input, single supply, exponential amplifier (DSX-AMP) architecture. Each of the DSX-AMPs comprise a variable attenuator of 0 dB to –48 dB followed by a high speed fixed gain amplifier. The attenuator is based on a seven-stage R-1.5-R ladder network. The attenuation between tap points is 6.908 dB (48.36 dB for the ladder network). The DSX-AMP architecture results in 1.8 nV/√Hz input noise spectral density and will accept a ±2 V input signal when V_{OCM} is biased at the supply midpoint.

Each independent channel of the AD605 provides a gain range of 48 dB which can be optimized for the application. Gain ranges between –14 dB to +34 dB and 0 dB to +48 dB can be selected by a single resistor between pins FBK and OUT. The lower and upper gain range are determined by shorting pin FBK to OUT, or leaving pin FBK unconnected respectively. The two channels of the AD605 can be cascaded to provide 96 dB of very accurate gain range in a monolithic package.

The gain control interface provides an input resistance of approximately 50 MΩ and scale factors from 20 dB/V to 30 dB/V for a V_{REF} input voltage of 2.5 V to 1.67 V respectively. The gain scales linear-in-dB with control voltages of 0.5 V to 2.5 V for the 20 dB/V scale. Below and above these gain control ranges the gain starts to deviate from the ideal linear-in-dB control law. The gain control region below 0.1 V is not used for gain control, in fact when the gain control is <50 mV the amplifier is powered-down to draw 1.9 mA. The quiescent supply current of each amplifier channel is only 19 mA under normal operation.

The AD605 is available in a 16-pin plastic DIP and SOIC, and is guaranteed for operation over the –40°C to +85°C temperature range.

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AD605–SPECIFICATIONS (Each channel at T_A = +25°C, V_S = +5 V, R_S = 50 Ω, R_L = 500 Ω, C_L = 5 pF, 0.5 V ≤ V_G ≤ 2.5 V (Scaling = 20 dB/V), –14 dB to +34 dB gain range, unless otherwise noted.)

Parameter	Conditions	Specs/Channel Typical	Unit
INPUT CHARACTERISTICS			
Input Resistance		175 ±40	Ω
Input Capacitance		TBD	pF
Peak Input Voltage		2.5 ±2	V
Input Voltage Noise	VGN = 2.9 V	1.8	nV/√Hz
Input Current Noise	VGN = 2.9 V	2.7	pA/√Hz
Noise Figure	R_S = 50 Ω, f = 1 MHz, VGN = 2.9 V	8.4	dB
	R_S = 200 Ω, f = 1 MHz, VGN = 2.9 V	7	dB
Common-Mode Rejection Ratio	f = 1 MHz	TBD	dB
OUTPUT CHARACTERISTICS			
–3 dB Bandwidth	Constant with Gain	40	MHz
Slew Rate	VGN = 1.5 V, Output = 1 V Step	TBD	V/µs
Output Signal Range	R_L ≥ 500 Ω	2.5 ± 1.5	V
Output Impedance	f = 10 MHz	2	Ω
Output Short Circuit Current		±40	mA
Harmonic Distortion	VGN = 1 V, VOUT = 1 V p-p,		
HD2	f = 1 MHz	65	dBc
HD3	f = 1 MHz	–60	dBc
HD2	f = 10 MHz	–52	dBc
HD3	f = 10 MHz	–42	dBc
Two-Tone Intermodulation	VGN = 2.9 V, VOUT = 1 V p-p		
Distortion (IMD)	f = 1 MHz	–72	dBc
	f = 10 MHz	–60	dBc
1 dB Compression Point	f = 10 MHz, V_G = 2.9 V, Output Referred	+15.5	dBm
3rd Order Intercept	f = 10 MHz, V_G = 2.9 V, VOUT = 1 V p-p, Input Referred	–6	dBm
Channel to Channel Crosstalk	VOUT = 1 V p-p Ch #1: VGN = 2.9 V, Inputs Shorted, Ch #2: VGN = 1.5 V (Midgain),	TBD	dB
Group Delay	1 MHz < f < 10 MHz, Full Gain Range	TBD	ns
V_{OCM} Input Resistance		TBD	kΩ
ACCURACY			
Absolute Gain Error	VGN = 1.5 V	±0.5	dB
Gain Scaling Error	0.5 V < VGN < 2.5 V	±0.25	dB
Output Offset Voltage	VREF = 2.500 V, VOCM = 2.500 V	±30	mV max
GAIN CONTROL INTERFACE			
Gain Scaling Factor	VREF = 2.5 V	20	dB/V
	VREF = 1.67 V	30	dB/V
Gain Range		48	dB
Input Voltage (V_G) Range	20 dB/V, VREF = 2.5 V	0.1 to 2.9	V
Input Bias Current		–0.4	µA
Input Resistance		50	MΩ
Input Capacitance		TBD	pF
Response Time	48 dB Gain Change	0.5	µs
V_{REF} Input Resistance	Complete AD604	11	kΩ
POWER SUPPLY	Operating Range	+5	V
Power Dissipation		90	mW
Quiescent Supply Current	VP	19	mA
Power Down	VP, VGN < 50 mV	1.9	mA
Power-Up Response Time	48 dB Gain, V_{OUT} = 2 V p-p	1	µs
Power-Down Response Time		400	ns
Supply Rejection, from V	f = 1 MHz, V_G = 2.9 V	TBD	dB

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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V/F & F/V Converters
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ADVFC32 – Voltage-to-Frequency and Frequency-to-Voltage Converter	14–9

Voltage-to-Frequency & Frequency-to-Voltage Converters–Selection Guide

Model	Power Supply Requirements $+V_{CC}$ Volts	$+I_{CC}$ mA	$-V_{EE}$ Volts	$-I_{EE}$ mA	Input Voltage Range Volts	Full-Scale Frequency kHz	Accuracy	Accuracy	Voltage Reference Volts Int	I/O	# Pins	Page No.	Comments	Fax-code
AD537J	+5	2.5			0–1	150	0.15%/10 kHz	0.25%/100 kHz	+1	Open Col	10/14	14–3	With 1 mV/K Temp Sensor	1148
AD537K	+5	2.5			0–1	150	0.07%/10 kHz	0.1%/100 kHz	+1	Open Col		14–3		
AD537J	+15	2.5	–15	2.5	±11	150	0.15%/10 kHz	0.25%/100 kHz	+1	Open Col	10/14	14–3	With 1 mV/K Temp Sensor	1148
AD537K	+15	2.5	–15	2.5	±11	150	0.07%/10 kHz	0.1%/100 kHz	+1	Open Col		14–3		
AD650J	+15	8	–15	8	0–11	1000	0.02%/100 kHz	ns @ 1 MHz	NA	Open Col	14/20	*	100 kHz F/V Mode	1214
AD650K	+15	8	–15	8	0–11	1000	0.02%/100 kHz	0.1%/1 MHz	NA	Open Col		*		
AD652J	+15	15	–15	15	±10	2000	1%/100 kHz	1.5%/2 MHz	+5	Open Col	16/20	14–5	Synchronous, F/V = 100 kHz	1215
AD652K	+15	15	–15	15	±10	2000	0.5%/100 kHz	0.75%/2 MHz	+5	& Emitter		14–5		
AD654	+5	2.5			0–1	500	0.1%/250 kHz	0.4%/500 kHz	NA	Open Col & Emitter	8	14–7	+5 V, ±5 V or ±15 V Rails	1216
ADVFC32	+15	8	–15	8	0–10	500	0.05%/100 kHz	0.2%/500 kHz	NA	Open Col	10/14	14–9	Pin for Pin BB VFC32	1605

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

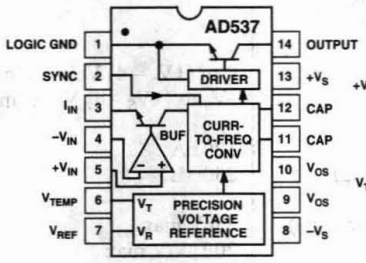
Integrated Circuit Voltage-to-Frequency Converter

AD537*

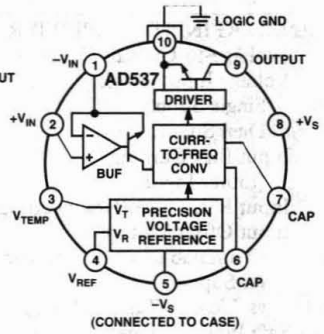
FEATURES
- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 V to 36 V
- Linearity: ±0.05% FS
- Low Power: 1.2 mA Quiescent Current
- Full-Scale Frequency up to 100 kHz
- 1.00 V Reference
- Thermometer Output (1 mV/K)
- F-V Applications
- MIL-STD-883 Compliant Versions Available

PIN CONFIGURATIONS

"D" package (TO-116)



"H" Package (TO-100)



PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full-scale (F.S.) frequency up to 100 kHz and any F.S. input voltage up to ±30 V. Linearity error is as low as ±0.05% for 10 kHz F.S., and operation is guaranteed over an 80 dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30 ppm/°C. The AD537 operates from a single supply of 5 V to 36 V and consumes only 1.2 mA quiescent current.

A temperature-proportional output, scaled to 1.00 mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00 V, offset scales such as 0°C or 0°F can be generated.

The low drift (1 μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250 MΩ) input resistance. Unlike most V–F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary bandgap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0°C to +70°C range while the AD537S is specified for operation over the extended temperature range, –55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full-scale frequency and a selectable pull-up resistor for the open collector output stage. Any full-scale input voltage range from 100 mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full-scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2 mA quiescent current is drawn from a single positive supply from 4.5 volts to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ – 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristic are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 6.
4. The versatile open-collector NPN output stage can sink up to 20 mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.
5. The AD537 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Product Databook or current AD537/883B data sheet for detailed specifications.

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*Protected by Patent Nos. 3,887,963 and RE 30,586.

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AD537–SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 V to 36 V, unless otherwise noted)

Model	AD537JH	AD537JD	AD537KD AD537KH	AD537SD[1] AD537SH[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 kHz to 150 kHz	*	*	*
Nonlinearity[1]				
f_{MAX} = 10 kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{MAX} = 100 kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full-Scale Calibration Error				
C = 0.01 µF, I_{IN} = 1.000 mA	±10% max	±7% max	±5% max	* *
vs. Supply (f_{MAX} < 100 kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp (T_{MIN} to T_{MAX})	±150 ppm/°C max (50 ppm typ)	*	50 ppm/°C max (30 ppm typ)[2]	250 ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S – 4) Volts (min)	*	*	*
Dual Supply	–V_S to (+V_S – 4) Volts (min)	*	*	*
Input Bias Current				
(Either Input)	100 nA	*	*	*
Input Resistance (Noninverting)	250 MΩ	*	*	*
Input Offset Voltage				
(Trimmable in "D" Package Only)	5 mV max	*	2 mV max	**
vs. Supply	200 µV/V max	100 µV/V max	100 µV/V max	**
vs. Temp (T_{MIN} to T_{MAX})	5 µV/°C	*	1 µV/°C	10 µV/°C max
Safe Input Voltage[3]	±V_S	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ± 5% max	*	*	*
vs. Temp (T_{MIN} to T_{MAX})	50 ppm/°C	*	100 ppm/°C max	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[4]	380 Ω	*	*	*
Absolute Temperature Reference[5]				
Nominal Output Level	1.00 mV/K	*	*	*
Initial Calibration @ +25°C	298 mV (±5 mV)	*	298 mV (±5 mV max)	**
Slope Error from 1.00 mV/K	±0.02 mV/K	*	*	*
Slope Nonlinearity	±0.1 K	*	*	*
Output Resistance[5]	900 Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4 V max (T_{MIN} to T_{MAX})	20 mA min	20 mA min	20 mA min	10 mA min
Output Leakage Current in Logic "1"				
(T_{MIN} to T_{MAX})	200 nA max	*	*	2 µA max
Logic Common Level Range	–V_S to (+V_S – 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01 µF)				
I_{IN} = 1 mA	0.2 µs	*	*	*
I_{IN} = 1 µA	1 µs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5 V to 36 V	*	*	*
Dual Supply	±5 V to ±18 V	*	*	*
Quiescent Current	1.2 mA (2.5 mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0°C to +70°C	*	*	–55°C to +125°C
Storage	–65°C to +150°C	*	*	*
PACKAGE OPTIONS[6, 7]				
TO-116 Ceramic DIP (D-14)		AD537JD	AD537KD	AD537SD
TO-100 Header (H-10A)	AD537JH		AD537KH	AD537SH

NOTES

*Specifications same as AD537JH.

**Specifications same as AD537K.

[1]Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 µA to 1000 µA. Converter has 100% overrange capability up to I_{IN} = 2000 µA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2]Guaranteed not tested.

[3]Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1 mA full scale through an appropriate value resistor (See Figure 2).

[4]Loading the 1.0 volt or 1 mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the external buffer or an external amplifier.

[5]Temperature reference output performance is specified from 0°C to +70°C for "J" and "K" devices, –55°C to +125°C for "S" model.

[6]D = Ceramic DIP; H = Hermetic Metal Can. For outline information see Package Information section.

[7]For AD537/883B specifications, refer to *Analog Devices Military Products Databook*.

Specifications subject to change without notice.

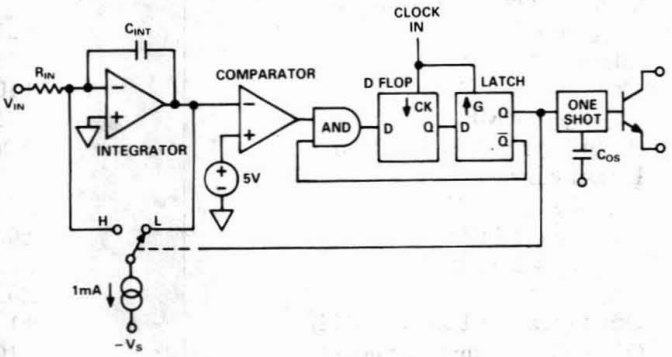
Monolithic Synchronous Voltage-to-Frequency Converter

AD652

FEATURES

Full-Scale Frequency (Up to 2 MHz) Set by External System Clock
Extremely Low Linearity Error (0.005% max at 1 MHz FS, 0.02% max at 2 MHz FS)
No Critical External Components Required
Accurate 5 V Reference Voltage
Low Drift (25 ppm/°C max)
Dual or Single Supply Operation
Voltage or Current Input
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD652 Synchronous Voltage-to-Frequency Converter (SVFC) is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100 kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allows the conversion time and resolution to be optimized for specific applications.

The AD652 uses a variation of the popular charge-balancing technique to perform the conversion function. The AD652 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multichannel systems.

Gain drift is minimized using a precision low drift reference and low TC on-chip thin-film scaling resistors. Furthermore, the initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD652 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD652 is available in five performance grades. The 20-pin PLCC packaged JP and KP grades are specified for operation over the 0°C to +70°C commercial temperature range. The 16-pin cerdip-packaged AQ and BQ grades are specified for operation over the –40°C to +85°C industrial temperature range, and the AD652SQ is available for operation over the full –55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD652 to achieve linearity and stability far superior to other monolithic VFCs. By using the same clock to drive the AD652 and (through a suitable divider) also set the counting period, conversion accuracy is maintained independent of variations in clock frequency.
2. The AD652 Synchronous VFC requires only a single external component (a noncritical integrator capacitor) for operation.
3. The AD652 includes a buffered, accurate 5 V reference which is available to the user.
4. The clock input of the AD652 is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as for optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
5. The AD652 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.
6. The AD652 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD652/883B data sheet for detailed specifications.

ORDERING GUIDE

Part Number[1]	Gain Drift ppm/°C 100 kHz	1 MHz Linearity %	Specified Temperature Range °C	Package Options[2]
AD652JP	50 max	0.02 max	0 to +70	PLCC (P-20A)
AD652KP	25 max	0.005 max	0 to +70	PLCC (P-20A)
AD652AQ	50 max	0.02 max	–40 to +85	Cerdip (Q-16)
AD652BQ	25 max	0.005 max	–40 to +85	Cerdip (Q-16)
AD652SQ	50 max	0.02 max	–55 to +125	Cerdip (Q-16)

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD652/883 data sheet.
[2]P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

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AD652–SPECIFICATIONS (typical @ T_A = +25°C, V_S = ±15 V, unless otherwise noted)

Parameter	AD652JP/AQ/SQ Min	Typ	Max	AD652KP/BQ Min	Typ	Max	Units
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{CLOCK} = 200 kHz		±0.5	±1		±0.25	±0.5	%
f_{CLOCK} = 1 MHz		±0.5	**±1**		±0.25	**±0.5**	%
f_{CLOCK} = 4 MHz		±0.5	**±1.5**		±0.25	**±0.75**	%
Gain Temperature Coefficient							
f_{CLOCK} = 200 kHz		±25	±50		±15	±25	ppm/°C
f_{CLOCK} = 1 MHz		±25	**±50**		±15	**±25**	ppm/°C
		±10	**±50**		±10	**±30**	ppm/°C
f_{CLOCK} = 4 MHz		±25	**±75**		±15	**±50**	ppm/°C
Power Supply Rejection Ratio		0.001	**0.01**		0.001	**0.01**	%/V
Linearity Error							
f_{CLOCK} = 200 kHz		±0.002	±0.02		±0.002	±0.005	%
f_{CLOCK} = 1 MHz		±0.002	**±0.02**		±0.002	**±0.005**	%
f_{CLOCK} = 2 MHz		±0.01	±0.02		±0.002	±0.005	%
f_{CLOCK} = 4 MHz		±0.02	**±0.05**		±0.01	**±0.02**	%
Offset (Transfer Function, RTI)		±1	**±3**		±1	**±2**	mV
Offset Temperature Coefficient		±10	**±50**		±10	**±25**	µV/°C
Response Time	One Period of New Output Frequency Plus One Clock Period.						
CLOCK INPUT							
Maximum Frequency	**4**	5		**4**	5		MHz
Threshold Voltage (Referred to Pin 12)		1.2			1.2		V
T_{MIN} to T_{MAX}	**0.8**		**2.0**	**0.8**		**2.0**	V
Input Current							
($-V_S < V_{CLK} < +V_S$)		5	**20**		5	**20**	µA
Voltage Range	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Rise Time			2			2	µs
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10 mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL} < 0.8 V			**15**			**15**	mA
V_{OL} < 0.4 V, T_{MIN}–T_{MAX}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**150**	200	**250**	**150**	200	**250**	ns
Fall Time (Load = 500 pF and I_{SINK} = 5 mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width							
C_{OS} = 300 pF	**1**	1.5	**2**	1	1.5	**2**	µs
C_{OS} = 1000 pF	4	5	6	4	5	6	µs
POWER SUPPLY							
Rated Voltage		±15			±15		V
Operating Range							
Dual Supplies	±6	±15	±18	±6	±15	±18	V
Single Supply ($-V_S$ = 0)	+12		+36	+12		+36	V
Quiescent Current		±11	**±15**		±11	**±15**	mA
Digital Common	$-V_S$		$+V_S - 4$	$-V_S$		$+V_S - 4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
JP, KP Grade	0		+70	0		+70	°C
AQ, BQ Grade	–40		+85	–40		+85	°C
SQ Grade	–55		+125				°C

Specifications in **boldface** are **100%** tested at final test and are used to measure outgoing quality levels.

Specifications subject to change without notice.

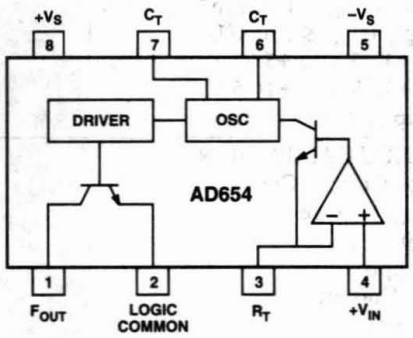
Low Cost Monolithic Voltage-to-Frequency Converter

AD654

FEATURES

- **Low Cost**
- **Single or Dual Supply, 5 V to 36 V, ±5 V to ±18 V**
- **Full-Scale Frequency Up to 500 kHz**
- **Minimum Number of External Components Needed**
- **Versatile Input Amplifier**
  - **Positive or Negative Voltage Modes**
  - **Negative Current Mode**
  - **High Input Impedance, Low Drift**
- **Low Power: 2.0 mA Quiescent Current**
- **Low Offset: 1 mV**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (FS) frequency up to 500 kHz and any FS input voltage up to ±30 V. Linearity error is only 0.03% for a 250 kHz FS, and operation is guaranteed over an 80 dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50 ppm/°C. The AD654 operates from a single supply of 5 V to 36 V and consumes only 2.0 mA quiescent current.

The low drift (4 μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250 MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, optocouplers, long cables, or similar loads.

PRODUCT HIGHLIGHTS

1. Packaged in both an 8-pin mini-DIP and an 8-pin SOIC package, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full-scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full scale input voltage range from 100 mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full-scale frequency is then set by the timing capacitor from the simple relationship, f = V/10 RC.
2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500 kHz and any full-scale input voltage up to ±30 V.
3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.
4. Power supply requirements are minimal; only 2.0 mA of quiescent current is drawn from the single positive supply from 4.5 volts to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S - 4$) volts. Negative inputs can easily be connected for below ground operation.
5. The versatile open-collector output stage can sink more than 10 mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

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AD654–SPECIFICATIONS

(T_A = +25°C and V_S (total) = 5 V to 16.5 V, unless otherwise noted. All testing done@ V_S = +5 V.)

Model	AD654JN/JR Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{MAX} = 250 kHz		0.06	**0.1**	%
f_{MAX} = 500 kHz		0.20	0.4	%
Full-Scale Calibration Error				
C = 390 pF, I_{IN} = 1.000 mA	**–10**		**10**	%
vs. Supply ($f_{MAX} \leq$ 250 kHz)				
V_S = +4.75 V to +5.25 V		0.20	**0.40**	%/V
V_S = +5.25 V to +16.5 V		0.05	**0.10**	%/V
vs. Temp (0°C to +70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S – 4)	V
Dual Supply	–V_S		(+V_S – 4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Noninverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 V to +5.25 V		0.1	**0.25**	mV/V
V_S = +5.25 V to +16.5 V		0.03	**0.1**	mV/V
vs. Temp (0°C to +70°C)		4		µV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4 V max, +25°C	**10**	20		mA
V_{OUT} = 0.4 V max, 0°C to +70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0°C to +70°C		50	500	nA
Logic Common Level Range	–V_S		(+V_S – 4)	V
Rise/Fall Times (C_T = 0.01 µF)				
I_{IN} = 1 mA		0.2		µs
I_{IN} = 1 µA		1		µs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5 V		1.5	**2.5**	mA
V_S (Total) = 30 V		2.0	**3.0**	mA
TEMPERATURE RANGE				
Operating Range	–40		+85	°C
PACKAGE OPTIONS[3]				
SOIC (R-8)		AD654JR		
Plastic DIP (N-8)		AD654JN		

NOTES

[1]At f_{MAX} = 250 kHz; R_T = 1 kΩ, C_T = 390 pF, I_{IN} = 0 mA–1 mA. f_{MAX} = 500 kHz; R_T = 1 kΩ, C_T = 200 pF, I_{IN} = 0 mA–1 mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4 V between Pin 1 and Logic Common.

[3]N = Plastic DIP; R = SOIC. For outline information see Package Information section.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage +V_S to –V_S . . . . . 36 V

Maximum Input Voltage

(Pins 3, 4) to –V_S . . . . . –300 mV to +V_S

Maximum Output Current

Instantaneous . . . . . 50 mA

Sustained . . . . . 25 mA

Logic Common to –V_S . . . . . –500 mV to (+V_S – 4)

Storage Temperature Range . . . . . –65°C to +150°C

ANALOG DEVICES

Voltage-to-Frequency and Frequency-to-Voltage Converter

ADVFC32

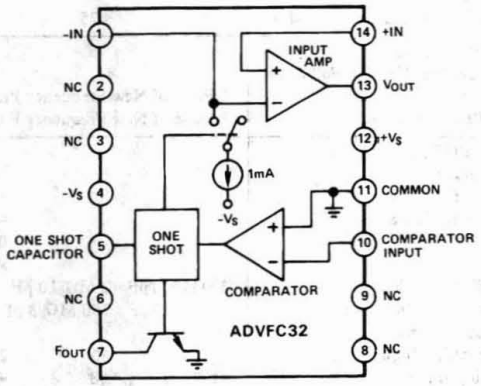
FEATURES

High Linearity
- **±0.01% max at 10 kHz FS**
- **±0.05% max at 100 kHz FS**
- **±0.2% max at 500 kHz FS**

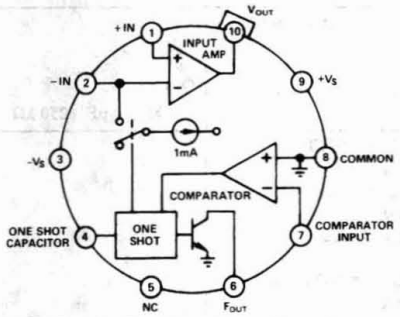
Output TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction
MIL-STD-883 Compliant Versions Available

PIN CONFIGURATION
(TOP VIEW)

"N" Package



"H" Package – TO-100



NC = NO CONNECT

PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage-to-frequency (V/F) converter or frequency-to-voltage (F/V) converter with good linearity (0.01% max error at 10 kHz) and operating frequency up to 0.5 MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using only a few external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15 V or +5 V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8 mA. A larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full-scale calibration drift is held to a maximum of 100 ppm/°C (ADVFC32BH) due to a low T.C. Zener diode.

The ADVFC32 is available in commercial, industrial, and extended temperature grades. The commercial grade is packaged in a 14-pin plastic DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans.

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to high accuracy voltage-to-frequency conversion. The full-scale operating frequency is determined by only one precision resistor and capacitor. The tolerance of other support components (including the integration capacitor) is not critical. Inexpensive ±20% resistors and capacitors can be used without affecting linearity or temperature drift.
2. The ADVFC32 is easily configured to satisfy a wide range of system requirements. Input voltage scaling is set by selecting the input resistor which sets the input current to 0.25 mA at the maximum input voltage.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. The ADVFC32 is intended as a pin-for-pin replacement for VFC32 devices from other manufacturers.
5. The ADVFC32 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current ADVFC32/883B data sheet for detailed specifications.

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ORDERING GUIDE

Part Number[1]	Gain Tempco	Temp Range	Package Option[2]
ADVFC32KN	±75 ppm/°C typ	0°C to +70°C	14-Pin Plastic DIP
ADVFC32BH	±100 ppm/°C max	–25°C to +85°C	TO-100
ADVFC32SH	±150 ppm/°C max	–55°C to +125°C	TO-100

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current ADVFC32/883B data sheet.
[2]For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ADVFC32—SPECIFICATIONS (typical @ +25°C with V_S = ±15 V unless otherwise noted)

Model	ADVFC32K Min	ADVFC32K Typ	ADVFC32K Max	ADVFC32B Min	ADVFC32B Typ	ADVFC32B Max	ADVFC32S Min	ADVFC32S Typ	ADVFC32S Max	Units
DYNAMIC PERFORMANCE										
Full-Scale Frequency Range	0		500	0		500	0		500	kHz
Nonlinearity[1]										
f_{MAX} = 10 kHz	–0.01		±0.01	–0.01		+0.01	–0.01		+0.01	%
f_{MAX} = 100 kHz	**–0.05**		**+0.05**	**–0.05**		**+0.05**	**–0.05**		**+0.05**	%
f_{MAX} = 0.5 MHz	–0.20	±0.05	+0.20	–0.20	±0.05	+0.20	–0.20	±0.05	+0.20	%
Full-Scale Calibration Error (Adjustable to Zero)		±5			±5			±5		%
vs. Supply (Full-Scale Frequency = 100 kHz)	**–0.015**		**+0.015**	**–0.015**		**+0.015**	**–0.015**		**+0.015**	% of FSR%
vs. Temperature (Full-Scale Frequency = 10 kHz)		±75		–100		+100	**+150**		**+150**	ppm/°C
DYNAMIC RESPONSE										
Maximum Settling Time for Full-Scale Step Input	1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			
Overload Recovery Time	1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			
ANALOG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range	0		+0.25	0		+0.25	0		+0.25	mA
Voltage Input Range	0		–10 to 0.25 × R_{IN}[3]	0		–10 to 0.25 × R_{IN}[3]	0		–10 to 0.25 × R_{IN}[3]	V[2] / mA
Differential Impedance	300 kΩ‖10 pF	2 MΩ‖10 pF		300 kΩ‖10 pF	2 MΩ‖10 pF		300 kΩ‖10 pF	2 MΩ‖10 pF		
Common-Mode Impedance	300 MΩ‖3 pF	750 MΩ‖3 pF		300 MΩ‖3 pF	750 MΩ‖10 pF		300 MΩ‖3 pF	750 MΩ‖10 pF		
Input Bias Current										
Noninverting Input		40	**250**		40	**250**		40	**250**	nA
Inverting Input	**–100**	±8	**+100**	**–100**	±8	**+100**	**–100**	±8	**+100**	nA
Input Offset Voltage (Trimmable to Zero)[2, 3]			**4**			**4**			**4**	mV
vs. Temperature (T_{MIN} to T_{MAX})			30			30			**30**	µV/°C
Safe Input Voltage		±V_S			±V_S			±V_S		
COMPARATOR (F/V Conversion)										
Logic "0" Level	–V_S		–0.6	–V_S		–0.6	–V_S		–0.6	V
Logic "1" Level	+1		+V_S	+1		+V_S	+1		+V_S	V
Pulse Width Range[4]	0.1		0.15/f_{MAX}	0.1		0.15/f_{MAX}	0.1		0.15/f_{MAX}	µs
Input Impedance	50 kΩ‖10 pF	250 kΩ		50 kΩ‖10 pF	250 kΩ		50 kΩ‖10 pF	250 kΩ		
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0" I_{SINK} = 8 mA			**0.4**			**0.4**			**0.4**	V
Output Leakage Current in Logic "1"			**1**			**1**			**1**	µA
Voltage Range	0		+30	0		+30	0		+30	V
Fall Times (Load = 500 pF and I_{SINK} = 5 mA)			400			400			400	ns
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (0 mA≤I_O≤7 mA)	0		+10	0		+10	0		+10	V
Source Current (0≤V_O≤7 V)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
Closed Loop Output Impedance			1			1			1	Ω
POWER SUPPLY										
Rated Voltage		±15			±15			±15		V
Voltage Range	±9		±18	±9		±18	±9		±18	V
Quiescent Current		6	**8**		6	**8**		6	**8**	mA
TEMPERATURE RANGE										
Specified Range	0		+70	–25		+85	–55		+125	°C
Operating Range	–25		+85	–55		+125	–55		+125	°C
Storage	–25		+85	–65		+150	–65		+150	°C
PACKAGE OPTIONS										
Plastic DIP (N-14)		ADVFC32KN								
TO-100 (H-10A)					ADVFC32BH			ADVFC32SH		

NOTES
[1]Nonlinearity defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.
[2]See Figure 3.
[3]See Figure 1.
[4]f_{MAX} expressed in units of MHz.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Accelerometers & Motion Control Circuits
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Accelerometers & Motion Control Circuits–Selection Guides

Resolver-to-Digital Converters

Model	Resolution	Accuracy	Max Track RPS	Max Bandwidth	Input Signal Format	Reference Frequency Hz	Velocity Linearity	# Pins	Page No.	Comments	Fax-code
AD2S80A	10–16	±1.3'–8	1040	Selectable	R only	50–20k	±3%	40	15–5	Military Grade Available	1118
AD2S81A	12	±30'	260	Selectable	R only	400–20k	±3%	28	*		1119
AD2S90	12	±8' ± 1 LSB	750	10 kHz	R only	10 kHz	±1.0%	20	15–9		1122
AD2S82A	10–16	±2'–22	1040	Selectable	R only	50–20k	±3%	44	15–5		1120
AD2S83	10–16	±8'	1040	Selectable	R only	50–20k	±0.25%	44	15–7		1121

LVDT-to-Digital Converter

AD2S93	14	0.05–0.1%		1 kHz	LVDT	10 kHz	N/A	28	*		1123

Programmable Sine Wave Oscillator

AD2S99	N/A	0.05–0.1%				2k–20k		28	15–11		1823

LVDT Signal Conditioners

Model	Transfer Function	Gain Error %	Gain Drift ppm	Excitation Output Voltage V rms	Supply Voltage	# Pins	Page No.	Comments	Fax-code
AD598	V_{OUT} = (Va – Vb)/Va + Vb)*500 µA*R	1	50	2.1–24	+13–36 ± 13 V	24/28	15–13	Can Interface to RVDT	1192
AD698	V_{OUT} = (Va)/Vb)*500 µA*R	1	100	2.1–24	+13–36 ± 13 V	20	15–15		1237

AC Vector Coprocessors

Model	Digital Input Bits	Analog Output	Radius Error %	Angular Error arc min	Supply Voltage	# Pins	Page No.	Fax-code
AD2S100	12	2 & 3 Phase	0.7	18	±5 @ 10 mA	44	*	1110
AD2S105	12	2 Phase	1	30	±5 @ 10 mA	44	*	1111

AC Vector Coprocessors with 11-Bit A/D, 4 T/H, PWM, 8-Bit Digital I/O

ADMC200								44	15–17		1960
ADMC201								44	15–17		1961

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

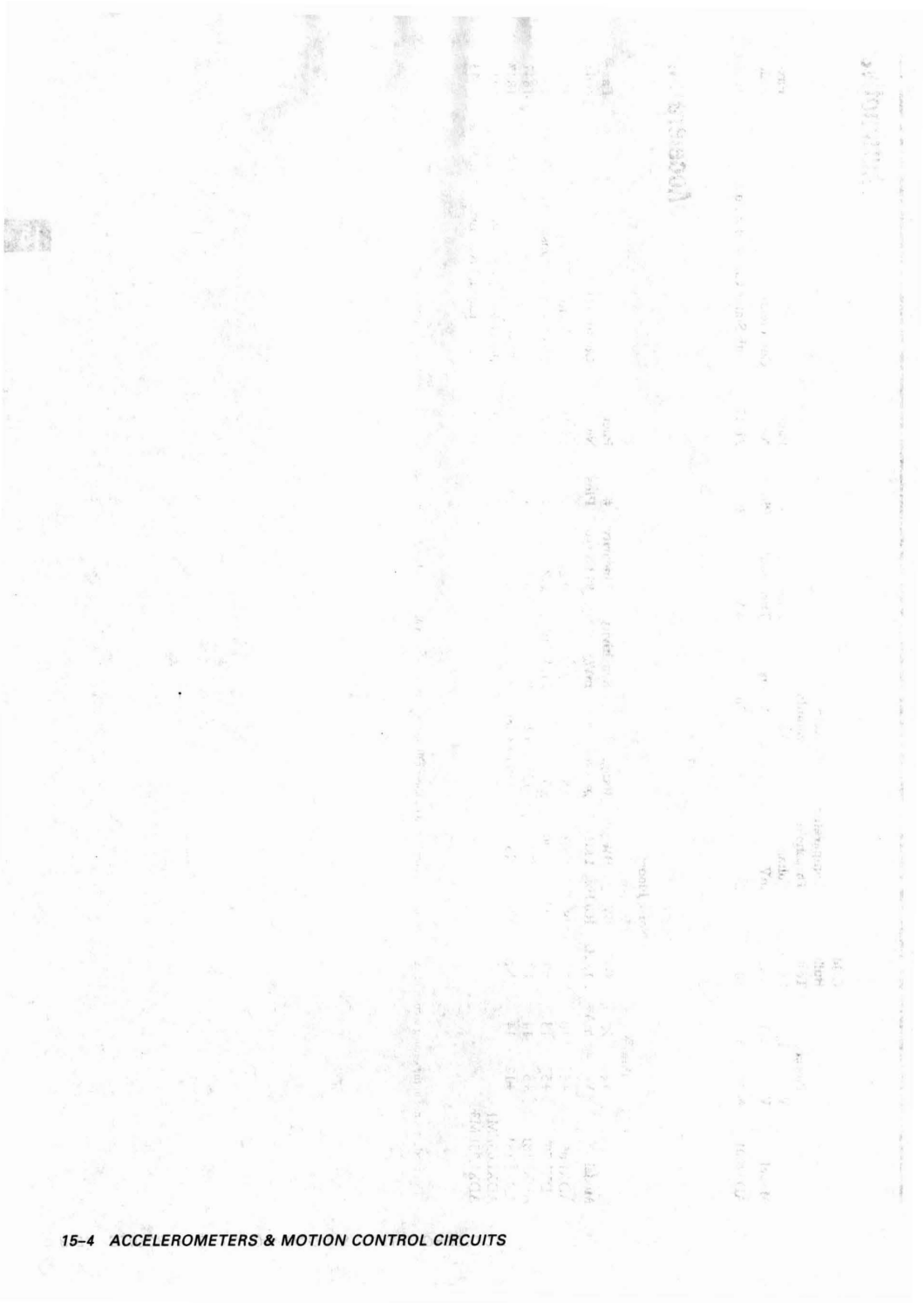
Automotive

Model	Power V_S V	Power I_S mA	Cold Bulb Test Current µA	Comparator Threshold Voltage mV	Auto Shutdown V_S V min	Auto Shutdown V_S V max	Fuse Threshold	# Pins	Page No.	Comments	Fax-code
AD22001	9–30	5	30	2	9	36	4 V	20	21–17	With Status Check of 2 Fuses	1090

Acceleration

Model	Power V_S V	Power I_S mA	Noise Floor MG p-p BW 10 Hz	BW 100 Hz	BW 1 kHz	Range *g*	Sensitivity mV/*g*	Linearity 90 FS typ	# Pins	Page No.	Comments	Fax-code
ADXL05	+5	10	2	48	120	±5	220	0.2	10	15–19	Sensitivity to 500 µ*g*	1943
ADXL50	+5	13	80	400	1300	±50	21.3–21.9	0.2	10	15–21	Frequency Response, DC to 10 kHz	1606
ADXL181	+5	14	NS	NS	NS	–125 to +250	8	0.2	10	*		1847
ADXL181	+12	14	NS	NS	NS	–150 to +880	8	0.2	10	*		1847
ADXL05EM1										15–19	Prepackaged 1 Axis Evaluation Model	1943
ADXL05EM3										15–19	Prepackaged 3 Axis Evaluation Model	1943

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.



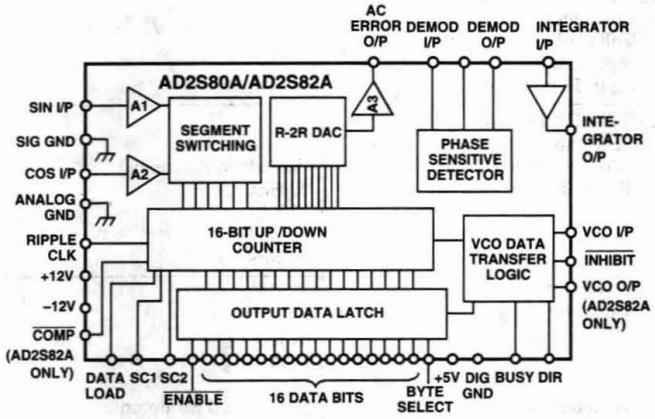
Variable Resolution, Monolithic Resolver-to-Digital Converters

AD2S80A/AD2S82A

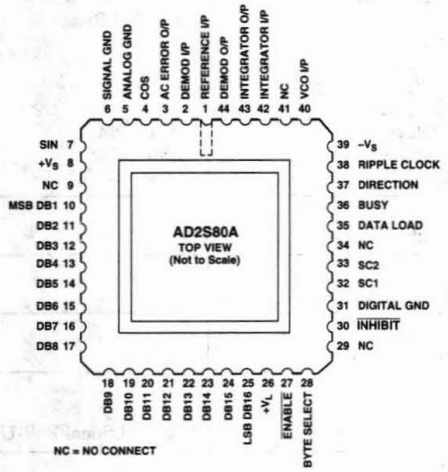
FEATURES
Ratiometric Conversion
Low Power Consumption: 300 mW typ
Dynamic Performance Set by User
Velocity Output
ESD Class 2 Protection (2,000 V min)
10-, 12-, 14- and 16-Bit Resolution Set by User
High Max Tracking Rate 1040 RPS (10 Bits)
VCO Output (AD2S82A Only)

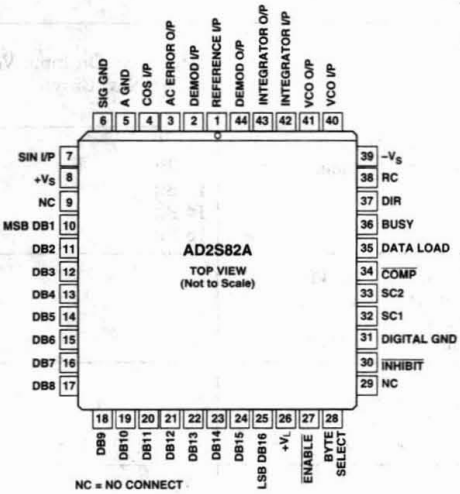
APPLICATIONS
DC Brushless and AC Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





GENERAL DESCRIPTION

The AD2S82A is a monolithic 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter contained in a 44-pin J leaded PLCC package. Two extra functions are provided in the AD2S82A–COMPLEMENT and VCO output.

The converters allow users to *select their own dynamic performance with external components.* This allows great flexibility in matching the converter to system requirements. The AD2S80A/AD2S82A allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S80A and AD2S82A convert resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures noise immunity and tolerance of lead length when the converter is remote from the resolver.

The output word is in a three-state digital logic form available in 2 bytes on the 16 output data lines for the AD2S80A/AD2S82A. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data buses, and outputs are provided to allow for cycle or pitch counting in external counters.

An analog signal proportional to velocity is also available and can be used to replace a tachogenerator.

PRODUCT HIGHLIGHTS

Resolution. Two control pins are used to select the resolution of the AD2S80A/AD2S82A to be 10, 12, 14 or 16 bits allowing optimum resolution for each application.

Ratiometric Tracking Conversion. This conversion technique provides continuous output position data without conversion delay and is insensitive to absolute signal levels. It also provides noise immunity and tolerance to harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values, the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match system requirements. A software component selection disk facilities component selection.

Velocity Output. An analog velocity signal is available and is linear to typically one percent. This can be used in place of a velocity transducer in many applications to provide loop stabilization in servo controls and velocity feedback data.

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AD2S80A/AD2S82A–SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Parameter	Conditions	AD2S80A Min	AD2S80A Typ	AD2S80A Max	AD2S82A Min	AD2S82A Typ	AD2S82A Max	Units
SIGNAL INPUTS								
Frequency		50		20,000	50		20,000	Hz
Voltage Level		1.8	2.0	2.2	1.8	2.0	2.2	V rms
Input Bias Current			60	150		60	150	nA
Input Impedance		1.0			1.0			MΩ
Maximum Voltage				8			8	V pk
REFERENCE INPUT								
Frequency		50		20,000	50		20,000	Hz
Voltage Level		1.0		8.0	1.0		8.0	V pk
Input Bias Current			60	150		60	150	nA
Input Impedance		1.0			1.0			MΩ
CONTROL DYNAMICS								
Repeatability				1			1	LSB
Allowable Phase Shift	(Signals to Reference)	–10		+10	–10		+10	Degrees
Tracking Rate	10 Bits			1040			1040	rps
	12 Bits			260			260	rps
	14 Bits			65			65	rps
	16 Bits			16.25			16.25	rps
ACCURACY								
Angular Accuracy	H						**±22 + 1 LSB**	arc min
	A, J, S			**±8 + 1 LSB**			**±8 + 1 LSB**	arc min
	B, K, T			**±4 + 1 LSB**			**±4 + 1 LSB**	arc min
	L, U			**±2 + 1 LSB**			**±2 + 1 LSB**	arc min
Monotonicity	Guaranteed Monotonic							
Missing Codes (16-Bit Resolution)	A, B, J, K, S, T						**4**	Codes
	L, U						**1**	Code
VELOCITY SIGNAL								
Linearity	Over Full Range		±1	**±3**		±1	**±3**	% FSD
Reversion Error				±2			±2	% FSD
DC Zero Offset				**6**			**6**	mV
DC Zero Offset Tempco			–22			–22		µV/°C
Gain Scaling Accuracy				**±10**			**±10**	% FSD
Output Voltage	1 mA Load	±8	±9	±10.5	±8	±9	±10.5	V
Dynamic Ripple	Mean Value			1.5			1.5	% rms O/P
Output Load				1.0			1.0	kΩ
$\overline{\text{INHIBIT}}$								
Time to Stable Data				600			600	ns
$\overline{\text{ENABLE}}$								
$\overline{\text{ENABLE}}$/Disable Time		35		110	35		110	ns
BYTE SELECT								
Time to Data Available		60		140	60		140	ns
BUSY								
Width		**200**		**600**	**200**		**600**	ns
Load	Use Additional Pull-Up			1			1	LSTTL
DIRECTION								
Max Load				3			3	LSTTL
RIPPLE CLOCK								
Width	Dependent On Input Velocity	**300**			**300**			
Reset	Before Next Busy							
Load				3			3	LSTTL
RATIO MULTIPLIER								
AC Error Output Scaling	10 Bit		**177.6**			**177.6**		mV/Bit
	12 Bit		**44.4**			**44.4**		mV/Bit
	14 Bit		**11.1**			**11.1**		mV/Bit
	16 Bit		**2.775**			**2.775**		mV/Bit
PHASE SENSITIVE DETECTOR								
Output Offset Voltage				**12**			**12**	mV
Input Bias Current			60	**150**		60	**150**	nA
Input Voltage				±8			±8	V
INTEGRATOR								
Input Offset Voltage			1	5		1	5	mV
Input Bias Current			60	150		60	150	nA
Output Voltage Range	$\pm V_S$ = ±10.8 V dc	±7			±7			V
VCO	$\pm V_S$ = ±12 V dc							
Maximum Rate		1.0	1.1		1.0	1.1		MHz
VCO Rate	Positive DIR	**7.1**	**7.9**	**8.7**	**7.1**	**7.9**	**8.7**	kHz/µA
	Negative DIR	**7.1**	**7.9**	**8.7**	**7.1**	**7.9**	**8.7**	kHz/µA
Reversion Error				1.5			1.5	% FSD

Specifications subject to change without notice.

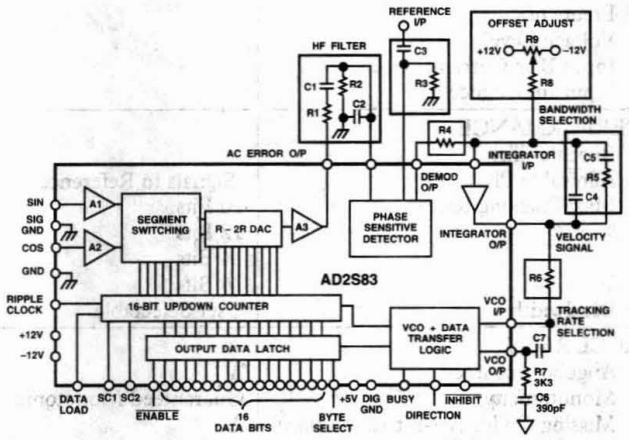
Variable Resolution, Resolver-to-Digital Converter

AD2S83

FEATURES
- Tracking R/D Converter
- High Accuracy Velocity Output
- High Max Tracking Rate 1040 RPS (10 Bits)
- 10-, 12-, 14- or 16-Bit Resolution Set by User
- Ratiometric Conversion
- Stabilized Velocity Reference
- Dynamic Performance Set by User
- Industrial Temperature Range

APPLICATIONS
- DC and AC Servo Motor Control
- Process Control
- Numerical Control of Machine Tools
- Robotics
- Axis Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S83 is a 10-, 12-, 14- or 16-bit tracking resolver-to-digital converter.

The converter allows users to *select their own resolution and dynamic performance with external components.* The converter allows users to select the resolution to be 10, 12, 14 or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S83 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long leads allowing the converter to be located remote from the resolver.

The position output from the converter is presented via 3-state output pins which can be configured for operations with 8- or 16-bit bus. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data bus, and outputs are provided to allow for cycle or pitch counting in external counters.

A precise analog signal proportional to velocity is also available and will replace a tachogenerator.

The AD2S83 operates over reference frequencies in the range 0 Hz to 20,000 Hz.

PRODUCT HIGHLIGHTS

High Accuracy Velocity Output. A precision analog velocity signal with a typical linearity of ±0.1% and reversion error less than ±0.3% is generated by the AD2S83. The provision of this signal removes the need for mechanical tachogenerators used in servo systems to provide loop stabilization and speed control.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S83 to be 10, 12, 14 or 16 bits allowing optimum resolution for each application.

Ratiometric Tracking Conversion. This technique provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The component values are easy to select using the free component selection software design aid.

MODELS AVAILABLE

Information on the models available is given in the section "Ordering Information."

ORDERING GUIDE

Model	Temperature Range	Accuracy	Package Option*
AD2S83AP	–40°C to +85°C	8 arc min	P-44A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

AD2S83–SPECIFICATIONS ($\pm V_S = \pm 12$ V dc ± 5%; $V_L = +5$ V dc ± 10%; $T_A = -40°C$ to $+85°C$)

Parameter	Conditions	AD2S83A Min	AD2S83A Typ	AD2S83A Max	Units
SIGNAL INPUTS (SIN, COS)					
Frequency[1]		0		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
REFERENCE INPUT (REF)					
Frequency		0		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
PERFORMANCE					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	–10		+10	Degree
Max Tracking Rate	10 Bits	1040			rps
	12 Bits	260			rps
	14 Bits	65			rps
	16 Bits	16.25			rps
Bandwidth	User Selectable				
ACCURACY					
Angular Accuracy	A			**±8 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A			**4**	Codes
VELOCITY SIGNAL					
Linearity[2, 3, 4]	VCO Rate 0 kHz–500 kHz		±0.15	**±0.25**	%
	VCO Rate 500 kHz–1000 kHz		±0.25	**±1.0**	%
Reversion Error			±0.5	**±1.0**	% Output
DC Zero Offset[5]			±3		mV
Gain Scaling Accuracy			±1.5	**±3**	% FSR
Output Voltage	1 mA Load	±8			V
Dynamic Ripple	Mean Value			1.0	% rms O/P
$\overline{\text{INHIBIT}}$[6]					
Time to Stable Data		240	390	490	ns
$\overline{\text{ENABLE}}$[6]					
Disable Time	Impedance State	35		110	ns
BYTE SELECT[6]					
Time to Data Available		60		140	ns
BUSY[6, 7]					
Width		200		**350**	ns
Load	Use Additional Pull-Up (See Figure 2)			1	LSTTL
DIRECTION[6]					
Max Load				**3**	LSTTL
RIPPLE CLOCK[6]					
Width	Dependent on Input Velocity	**300**			ns
Reset	Before Next Busy				
Load				**3**	LSTTL
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		177.6		mV/Bit
	12 Bit		44.4		mV/Bit
	14 Bit		11.1		mV/Bit
	16 Bit		2.775		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				**12**	mV
Input Voltage				±8	V
INTEGRATOR					
Input Offset Voltage			1	5	mV
Input Bias Current			60	**150**	nA
Output Voltage Range		**±8**			V
VCO					
Maximum Rate		1.1			MHz
VCO Rate	+ve DIR	**8.25**	8.50	**8.75**	kHz/μA
	–ve DIR	**8.25**	8.50	**8.75**	kHz/μA

Specifications subject to change without notice.

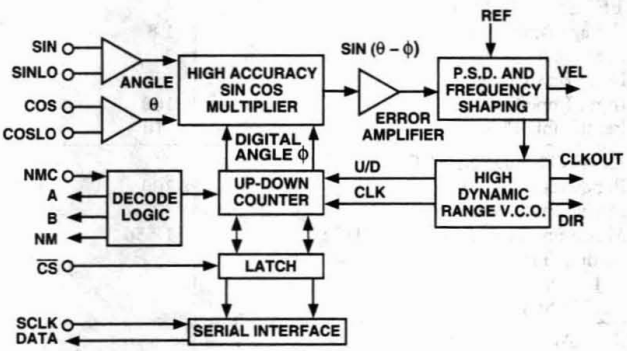
Low Cost, Complete 12-Bit Resolver-to-Digital Converter

AD2S90

FEATURES
Complete Monolithic Resolver-to-Digital Converter
Incremental Encoder Emulation (1024-Line)
Absolute Serial Data (12-Bit)
Differential Inputs
12-Bit Resolution
Industrial Temperature Range
20-Pin PLCC
Low Power (50 mW)

APPLICATIONS
Industrial Motor Control
Servo Motor Control
Industrial Gauging
Encoder Emulation
Automotive Motion Sensing and Control
Factory Automation
Limit Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S90 is a complete 12-bit resolution tracking resolver-to-digital converter. No external components are required to operate the device.

The converter accepts 2 V rms ± 10% input signals in the range 3 kHz–20 kHz on the SIN, COS and REF inputs. A Type II servo loop is employed to track the inputs and convert the input SIN and COS information into a digital representation of the input angle. The bandwidth of the converter is set internally at 1 kHz. The maximum tracking rate is 375 rps at 12-bit resolution.

Angular position output information is available in two forms, absolute serial binary and incremental A quad B.

The absolute serial binary output is 12-bit (1 in 4096). The data output pin is high impedance when Chip Select $\overline{CS}$ is logic HI. This allows the connection of multiple converters onto a common bus. Absolute angular information in serial pure binary form is accessed by $\overline{CS}$ followed by the application of an external clock (SCLK) with a maximum rate of 2 MHz.

The encoder emulation outputs A, B and NM continuously produce signals equivalent to a 1024 line encoder. When decoded this corresponds to 12-bits resolution. Three common north marker pulse widths are selected via a single pin (NMC).

An analog velocity output signal provides a representation of velocity from a rotating resolver shaft traveling in either a clockwise or counterclockwise direction.

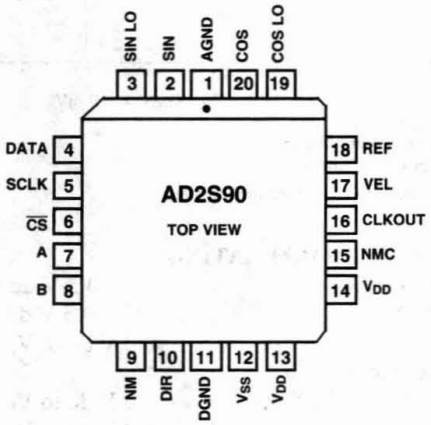
The AD2S90 operates on a ±5 V dc ± 5% power supplies and is fabricated on Analog Devices' Linear Compatible CMOS process (LC^2MOS). LC^2MOS is a mixed technology process that combines precision bipolar circuits with low power CMOS logic circuits.

ORDERING GUIDE

Model	Temperature Range	Accuracy	Package Option*
AD2S90AP	–40°C to +85°C	10.6 arc min	P-20A

*P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

PIN CONFIGURATION



AD2S90–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, T_A = –40°C to +85°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Condition
SIGNAL INPUTS					
Voltage Amplitude	1.8	2.0	2.2	V rms	Differential SIN to SIN LO, COS to COS LO
Frequency	3		20	kHz	
Input Bias Current			100	nA	V_{IN} = 2 ± 10% V rms
Input Impedance	1.0			MΩ	V_{IN} = 2 ± 10% V rms
Common-Mode Volts[1]			100	mV peak	CMV @ SINLO, COSLO w.r.t.
CMRR	60			dB	AGND @ 10 kHz
REFERENCE INPUT					
Voltage Amplitude	1.8	2.0	3.35	V rms	
Frequency	3		20	kHz	
Input Bias Current			100	nA	
Input Impedance	100			kΩ	
Permissible Phase Shift	–10		+10	Degrees	Relative to SIN, COS Inputs
CONVERTER DYNAMICS					
Bandwidth	700	840	1000	Hz	
Maximum Tracking Rate	375			rps	
Maximum VCO Rate (CLKOUT)	1.536			MHz	
Settling Time					
1° Step			7	ms	
179° Step			20	ms	
ACCURACY					
Angular Accuracy[2]			±10.6 + 1 LSB	arc min	
Repeatability[3]			1	LSB	
VELOCITY OUTPUT					
Scaling	127.5	150	172.5	rps/V dc	
Output Voltage at max rps	±2.17		±2.875	V dc	
Load Drive Capability			±250	µA	V_{OUT} = ±2.5 V dc
LOGIC INPUTS SCLK, $\overline{CS}$					
Input High Voltage (V_{INH})	3.5			V dc	V_{DD} = +5 V dc, V_{SS} = –5 V dc
Input Low Voltage (V_{INL})			1.5	V dc	V_{DD} = +5 V dc, V_{SS} = –5 V dc
Input Current (I_{IN})			10	µA	
Input Capacitance			10	pF	
LOGIC OUTPUTS DATA, A, B,[4]					
NM, CLKOUT, DIR					V_{DD} = +5 V dc, V_{SS} = –5 V dc
Output High Voltage	4.0			V dc	I_{OH} = 1 mA
Output Low Voltage			1.0	V dc	I_{OL} = 1 mA
			0.4	V dc	I_{OL} = 400 µA
SERIAL CLOCK (SCLK)					
SCLK Input Rate			2	MHz	1:1 Mark Space Ratio
NORTH MARKER CONTROL (NMC)					
90°	+4.75	+5.0	+5.25	V dc	North Marker Width Relative to
180°	–0.75	DGND	+0.75	V dc	to "A" Cycle
360°	–4.75	–5.0	–5.25	V dc	
POWER SUPPLIES					
V_{DD}	+4.75	+5.00	+5.25	V dc	
V_{SS}	–4.75	–5.00	–5.25	V dc	
I_{DD}			7	mA	
I_{SS}			9	mA	

NOTES
[1]If the tolerance on signal inputs = ±5%, then CMV = 200 mV.
[2]1 LSB = 5.3 arc minute.
[3]Specified at constant temperature.
[4]Output load drive capability.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND ..... –0.3 V dc to +7.0 V dc
V_{SS} to AGND ..... +0.3 V dc to –7.0 V dc
AGND to DGND ..... –0.3 V dc to V_{DD} + 0.3 V dc
Analog Inputs to AGND
REF ..... V_{SS} – 0.3 V dc to V_{DD} + 0.3 V dc
SIN, SIN LO ..... V_{SS} – 0.3 V dc to V_{DD} + 0.3 V dc
COS, COS LO ..... V_{SS} – 0.3 V dc to V_{DD} + 0.3 V dc
Analog Output to AGND
VEL ..... V_{SS} to V_{DD}
Digital Inputs to DGND, CSB,
SCLK, RES ..... –0.3 V dc to V_{DD} + 0.3 V dc
Digital Outputs to DGND, NM, A, B,
DIR, CLKOUT DATA ..... –0.3 V dc to V_{DD} + 0.3 V dc
Operating Temperature Range
Industrial (AP) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 10 secs) ..... 300°C
Power Dissipation to +75°C ..... 300 mW
Derates above +75°C by ..... 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

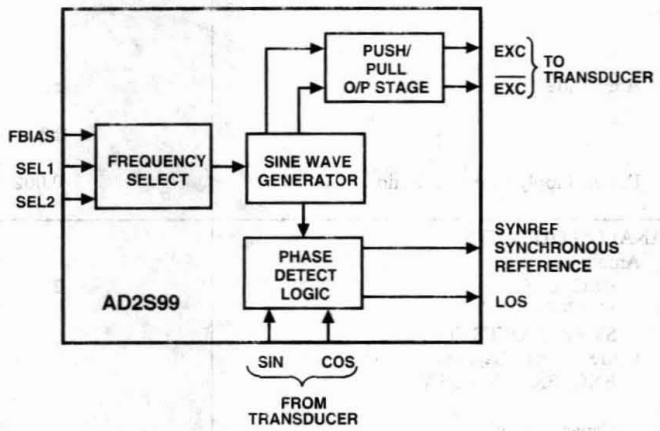
Programmable Oscillator

AD2S99

FEATURES
Programmable Sinusoidal Oscillator
Synthesized Synchronous Reference Output
Programmable Output Frequency Range: 2 kHz–20 kHz
"Loss-of-Signal" Indicator
20-Pin PLCC Package
Low Cost

APPLICATIONS
Excitation Source for:
Resolvers
Synchros
LVDTs
RVDTs
Pressure Transducers
Load Cells
AC Bridges

FUNCTIONAL BLOCK DIAGRAM



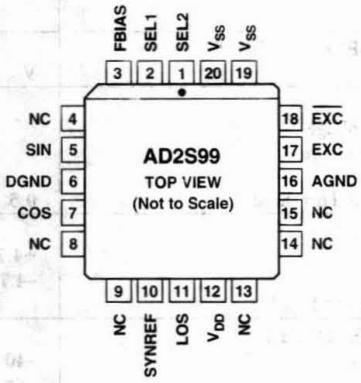
GENERAL DESCRIPTION

The AD2S99 programmable sinusoidal oscillator provides sine wave excitation for resolvers and a wide variety of ac transducers. The AD2S99 also provides a synchronous reference output signal (3 V p-p square wave) that is phase locked to its SIN and COS inputs. In an application, the SIN and COS inputs are connected to the transducer's secondary windings.

The synchronous reference output compensates for temperature and cabling dependent phase shifts and eliminates the need for external preset phase compensation circuits. The synchronous reference output can be used as a zero crossing reference for resolver-to-digital converters such as Analog Devices' AD2S80A, AD2S82A, AD2S83 and AD2S90.

The AD2S99 is packaged in a 20-pin PLCC and operates over –40°C to +85°C.

PIN CONFIGURATION



NC = NO CONNECT

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD2S99AP	–40°C to +85°C	P-20A
AD2S99BP	–40°C to +85°C	P-20A

*P = PLCC. For outline information see Package Information section.

AD2S99–SPECIFICATIONS (V_S = ±4.75 V to ±5.25 V @ –40°C to +85°C unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
FREQUENCY OUTPUT RANGE					SEL1 SEL2
2 kHz		2000		Hz	V_{SS} V_{SS}
5 kHz		5000		Hz	V_{SS} GND
10 kHz		10000		Hz	GND V_{SS}
20 kHz		20000		Hz	GND GND
ACCURACY					
Frequency			±10	%	AP Grade @ +25°C
			±20	%	AP Grade –40°C to +85°C
			±5	%	BP Grade @ +25°C
			±10	%	BP Grade –40°C to +85°C
Amplitude		±3	±10	%	AP Grade @ +25°C
			±20	%	AP Grade –40°C to +85°C
		±3	±5	%	BP Grade @ +25°C
			±10	%	BP Grade –40°C to +85°C
Power Supply Rejection Ratio		0.002		V p-p/V	Output Variation as Function of Change in Power Supply Voltage
ANALOG OUTPUTS					
Amplitude					
EXC, $\overline{EXC}$		2		V rms	EXC to GND, $\overline{EXC}$ to GND
SYNREF		±3		V p-p	Square Wave
SYNREF OFFSET			±200	mV	
Current Drive Capability					
EXC, $\overline{EXC}$ V_S = ±5 V			8	mA rms	R_{LOAD} = 500 Ω $\overline{EXC}$ to EXC C_{LOAD} = 1000 pF
Capacitive Drive			1000	pF	
Total Harmonic Distortion					
EXC, $\overline{EXC}$		–25		dB	
ANALOG INPUTS SIN, COS					
Amplitude	1.8	2.0	2.2	V rms	
Phase Lock Range	–45		+45	Degrees	
Additional Phase Delay					
			±10	Degrees	AP Grade
			±10	Degrees	BP Grade
FREQUENCY SELECT INPUTS					
SEL1, SEL2[1]	V_{SS}		AGND	V dc	
LOS OUTPUT					
Output Low Voltage			0.7	V dc	I_{OL} = 400 µA
Output High Voltage		V_{DD}		V dc	50 kΩ Pull Up to V_{DD} (Open Drain Output)
SIN, COS LOS Threshold	0.5	0.6	0.8	V rms	
POWER SUPPLIES					
V_{DD}	+4.75		+5.25	V dc	
V_{SS}	–4.75		–5.25	V dc	
Quiescent Current I_{DD}, I_{SS}		±8	±15	mA	No Load
TEMPERATURE RANGE					
Operating	–40		+85	°C	
Storage	–65		+150	°C	

NOTES
[1]Frequency select pins SEL1 and SEL2 must be connected to appropriate voltage levels before power is applied.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} ..... +7 V
V_{SS} ..... –7 V
Operating Temperature .....–40°C to +85°C
Storage Temperature .....–65°C to +150°C
Analog Input Voltages (SIN and COS) ..... V_{SS} – 0.3 V
.....to V_{DD} + 0.3 V
Frequency Select (SEL1, SEL2) .....V_{SS} – 0.4 V
..... to AGND + 0.4 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage (V_{DD} to V_{SS}) ..... ±4.75 V to ±5.25 V
Analog Input Voltage (SIN and COS) ..... 2 V rms ±10%
Frequency Select (SEL1 and SEL2) .....V_{SS} to AGND
Operating Temperature Range .....–40°C to +85°C

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S99 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ANALOG DEVICES

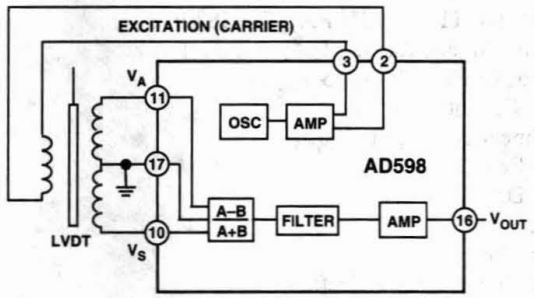
LVDT Signal Conditioner

AD598

FEATURES

- **Single Chip Solution, Contains Internal Oscillator and Voltage Reference**
- **Insensitive to Transducer Null Voltage**
- **Insensitive to Primary to Secondary Phase Shifts**
- **DC Output Proportional to Position**
- **20 Hz to 20 kHz Frequency Range**
- **Single or Dual Supply Operation**
- **Unipolar or Bipolar Output**
- **Will Also Interface to an RVDT**
- **Outstanding Performance**
  - **Linearity: 0.05% of FS max**
  - **Output Voltage: ±11 V min**
  - **Gain Drift: 50 ppm/°C of FS max**
  - **Offset Drift: 50 ppm/°C of FS max**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD598 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD598 converts the raw LVDT secondary output to a scaled dc signal. The device can also be used with RVDT transducers.

The AD598 contains a low distortion sine wave oscillator to drive the LVDT primary. The LVDT secondary output consists of two sine waves that drive the AD598 directly. The AD598 operates upon the two signals, dividing their difference by their sum, producing a scaled unipolar or bipolar dc output.

The AD598 uses a unique ratiometric architecture to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary, transformer null voltage and primary to secondary phase shift does not affect system accuracy, temperature stability is improved, and transducer interchangeability is improved.

The AD598 is available in two performance grades. It is also available processed to MIL-STD-883B, for the military range of –55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD598 can be used with many different types of LVDTs. The AD598 can drive an LVDT primary with up to 24 V rms and accept secondary input levels as low as 100 mV rms.
2. The 20 Hz to 20 kHz LVDT excitation frequency is determined by a single external capacitor. The AD598 input signal need not be synchronous with the LVDT primary drive. This means that an external primary excitation, such as the 400 Hz power mains in aircraft, can be used.
3. The AD598 uses a ratiometric decoding scheme such that primary to secondary phase shifts and transducer null voltage have no effect on overall circuit performance.
4. Multiple LVDTs can be driven by a single AD598, either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
5. The AD598 may be used as a loop integrator in the design of simple electromechanical servo loops.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD598JR	0°C to +70°C	20-Pin Small Outline (SOIC)	R-20
AD598AD	–40°C to +85°C	20-Pin Ceramic DIP	D-20

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD598–SPECIFICATIONS (typical @ +25°C and ±15 V dc, C1 = 0.015 μF, R2 = 80 kΩ, R_L = 2 kΩ, unless otherwise noted. See Figure 7.)

Parameter	AD598J Min	AD598J Typ	AD598J Max	AD598A Min	AD598A Typ	AD598A Max	Unit
TRANSFER FUNCTION	$V_{OUT} = \frac{V_A - V_B}{V_A + V_B} \times 500\ \mu A \times R2$						V
OVERALL ERROR							
T_{MIN} to T_{MAX}		0.6	2.35		0.6	1.65	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range (T_{MIN} to T_{MAX})	±11			±11			V
Output Current (T_{MIN} to T_{MAX})	8			6			mA
Short Circuit Current		20			20		mA
Nonlinearity (T_{MIN} to T_{MAX})		75	±500		75	±500	ppm of FS
Gain Error		0.4	±1		0.4	±1	% of FS
Gain Drift		20	±100		20	±50	ppm/°C of FS
Offset		0.3	±1		0.3	±1	% of FS
Offset Drift		7	±200		7	±50	ppm/°C of FS
Excitation Voltage Rejection		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain (T_{MIN} to T_{MAX})	300	100		400	100		ppm/V
PSRR Offset (T_{MIN} to T_{MAX})	100	15		200	15		ppm/V
Common-Mode Rejection (±3 V)							
CMRR Gain (T_{MIN} to T_{MAX})	100	25		200	25		ppm/V
CMRR Offset (T_{MIN} to T_{MAX})	100	6		200	6		ppm/V
Output Ripple		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage							
(R1 = Open)	1.2		2.1	1.2		2.1	V rms
(R1 = 12.7 kΩ)	2.6		4.1	2.6		4.1	V rms
(R1 = 487 Ω)	14		20	14		20	V rms
Excitation Voltage TC		600			600		ppm/°C
Output Current	30			30			mA rms
T_{MIN} to T_{MAX}	12			12			mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{MIN} to T_{MAX}		30	±100		30	±100	mV
Frequency	20		20k	20		20k	Hz
Frequency TC, (R1 = 12.7 kΩ)		200			200		ppm/°C
Total Harmonic Distortion		–50			–50		dB
SIGNAL INPUT CHARACTERISTICS							
Signal Voltage	0.1		3.5	0.1		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (AIN and BIN)		1	5		1	5	μA
Signal Reference Bias Current		2	10		2	10	μA
Excitation Frequency	0		20	0		20	kHz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 to +10 V Output	17.5			17.5			V
0 to –10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	15		12	15	mA
T_{MIN} to T_{MAX}			16			18	mA

Specifications subject to change without notice.

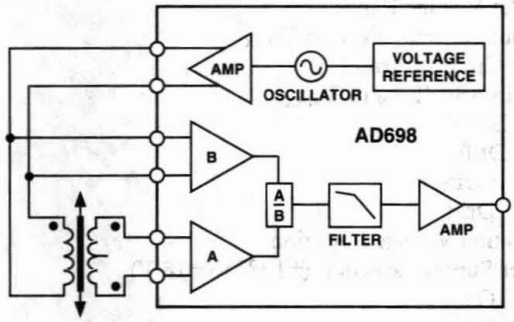
Universal LVDT Signal Conditioner

AD698

FEATURES

- **Single Chip Solution, Contains Internal Oscillator and Voltage Reference**
- **Interfaces to Half-Bridge, 4-Wire LVDT**
- **DC Output Proportional to Position**
- **20 Hz to 20 kHz Frequency Range**
- **Unipolar or Bipolar Output**
- **Will Also Decode AC Bridge Signals**
- **Outstanding Performance**
  - **Linearity: 0.05%**
  - **Output Voltage: ±11 V**
  - **Gain Drift: 20 ppm/°C (typ)**
  - **Offset Drift: 5 ppm/°C (typ)**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD698 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD698 converts the raw LVDT output to a scaled dc signal. The device will operate with half-bridge LVDTs, LVDTs connected in the series opposed configuration (4-wire), and RVDTs.

The AD698 contains a low distortion sine wave oscillator to drive the LVDT primary. Two synchronous demodulation channels of the AD698 are used to detect primary and secondary amplitude. The part divides the output of the secondary by the amplitude of the primary and multiplies by a scale factor. This eliminates scale factor errors due to drift in the amplitude of the primary drive, improving temperature performance and stability.

The AD698 uses a unique ratiometric architecture to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary; temperature stability is improved; and transducer interchangeability is improved.

The AD698 is available in two performance grades.

PRODUCT HIGHLIGHTS

1. The AD698 offers a single chip solution to LVDT signal conditioning problems. All active circuits are on the monolithic chip with only passive components required to complete the conversion from mechanical position to dc voltage.
2. The AD698 can be used with many different types of position sensors. The circuit is optimized for use with any LVDT, including half-bridge and series opposed, (4 wire) configurations. The AD698 accommodates a wide range of input and output voltages and frequencies.
3. The 20 Hz to 20 kHz excitation frequency is determined by a single external capacitor. The AD698 provides up to 24 volts rms to differentially drive the LVDT primary, and the AD698 meets its specifications with input levels as low as 100 millivolts rms.
4. Multiple LVDTs can be driven by a single AD698 either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
5. The AD698 may be used as a loop integrator in the design of simple electromechanical servo loops.

ORDERING GUIDE

Model	Package Description	Temperature Range	Package Option*
AD698AP	28-Pin PLCC	–40°C to +85°C	P-28A
AD698SQ	24-Pin Double Cerdip	–55°C to +125°C	Q-24A

*For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD698–SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and V+, V– = ±15 V dc, unless otherwise noted)

Parameter	AD698SQ Min	AD698SQ Typ	AD698SQ Max	AD698AP Min	AD698AP Typ	AD698AP Max	Unit
TRANSFER FUNCTION	$V_{OUT} = \frac{A}{B} \times 500\ \mu A \times R2$						V
OVERALL ERROR T_{MIN} to T_{MAX}		0.4	**1.65**		0.4	**1.65**	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range	**±11**			**±11**			V
Output Current, T_{MIN} to T_{MAX}		11			11		mA
Short Circuit Current		20			20		mA
Nonlinearity T_{MIN} to T_{MAX}		75	**±500**		75	**±500**	ppm of FS
Gain Error		0.1	**±1.0**		0.1	**±1.0**	% of FS
Gain Drift		20	**±100**		20	**±100**	ppm/°C of FS
Output Offset		0.02	**±1**		0.02	**±1**	% of FS
Offset Drift		5	**±25**		5	**±25**	ppm/°C of FS
Excitation Voltage Rejection		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain		50	**300**		50	**300**	ppm/V
PSRR Offset		15	**100**		15	**100**	ppm/V
Common-Mode Rejection (±3 V)							
CMRR Gain		25	**100**		25	**100**	ppm/V
CMRR Offset		2	**100**		2	**100**	ppm/V
Output Ripple		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage (Resistors Are 1% Absolute Values)							
(R1 = Open)	**1.2**		**2.15**	**1.2**		**2.15**	V rms
(R1 = 12.7 kΩ)	**2.6**		**4.35**	**2.6**		**4.35**	V rms
(R1 = 487 Ω)	**14**		**21.2**	**14**		**21.2**	V rms
Excitation Voltage TC		100			100		ppm/°C
Output Current	**30**	50		**30**	50		mA rms
T_{MIN} to T_{MAX}		40			40		mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{MIN} to T_{MAX}		30	**±100**		30	**±100**	mV
Frequency	20		20 k	20		20 k	Hz
Frequency TC		200			200		ppm/°C
Total Harmonic Distortion		–50			–50		dB
SIGNAL INPUT CHARACTERISTICS							
A/B Ratio Usable Full-Scale Range	0.1		0.9	0.1		0.9	
Signal Voltage B Channel	0.1		3.5	0.1		3.5	V rms
Signal Voltage A Channel	0.0		3.5	0.0		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (BIN, AIN)		1	5		1	5	μA
Signal Reference Bias Current		2	**10**		2	**10**	μA
Excitation Frequency	0		20 k	0		20 k	Hz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 V to +10 V Output	17.5			17.5			V
0 V to –10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	**15**		12	**15**	mA
T_{MIN} to T_{MAX}			**18**			**18**	mA

Specifications subject to change without notice.

ADMC200/ADMC201

FEATURES

Analog Input Block
- 11-Bit Resolution Analog-to-Digital (A/D) Converter
- 7 Single-Ended (SE) Analog Inputs
  - 4 Simultaneously Sampled Analog Inputs
  - Expansion with 4 Multiplexed Inputs (ADMC201 Only)
- 3.2 μs Conversion Time/Channel
- 0 V–5 V Analog Input Range
- Internal 2.5 V Reference
- PWM Synchronized Sampling Capability

12-Bit PWM Timer Block
- Three-Phase Center-Based PWM
- 1.5 kHz–25 kHz PWM Switching Frequency Range
- Programmable Deadtime
- Programmable Pulse Deletion
- PWM Synchronized Output
- External PWM Shutdown

Vector Transformation Block
- 12-Bit Vector Transformations
- Forward and Reverse Clarke Transformations
- Forward and Reverse Park Rotations
- 2.9 μs Transformation Time

Programmable Digital I/O Port (ADMC201 only)
- 6-Bit Configurable Digital I/O
- Change of State Interrupt Support

DSP & Microcontroller Interface
- 12-Bit Memory Mapped Registers
- Twos Complement Data Format

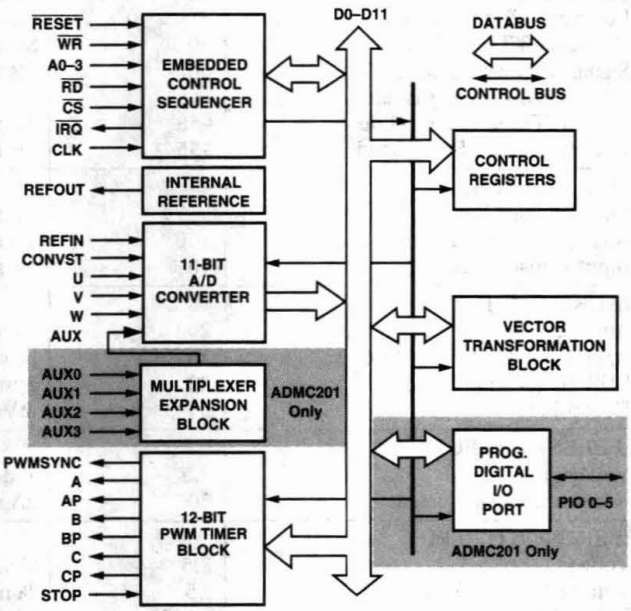
6.25 MHz to 25 MHz Operating Clock Range

68-Pin PLCC Package

Single 5 V DC Power Supply

Industrial Temperature Range

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADMC200/ADMC201 are motion coprocessors that can be used with either microcontrollers or digital signal processors (DSP). They provide the functionality that is required to implement a digital control system. In a typical application, the DSP or microcontroller performs the control algorithms (position, speed, torque and flux loops) and the ADMC200 or ADMC201 provides the necessary motor control functions: analog current data acquisition, vector transformation, and PWM drive signals.

PRODUCT HIGHLIGHTS

Simultaneous Sampling of Four Inputs

A four channel sample and hold amplifier allows three-phase motor currents to be sampled simultaneously, reducing errors from phase coherency. Sample and hold acquisition time is 1.6 μs and conversion time per channel is 3.2 μs (using a 12.5 MHz system clock).

Flexible Analog Channel Sequencing

The ADMC200/ADMC201 support acquisition of 2, 3, or 4 channels per group. Converted channel results are stored in registers and the data can be read in any order. The sampling and conversion time for two channels is 8 μs, three channels is 11.2 μs, and four channels is 14.4 μs (using a 12.5 MHz system clock).

Embedded Control Sequencer

The embedded control sequencer off-loads the DSP or microprocessor, reducing the instructions required to read analog input channels, control PWM timers and perform vector transformations. This frees the host processor for performing control algorithms.

Fast DSP/Microprocessor Interface

The high speed digital interface allows direct connection to 16-bit digital signal processors and microprocessors. The ADMC200/ADMC201 has 12-bit memory mapped registers with twos complement data format and can be mapped directly into the data memory map of a DSP. This allows for a single instruction read and write interface.

Integration

The ADMC200/ADMC201 integrates a four channel simultaneous sampling analog-to-digital converter, analog reference, vector transformation, and three-phase PWM timers into a 68-pin PLCC. Integration reduces cost, board space, power consumption, and design and test time.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option*
ADMC200AP	–40°C to +85°C	68-Pin PLCC	P-68A
ADMC201AP	–40°C to +85°C	68-Pin PLCC	P-68A

*For outline information see Package Information section.

ADMC200/ADMC201–SPECIFICATIONS (V_{DD} = +5 V ± 5%; AGND = DGND = 0 V; REFIN = 2.5 V; External Clock = 12.5 MHz; T_A = –40°C to +85°C unless otherwise noted)

Parameter	ADMC200AP/ ADMC201AP	Units	Conditions/Comments
ANALOG-TO-DIGITAL CONVERTER[1]			
Resolution	11	Bits	Twos Complement Data Format
Relative Accuracy	±2	LSB max	Integral Nonlinearity
Differential Nonlinearity	±2	LSB max	No Missing Codes Guaranteed
Bias Offset Error	±5	LSB max	Any Channel
Bias Offset Match	4	LSB max	Between Channels
Full-Scale Error	±6	LSB max	Any Channel
Full-Scale Error Match	4	LSB max	Between Channels
Conversion Time/Channel	40	System CLK Cycles	
Signal-to-Noise Ratio (SNR)[2]	60	dB min	f_{IN} = 600 Hz Sine Wave, f_{SAMPLE} = 55 kHz, 600 Hz
Channel-to-Channel Isolation			
Two-/Three-Phase Mode	–58	dB max	Sine Wave Applied to Unselected Channels
Three-/Three-Phase Mode	–55	dB max	
ANALOG INPUTS			
Input Voltage Level	0–5	Volts	
Analog Input Current	100	µA max	
Input Capacitance	10	pF typ	
TRACK AND HOLD			
Aperture Delay	200	ns max	Any Channel
Aperture Time Delay Match	20	ns max	Between Channels
SHA Acquisition Time	20	System CLK Cycles	
Droop Rate	5	mV/ms max	
REFERENCE INPUT			
Voltage Level	2.5	V dc	
Reference Input Current	50	µA max	
REFERENCE OUTPUT			
Voltage Level	2.5	Volts	
Voltage Level Tolerance	±5	% max	Full Load
Drive Capability	±200	µA max	
LOGIC			
V_{IL}	0.8	V max	
V_{IH}	2.0	V min	
V_{OL}	0.4	V max	I_{SINK} = 400 µA, V_{DD} = 5 V
V_{OH}	4.5	V min	I_{SOURCE} = 20 µA, V_{DD} = 5 V
Input Leakage Current	1	µA max	
Three-State Leakage Current	1	µA max	
Input Capacitance	20	pF typ	
PWM TIMERS			
Resolution	12	Bits	
Programmable Deadtime Range	0–10.08	µs	
Programmable Deadtime Increments	2	System CLK Cycles	160 ns
Programmable Pulse Deletion Range	0–10.16	µs	
Programmable Deletion Increments	1	System CLK Cycle	80 ns
Minimum PWM Frequency	1.5	kHz	Resolution Varies with PWM Switching Frequency (10 MHz Clock: 20 kHz = 9 Bits, 10 kHz = 10 Bits, 5 kHz = 11 Bits, 2.5 kHz = 12 Bits). Higher Frequencies are Available with Lower Resolution
VECTOR TRANSFORMATION			Park & Clarke Transformation
Radius Error	0.7	% max	
Angular Error	30	arc min max	
Reverse Transformation Time	37	System CLK Cycles	
Forward Transformation Time	40	System CLK Cycles	
EXTERNAL CLOCK INPUT			
Range	6.25–25	MHz	If > 12.5 MHz, Then It Is Necessary to Divide Down via SYSCTRL Register
INTERNAL SYSTEM CLOCK			
Range	6.25–12.5	MHz	
POWER SUPPLY CURRENT			
I_{DD}	20	mA max	

NOTES
[1]Measurements made with external reference.
[2]Tested with PWM Switching Frequency of 25 kHz.
Specifications subject to change without notice.

ANALOG DEVICES

±1 *g* to ±5 *g* Single Chip Accelerometer with Signal Conditioning

ADXL05*

FEATURES

5 milli-*g* Resolution
Noise Level 12× Less than the ADXL50
User Selectable Full Scale from ±1 *g* to ±5 *g*
Output Scale Selectable from 200 mV/*g* to 1 V/*g*
Complete Acceleration Measurement System on a Single Chip IC
Self Test on Digital Command
+5 V Single Supply Operation
1000 *g* Shock Survival

APPLICATIONS

Low Cost Sensor for Vibration Measurement
Tilt Sensing with Faster Response than Electrolytic or Mercury Sensors
More Sensitive Alarms and Motion Detectors
Affordable Inertial Sensing of Velocity and Position

GENERAL DESCRIPTION

The ADXL05 is a complete acceleration measurement system on a single monolithic IC. The ADXL05 will measure accelerations with full-scale ranges of ±5 *g* to ±1 *g* or less. Typical noise floor is 500 $\mu g/\sqrt{Hz}$, (12× less than the ADXL50), allowing signals below 5 milli-*g* to be resolved. The ADXL05 is a force balanced capacitive accelerometer with the capability to measure both ac accelerations (typical of vibration) or dc accelerations (such as inertial force or gravity). Three external capacitors and a +5 volt regulated power supply are all that is required to measure accelerations up to ±5 *g*. Three resistors are used to configure the output buffer amplifier to set scale factors from 200 mV/*g* to 1 V/*g*. External capacitors may be added to the resistor network to provide 1 or 2 poles of filtering. No additional active components are required to interface directly to most analog to digital converters (ADCs).

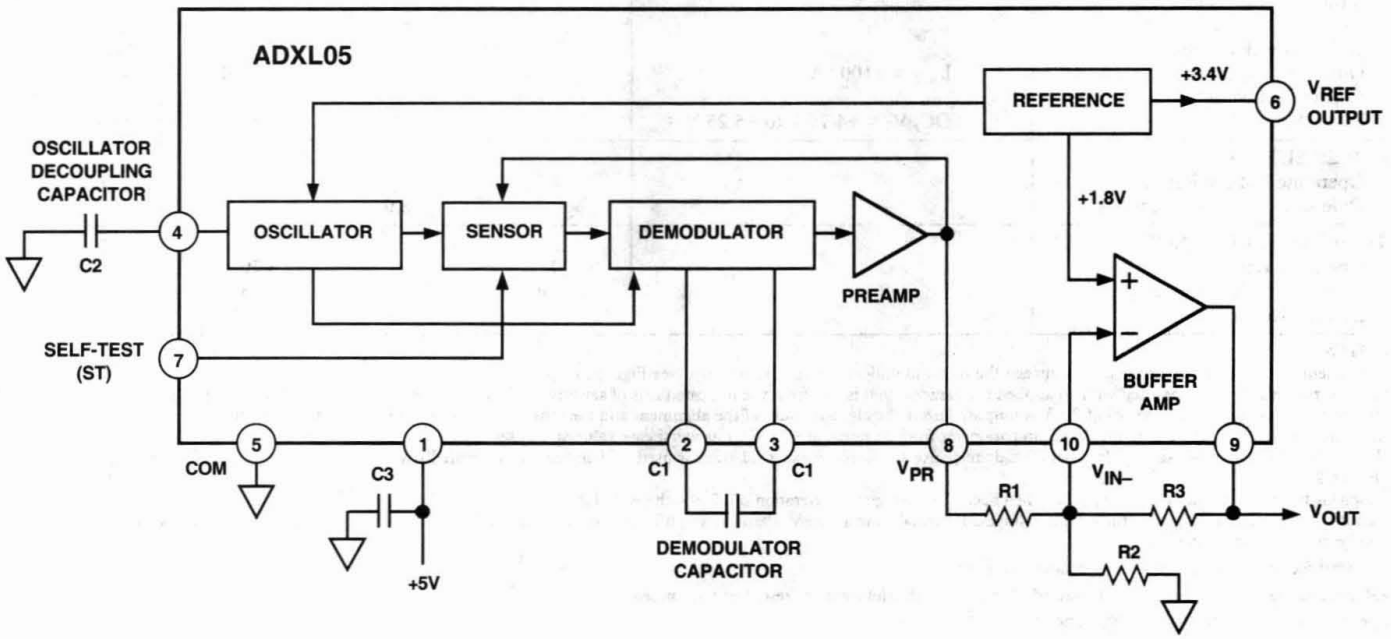
The device features a TTL compatible self-test function that can electrostatically deflect the sensor beam at any time to verify that the sensor and its electronics are functioning correctly.

The ADXL05 is available in a hermetic 10-pin TO-100 metal can, specified over the 0°C to +70°C commercial, and –40°C to +85°C industrial temperature ranges. Contact factory for availability of automotive grade devices.

ORDERING GUIDE

Model	Temperature Range
ADXL05JH	0°C to +70°C
ADXL05AH	–40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



*Patents pending.

ADXL05–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, T_A = +25°C for J Grade Only, V_S = +5 V, @ Acceleration = 0 *g*, unless otherwise noted)

Parameter	Conditions	ADXL05J/A Min	Typ	Max	Units
SENSOR INPUT					
Measurement Range	Guaranteed Full Scale	–5		+5	*g*
Nonlinearity	Best Fit Straight Line, 5 *g* FS		0.2		% of FS
Alignment Error[1]			±1		Degrees
Transverse Sensitivity[2]			±2		%
SENSITIVITY					
Initial Sensitivity at V_{PR}	+25°C	175	200	225	mV/*g*
Initial Sensitivity at V_{OUT}	+25°C, R3/R1 = 5	0.875	1.000	1.125	V/*g*
Temperature Drift[3]			±0.5		% of Reading
ZERO *g* BIAS LEVEL	at V_{PR}				
Initial Offset		1.50	1.80	2.10	V
vs. Temperature[3]			±25/40		mV
vs. Supply	V_S = 4.75 V to 5.25 V		10	32	mV/V
NOISE PERFORMANCE	at V_{PR}				
Voltage Noise Density	BW = 4 Hz to 1 kHz		500	1000	$\mu g/\sqrt{Hz}$
Noise in 100 Hz Bandwidth			5		*mg* rms
Noise in 10 Hz Bandwidth			1.6		*mg* rms
FREQUENCY RESPONSE					
3 dB Bandwidth[4]	C1 = 0.022 µF (See Figure 9)	1000	1600		Hz
3 dB Bandwidth[4]	C1 = 0.010 µF		4		kHz
Sensor Resonant Frequency			12		kHz
SELF TEST INPUT					
Output Change at V_{PR}[5]	ST Pin from Logic "0" to "1"	–0.85	–1.00	–1.15	V
Logic "1" Voltage		2.0			V
Logic "0" Voltage				0.8	V
Input Resistance	To Common		50		kΩ
+3.4 V REFERENCE					
Output Voltage		3.350	3.400	3.450	V
Output Temperature Drift[3]			±5		mV
Power Supply Rejection	DC, V_S = +4.75 V to +5.25 V		1	10	mV/V
Output Current	Sourcing	500			µA
PREAMPLIFIER OUTPUT					
Voltage Swing		0.25		V_S – 1.4	V
Current Output	Source or Sink	30	80		µA
Capacitive Load Drive			100		pF
BUFFER AMPLIFIER					
Input Offset Voltage[6]	Delta from Nominal 1.800 V		±10	±25	mV
Input Bias Current			5	20	nA
Open-Loop Gain	DC		80		dB
Unity Gain Bandwidth			200		kHz
Output Voltage Swing	I_{OUT} = ±100 µA	0.25		V_S – 0.25	V
Capacitive Load Drive		1000			pF
Power Supply Rejection	DC, V_S = +4.75 V to +5.25 V		1	10	mV/V
POWER SUPPLY					
Operating Voltage Range		4.75		5.25	V
Quiescent Supply Current			8.0	10.0	mA
TEMPERATURE RANGE					
Operating Range J		0		+70	°C
Specified Performance A		–40		+85	°C
Automotive Grade*		–40		+125	°C

NOTES

[1]Alignment error is specified as the angle between the true and indicated axis of sensitivity, (see Figure 2).

[2]Transverse sensitivity is measured with an applied acceleration that is 90° from the indicated axis of sensitivity. Transverse sensitivity is specified as the percent of transverse acceleration that appears at the V_{PR} output. This is the algebraic sum of the alignment and the inherent sensor sensitivity errors, (see Figure 2).

[3]Specification refers to the maximum change in parameter from its initial at +25°C to its worst case value at T_{MIN} to T_{MAX}.

[4]Frequency at which response is 3 dB down from dc response assuming an exact C1 value is used. Maximum recommended BW is 6 kHz using a 0.010 µF capacitor, refer to Figure 9.

[5]Applying logic high to the self-test input has the effect of applying an acceleration of –5 *g* to the ADXL05.

[6]Input offset voltage is defined as the output voltage differential from 1.800 V when the amplifier is connected as a follower. The voltage at this pin has a temperature drift proportional to that of the 3.4 V reference.

*Contact factory for availability of automotive grade devices.

All min and max specifications are guaranteed. Typical specifications are not tested or guaranteed.

Specifications subject to change without notice.

ANALOG DEVICES

Monolithic Accelerometer with Signal Conditioning

ADXL50*

FEATURES

Complete Acceleration Measurement System on a Single Monolithic IC
Full-Scale Measurement Range: ±50 *g*
Self-Test on Digital Command
+5 V Single Supply Operation
Sensitivity Precalibrated to 19 mV/*g*
Internal Buffer Amplifier for User Adjustable Sensitivity and Zero-*g* Level
Frequency Response: DC to 10 kHz
Post Filtering with External Passive Components
High Shock Survival: >2000 *g* Unpowered
Other Versions Available: ADXL05 (±5 *g*)

GENERAL DESCRIPTION

The ADXL50 is a complete acceleration measurement system on a single monolithic IC. Three external capacitors and a +5 volt power supply are all that is required to measure accelerations up to ±50 *g*. Device sensitivity is factory trimmed to 19 mV/*g*, resulting in a full-scale output swing of ±0.95 volts for a ±50 *g* applied acceleration. Its zero *g* output level is +1.8 volts.

A TTL compatible self-test function can electrostatically deflect the sensor beam at any time to verify device functionality.

For convenience, the ADXL50 has an internal buffer amplifier with a full 0.25 V to 4.75 V output range. This may be used to set the zero-g level and change the output sensitivity by using external resistors. External capacitors may be added to the resistor network to provide 1 or 2 poles of filtering. No external active components are required to interface directly to most analog-to-digital converters (ADCs) or microcontrollers.

The ADXL50 uses a capacitive measurement method. The analog output voltage is directly proportional to acceleration, and is fully scaled, referenced and temperature compensated, resulting in high accuracy and linearity over a wide temperature range. Internal circuitry implements a forced-balance control loop that improves accuracy by compensating for any mechanical sensor variations.

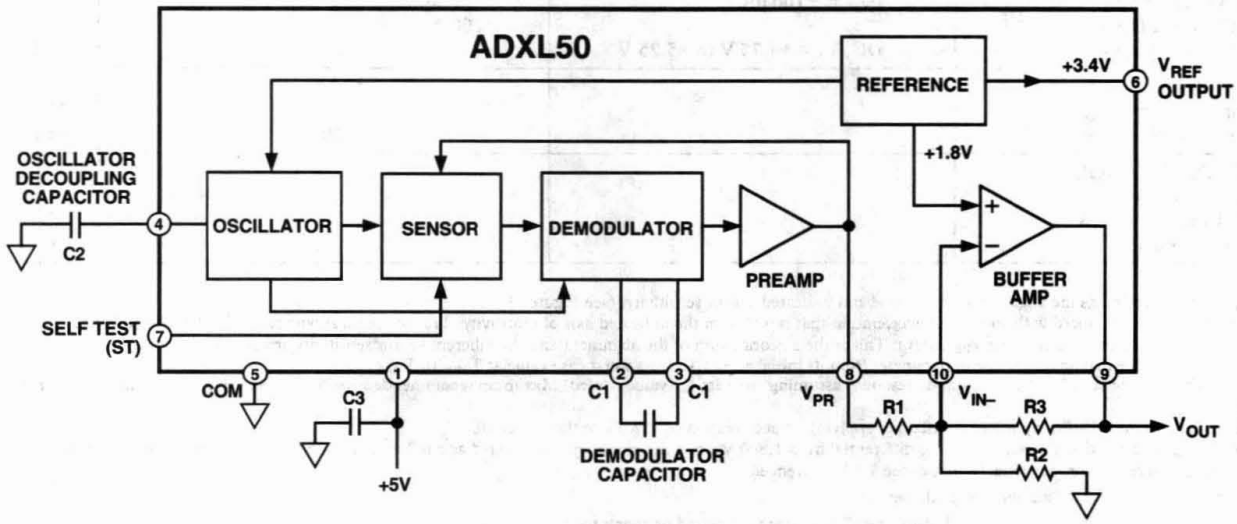
The ADXL50 is powered from a standard +5 V supply and is robust for use in harsh industrial and automotive environments and will survive shocks of more than 2000 *g* unpowered.

The ADXL50 is available in a hermetic 10-pin TO-100 metal can, specified over the 0°C to +70°C commercial, and –40°C to +85°C industrial temperature ranges. Contact factory for availability of devices specified for operation over the –40°C to +105°C automotive temperature range.

ORDERING GUIDE

Model	Temperature Range
ADXL50JH	0°C to +70°C
ADXL50AH	–40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



*Patents pending.

ADXL50–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, T_A = +25°C for J Grade Only, V_S = +5 V, @ Acceleration = 0 *g*, unless otherwise noted)

Parameter	Conditions	ADXL50J/A Min	Typ	Max	Units
SENSOR INPUT					
Measurement Range	Guaranteed Full Scale	–50		+50	*g*
Nonlinearity	Best Fit Straight Line, 50 *g* FS		0.2		% of FS
Alignment Error[1]			±1		Degrees
Transverse Sensitivity[2]			±2		%
SENSITIVITY					
Initial Sensitivity at V_{PR}	+25°C	16.1	19.0	21.9	mV/*g*
Temperature Drift[3]			0.75/1.0		% of Reading
ZERO *g* BIAS LEVEL	at V_{PR}				
Initial Offset		1.55/1.60	1.80	2.05/2.00	V
vs. Temperature[3]			±15/35		mV
vs. Supply	V_S = 4.75 V to 5.25 V		10	32	mV/V
NOISE PERFORMANCE	at V_{PR}				
Voltage Noise Density	BW = 10 Hz to 1 kHz		6.6	12	mg/√Hz
Noise in 100 Hz Bandwidth			66		mg rms
Noise in 10 Hz Bandwidth			20		mg rms
FREQUENCY RESPONSE					
3 dB Bandwidth[4]	C1 = 0.022 µF (See Figure 22)	800	1300		Hz
3 dB Bandwidth[4]	C1 = 0.0068 µF		10		kHz
Sensor Resonant Frequency			24		kHz
SELF TEST INPUT					
Output Change at V_{PR}[5]	ST Pin from Logic "0" to "1"	–0.85	–1.00	–1.15	V
Logic "1" Voltage		2.0			V
Logic "0" Voltage				0.8	V
Input Resistance	To Common		50		kΩ
+3.4 V REFERENCE					
Output Voltage		3.350	3.400	3.450	V
Output Temperature Drift[3]			±10		mV
Power Supply Rejection	DC, V_S = +4.75 V to +5.25 V		1	10	mV/V
Output Current	Sourcing	500			µA
PREAMPLIFIER OUTPUT					
Voltage Swing		0.25		V_S – 1.4	V
Current Output	Source or Sink	30	80		µA
Capacitive Load Drive			100		pF
BUFFER AMPLIFIER					
Input Offset Voltage[6]	Delta from Nominal 1.800 V		±10	±25	mV
Input Bias Current			5	20	nA
Open-Loop Gain	DC		80		dB
Unity Gain Bandwidth			200		kHz
Output Voltage Swing	I_{OUT} = ±100 µA	0.25		V_S – 0.25	V
Capacitive Load Drive		1000			pF
Power Supply Rejection	DC, V_S = +4.75 V to +5.25 V		1	10	mV/V
POWER SUPPLY					
Operating Voltage Range		4.75		5.25	V
Quiescent Supply Current			10	13	mA
TEMPERATURE RANGE					
Operating Range J		0		+70	°C
Specified Performance A		–40		+85	°C
Automotive Grade*		–40		+125	°C

NOTES

[1]Alignment error is specified as the angle between the true and indicated axis of sensitivity, (see Figure 2).

[2]Transverse sensitivity is measured with an applied acceleration that is 90° from the indicated axis of sensitivity. Transverse sensitivity is specified as the percent of transverse acceleration that appears at the V_{PR} output. This is the algebraic sum of the alignment and the inherent sensor sensitivity errors, (see Figure 2).

[3]Specification refers to the maximum change in parameter from its initial at +25°C to its worst case value at T_{MIN} to T_{MAX}.

[4]Frequency at which response is 3 dB down from dc response assuming an exact C1 value is used. Maximum recommended BW is 10 kHz using a 0.007 µF capacitor, refer to Figure 22.

[5]Applying logic high to the self-test input has the effect of applying an acceleration of –52.6 *g* to the ADXL50.

[6]Input offset voltage is defined as the output voltage differential from 1.800 V when the amplifier is connected as a follower (i.e., Pins 9 and 10 tied together). The voltage at Pin 9 has a temperature drift proportional to that of the 3.4 V reference.

*Contact factory for availability of automotive grade devices.

All min and max specifications are guaranteed. Typical specifications are not tested or guaranteed.

Specifications subject to change without notice.

Analog Audio Components
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SSM2120/SSM2122 – Dynamic Range Processors/Dual VCAs	16–13
SSM2125/SSM2126 – Dolby Pro-Logic Surround Matrix Decoders	16–15
SSM2135 – Dual Single-Supply Audio Operational Amplifier	16–17
SSM2141 – High Common-Mode Rejection Differential Line Receiver	16–19
SSM2142 – Balanced Line Driver	16–21
SSM2143 – –6 dB Differential Line Receiver	16–23
SSM2160/SSM2161 – 6- and 4-Channel, "Clickless" Serial Input Balance/Master Volume Controls	16–25
SSM2163 – Digitally Controlled 8 × 2 Audio Mixer	16–27
SSM2164 – Low Cost Quad Voltage Controlled Amplifier	16–29
SSM2166 – Microphone Preamplifier with Variable Compression & Noise Gating	16–31
SSM2402/SSM2412 – Dual Audio Analog Switches	16–33
SSM2404 – Quad Audio Switch	16–35

Analog Audio Components–Selection Guides

Model	e_{NOISE} @ 20 kHz µV p-p	SNR dBu	THD+N @ 1 kHz %	CMRR dB	Gain BW MHz	Slew Rate µs	# Pins	Page No.	Comments	Fax-code
Low Noise Preamplifier										
SSM2017	0.95	–121	0.001	87	4	NS	8/16	16–9	A_V = 1 to 1000	1782
Microphone PreAmp										
SSM2165	2 µV rms	–112	–25%	NA	20	NS	8	*	With Variable Compression, Preset Noise Gating	1995
SSM2166	14 µV/√Hz	–112	–25%	NA	20	NS	14	16–31	With Variable Compression and Noise Gating	1956
Differential Line Receiver										
SSM2141	22	100	0.001	80	3	NS	8	16–19	Gain = 0 dB	1796
SSM2143	23.6	107.3	0.0006	70	7	6	8	16–23	Gain = –6 dB	1797
Balanced Line Driver										
SSM2142	117	93.4	0.006	NA	NS	NS	8	16–21	10 V rms into 600 ohm	1798
AD815					100	900	15	10–49	30 V_{LL} into 8 ohms, Diff Input	1938
Operational Amplifiers										
Singles										
OP176	6	NS	0.001	80	10	15	8	10–127	Butler Input Stage	1673
AD797	7.7	NS	–120 dB	114	8	20	8	10–39	Ultralow Noise & Distortion	1394
SSM2211								*	1 Watt Power Amp	1979
BUF04	2	100	0.001	NA	110	3000	8	10–109	Unity Gain Buffer	1613
SSM2135	5.2	121	0.003	87	3.5	0.6	8	16–17	Single Supply +4 V to ±18 V	1794
Duals										
OP275	7	NS	0.0006	80	9	15	8	10–149	Butler Input Stage	1619
OP285	7	NS	0.001	80	9	15	8	10–155	Butler Input Stage. Good DC Specs	1694
OP279	22	NS	0.01	70	5	13	8	10–151	±5 V, Rail-to-Rail In/Out	1811

Note: See Section 10 for other amplifiers recommended for audio.
*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Digital Volume Control, Mixer

Model	e_{NOISE} @ 20 kHz BW	Head Room % THD+N	THD+N A_V=0	THD+N A_V=10 dB	CH Separation dB	Digital Section Master Range	Digital Section Channel Range	# Pins	Page No.	Comments	Fax-code
SSM2160	–160 dBu	+10	0.008	0.02	80	0 to –60 dB	0 to +20 dB	24	16–25	6 Channel "Clickless"	1848
SSM2161	–160 dBu	+10	0.008	0.02	80	0 to –60 dB	0 to +20 dB	20	16–25	4 Channel "Clickless"	1848
SSM2163	–82 dBu	+10	0.03		(See Data Sheet for Specs)			28	16–27	8 Input, 2 Output Audio Mixer	1954

Surround Matrix Decoders

Model	Power Supply Volts	Channel Separation Center to Left, Right Outputs dB	Channel Separation All Other Combinations dB	THD All Channels %	SNR dB	Auto Balance Capture Range dB	# Pins	Page No.	Comments	Fax-code
SSM2125†	+12 @ 50 mA	35	25	0.1	–83	±3	48	16–15	Must Be a Dolby† Licensee to Purchase	1790
SSM2126†	+12 @ 50 mA	25	25	0.1	–80	±3.8	48	16–15	Must Be a Dolby Licensee to Purchase	1790
SSM2005‡	(See Data Sheet for Specs. 5:1, 5:2:5-Channel Circle Surround‡ Decoder.)							16–7	No License Fee/No Royalty	1965

Stereo Noise Reduction: HUSH¶

SSM2000	25 dB Noise Reduction "Single Ended" (Works with any Audio Source) Effectively Decodes Dolby Encoded Sources, 0.02 THD @ 1 kHz	16–5	+7 V to +18 V Supply Voltage 100 dB Dynamic Range	1952

†Dolby is a registered trademark of Dolby Laboratories, Inc., (SSM2125, SSM2126).
‡Circle Surround is a registered trademark of Rocktron Corporation (SSM2005).
¶HUSH is a registered trademark of Hush Systems (SSM2000).

Analog Audio Components–Selection Guides

VCA, Voltage Controlled Amplifiers

Model	V_{SS} Volts	Gain Range dB	–3 dB BW MHz	Input Spectral Noise nV√Hz	Input Resistance Ω	Slew Rate V/µs	# Pins	Page No.	Comments	Fax-code
Singles										
SSM2018T	±5 to ±18	–100–+40	0.7	–93 dBu	4M	10	16	16–11	THD = 0.006%, Voltage Out	1784
SSM2118T	@ 15 mA	–100–+40	0.7	–93 dBu	4M	10	16	16–11	THD = 0.006%, Current Out	1784
Quads										
SSM2024	±15 @ 2 mA	–82–+2	0.5	NS	R_{EXT}	NS	16	*	THD = 0.3%, Current In/Out	1785
SSM2164	±4–+18	–94–+20	0.5	–94 dBu	R_{EXT}	0.7	16	16–29	THD = 0.1%, Current In/Out	1849
Duals										
SSM2120/SSM2122	±5–±18	100	0.25	–80 dBu	36K	NS	20/16	16–13	SSM2120, 2-Level Detectors	1788

J-FET "Clickless" Audio Switches

Model	Type	Rails for Specs	I_{DD} max mA	I_{SS} max mA	R_{ON} max Ohms	t_{ON} ms	t_{OFF} ms	# Pins	Page No.	Comments	Fax-code
SSM2402/SSM2412	2 SPST	±12 V	6	7.5	85	10/3.5	4/1.5	16	16–33	Off Isolation 120 dB	1801
SSM2404	4 SPST	±12 V	0.6	0.9	28		30	16	16–35	THD+N = 0.0008%	1802

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

HUSH Stereo Noise Reduction System with Adaptive Threshold

SSM2000

FEATURES

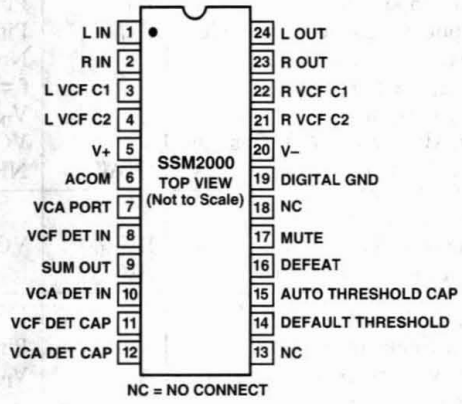
- Up to 25 dB of Noise Reduction from Virtually Any Audio Source without Sonic Artifacts
- "Single-Ended" Operation Eliminates Need for Encode-Decode Process
- Adaptive Threshold Dynamically Adjusts to Changing Nominal Signal Levels
- Effectively Decodes Dolby B® Encoded Sources
- Direct VCA Control Port Access for Additional Level Control Functionality
- Logic-Controllable Bypass and Muting
- 100 dB Dynamic Range (Noise Reduction OFF)
- 0.02% Typical THD+N (@ 1 kHz, Noise Reduction OFF)
- +7 V to +18 V Operation
- No Royalty Requirements

APPLICATIONS

- Auto Radio Sound Processing
- Multimedia PC Sound Cards
- Television Sound Processing
- Cassette Tape Players
- AM/FM Receivers
- Telephone & Wireless Links
- Professional Audio

PIN CONFIGURATION

24-Lead Plastic DIP
24-Lead SOIC

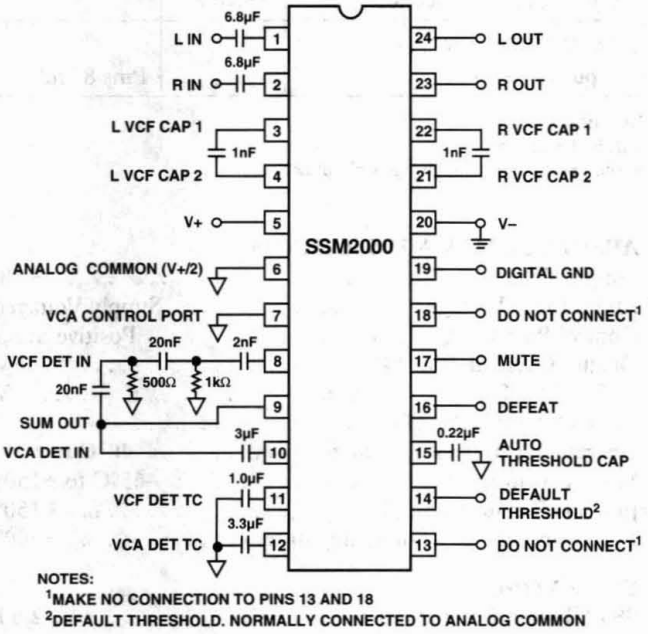


NC = NO CONNECT

GENERAL DESCRIPTION

The SSM2000 is an advanced audio noise reduction system based on proprietary HUSH® circuitry. HUSH combines a dynamic filter and downward expander to provide a high level of effectiveness without the sonic artifacts normally associated with noise reduction systems. In addition, an Adaptive Threshold circuit detects nominal signal levels and dynamically adjusts both thresholds, thereby providing optimal results regardless of program source. Since it is a single-ended system, HUSH can be used on virtually any audio source, including audio and video tapes, radio and television broadcasts, or any other source with objectionable noise. The SSM2000 can be used with Dolby B encoded sources with excellent results. A key feature is direct access to the Voltage Controlled Amplifier port enabling additional functions such as dc volume control, automatic leveling, compression, etc. with minimal external circuitry.

Dolby B is a registered trademark of Dolby Laboratories, Inc.
HUSH is a registered trademark of Rocktron Corporation.



NOTES:
[1]MAKE NO CONNECTION TO PINS 13 AND 18
[2]DEFAULT THRESHOLD. NORMALLY CONNECTED TO ANALOG COMMON

Figure 1. Typical Basic Application

SSM2000–SPECIFICATIONS (V_S = +8.5 V, ACOM = V_S/2, f = 1 kHz, R_L = 100 kΩ, 0 dBu = 0.775 V rms. T_A = +25°C, Noise Reduction and Adaptive Threshold enabled (Pin 14 at V_S/2), unless otherwise noted.)

Parameter	Symbol	Conditions	SSM2000 Min	SSM2000 Typ	SSM2000 Max	Units
AUDIO SIGNAL PATH						
Signal-to-Noise Ratio	SNR	V_{IN} = 0 V, 20 Hz to 20 kHz (Flat)	80	86		dB
Headroom	HR	Clip Point, THD = 1%		4.5		dBu
Dynamic Range		Clipping to Noise Floor		91		dB
Total Harmonic Distortion	THD+N	V_{IN} = 300 mV rms, 2nd & 3rd Harmonics[1]		0.02	0.04	%
Effective Noise Reduction		20 kHz Bandwidth (Flat)				
		Downward Expander Section		15		dB
		Dynamic Filter Section		10		dB
Input Impedance	Z_{IN}	Pins 1 and 2	6	8		kΩ
Output Impedance, Dynamic	Z_{OUT}	Pins 23 and 24		7		Ω
Capacitive Load		No Oscillation		300		pF
Channel Separation		f = 1 kHz, V_{IN} = 300 mV rms		60		dB
Mute Output		V_{IN} = 300 mV rms		–85		dB
Gain Matching, L & R Channels		VCA at A_V = 0 dB		±1		dB
Gain Bandwidth	GBW	NR Disabled		37		kHz
DYNAMIC FILTER						
Minimum Bandwidth	BW_{MIN}	VCF C = 0.001 µF		3		kHz
Maximum Bandwidth	BW_{MAX}			37		kHz
VCA CONTROL PORT						
Input Impedance		Pin 7		3.8		kΩ
VCA Voltage Gain Range	A_V	V_{IN} = 300 mV rms (Pin 7 = 2.0 V & 0 V)	–70		+1	dB
Gain Constant			20	22	26	mV/dB
Control Feedthrough		Pin 7		1	10	mV
POWER SUPPLY						
Voltage Range	V_S		+7.0		18	V
Supply Current	I_{SY}			7.5	11	mA
Power Supply Rejection	PSRR+			70		dB
VCA, VCF DETECTOR						
Input Impedance	R_{IN}	Pins 8 and 10	4.0	5.4	7.0	kΩ

NOTES
[1]NR in defeat mode.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +18 V
Audio Input Voltage ..... Supply Voltage(s)
Control Port Voltage (Pin 7) ..... Positive Supply
Default Override (Pin 14) ..... V+
Defeat (Pin 16) ..... V+
Mute Override (Pin 17) ..... V+
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

ESD RATINGS

883 (Human Body) Model ..... 2.5 kV
EIAJ Model ..... 300 V

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2000P	–40°C to +85°C	24-Pin Plastic DIP	N-24
SSM2000S	–40°C to +85°C	24-Pin SOIC	SOL-24

*For outline information see Package Information section.

THERMAL CHARACTERISTICS

Package Type	θ_{JA}[1]	θ_{JC}	Units
24-Pin Plastic DIP (P)	54	27	°C/W
24-Pin SOIC (S)	72	24	°C/W

NOTE
[1]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered onto a circuit board for surface mount packages.

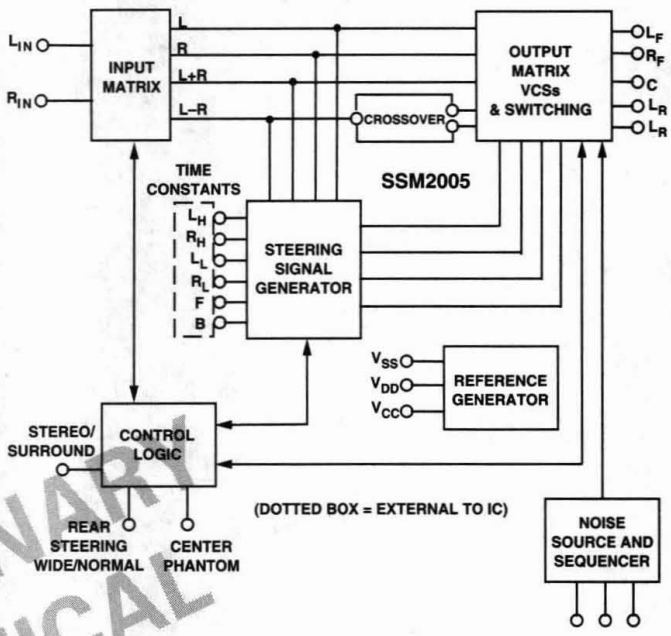
Circle Surround 5-Channel Soundfield Generator

SSM2005

FEATURES

- Generates True 5-Channel Soundfield
- No Pre-Encoding Required—Only Stereo L and R
- Excellent Surround Image At All Positions
- Superior Sound in Automobiles
- Distinct Left Rear vs. Right Rear, Full Bass Response
- No Delay Required—Natural Ambiance Preserved
- 4 or 5 Speaker Operation
- Full Bandwidth on All Channels
- Optimized for Music Reproduction
- Superior Decoding of Dolby* Surround Material
- Excellent Decoding of "Pre-Encoded" Sources
- Usable in Home Theater and Video Games
- +7 V to +20 V Operation

CIRCLE SURROUND SYSTEM BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSM2005 Circle Surround† 5-Channel Soundfield Generator produces a true 5-channel surround soundfield using only standard unencoded left/right stereo sources. Left front, right front, center, and differentiated left and right rear channels are generated providing a realistic ambiance effect with either 4 or 5 speaker configurations. Unlike previous designs, Circle Surround is optimized for music reproduction with full bandwidth on all channels and proper separation of the front channels. The differentiated rear channels provide excellent imaging, especially in automotive applications. Listener position is not critical; well-balanced sound is obtained anywhere within the soundfield.

The Circle Surround process does not require the audio signal to be encoded, as it uses the ambiance and directional information already present in the original media to generate the multidimensional effects. Circle Surround does not add any artificial ambiance or reverberation, nor does it require any delay generators. The fully differentiated rear channels provide rear stereo separation for enhanced spacial perception while maintaining full bass response, especially important in automotive applications.

PRELIMINARY TECHNICAL DATA

*Dolby is a registered trademark of Dolby Laboratories, Inc.
†Circle Surround is a registered trademark of Rocktron Corporation and is protected by patents granted and applied for.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ANALOG DEVICES

Self-Contained Audio Preamplifier

SSM2017

FEATURES

- Excellent Noise Performance: 950 pV/√Hz or 1.5 dB Noise Figure
- Ultralow THD: < 0.01% @ G = 100 Over the Full Audio Band
- Wide Bandwidth: 1 MHz @ G = 100
- High Slew Rate: 17 V/μs typ
- Unity Gain Stable
- True Differential Inputs
- Subaudio 1/f Noise Corner
- 8-Pin Mini-DIP with Only One External Component Required
- Very Low Cost
- Extended Temperature Range: –40°C to +85°C

APPLICATIONS

- Audio Mix Consoles
- Intercom/Paging Systems
- Two-Way Radio
- Sonar
- Digital Audio Systems

GENERAL DESCRIPTION

The SSM2017 is a latest generation audio preamplifier combining SSM preamplifier design expertise with advanced processing. The result is excellent audio performance from a self-contained 8-pin mini-DIP device, requiring only one external gain set resistor or potentiometer. The SSM2017 is further enhanced by its unity gain stability.

Key specifications include ultralow noise (1.5 dB noise figure) and THD (<0.01% at G = 100), complemented by wide bandwidth and high slew rate.

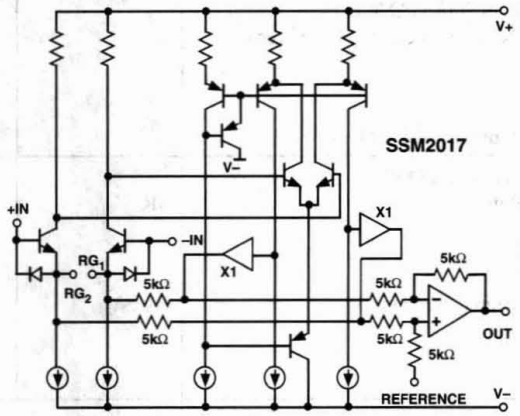
Applications for this low cost device include microphone preamplifiers and bus summing amplifiers in professional and consumer audio equipment, sonar, and other applications requiring a low noise instrumentation amplifier with high gain capability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Input Voltage	Supply Voltage
Output Short Circuit Duration	10 sec
Storage Temperature Range (P, Z Packages)	–65°C to +150°C
Junction Temperature (T_J)	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	–40°C to +85°C
Thermal Resistance*	
8-Pin Hermetic DIP (Z): θ_{JA} = 134; θ_{JC} = 12	°C/W
8-Pin Plastic DIP (P): θ_{JA} = 96; θ_{JC} = 37	°C/W
16-Pin SOIC (S): θ_{JA} = 92; θ_{JC} = 27	°C/W

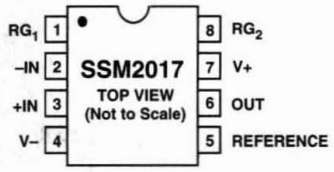
*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

FUNCTIONAL BLOCK DIAGRAM

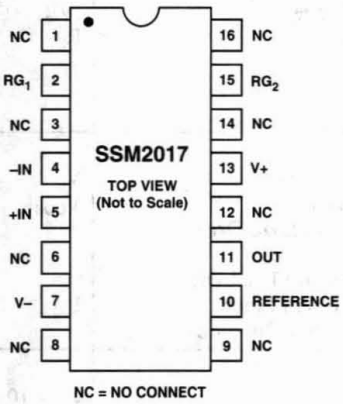


PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)



16-Pin Wide Body SOL (S Suffix)



ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option[2]
SSM2017P	–40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2017S	–40°C to +85°C	16-Lead SOL	R-16
SSM2017S-REEL	–40°C to +85°C	16-Lead SOL	R-16

NOTES
[1]XIND = –40°C to +85°C.
[2]For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

SSM2017—SPECIFICATIONS

(V_S = ±15 V and –40°C ≤ T_A ≤ +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DISTORTION PERFORMANCE		T_A = +25°C V_O = 7 V rms R_L = 5 kΩ				
Total Harmonic Distortion Plus Noise	THD+N	G = 1000, f = 1 kHz		0.012		%
		G = 100, f = 1 kHz		0.005		%
		G = 10, f = 1 kHz		0.004		%
		G = 1, f = 1 kHz		0.008		%
NOISE PERFORMANCE						
Input Referred Voltage Noise Density	e_n	f = 1 kHz, G = 1000		0.95		nV/√Hz
		f = 1 kHz; G = 100		1.95		nV/√Hz
		f = 1 kHz; G = 10		11.83		nV/√Hz
		f = 1 kHz; G = 1		107.14		nV/√Hz
Input Current Noise Density	i_n	f = 1 kHz, G = 1000		2		pA/√Hz
DYNAMIC RESPONSE						
Slew Rate	SR	G = 10 R_L = 4.7 kΩ C_L = 50 pF T_A = +25°C	10	17		V/µs
Small Signal Bandwidth	$BW_{-3\ dB}$	G = 1000		200		kHz
		G = 100		1000		kHz
		G = 10		2000		kHz
		G = 1		4000		kHz
INPUT						
Input Offset Voltage	V_{IOS}			0.1	1.2	mV
Input Bias Current	I_B	V_{CM} = 0 V		6	25	µA
Input Offset Current	Ios	V_{CM} = 0 V		±0.002	±2.5	µA
Common-Mode Rejection	CMR	V_{CM} = ±8 V				
		G = 1000	80	112		dB
		G = 100	60	92		dB
		G = 10	40	74		dB
		G = 1, T_A = +25°C	26	54		dB
		G = 1, T_A = – 40°C to +85°C	20	54		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V				
		G = 1000	80	124		dB
		G = 100	60	118		dB
		G = 10	40	101		dB
		G = 1	26	82		dB
Input Voltage Range	IVR		±8			V
Input Resistance	R_{IN}	Differential, G = 1000		1		MΩ
		G = 1		30		MΩ
		Common Mode, G = 1000		5.3		MΩ
		G = 1		7.1		MΩ
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ; T_A = +25°C	±11.0	±12.3		V
Output Offset Voltage	V_{OOS}			–40	500	mV
Minimum Resistive Load Drive		T_A = +25°C		2		kΩ
		T_A = –40°C to +85°C		4.7		kΩ
Maximum Capacitive Load Drive				50		pF
Short Circuit Current Limit	I_{SC}	Output-to-Ground Short		±50		mA
Output Short Circuit Duration					10	sec
GAIN						
Gain Accuracy	$R_G = \frac{10\ k\Omega}{G-1}$	T_A = +25°C				
		R_G = 10 Ω, G = 1000		0.25	1	dB
		R_G = 101 Ω, G = 100		0.20	1	dB
		R_G = 1.1 kΩ, G = 10		0.20	1	dB
		R_G = ∞, G = 1		0.05	0.5	dB
Maximum Gain	G			70		dB
REFERENCE INPUT						
Input Resistance				10		kΩ
Voltage Range				±8		V
Gain to Output				1		V/V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±22	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±10.6	±14.0	mA

Specifications subject to change without notice.

Trimless Voltage Controlled Amplifiers

SSM2018T/SSM2118T*

FEATURES

- 117 dB Dynamic Range
- 0.006% Typical THD+N (@ 1 kHz, Unity Gain)
- 140 dB Gain Range
- No External Trimming Required
- Differential Inputs
- Complementary Gain Outputs
- Buffered Control Port
- I–V Converter On-Chip (SSM2018T)
- Differential Current Outputs (SSM2118T)
- Low External Parts Count
- Low Cost

GENERAL DESCRIPTION

The SSM2018T and SSM2118T represent continuing evolution of the Frey Operational Voltage Controlled Element (OVCE) topology that permits flexibility in the design of high performance volume control systems. Voltage (SSM2018T) and differential current (SSM2118T) output versions are offered, both laser-trimmed for gain core symmetry and offset. As a result, the SSM2018T is the first professional audio quality VCA to offer trimless operation. The SSM2118T is ideal for low noise summing in large VCA based systems.

Due to careful gain core layout, the SSM2018T/SSM2118T combine the low noise of Class AB topologies with the low distortion of Class A circuits to offer an unprecedented level of sonic transparency. Additional features include differential inputs, a 140 dB gain range, and a high impedance control port. The SSM2018T provides an internal current-to-voltage converter; thus no external active components are required. The SSM2118T has fully differential current outputs that permit high noise-immunity summing of multiple channels.

Both devices are offered in 16-pin plastic DIP and SOIC packages and guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.

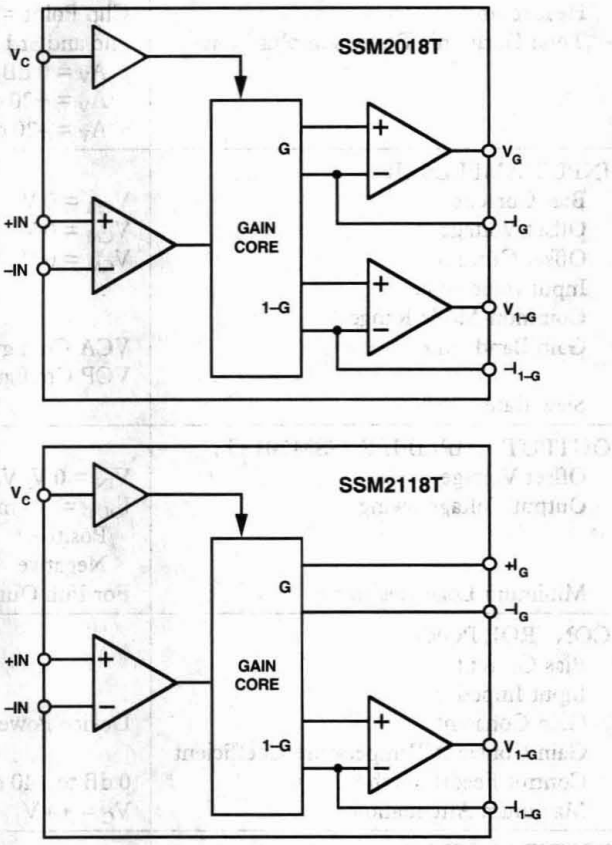
ORDERING GUIDE

Model	Temperature Range	Package Option*
SSM2018TP	–40°C to +85°C	N-16
SSM2018TS	–40°C to +85°C	R-16
SSM2118TP	–40°C to +85°C	N-16
SSM2118TS	–40°C to +85°C	R-16

*N = Plastic DIP; R = SOL. For outline information see Package Information section.

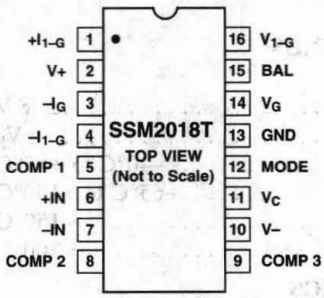
†Protected by U.S. Patent Nos. 4,471,320 and 4,560,947.

FUNCTIONAL BLOCK DIAGRAMS

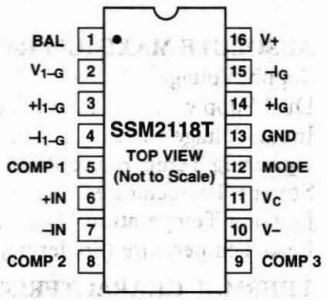


PIN CONFIGURATIONS

16-Lead Plastic DIP and SOL



16-Lead Plastic DIP and SOL



SSM2018T/SSM2118T–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS [V_S = ±15 V, A_V = 0 dB, R_L = 100 kΩ, f = 1 kHz, 0 dBu = 0.775 V rms, simple VCA application circuit with 18 kΩ resistors, $-V_{IN}$ floating, and Class AB gain core bias (R_B = 150 kΩ), –40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.]

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE[1]					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–95	–93	dBu
Headroom	Clip Point = 1% THD+N		+22		dBu
Total Harmonic Distortion plus Noise	2nd and 3rd Harmonics Only (+25°C to +85°C)				
	A_V = 0 dB, V_{IN} = +10 dBu		0.006	0.025	%
	A_V = +20 dB, V_{IN} = –10 dBu		0.013	0.04	%
	A_V = –20 dB, V_{IN} = +10 dBu[2]		0.013	0.04	%
INPUT AMPLIFIER					
Bias Current	V_{CM} = 0 V		0.25	1	µA
Offset Voltage	V_{CM} = 0 V		1	15	mV
Offset Current	V_{CM} = 0 V		10	100	nA
Input Impedance			4		MΩ
Common-Mode Range			±13		V
Gain Bandwidth	VCA Configuration		0.7		MHz
	VCP Configuration		14		MHz
Slew Rate			5		V/µs
OUTPUT AMPLIFIER (SSM2018T)					
Offset Voltage	V_{IN} = 0 V, V_C = +4 V		1.0	15	mV
Output Voltage Swing	I_{OUT} = 1.5 mA				
	Positive	+10	+13		V
	Negative	–10	–14		V
Minimum Load Resistance	For Full Output Swing		9		kΩ
CONTROL PORT					
Bias Current			0.36	1	µA
Input Impedance			1		MΩ
Gain Constant	Device Powered in Socket > 60 sec		–30		mV/dB
Gain Constant Temperature Coefficient			–3500		ppm/°C
Control Feedthrough	0 dB to –40 dB Gain Range		±1	±4	mV
Maximum Attenuation	V_C = +4 V		100		dB
POWER SUPPLIES					
Supply Voltage Range		±5		±18	V
Supply Current			11	15	mA
Power Supply Rejection Ratio			80		dB

NOTES
[1]SSM2118T tested and characterized using OP275 as current-to-voltage converter, see figure next page.
[2]Guaranteed by characterization data and testing at A_V = 0 dB.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
Dual Supply . . . . . ±18 V
Input Voltage . . . . . $\pm V_S$
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

THERMAL CHARACTERISTICS

Thermal Resistance[2]
16-Pin Plastic DIP
θ_{JA} . . . . . 76°C/W
θ_{JC} . . . . . 33°C/W
16-Pin SOIC
θ_{JA} . . . . . 92°C/W
θ_{JC} . . . . . 27°C/W

TRANSISTOR COUNT

Number of Transistors
SSM2018T 125
SSM2118T 108

ESD RATINGS

883 (Human Body) Model . . . . . 500 V
EIAJ Model . . . . . 100 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

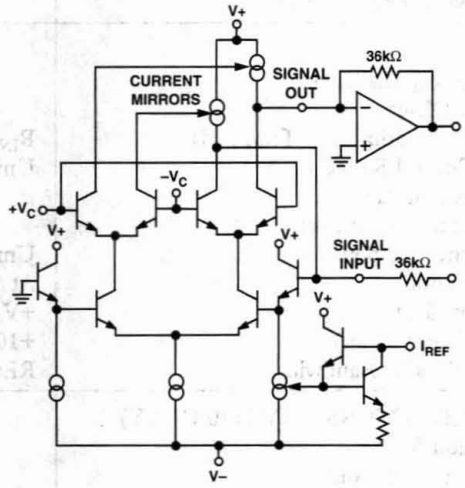
Dynamic Range Processors/Dual VCAs

SSM2120/SSM2122

FEATURES
- 0.01% THD at +10 dBV In/Out
- 100 dB VCA Dynamic Range
- Low VCA Control Feedthrough
- 100 dB Level Detection Range
- Log/Antilog Control Paths
- Low External Component Count

APPLICATIONS
- Compressors
- Expanders
- Limiters
- AGC Circuits
- Voltage-Controlled Filters
- Noise Reduction Systems
- Stereo Noise Gates

FUNCTIONAL BLOCK DIAGRAM

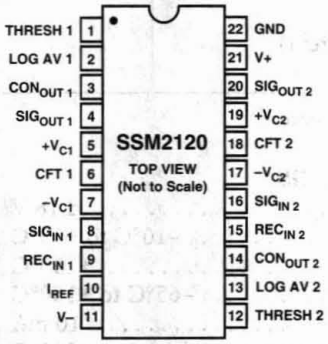


GENERAL DESCRIPTION

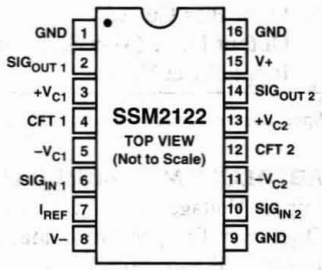
The SSM2120 is a monolithic integrated circuit designed for the purpose of processing dynamic signals in various analog systems including audio. This "dynamic range processor" consists of two VCAs and two level detectors (the SSM2122 consists of two VCAs only). These circuit blocks allow the user to logarithmically control the gain or attenuation of the signals presented to the level detectors depending on their magnitudes. This allows the compression, expansion or limiting of ac signals, some of the primary applications for the SSM2120.

PIN CONNECTIONS

22-Pin Plastic DIP (P Suffix)



16-Pin Plastic DIP (P Suffix)



SSM2120/SSM2122–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@V_S = ±15 V, T_A = +25°C, I_{REF} = 200 µA, $+V_C = -V_C$ = GND (A_V = 0 dB). 0 dB = 1 V rms unless otherwise noted)

Parameter	Conditions	SSM2120/SSM2122 Min	Typ	Max	Units
POWER SUPPLY					
Supply Voltage Range		±5		±18	V
Positive Supply Current			8	10	mA
Negative Supply Current			–6	–8	mA
VCAs					
Max I_{SIGNAL} (In/Out)		±300	±325	±350	µA
Output Offset			±1	±8	µA
Control Feedthrough (Trimmed)	$R_{IN} = R_{OUT}$ = 36 kΩ, –30 dB ≤ A_V ≤ 0 dB		±750		µV
Gain Control Range	Unity-Gain	–85		+40	dB
Control Sensitivity			6		mV/dB
Gain Scale Factor Drift			–3300		ppm/°C
Frequency Response	Unity Gain or Less		250		kHz
Off Isolation	At 1 kHz		100		dB
Current Gain	$+V_C = -V_C$ = 0 V	–0.5		+0.5	dB
THD (Unity-Gain)	+10 dBV IN/OUT		0.005	0.04	%
Noise (20 kHz Bandwidth)	RE: 0 dBV		–80		dB
LEVEL DETECTORS (SSM2120 ONLY)					
Detection Range		90	95		dB
Input Current Range		0.085		2800	µA p-p
Rectifier Input Bias Current			4		nA
Output Sensitivity (At LOG AV Pin)			3		mV/dB
Output Offset Voltage			±0.5	±3.4	mV
Frequency Response					
I_{IN} = 1 mA p-p			1000		
I_{IN} = 10 µA p-p			50		kHz
I_{IN} = 1 µA p-p			7.5		
CONTROL AMPLIFIERS (SSM2120 ONLY)					
Input Bias Current			±85	±175	nA
Output Drive (Max Sink Current)		5.0	7.5		mA
Input Offset Voltage			±0.5	±4.2	mV

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18 V
Operating Temperature Range ..... –10°C to +55°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Maximum Current into Any Pin ..... 10 mA
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
16-Pin Plastic DIP (P)	86	10	°C/W
22-Pin Plastic DIP (P)	70	7	°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2120P	–10°C to +50°C	22-Pin Plastic DIP	N-22
SSM2122P	–10°C to +50°C	16-Pin Plastic DIP	N-16

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2120/SSM2122 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Dolby Pro-Logic Surround Matrix Decoders

SSM2125/SSM2126

FEATURES

- Noise Generator and Autobalance Circuits are Contained On-Chip
- Autobalance On/Off Control
- 4-Channel Pro-Logic and Dolby 3 (Surround Channel Defeat) Modes Available
- Selectable Center Channel Modes – Normal, Wideband, Phantom, Off
- Direct Path Bypass (Normal 2-Channel Stereo Mode)
- Wide Channel Separation
  - Center to Left, Right Channels – 35 dB min (SSM2125)
  - Any Channel to Another – 25 dB min (SSM2126)
- Wide Dynamic Range – 103 dB typ
- Low Total Harmonic Distortion – 0.02% typ
- Available in a 48-Pin Plastic DIP
- CMOS and TTL Compatible Control Logic

APPLICATIONS

- Direct View and Projection TV
- Integrated A/V Amplifiers
- Laserdisc and CD-V Players
- Video Cassette Recorders
- Stand-Alone Surround Decoders
- Home Satellite Receiver/Descramblers

GENERAL DESCRIPTION

The SSM2125 and SSM2126 are Dolby* Pro-Logic Surround Decoders developed to provide multichannel outputs from Dolby Surround encoded stereo sources.

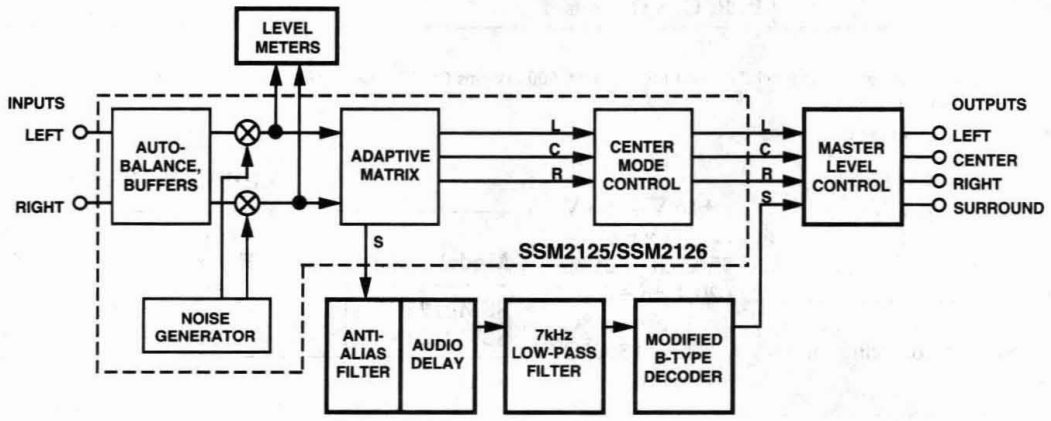
Over 2000 major films and an increasing number of broadcasts are available in Dolby Surround. Surround encoding is preserved in the stereo audio tracks of normal video discs, video cassettes, and television broadcasts, permitting the decoding to multichannel audio in the home.

Major design considerations of the SSM2125/SSM2126 are excellent audio performance and a high level of integration. In addition to the Adaptive Matrix and Center Mode Control, also included on-chip are the Automatic Balance Control and Noise Generator functions. A complete Pro-Logic system can be realized using the SSM2125/SSM2126 and few external components. Using SSM's extensive experience in the design of professional audio integrated circuits, the SSM2125/SSM2126 offers typical 103 dB dynamic range and 0.025% THD. A direct path bypass mode allows normal stereo operation with high fidelity without the need for external switching or parallel signal paths.

The SSM2125 is a premium grade that is selected to a minimum channel separation specification of 35 dB for the center to left and right channels, and 25 dB for the remaining channels. The standard grade, the SSM2126, provides minimum channel separation of 25 dB from any channel to another.

The SSM2125/SSM2126 is available only to licensees of Dolby Licensing Corporation, San Francisco, California, from whom licensing and application information must be obtained.

FUNCTIONAL BLOCK DIAGRAM



*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation, San Francisco, California.

SSM2125/SSM2126–SPECIFICATIONS

(V_S = ±6 V, T_A = +25°C, V_{IN} = 0 dBd at 1 kHz,[1] Center Mode Control: Wide, unless otherwise noted.)

Parameter	Symbol	Conditions	SSM2125 Min	SSM2125 Typ	SSM2125 Max	SSM2126 Min	SSM2126 Typ	SSM2126 Max	Units
CHANNEL SEPARATION									
Center		C Input; R, L Outputs	35	48		25	35		dB
		C Input; S Output	25	35		25	35		dB
Right		R Input; L, C, S Outputs	25	35		25	35		dB
Left		L Input; C, R, S Outputs	25	35		25	35		dB
Surround		S Input; L, R, C Outputs	25	35		25	35		dB
CHANNEL OUTPUT LEVEL		V_{IN} = 0 dB; L, R, C, S Output			±0.5			±0.5	dBd
TOTAL HARMONIC DISTORTION	THD	All Channels		0.02	0.1		0.02	0.1	%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V, CCIR2K/ARM All Channels	–83	–87		–80	–87		dBd
HEADROOM	HR	Clipping = 3% THD All Channels	15	16		15	16		dBd
BYPASS MODE DYNAMIC RANGE		Clipping to Noise Floor		104			104		dB
NOISE SOURCE OUTPUT LEVEL		All Channels		–13.5			–13.5		dBd
NOISE SOURCE OUTPUT LEVEL MATCHING		Any Channel to Another		I			1		dB
AUTOBALANCE CAPTURE RANGE			±3	±3.8	±6		±3.8		dB
LOGIC THRESHOLD HI		Relative to L_{REF}	+2.4				+2.4		V
LO					+0.8			+0.8	V
OPERATING SUPPLY VOLTAGE	V_S	Single Supply		+12			+12		V
		Dual Supply		±6			±6		V
SUPPLY CURRENT	I_{SY}	No Input Signal		40	50		40	50	mA
INPUT IMPEDANCE	Z_{IN}	L, R Inputs		5			5		kΩ
OUTPUT IMPEDANCE	Z_{OUT}	L, R, C, S Outputs		600			600		Ω

NOTE
[1]0 dBd = 500 mV rms Dolby level output at any channel; Left and Right inputs: 500 mV rms (0 dBd); Center input: L = R = 354 mV rms (–3 dBd); Surround input: L = –R = 354 mV rms (–3 dBd).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +16 V or ±8 V
Logic Inputs . . . . . V+ to V–
Storage Temperature Range . . . . . –55°C to +125°C
Operating Temperature Range . . . . . –20°C to +70°C
Junction Temperature . . . . . +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C
Thermal Resistance[1]
θ_{JA} . . . . . 38°C/W
θ_{JC} . . . . . 14°C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., device in socket.

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
SSM2125XXXP[2]	–20°C to +70°C	48-Pin P-DIP
SSM2126XXXP[2]	–20°C to +70°C	48-Pin P-DIP

NOTES
[1]For outline information see Package Information section.
[2]The SSM2125/SSM2126 is available only to licensees of Dolby Laboratories. Each customer will be assigned a special part number for ordering purposes. Contact local ADI sales office for further details.

Dual Single-Supply Audio Operational Amplifier

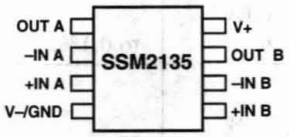
SSM2135

FEATURES
Excellent Sonic Characteristics
High Output Drive Capability
5.2 nV/√Hz Equivalent Input Noise @ 1 kHz
0.001% THD+N (V_O = 2.5 V p-p @ 1 kHz)
3.5 MHz Gain Bandwidth
Unity-Gain Stable
Low Cost

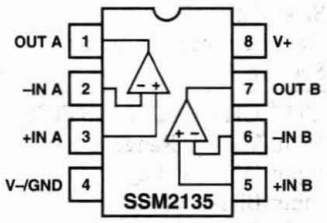
APPLICATIONS
Multimedia Audio Systems
Microphone Preamplifier
Headphone Driver
Differential Line Receiver
Balanced Line Driver
Audio ADC Input Buffer
Audio DAC I-V Converter and Filter
Pseudo-Ground Generator

PIN CONNECTIONS

8-Lead Narrow-Body SOIC (S Suffix)



8-Lead Epoxy DIP (P Suffix)



GENERAL DESCRIPTION

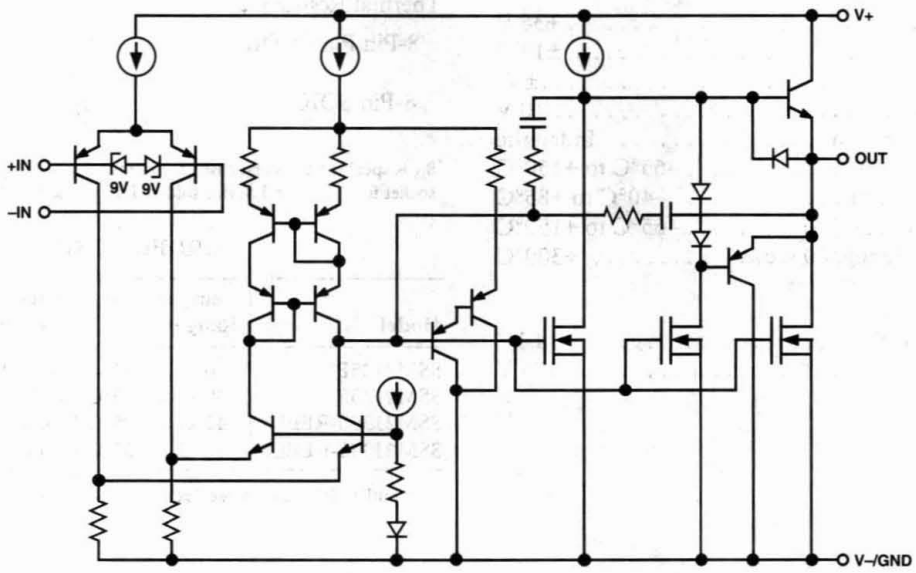
The SSM2135 Dual Audio Operational Amplifier permits excellent performance in portable or low power audio systems, with an operating supply range of +4 V to +36 V or ±2 V to ±18 V. The unity gain stable device has very low voltage noise of 4.7 nV/√Hz, and total harmonic distortion plus noise below 0.01% over normal signal levels and loads. Such characteristics are enhanced by wide output swing and load drive capability. A unique output stage* permits output swing approaching the rail under moderate load conditions. Under severe loading, the SSM2135 still maintains a wide output swing with ultralow distortion.

Particularly well suited for computer audio systems and portable digital audio units, the SSM2135 can perform preamplification, headphone and speaker driving, and balanced line driving and receiving. Additionally, the device is ideal for input signal conditioning in single-supply sigma-delta analog-to-digital converter subsystems such as the AD1878/AD1879.

The SSM2135 is available in 8-pin plastic DIP and SOIC packages, and is guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.

*Protected by U. S. Patent No. 5,146,181.

FUNCTIONAL BLOCK DIAGRAM



SSM2135–SPECIFICATIONS

(V_S = +5 V, –40°C < T_A < +85°C unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		5.2		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.5		$pA/\sqrt{Hz}$
Signal-To-Noise Ratio	SNR	20 Hz to 20 kHz, 0 dBu = 0.775 V rms		121		dBu
Headroom	HR	Clip Point = 1% THD+N, f = 1 kHz, R_L = 10 kΩ		5.3		dBu
Total Harmonic Distortion	THD+N	A_V = +1, V_O = 1 V p-p, f = 1 kHz, 80 kHz LPF				
		R_L = 10 kΩ		0.003		%
		R_L = 32 Ω		0.005		%
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, T_A = +25°C	0.6	0.9		V/µs
Gain Bandwidth Product	GBW			3.5		MHz
Settling Time	t_S	to 0.1%, 2 V Step		5.8		µs
INPUT CHARACTERISTICS						
Input Voltage Range	V_{CM}		0		+4.0	V
Input Offset Voltage	V_{OS}	V_{OUT} = 2 V		0.2	2.0	mV
Input Bias Current	I_B	V_{CM} = 0 V, V_{OUT} = 2 V		300	750	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, V_{OUT} = 2 V			50	nA
Differential Input Impedance	Z_{IN}			4		MΩ
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 4 V, f = dc	87	112		dB
Large Signal Voltage Gain	A_{VO}	0.01 V ≤ V_{OUT} ≤ 3.9 V, R_L = 600 Ω	2			V/µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ	4.1			V
		R_L = 600 Ω	3.9			V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ			3.5	mV
		R_L = 600 Ω			3.0	mV
Short Circuit Current Limit	I_{SC}			±30		mA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+4		+36	V
		Dual Supply	±2		±18	V
Power Supply Rejection Ratio	PSRR	V_S = +4 V to +6 V, f = dc	90	120		dB
Supply Current	I_{SY}	V_{OUT} = 2.0 V, No Load				
		V_S = +5 V		2.8	4.0	mA
		V_S = ±18 V		3.7	5.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Single Supply ..... +36 V
- Dual Supply ..... ±18 V

Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... 10 V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range ..... –40°C to +85°C
Junction Temperature Range (T_J) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

ESD RATINGS

883 (Human Body) Model ..... 1 kV
EIAJ Model ..... 175 V

THERMAL CHARACTERISTICS

Thermal Resistance[1]

8-Pin Plastic DIP	θ_{JA}	103°C/W
	θ_{JC}	43°C/W
8-Pin SOIC	θ_{JA}	158°C/W
	θ_{JC}	43°C/W

[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2135P	–40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2135S	–40°C to +85°C	8-Pin SOIC	SO-8
SSM2135S-REEL	–40°C to +85°C	8-Pin SOIC	SO-8
SSM2135S-REEL7	–40°C to +85°C	8-Pin SOIC	SO-8

*For outline information see Package Information section.

High Common-Mode Rejection Differential Line Receiver

SSM2141

FEATURES

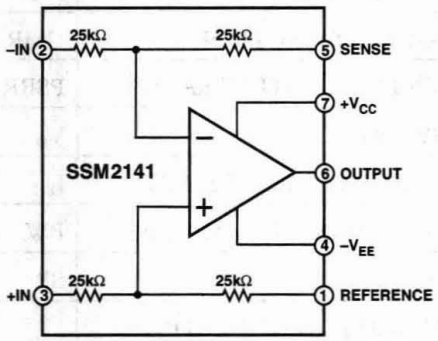
High Common-Mode Rejection
- **DC: 100 dB typ**
- **60 Hz: 100 dB typ**
- **20 kHz: 70 dB typ**
- **40 kHz: 62 dB typ**

Low Distortion: 0.001% typ
Fast Slew Rate: 9.5 V/μs typ
Wide Bandwidth: 3 MHz typ
Low Cost
Complements SSM2142 Differential Line Driver

APPLICATIONS

Line Receivers
Summing Amplifiers
Buffer Amplifiers–Drives 600 Ω Load

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

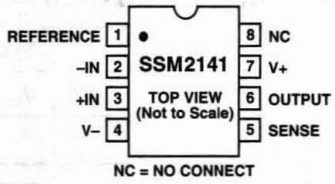
The SSM2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM2141 typically achieves 100 dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40 dB of CMR—inadequate for high-performance audio.

The SSM2141 achieves low distortion performance by maintaining a large slew rate of 9.5 V/μs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM2141 complements the SSM2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM2141 include summing signals, differential preamplifiers, and 600 Ω low distortion buffer amplifiers. For similar performance with G = 1/2, see SSM2143.

PIN CONNECTIONS

8-Pin Plastic Mini-DIP
(P Suffix)
Narrow Body SO
(S Suffix)



ORDERING GUIDE

Model	Operating Temperature Range	Package Description	Package Option*
SSM2141P	XIND (–40°C ≤ T_A ≤ +85°C)	8-Pin Plastic DIP	N-8
SSM2141S	XIND (–40°C ≤ T_A ≤ +85°C)	8-Pin Narrow Body SO	SO-8

*For outline information see Package Information section.

SSM2141–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±18 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	SSM2141 Min	Typ	Max	Units
OFFSET VOLTAGE	V_{OS}	V_{CM} = 0 V	–1000	25	1000	µV
GAIN ERROR		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.001	0.01	%
INPUT VOLTAGE RANGE	IVR	(Note 1)	±10			V
COMMON-MODE REJECTION	CMR	V_{CM} = ±10 V	80	100		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±6 V to ±18 V		0.7	15	µV/V
OUTPUT SWING	V_O	R_L = 2 kΩ	±13	±14.7		V
SHORT-CIRCUIT CURRENT LIMIT	I_{SC}	Output Shorted to Ground	+45/–15			mA
SMALL-SIGNAL BANDWIDTH (–3 dB)	BW	R_L = 2 kΩ		3		MHz
SLEW RATE	SR	R_L = 2 kΩ	6	9.5		V/µs
TOTAL HARMONIC DISTORTION	THD	R_L = 100 kΩ R_L = 600 Ω		0.001 0.01		%
CAPACITIVE LOAD DRIVE CAPABILITY	C_L	No Oscillation		300		pF
SUPPLY CURRENT	I_{SY}	No Load		2.5	3.5	mA

NOTES
[1]Input Voltage Range Guaranteed by CMR test.
Specifications subject to change without notice

ELECTRICAL CHARACTERISTICS (@ V_S = ±18 V, –40°C ≤ T_A ≤ +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFFSET VOLTAGE	V_{OS}	V_{CM} = 0 V	–2500	200	2500	µV
GAIN ERROR		No Load, V_{IN} = ±10 V, R_S = 0 Ω		0.002	0.02	%
INPUT VOLTAGE RANGE	IVR	(Note 1)	±10			V
COMMON-MODE REJECTION	CMR	V_{CM} = ±10 V	75	90		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±6 V to ±18 V		1.0	20	µV/V
OUTPUT SWING	V_O	R_L = 2 kΩ	±13	±14.7		V
SLEW RATE	SR	R_L = 2 kΩ		9.5		V/µs
SUPPLY CURRENT	I_{SY}	No Load		2.6	4.0	mA

NOTES
[1]Input Voltage Range Guaranteed by CMR test.
Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Input Voltage[1] ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –40°C to +85°C

THERMAL CHARACTERISTICS

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES
[1]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

ANALOG DEVICES

Balanced Line Driver

SSM2142

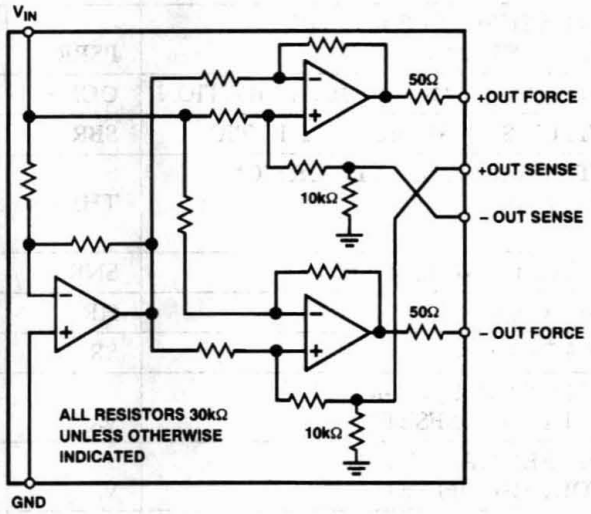
FEATURES

- Transformer-Like Balanced Output
- Drives 10 V RMS Into a 600 Ω Load
- Stable When Driving Large Capacitive Loads and Long Cables
- Low Distortion
  - 0.006% typ 20 Hz–20 kHz, 10 V RMS into 600 Ω
- High Slew Rate
  - 15 V/μs typ
- Low Gain Error
  - (Differential or Single-Ended); 0.7% typ
- Outputs Short-Circuit Protected
- Available In Space-Saving 8-Pin Mini-DIP Package
- Low Cost

APPLICATIONS

- Audio Mix Consoles
- Distribution Amplifiers
- Graphic and Parametric Equalizers
- Dynamic Range Processors
- Digital Effects Processors
- Telecommunications Systems
- Industrial Instrumentation
- Hi-Fi Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSM2142 is an integrated differential-output buffer amplifier that converts a single-ended input signal to a balanced output signal pair with high output drive. By utilizing low noise thermally matched thin film resistors and high slew rate amplifiers, the SSM2142 helps maintain the sonic quality of audio systems by eliminating power line hum, RF interference, voltage drops, and other externally generated noise commonly encountered with long audio cable runs. Excellent rejection of common-mode noise and offset errors is achieved by laser trimming of the onboard resistors, assuring high gain accuracy. The carefully designed output stage of the SSM2142 is capable of driving difficult loads, yielding low distortion performance despite extremely long cables or loads as low as 600 Ω, and is stable over a wide range of operating conditions.

Based on a cross-coupled, electronically balanced topology, the SSM2142 mimics the performance of fully balanced transformer-based solutions for line driving. However, the SSM2142 maintains lower distortion and occupies much less board space than transformers while achieving comparable common-mode rejection performance with reduced parts count.

The SSM2142 in tandem with the SSM2141 differential receiver establishes a complete, reliable solution for driving and receiving audio signals over long cables. The SSM2141 features an Input Common-Mode Rejection Ratio of 100 dB at 60 Hz. Specifications demonstrating the performance of this typical system are included in the data sheet.

SSM2142–SPECIFICATIONS ($V_S = \pm 18$ V, $-40°C \le T_A \le +85°C$, operating in differential mode unless otherwise noted. Typical characteristics apply to operation at $T_A = +25°C$.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT IMPEDANCE	Z_{IN}			10		kΩ
INPUT CURRENT	I_{IN}	$V_{IN} = \pm 7.071$ V		±750	±900	µA
GAIN, DIFFERENTIAL			5.8	5.98		dB
GAIN, SINGLE-ENDED		Single-Ended Mode	5.7	5.94		dB
GAIN ERROR, DIFFERENTIAL		$R_L = 600\ \Omega$		0.7	2	%
POWER SUPPLY REJECTION RATIO STATIC	PSRR	$V_S = \pm 13$ V to ± 18 V	60	80		dB
OUTPUT COMMON-MODE REJECTION	OCMR	See Test Circuit; f = 1 kHz	–38	–45		dB
OUTPUT SIGNAL BALANCE RATIO	SBR	See Test Circuit; f = 1 kHz	–35	–40		dB
TOTAL HARMONIC DISTORTION Plus Noise	THD+N	20 Hz to 20 kHz, $V_O = 10$ V rms, $R_L = 600\ \Omega$		0.006		%
SIGNAL-TO-NOISE RATIO	SNR	$V_{IN} = 0$ V		–93.4		dBu
HEADROOM	HR	CLIP Level = 10.5 V rms		+93.4		dBu
SLEW RATE	SR			15		V/µs
OUTPUT COMMON-MODE VOLTAGE OFFSET[1]	V_{OOS}	$R_L = 600\ \Omega$	–250	25	250	mV
DIFFERENTIAL OUTPUT VOLTAGE OFFSET	V_{OOD}	$R_L = 600\ \Omega$	–50	15	50	mV
DIFFERENTIAL OUTPUT VOLTAGE SWING		$V_{IN} = \pm 7.071$ V	±13.8	±14.14		V
OUTPUT IMPEDANCE	Z_O		45	50	55	Ω
SUPPLY CURRENT	I_{SY}	Unloaded, $V_{IN} = 0$ V		5.5	7.0	mA
OUTPUT CURRENT, SHORT CIRCUIT	I_{SC}		60	70		mA

NOTES
[1]Output common-mode offset voltage can be removed by inserting dc blocking capacitors in the sense lines. See Applications Information.
Specifications subject to change without notice.

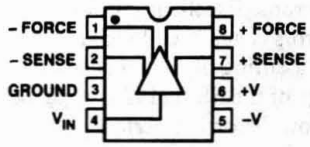
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18 V
Storage Temperature . . . . . –60°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Junction Temperature . . . . . +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Output Short Circuit Duration (Both Outputs) . . . . Indefinite

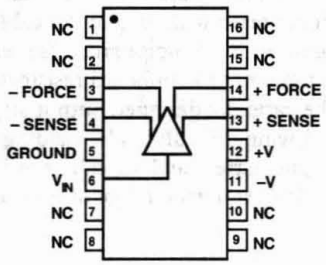
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONNECTIONS

8-Pin Plastic DIP (P Suffix)



16-Pin Wide Body SOL (S Suffix)



NC = NO CONNECT

ORDERING GUIDE

Model	Operating Temperature Range	Package Description	Package Option[1]
SSM2142P	–40°C to +85°C	Plastic DIP	N-8
SSM2142S[2]	–40°C to +85°C	SOL	R-16

NOTES
[1]For outline information see Package Information section.
[2]For availability of SOIC package, contact your local sales office.

–6 dB Differential Line Receiver

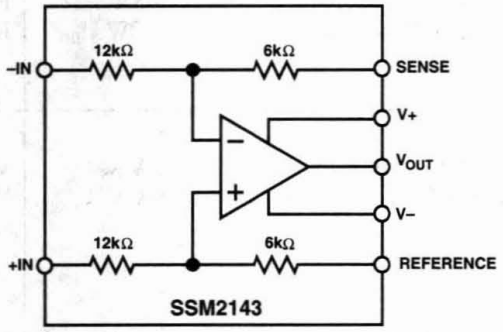
SSM2143

FEATURES

High Common-Mode Rejection
- **DC: 90 dB typ**
- **60 Hz: 90 dB typ**
- **20 kHz: 85 dB typ**

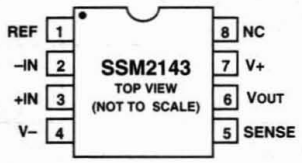
Ultralow THD: 0.0006% typ @ 1 kHz
Fast Slew Rate: 10 V/μs typ
Wide Bandwidth: 7 MHz typ (G = 1/2)
Two Gain Levels Available: G = 1/2 or 2
Low Cost

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and
SOIC (S Suffix)



NC = NO CONNECT

GENERAL DESCRIPTION

The SSM2143 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of immunity from common-mode noise. The device provides a typical 90 dB of common-mode rejection (CMR), which is achieved by laser trimming of resistances to better than 0.005%.

Additional features of the device include a slew rate of 10 V/μs and wide bandwidth. Total harmonic distortion (THD) is less than 0.004% over the full audio band, even while driving low impedance loads. The SSM2143 input stage is designed to handle input signals as large as +28 dBu at G = 1/2. Although primarily intended for G = 1/2 applications, a gain of 2 can be realized by reversing the +IN/–IN and SENSE/REFERENCE connections.

When configured for a gain of 1/2, the SSM2143 and SSM2142 Balanced Line Driver provide a fully integrated, unity gain solution to driving audio signals over long cable runs. For similar performance with G = 1, see SSM2141.

ORDERING GUIDE

Model	Operating Temperature Range	Package Description	Package Option[1]
SSM2143P	–40°C to +85°C	8-Pin Plastic DIP	N-8
SSM2143S[2]	–40°C to +85°C	8-Pin SOIC	SO-8

NOTES
[1]For outline information see Package Information section.
[2]Contact sales office for availability.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

SSM2143–SPECIFICATIONS

(V_S = ±15 V, –40°C ≤ T_A ≤ +85°C, G = 1/2, unless otherwise noted. Typical specifications apply at T_A = +25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	V_{IN} = 10 V rms, R_L = 10 kΩ, f = 1 kHz		0.0006		%
Signal-to-Noise Ratio	SNR	0 dBu = 0.775 V rms, 20 kHz BW, RTI		–107.3		dBu
Headroom	HR	Clip Point = 1% THD+N		+28.0		dBu
DYNAMIC RESPONSE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	6	10		V/µs
Small Signal Bandwidth	$BW_{-3\ dB}$	R_L = 2 kΩ, C_L = 200 pF				
		G = 1/2		7		MHz
		G = 2		3.5		MHz
INPUT						
Input Offset Voltage	V_{IOS}	V_{CM} = 0 V, RTI, G = 2	–1.2	0.05	+1.2	mV
Common-Mode Rejection	CMR	V_{CM} = ±10 V, RTO				
		f = dc	70	90		dB
		f = 60 Hz		90		dB
		f = 20 kHz		85		dB
		f = 400 kHz		60		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V	90	110		dB
Input Voltage Range	IVR	Common Mode		±15		V
		Differential		±28		V
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±14		V
Minimum Resistive Load Drive				2		kΩ
Maximum Capacitive Load Drive				300		pF
Short Circuit Current Limit	I_{SC}			+45, –20		mA
GAIN						
Gain Accuracy			–0.1	0.03	0.1	%
REFERENCE INPUT						
Input Resistance				18		kΩ
Voltage Range				±10		V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±18	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±2.7	±4.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage . . . . . ±22 V
Differential Input Voltage . . . . . ±44 V
Output Short Circuit Duration . . . . . Continuous
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Thermal Resistance
8-Pin Plastic DIP (P): θ_{JA} = 103, θ_{JC} = 43 . . . . . °C/W
8-Pin SOIC (S): θ_{JA} = 150, θ_{JC} = 43 . . . . . °C/W

6 and 4 Channel, "Clickless" Serial Input Balance/Master Volume Controls

SSM2160/SSM2161

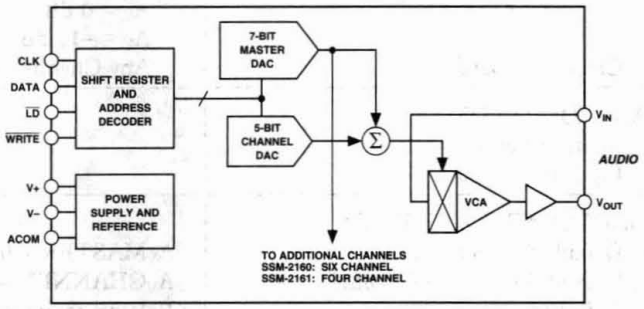
FEATURES

Digitally-Controlled "Clickless" Level Adjustment
SSM2160: Six Channels
SSM2161: Four Channels
Master Control has 128 1 dB Steps
Each Channel has 32 1 dB Steps
Step Sizes Can Be Changed Using External Resistors
High Gain Accuracy
100 dB Gain Range
Power On Mute
Excellent Audio Characteristics:
–100 dBu SNR (0 dBu = 0.775 V rms, V_S = ±5 V)
+10 dBu Headroom (V_S = ±5 V)
0.008% THD+N (@ 1 kHz, V_{IN} = –10 dBu, Unity Gain)
–80 dB Crosstalk (@ 1 kHz)
Single or Dual Supply Operation

APPLICATIONS

Dolby* Pro-Logic Master Volume/Balance Control
Home THX† Systems
DSP Soundfield Processors
Automotive Audio Systems
HDTV Audio Systems

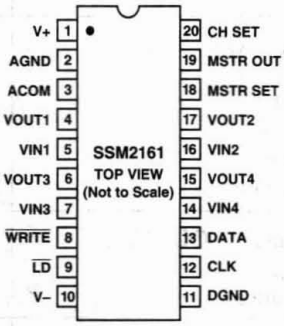
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

24-Lead Epoxy DIP and SOIC

20-Lead Epoxy DIP and SOIC



GENERAL DESCRIPTION

The SSM2160 and SSM2161 allow digital control of volume for six and four channels, respectively, with a master level control. "Clicking" normally encountered with resistor-ladder attenuators is eliminated by using high performance Voltage Controlled Amplifiers (VCAs) in the signal path. The VCA control ports are driven by DACs with controlled output rate-of-change to insure noiseless volume changes. Each channel is controlled by a dedicated 5-bit DAC, providing 32 steps of adjustment. In addition, a master 7-bit DAC feeds every control port, with 128 steps. Therefore, a balance can be achieved among all channels over a 32 step range, and the master control allows adjustment over its entire range while maintaining the desired channel-to-channel balance. Master and channel step sizes are nominally 1 dB; master step sizes can be reduced by an external resistor. Approximately 80 dB of attenuation and up to 20 dB of gain is possible. Upon power-up, the output is automatically muted.

The SSM2160/SSM2161 can operate from single supplies of 8 V to 14 V and dual supplies from ±4 V to ±7 V. An on-chip buffered supply splitter provides an analog common for single-supply applications.

ORDERING GUIDE

Model	Temperature Range	Package Option*
SSM2160P	–40°C to +85°C	24-Lead Plastic DIP
SSM2160S	–40°C to +85°C	24-Lead SOL
SSM2160S-REEL	–40°C to +85°C	24-Lead SOL
SSM2161P	–40°C to +85°C	20-Lead Plastic DIP
SSM2161S	–40°C to +85°C	20-Lead SOL
SSM2161S-REEL	–40°C to +85°C	20-Lead SOL

*For outline information see Package Information section.

*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.
†Home THX is a registered trademark of Lucasfilm, Ltd.

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SSM2160/SSM2161–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

(V_S = ±5 V, A_V = 0 dB, 0 dBu = 0.775 Vrms, V_{IN} = 0 dBu, f_{AUDIO} = 1 kHz, f_{CLK} = 250 kHz, R_L = 10 kΩ, –40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–100		dBu
Headroom	Clip Point = 1% THD+N		+10		dBu
Total Harmonic Distortion Plus Noise	2nd and 3rd Harmonics Only				
	A_V = 0 dB		0.008	TBD	%
	A_V = –10 dB		0.02	TBD	%
Channel Separation	Any Channel to Another		80		dB
ANALOG INPUT					
Input Offset Voltage			10		mV
Input Impedance			10		kΩ
GAIN CONTROL ELEMENTS					
Default Step Size – Master	A_VMASTER = 0 dB to –60 dB		1.0		dB
Default Step Size – Channel	A_VCHANNEL = 0 dB to +20 dB		1.0		dB
Gain Error	Relative to Same Channel				
	A_VMASTER = 0 dB			0.25	dB
	A_VMASTER = –20 dB			0.25	dB
	A_VMASTER = –40 dB			1	dB
	A_VMASTER = –60 dB			2	dB
Gain Match Error	Channel-to-Channel; Same Level Setting				
	A_VMASTER = 0 dB			0.25	dB
	A_VMASTER = –20 dB			0.25	dB
	A_VMASTER = –20 dB, A_VCH = +20 dB			0.25	dB
	A_VMASTER = –40 dB			1	dB
	A_VMASTER = –60 dB			2	dB
Power On Mute Attenuation	V_{IN} = +10 dBu		–100		dB
ANALOG OUTPUT					
Output Impedance			5		Ω
Mute Output Impedance			5		Ω
Output Current			±2		mA
Minimum Resistive Load Drive			1		kΩ
Maximum Capacitive Drive			TBD		pF
Offset Voltage	Channel Muted		10		mV
CONTROL SECTION					
Logic Input LO				0.8	V
Logic Input HI		2.0			V
Logic Input Current	Logic LO or HI		1		µA
Clock Frequency		1		2000	kHz
Timing Characteristics	See Timing Diagram				
ANALOG COMMON OUTPUT					
Output Voltage	See Note 1	–5		+5	%
Output Impedance			5.0		Ω
POWER SUPPLIES					
Supply Voltage Range	Dual Supply	±4		±15	V
	Single Supply	+8		+15	V
Supply Current	Positive		17	28	mA
	Negative		17	28	mA
Power Supply Rejection Ratio	Dual Supply		TBD		dB

NOTES

[1]Analog Common Output is used in single supply applications. It is nominally half the voltage between V+ and V–, e.g., $\frac{V+ - (V-)}{2}$.

Specifications subject to change without notice.

Digitally Controlled 8 × 2 Audio Mixer

SSM2163

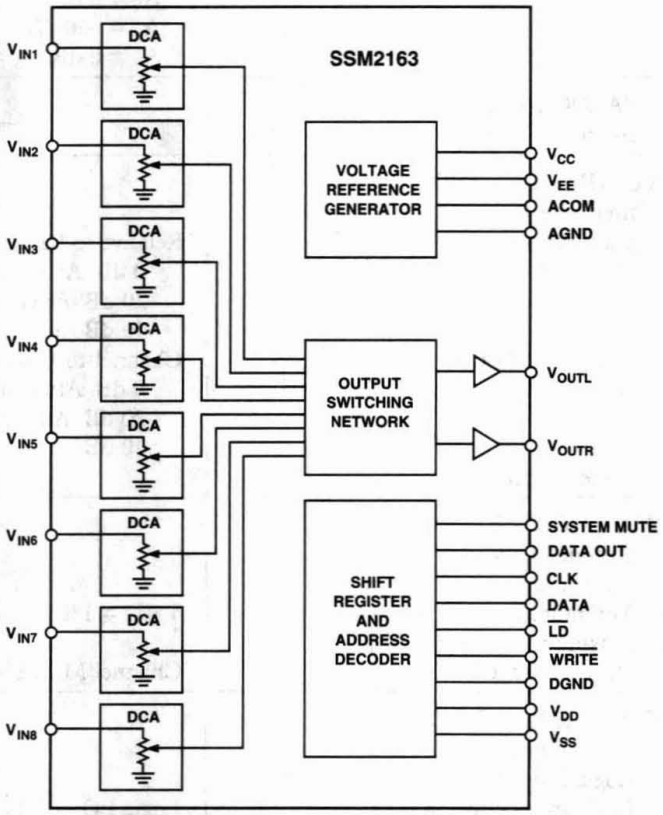
FEATURES

- Each of 8 Inputs Can Be Assigned to Either or Both Outputs
- Voltage Inputs and Outputs – No Need For External Amplifiers
- Each Input Provides 63 dB of Attenuation in 1 dB Steps, Plus Mute
- –82 dBu Signal-to-Noise Ratio (0 dBu = 0.775 V rms)
- +10 dBu of Headroom
- 0.007% THD+N (Unity Gain, @ 1 kHz, 0 dBu)
- Power-Up/System Mute Feature
- Industry-Standard 3-Wire Serial Interface
- Data Out Terminal Permits Daisy Chaining of Multiple SSM2163s
- Single or Dual Supply Operation
- 28-Pin Plastic DIP and SOIC Package

APPLICATIONS

- Multimedia System Mixing
- Audio Mixing Consoles
- Broadcast Equipment
- Intercom/Paging Systems
- Musical Instruments

SIMPLIFIED BLOCK DIAGRAM



DCA: DIGITALLY CONTROLLED ATTENUATOR

GENERAL DESCRIPTION

The SSM2163 provides eight audio inputs, each of which can be mixed under digital control to a stereo output. Each input channel can be attenuated up to 63 dB in 1 dB intervals, plus fully muted. Additionally, any input can be assigned to either or both outputs. A standard 3-wire serial interface is employed, plus a Data Out terminal to facilitate daisy chaining of multiple mixer ICs. No external components are required for normal operation.

Excellent audio performance is attained. The SSM2163 has a signal-to-noise ratio of –82 dBu (0 dBu = 0.775 V rms), with 10 dBu of headroom resulting in total dynamic range of 92 dBu. Total harmonic distortion plus noise is 0.007% at 1 kHz with all levels set at unity gain.

The SSM2163 can be operated from single (+5 V to +14 V) or dual (±4 V to ±7 V) supplies, and is housed in 28-pin plastic DIP and SOIC packages.

The SSM2163 is an ideal companion product to the Analog Devices family of stereo codecs in high performance multimedia systems requiring mixing of multiple signals.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2163P	–40°C to +85°C	Plastic DIP	N-28
SSM2163S	–40°C to +85°C	SOIC	R-28

*For outline information see Package Information section.

SSM2163–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

(V_S = ±5 V, A_V = 0 dB, V_{IN} = 0 dBu = 0.775 V rms, f_{AUDIO} = 1 kHz, f_{CLK} = 250 kHz, R_L = 100 kΩ, −40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–82		dBu
Headroom	Clip Point = 1% THD+N		+10		dBu
Total Harmonic Distortion Plus Noise	2nd and 3rd Harmonics Only				
	A_V = 0 dB		0.007	0.03	%
	A_V = –20 dB		0.02		%
	A_V = 0 dB, V_S = +5 V, Single Supply		0.035		%
ANALOG INPUT					
Input Impedance		7	10	15	kΩ
VOLUME CONTROL					
Step Size			1.0		dB
Gain Error	Relative to Same Channel				
	0 dB Attenuation		0.1	1.0	dB
	–20 dB Attenuation		0.1		dB
	–40 dB Attenuation		0.25		
Gain Match Error	Channel-to-Channel; Same Level Setting				
	0 dB Attenuation		0.01		dB
	–20 dB Attenuation		0.05		dB
	–40 dB		0.4		dB
Mute Attenuation			64		dB
ANALOG OUTPUT					
Output Impedance			15		Ω
Output Current			500		µA
Minimum Resistive Load	THD = 1%		4		kΩ
Maximum Capacitive Drive			5000		pF
Offset Voltage	Channel Muted		50		mV
CONTROL SECTION					
Logic Input LO				0.8	V
Logic Input HI		2.0			V
Logic Input Current	Logic LO or HI		1		µA
Logic Out LO	I_{OUT} = 0.2 mA			0.4	V
Logic Out HI	I_{OUT} = 0.2 mA	2.4			V
Timing Characteristics	See Timing Diagram				
REFERENCE (ACOM)					
Output Voltage	V_S = +10 V (Single Supply)	4.7	5.0	5.3	V
Output Impedance			10		Ω
Load Regulation	–0.5 mA ≤ I_L ≤ +0.5 mA (Single Supply)		0.2		%
POWER SUPPLIES					
Supply Voltage Range	Dual Supply	±4		±7	V
	Single Supply	+5		+14	V
Supply Current	V_S = +10 V (Single Supply)		8	15	mA
Power Supply Rejection Ratio	Delta Gain		0.005		dB/V

Specifications subject to change without notice.

Low Cost Quad Voltage Controlled Amplifier

SSM2164

FEATURES

Four High Performance VCAs in a Single Package
0.02% THD
No External Trimming
120 dB Gain Range
0.07 dB Gain Matching (Unity Gain)
Class A or AB Operation

APPLICATIONS

Remote, Automatic, or Computer Volume Controls
Automotive Volume/Balance/Faders
Audio Mixers
Compressor/Limiters/Compandors
Noise Reduction Systems
Automatic Gain Controls
Voltage Controlled Filters
Spatial Sound Processors
Effects Processors

GENERAL DESCRIPTION

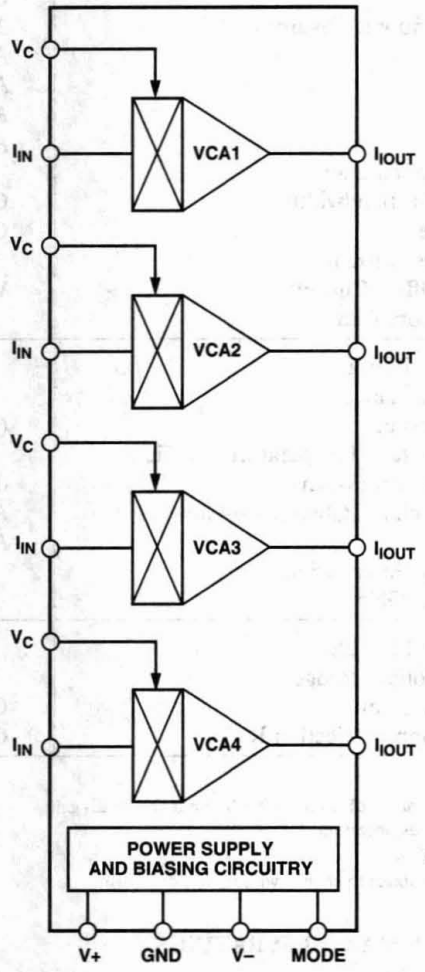
The SSM2164 contains four independent voltage controlled amplifiers (VCAs) in a single package. High performance (100 dB dynamic range, 0.02% THD) is provided at a very low cost-per-VCA, resulting in excellent value for cost sensitive gain control applications. Each VCA offers current input and output for maximum design flexibility, and a ground referenced –33 mV/dB control port.

All channels are closely matched to within 0.07 dB at unity gain, and 0.24 dB at 40 dB of attenuation. A 120 dB gain range is possible.

A single resistor tailors operation between full Class A and AB modes. The pinout allows upgrading of SSM2024 designs with minimal additional circuitry.

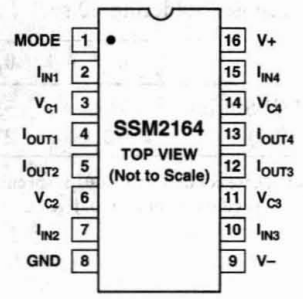
The SSM2164 will operate over a wide supply voltage range of ±4 V to ±18 V. Available in 16-pin P-DIP and SOIC packages, the device is guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

16-Lead Epoxy DIP and SOIC



SSM2164–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (V_S = ±15 V, A_V = 0 dB, 0 dBu = 0.775 V rms, V_{IN} = 0 dBu, R_{IN} = R_{OUT} = 30 kΩ, f = 1 kHz, –40°C < T_A < +85°C using Typical Application Circuit (Class AB), unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Conditions	SSM2164 Min	Typ	Max	Units
AUDIO SIGNAL PATH					
Noise	V_{IN} = GND, 20 kHz Bandwidth		–94		dBu
Headroom	Clip Point = 1% THD+N		22		dBu
Total Harmonic Distortion	2nd and 3rd Harmonics Only				
	A_V = 0 dB, Class A		0.02	.1	%
	A_V = ±20 dB, Class A[1]		0.15		%
	A_V = 0 dB, Class AB		0.16		%
	A_V = ±20 dB, Class AB[1]		0.3		%
Channel Separation			–110		dB
Unity Gain Bandwidth	C_F = 10 pF		500		kHz
Slew Rate	C_F = 10 pF		0.7		mA/µs
Input Bias Current			±10		nA
Output Offset Current	V_{IN} = 0		±50		nA
Output Compliance			±0.1		V
CONTROL PORT					
Input Impedance			5		kΩ
Gain Constant	(Note 2)		–33		mV/dB
Gain Constant Temperature Coefficient			–3300		ppm/°C
Control Feedthrough	0 dB to –40 dB Gain Range[3]		1.5	8.5	mV
Gain Matching, Channel-to-Channel	A_V = 0 dB		0.07		dB
	A_V = –40 dB		0.24		dB
Maximum Attenuation			–100		dB
Maximum Gain			+20		dB
POWER SUPPLIES					
Supply Voltage Range		±4		±18	V
Supply Current	Class AB		6	8	mA
Power Supply Rejection Ratio	60 Hz		90		dB

NOTES
[1]–10 dBu input @ 20 dB gain; +10 dBu input @ –20 dB gain.
[2]After 60 seconds operation.
[3]+25°C to +85°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Input, Output, Control Voltages . . . . . V– to V+
Output Short Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
16-Pin Plastic DIP (P Suffix)	76	33	°C/W
16-Pin SOIC (S Suffix)	92	27	°C/W

*θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for P-DIP packages, θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
SSM2164P	–40°C to +85°C	Plastic DIP	N-16
SSM2164S	–40°C to +85°C	Narrow SOIC	R-16A

*For outline information see Package Information section.

Microphone Preamplifier with Variable Compression & Noise Gating

SSM2166*

FEATURES

Complete Microphone Conditioner in a 14-Pin Package
Single +5 V Operation
Adjustable Noise Gate Threshold
Compression Ratio Set by External Resistor
Automatic Limiting Feature—Prevents ADC Overload
Adjustable Release Time
Low Noise and Distortion
Power-Down Feature
20 kHz Bandwidth (±1 dB)
Low Cost

APPLICATIONS

Microphone Preamplifier/Processor
Computer Sound Cards
Public Address/Paging Systems
Communication Headsets
Telephone Conferencing
Guitar Sustain Effects Generator
Computerized Voice Recognition
Surveillance Systems
Karaoke and DJ Mixers

GENERAL DESCRIPTION

The SSM2166 integrates a complete and flexible solution for conditioning microphone inputs in computer audio systems. It is also excellent for improving vocal clarity in communications and public address systems. A low noise voltage controlled amplifier (VCA) provides a gain that is dynamically adjusted by a control loop to maintain a set compression characteristic. The compression ratio is set by a single resistor and can be varied from 1:1 to over 15:1 relative to a user defined "rotation point;" signals above the rotation point are limited to prevent overload and eliminate "popping." In the 1:1 compression setting the SSM2166 can be programmed with a fixed gain of up to 20 dB; this gain is in addition to the variable gain in other compression settings. The input buffer can also be configured for front-end gains of 0 dB to 20 dB. A downward expander (noise gate) prevents amplification of noise or hum. This results in optimized signal levels prior to digitization, thereby eliminating the need for additional gain or attenuation in the digital domain that could add noise or impair accuracy of speech recognition algorithms. The compression ratio and time constants are set externally. A high degree of flexibility is provided by the Gain, Rotation Point, and Noise Gate adjustment pins.

The SSM2166 is an ideal companion product for audio codecs used in computer systems, such as the AD1845 and AD1847. The device is available in 14-pin SOIC and P-DIP packages, and guaranteed for operation over the extended industrial temperature range of –40°C to +85°C. For similar features/performance in an 8-pin package, please refer to the SSM2165.

PRELIMINARY TECHNICAL DATA

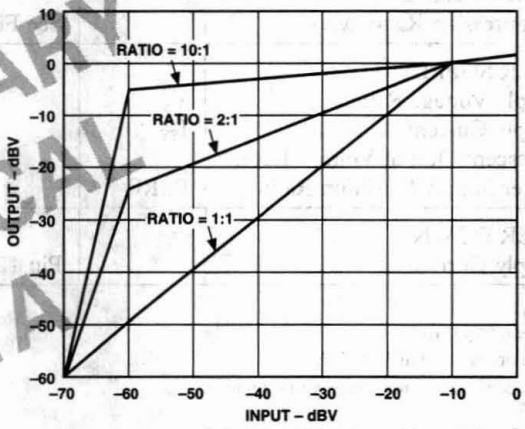


Figure 1. SSM2166 Compression and Gating Characteristics with 10 dB of Fixed Gain (The Gain Adjust Pin Can Be Used to Vary This Fixed Gain Amount)

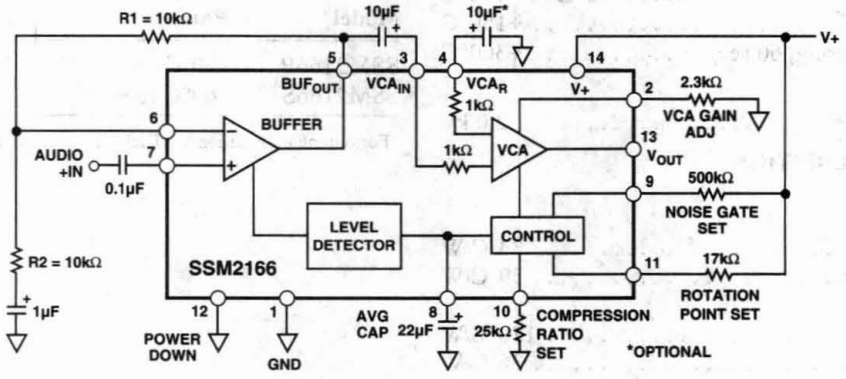


Figure 2. Functional Block Diagram and Typical Speech Application

*Patents pending.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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SSM2166–SPECIFICATIONS (V_S = +5 V, f = 1 kHz, R_L = 100 kΩ, –40°C < T_A < +85°C, unless otherwise noted; V_{IN} = 300 mV rms, typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO SIGNAL PATH						
Voltage Noise Density	e_n	15:1 Compression		17		nV/√Hz
Noise		20 kHz Bandwidth, V_{IN} = GND		–109		dBu[1]
Total Harmonic Distortion	THD+N	2nd & 3rd Harmonics, V_{IN} = –20 dBu 22 kHz Low-Pass Filter		0.25	0.5	%
Input Impedance	Z_{IN}			180		kΩ
Output Impedance	Z_{OUT}			75		Ω
Load Drive		Resistive	5			kΩ
		Capacitive			2	nF
Buffer						
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1		V rms
VCA						
Input Voltage Range		1% THD		1		V rms
Output Voltage Range		1% THD		1.4		V rms
Gain Bandwidth	GBW	1:1 Compression, VCA G = 60 dB		30		MHz
CONTROL SECTION						
VCA Dynamic Gain Range				60		dB
VCA Fixed Dynamic Gain Range				–60 to +19		dB
Compression Ratio, Min				1:1		
Control Feedthrough				±5		mV
Compression Ratio, Max		See Figure 5 for R_{COMP}		15:1		
POWER SUPPLY						
Supply Voltage Range	V_S		4.5		5.5	V
Supply Current	I_{SY}			7.5	10	mA
Quiescent Output Voltage Level			2.1	2.2		V
Power Supply Rejection Ratio	PSRR			50		dB
POWER DOWN						
Supply Current		Pin 12 = V+[2]	100			µA

NOTES
[1]0 dBu = 0.775 V rms.
[2]Normal operation: Pin 12 = 0 V.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +10 V
Audio Input Voltage . . . . . Supply Voltage
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . . +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

ESD RATINGS

883 (Human Body) Model . . . . . 2.0 kV

THERMAL CHARACTERISTICS

Thermal Resistance
14-Pin Plastic DIP
θ_{JA} . . . . . 83°C/W
θ_{JC} . . . . . 39°C/W
14-Pin SOIC
θ_{JA} . . . . . 120°C/W
θ_{JC} . . . . . 36°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
SSM2166P	–40°C to +85°C	Plastic DIP	N-14
SSM2166S	–40°C to +85°C	Narrow SOIC	R-14

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

Dual Audio Analog Switches

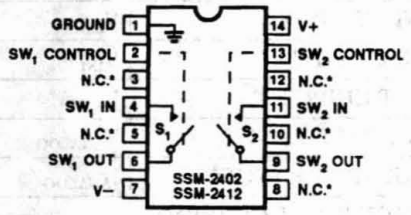
SSM2402/SSM2412

FEATURES

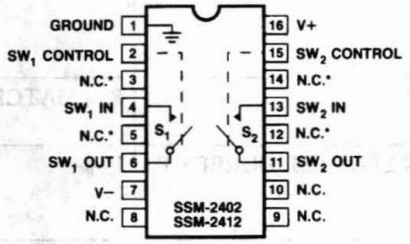
- "Clickless" Bilateral Audio Switching
- Guaranteed "Break-Before-Make" Switching
- Low Distortion: 0.003% typ
- Low Noise: 1 nV/$\sqrt{Hz}$
- Superb OFF-Isolation: 120 dB typ
- Low ON-Resistance: 60 Ω typ
- Wide Signal Range: V_S = ±18 V; 10 V rms
- Wide Power Supply Range: ±20 V max
- Available in Dice Form

PIN CONNECTIONS

14-Pin Epoxy DIP (P Suffix)



16-Pin SOL (S Suffix)



* GUARD PINS FOR INPUT/OUTPUT ISOLATION (GROUND FOR BEST PERFORMANCE)

GENERAL DESCRIPTION

The SSM2402/SSM2412 are dual analog switches designed specifically for high performance audio applications. Distortion and noise are negligible over the full audio operating range of 20 Hz to 20 kHz at signal levels of up to 10 V rms. The SSM2402/SSM2412 offer a monolithic integrated alternative to expensive and noisy relays or complex discrete JFET circuits. Unlike conventional general-purpose CMOS switches, the SSM2402/SSM2412 provide superb fidelity without audio "clicks" during switching.

Conventional TTL or CMOS logic can be used to control the switch state. No external pull-up resistors are needed. A "T" configuration provides superb OFF-isolation and true bilateral operation. The analog inputs and outputs are protected against overload and overvoltage.

An important feature is the guaranteed "break-before-make" for *all* units, even IC-to-IC. In large systems with multiple switching channels, all separate switching units must open before any switch goes into the ON-state. With the SSM2402/SSM2412, you can be certain that multiple circuits will all break-before-make.

The SSM2402/SSM2412 represent a significant step forward in audio switching technology. Distortion and switching noise are significantly reduced in the new SSM2402/SSM2412 bipolar-JFET switches relative to CMOS switching technology. Based on a new circuit topology that optimizes audio performance, the SSM2402/SSM2412 make use of a proprietary bipolar-JFET process with thin-film resistor network capability. Nitride capacitors, which are very area efficient, are used for the proprietary ramp generator that controls the switch resistance transition. Very wide bandwidth amplifiers control the gate-to-source voltage over the full audio operating range for each switch. The ON-resistance remains constant with changes in signal amplitude and frequency, thus distortion is very low, less than 0.01% max.

The SSM2402 is the first analog switch truly optimized for high-performance audio applications. For broadcasting and other switching applications which require a faster switching time, we recommend the SSM2412—a dual analog switch with one-third of the switching time of the SSM2402.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	–40°C to +85°C
Operating Supply Voltage Range	±20 V
Analog Input Voltage Range	
Continuous	V– +3.5 V ≤ V_A ≤ V+ –3.5 V
Maximum Current Through Switch	20 mA
Logic Input Voltage Range	V+ Supply to –2 V
V+ Supply to Ground	+36 V
V– Supply to Ground	–20 V
V_A to V– Supply	+36 V

Package Type	θ_{JA}*	θ_{JC}	Units
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

*θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ORDERING GUIDE

Model	Temperature Range	Package Description*
SSM2402P	–40°C to +85°C	14-Pin Plastic DIP
SSM2402S	–40°C to +85°C	16-Pin SOL
SSM2402S-REEL	–40°C to +85°C	16-Pin SOL
SSM2412P	–40°C to +85°C	14-Pin Plastic DIP
SSM2412S	–40°C to +85°C	16-Pin SOL
SSM2412S-REEL	–40°C to +85°C	16-Pin SOL

*For outline information see Package Information section.

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SSM2402/SSM2412–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±18 V, R_L = OPEN, and –40°C ≤ T_A ≤ +85°C unless otherwise noted.

All specifications, tables, graphs, and application data apply to both the SSM2402 and SSM2412, unless otherwise noted.)

Parameter	Symbol	Conditions		SSM2402/SSM2412 Min	Typ	Max	Units
POSITIVE SUPPLY CURRENT	$+I_{SY}$	V_{IL} = 0.8 V, 2.0 V[1]			6.0	7.5	mA
NEGATIVE SUPPLY CURRENT	$-I_{SY}$	V_{IL} = 0.8 V, 2.0 V[1]			4.8	6.0	mA
GROUND CURRENT	I_{GND}	V_{IL} = 0.8 V, 2.0 V[1]			0.6	1.5	mA
DIGITAL INPUT HIGH	V_{INH}	T_A = Full Temperature Range		2.0			V
DIGITAL INPUT LOW	V_{INL}	T_A = Full Temperature Range				0.8	V
LOGIC INPUT CURRENT	I_{LOGIC}	V_{IN} = 0 V to 15 V[2]			1.0	5.0	µA
ANALOG VOLTAGE RANGE[3]	V_{ANALOG}			–14.2		+14.2	V
ANALOG CURRENT RANGE[3]	I_{ANALOG}			–10		+10	mA
OVERVOLTAGE INPUT CURRENT		V_{IN} = ±V_{SUPPLY}			±40		mA
SWITCH ON RESISTANCE	R_{ON}	–14.2 V ≤ V_A ≤ +14.2 V I_A = ±10 mA, V_{IL} = 2.0 V T_A = +25°C T_A = Full Temperature Range Tempco ($\Delta R_{ON}/\Delta T$)			 60 0.2	 85 115 	 Ω Ω Ω/°C
R_{ON} MATCH	R_{ON} MATCH	–14.2 V ≤ V_A ≤ +14.2 V I_A = ±10 mA, V_{IL} = 2.0 V			1	5	%
SWITCH ON LEAKAGE CURRENT	$I_{S(ON)}$	V_{IL} = 2.0 V –14.2 V ≤ V_A ≤ +14.2 V V_A = 0 V			 0.05 0.05	 1.0 10.0	 µA nA
SWITCH OFF LEAKAGE CURRENT	$I_{S(OFF)}$	V_{IL} = 0.8 V –14.2 V ≤ V_A ≤ +14.2 V V_A = 0 V			 0.05 0.05	 1.0 10.0	 µA nA
TURN-ON TIME[4]	t_{ON}	V_A = +10 V, R_L = 2 kΩ T_A = +25°C, See Test Circuit	SSM2402 SSM2412		10.0 3.5		ms
TURN-OFF TIME[5]	t_{OFF}	V_A = +10 V, R_L = 2 kΩ T_A = +25°C, See Test Circuit	SSM2402 SSM2412		4.0 1.5		ms
BREAK-BEFORE-MAKE TIME DELAY[6]	t_{OFF}–t_{ON}	T_A = +25°C	SSM2402 SSM2412		6.0 2.0		ms
CHARGE INJECTION	Q	T_A = +25°C	SSM2402 SSM2412		50 150		pC
ON-STATE INPUT CAPACITANCE	$CS_{(ON)}$	V_A = 1 V rms f = 5 kHz, T_A = +25°C			12		pF
OFF-STATE INPUT CAPACITANCE	$CS_{(OFF)}$	V_A = 1 V rms f = 5 kHz, T_A = +25°C			4		pF
OFF ISOLATION	$I_{SO(OFF)}$	V_A = 10 V rms, 20 Hz to 20 kHz T_A = +25°C, See Test Circuit			120		dB
CHANNEL-TO-CHANNEL CROSSTALK	C_T	V_A = 10 V rms, 20 Hz to 20 kHz T_A = +25°C			96		dB
TOTAL HARMONIC DISTORTION[7]	THD	0 V to 10 V rms, 20 Hz to 20 kHz T_A = +25°C, R_L = 5 kΩ			0.003	0.01	%
SPECTRAL NOISE DENSITY	e_n	20 Hz to 20 kHz, T_A = +25°C			1		$nV/\sqrt{Hz}$
WIDEBAND NOISE DENSITY	e_n p-p	20 Hz to 20 kHz, T_A = +25°C			0.2		µV p-p

NOTES

[1]"V_{IL}" is the Logic Control Input.

[2]Current tested at V_{IN} = 0 V. This is the worst case condition.

[3]Guaranteed by R_{ON} test condition.

[4]Turn-ON time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.

[5]Turn-OFF time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.

[6]Switch is guaranteed by design to provide break-before-make operation.

[7]THD guaranteed by design and dynamic R_{ON} testing.

Specifications subject to change without notice.

ANALOG DEVICES

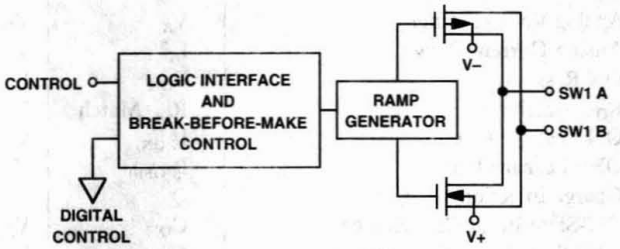
Quad Audio Switch

SSM2404

FEATURES

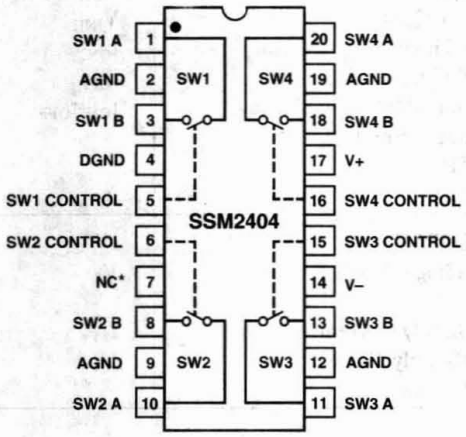
- "Clickless" Bilateral Audio Switching
- Four SPST Switches in a 20-Pin Package
- Ultralow THD+N: 0.0008% @ 1 kHz (2 V rms, R_L = 100 kΩ)
- Low Charge Injection: 35 pC typ
- High OFF Isolation: –100 dB typ (R_L = 10 kΩ @ 1 kHz)
- Low Crosstalk: –94 dB typ (R_L = 10 kΩ @ 1 kHz)
- Low ON Resistance: 28 Ω typ
- Low Supply Current: 900 μA typ
- Single or Dual Supply Operation: +11 V to +24 V or ±5.5 V to ±12 V
- Guaranteed Break-Before-Make
- TTL and CMOS Compatible Logic Inputs
- Low Cost-Per-Switch

BLOCK DIAGRAM OF ONE SWITCH CHANNEL



PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix) and SOIC (S Suffix)



NC = NO CONNECT

*CONNECT TO ANALOG GROUND FOR BEST NOISE ISOLATION

GENERAL DESCRIPTION

The SSM2404 integrates four SPST analog switches in a single 20-pin package. Developed specifically for high performance audio applications, distortion and noise are negligible over the full operating range of 20 Hz to 20 kHz. With very low charge injection of 35 pC, "clickless" audio switching is possible, even under the most demanding conditions.

Switch control is realized by conventional TTL or CMOS logic. Guaranteed "break-before-make" operation assures that all switches in a large system will open before any switch reaches the ON state.

Single or dual supply operation is possible. Additional features include –100 dB OFF isolation, –94 dB crosstalk and 28 Ω ON resistance. Optional current-mode switching permits an extended signal-handling range. Although optimized for large load impedances, the SSM2404 maintains good audio performance even under low load impedance conditions.

SSM2404–SPECIFICATIONS

(V_S = ±12 V, T_A = +25°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	@ 1 kHz, with 80 kHz Filter, R_L = 100 kΩ, V_{IN} = 2 V rms		0.0008		%
Spectral Noise Density	e_n	20 Hz to 20 kHz		0.8		nV/√Hz
Wideband Noise Density	e_n p-p	20 Hz to 20 kHz		0.6		μV p-p
ANALOG SIGNAL SECTION						
Analog Voltage Range	V_A	V_{INH} = 2.4 V, I_A = ±2 mA		±12		V
Analog Current Range	I_A	V_{INH} = 2.4 V, V_A = 0 V		±10		mA
ON Resistance	R_{ON}	I_A = ±10 mA, V_A = ±10 V dc		28	45	Ω
R_{ON} Matching	R_{ON} Match	I_A = ±10 mA, V_A = 0 V		1		%
ON Leakage Current	$I_{S(ON)}$	V_A = ±10 V	–20	0.1	+20	nA
OFF Leakage Current	$I_{S(OFF)}$	V_A = ±10 V	–20	0.1	+20	nA
Charge Injection	Q			35		pC
ON-State Input Capacitance	C_{ON}	V_A = 5 V rms		31		pF
OFF-State Input Capacitance	C_{OFF}	V_A = 5 V rms		17		pF
OFF Isolation	$I_{SO(OFF)}$	V_A = 50 mV rms, f = 1 kHz, R_L = 10 kΩ		–100		dB
Channel-to-Channel Crosstalk	C_T	V_A = 50 mV rms, f = 1 kHz, R_L = 10 kΩ		–94		dB
CONTROL SECTION						
Digital Input High	V_{INH}	DGND = 0 V	2.4		V_S	V
Digital Input Low	V_{INL}	DGND = 0 V	0		0.8	V
Turn-On Time[1]	t_{ON}	See Test Circuit		8	50	ms
Turn-Off Time[2]	t_{OFF}	See Test Circuit		5	30	ms
Break-Before-Make Time Delay	t_{ON}-t_{OFF}			3	20	ms
Logic Input Current						
Logic HI		V_{INH} = 2.4 V	–1000	1.3	+1000	nA
Logic LO		V_{INL} = 0.8 V	–1000	1.0	+1000	nA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+11		+24	V
		Dual Supply	±5.5		±12	V
Positive Supply Current	I_{SY+}	All Channels On		0.9	5	mA
Negative Supply Current	I_{SY-}	All Channels On	–1.5	–0.6		mA
Ground Current		All Channels On	–2.0	–0.3		mA

NOTES

[1]Turn-on time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.

[2]Turn-off time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Single Supply . . . . . +27 V
- Dual Supply . . . . . ±13.5 V

Analog Input Voltage (V_A) . . . . . V_S

Logic Input Voltage ($V_{INL/INH}$) . . . . . V_S

Maximum Current Through Any Switch . . . . . 20 mA

Operating Temperature Range . . . . . –40°C to +85°C

Storage Temperature Range . . . . . –65°C to +150°C

Junction Temperature (T_J) . . . . . +150°C

Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Thermal Resistance[1]
- 20-Pin Plastic DIP (P): θ_{JA} = 74, θ_{JC} = 32 . . . . . °C/W
- 20-Pin SOIC (S): θ_{JA} = 90, θ_{JC} = 27 . . . . . °C/W

NOTE

[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

ORDERING GUIDE

Model	Operating Temperature Range	Package	Package Option*
SSM2404P	–40°C to +85°C	20-Pin Plastic DIP	N-20
SSM2404S	–40°C to +85°C	20-Pin SOIC	R-20

*N = Plastic DIP, R = SOIC. For outline information see Package Information section.

Communications (Wireless, DDS & RF) Circuits
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Communications (Wireless, DDS & RF) Circuits–Selection Guides

Wireless

GSM Baseband I/O Port

	Power		Transmit Dual 10-Bit				Receive Dual 12-Bit					
Model	V_S V	I_S mA	Spurious Power	Update Rate	Frequency Response		Word Rate MSPS	Update Rate kSPS	# Pins	Page No.	Comments	Fax-code
AD7002	+5	30	–3 dBc–63 dBc 100 kHz	4.33 kHz 400 kHz	–0.05 dBc	–66 dB @ 100 kHz	13 @ 200 kHz	270/541	44	*	With Powerdown, 3 Aux D/As	1239

JDC π/4 Baseband Transmit Port

	Power		Transmit Dual 10-Bit			Receive Dual 12-Bit					
Model	V_S V	I_S mA	Spurious Power	Update Rate	Frequency Response	Word Rate MSPS	Update Rate kSPS	# Pins	Page No.	Comments	Fax-code
AD7010	+5	8	–25 dBc–55 dBc 25 kHz 50 kHz	NS		NA	NA	24	17–15	Japanese Cell Phone	1241

American Baseband Transmit Port

	Power		Transmit Dual 10-Bit			Receive Dual 12-Bit					
Model	V_S V	I_S mA	Spurious Power	Update Rate	Frequency Response	Word Rate MSPS	Update Rate kSPS	# Pins	Page No.	Comments	Fax-code
AD7011	5	8	–35 dBc–70 dBc 30 kHz 60 kHz	160 kHz		NA	NA	24	17–17	TIA, IS-54	1242

American Baseband Receive Port

	Power		Transmit Dual 10-Bit				Receive Dual 12-Bit					
Model	V_S V	I_S mA	Spurious Power	Update Rate	Frequency Response		Word Rate MSPS	Update Rate kSPS	# Pins	Page No.	Comments	Fax-code
AD7013†	5	10.5	NA	NA	–3 dBc @ 11.4 kHz	–24 dB @ 15 kHz	1.55	38/97	28	17–19	TIA, IS-54	1243
AD7015	+3	See D/S	Complete Baseband & Voiceband Codec GSM/DCS1800						80	17–21	See Data Sheet	1921
AD20msp410	NA	NA	GSM Baseband Processing Chip Set, ADSP-2171 & AD7015 & ASIC						NA	17–5	See Data Sheet	1920

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.
†AD7013 15-Bit Resolution

Direct Digital Synthesis

32 Bits

Model	# Bits	Power Supply Volts	Power Supply mA	I_{OUT} mA	THD dB	SNR dB	SFDR Wide-band	Update Rate MHz	# Pins	Page No.	Comments	Fax-code
AD7008	10	+5	160	20	–55	+50	–55	20/40	44	17–13	With Sine/Cosine LUT, Phase & Amp Modulation	1240
AD9830	10	+5	15	20	–55	+50	–55	50	48	17–23	With Frequency and Phase Modulators, Sine Lookup	1993
AD9831	10	+3	12	4	–55	+50	–55	15	48	17–25	With Frequency and Phase Modulators, Sine Lookup	1994

Phase Detector

Model	Power $+V_S$ V	Power $-I_S$ V	Power $+I_S$ mA	Power $-I_S$ mA	Linear Phase Detection Range @ 40 kHz	Linear Phase Detection Range @ 30 MHz	Linear Phase Detection Range @ 70 MHz	# Pins	Page No.	Comments	Fax-code
AD9901	+5	–5	54	52	360°	320°	270°	16/20	17–27	Linear Phase Detector/Frequency Discriminator	1482

IF Subsystems and Mixers

Model	Mixer Section RF & LO Range MHz	Mixer Section IPS dBm	Mixer Section IDM Comp dBm	IF Section @ 10.7 MHz Gain dB	I/Q Demod Section PLL	I/Q Demod Section BW	RSSI Section dBm	# Pins	Page No.	Comments	Fax-code
AD607	500	–5	–15	Linear 75 dB	0.4–40 MHz	2 MHz	90	20	17–7	Linear IF Arch	1824
AD608	500	–5	–15	Limiting 110	N/A		–75–+5	16	17–9	Limiting IF Arch	1825
AD831	500	+24	+10					20	17–11	Doubly Balanced Mixer	1413

Communications (Wireless, DDS & RF) Circuits–Selection Guides

Telecom/Datacom

Mixed Signal Processors

Model	Description	# Pins	Page No.	Comments	Fax-code
ADSP-21msp58	ADSP-2171 DSP with Voiceband Codec	100	17–29	26 MIPS	1901
ADSP-21msp59	ADSP-2171 DSP with Voiceband Codec		17–29	26 MIPS, with 4K × 24 ROM	1901

Communication & Sound Codec

Model	Description	# Pins	Page No.	Comments	Fax-code
AD1843	Supports V.34, V.32 BIS; with Continuous Time Oversampling	80/100	18–7	Speech, Audio, Fax & Modem	1902

ANALOG DEVICES

GSM Baseband Processing Chipset

AD20msp410

FEATURES

Complete Baseband Processing Chipset Performs:
- **Speech Coding/Decoding, According to GSM 06.XX**
- **DTMF and Call Progress Tone Generation**
- **Equalization with 16-State Viterbi, Soft Decision**
- **Channel Coding/Decoding According to GSM 05.03**
- **All ADC and DAC Interface Functions**
- **Includes All Radio, Auxiliary and Voice Interfaces**
- **Support for GSM Data Services**

Embedded 16-Bit Microcontroller
Layer 1 Software Provided with Chipset
Full Phase 2 Protocol Stack Software Available
Integrated SIM and Keyboard Interface
Ultralow Power Design
- **Optional 3 V or 5 V Operating Voltage**
- **Intelligent Power Management Features**

Low Power Dissipation in Talk Mode and Standby Mode
JTAG-Boundary Scan
Full Reference Design Available for:
- **Baseband Section**
- **Radio Subsystem**

Three TQFP Devices, Occupying Less than 12 cm^2

APPLICATIONS

GSM/DCS1800 Mobile Radios
GSM/DCS1800 PCMCIA Cards

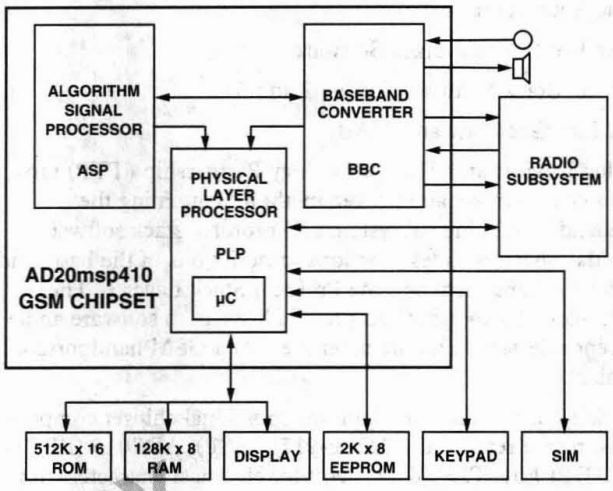

Figure 1. System Architecture

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The Analog Devices GSM baseband processing chipset provides a competitive solution for GSM based mobile radio systems. It is designed to be fully integrated, easy to use, and compatible with a wide range of product solutions.

The chipset consists of three highly integrated, submicron, low power CMOS components that form the core baseband signal processing of the GSM handset. The system architecture is designed to be easily integrated into current designs and form the basis of the next generation of designs.

The chipset can run from an operating voltage of 2.7 V which, coupled with the extensive power management features, significantly reduces the drain on battery power and extends the handset's talk time and standby time. As an alternative, the 5 V version of the chipset may be used to simplify the system interface or achieve lowest possible system cost.

Algorithm Signal Processor (ASP)

The ASP is an application specific variant of the ADSP-2171 standard DSP from Analog Devices. It has been optimized to meet the cost, size and power consumption requirements of GSM mobile applications. All necessary memory to run the GSM specific programs is provided on chip; no external memory is required. The ASP implements full rate speech transcoding according to GSM specifications, including discontinous transmission (DTX) and comfort noise insertion (CNI). A high performance soft-decision Viterbi equalizer is also implemented in software, embedded in the DSP. The ASP is delivered fully preprogrammed (ROM coded); no user programming is required.

Physical Layer Processor (PLP)

The PLP combines application specific hardware and an embedded 16-bit microcontroller (Hitachi H8/300H) to perform channel coding and decoding and execute the protocol stack and user software. The embedded processor executes the Layer 1, 2, 3 and user MMI software. The required Layer 1 software is supplied with the chipset. In addition, the source code for Layers 2 and 3 of the protocol stack are available separately from this chipset. The PLP can control all powerdown functions of the other chips and memory support components to achieve maximum power savings.

Baseband Converter (BBC)

The BBC is identical to the AD7015 baseband converter of Analog Devices available also as a standard standalone product. The BBC performs the voiceband and baseband analog-to-digital and digital-to-analog conversions, interfacing the digital sections of the chipset to the microphone, loudspeaker and radio section. In addition, the BBC contains all the auxiliary converters for burst-ramping, AFC, AGC, battery and temperature monitoring.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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AD20msp410

ARCHITECTURE OVERVIEW

A standard GSM Handset can be divided into five functional areas:

Analog and Digital Baseband Processing Subsystem (Voice to Radio)

Radio Subsystem

Layer 1 of Protocol Stack Software

Protocol Stack Software (Layers 2 and 3)

User Interface Software (MMI)

Analog Devices and The Technology Partnership (TTP) provide a cost effective and proven method of attaining the baseband processing subsystem and protocol stack software. This datasheet includes functional descriptions of the baseband processing subsystem and the Protocol Stack Layer 1. The Technology Partnership can provide licenses to software and reference designs in all the other areas of a GSM handportable terminal.

For detailed information about the individual chipset components, please refer to the ADSP-2178 (ASP), AD7015 (BBC) and ADPLP01 (PLP) data sheets for electrical characteristics and timing information.

SOFTWARE IMPLEMENTATIONS

A full implementation of the GSM Layer 1 functionality is supplied as an object code module, for execution on the controller, embedded in the PLP. Functions performed by this software include:

Initial scan of GSM/E-GSM/PCN band and selection of strongest thirty channels as required by 03.22 and 05.08.

Mobile oscillator adjustment, timing synchronization and BCCH decoding from serving cell (camping-on).

Base station frequency and timing measurements and BSIC extraction from neighbor cells under control of Layer 3.

Frequency hopping according to 05.02.

Full implementation of discontinous reception (DRX) and transmission (DTX).

Reporting of received level and signal quality.

Full engineering and test mode support.

Support for all phase 1 and phase 2 handover modes.

SIM Interface driver.

Message interfacing to Layer 3 (Radio Resources Manager) and Layer 2 (data link layer, both signaling and data).

External functions for AGC, AFC and synthesizer setting are called by Layer 1. These allow the user to configure the system for a wide range of radio architectures including the TTP GSM reference radio.

The higher layers of the protocol stack also reside on this embedded processor. A GSM phase 2 compliant, PLP compatible Layer 2/3 protocol stack is available from The Technology Partnership.

GSM Baseband Processing Key Parts List

Table I lists the major hardware components necessary to complete the GSM baseband processing subsystem. An example Bill Of Material is available from Analog Devices. A full reference design is available through Analog Devices/The Technology Partnership.

Table I. List of Key Components

Qty	Description	Specification
1	ASP[1]	ADSP-2178
1	PLP[1]	ADPLP01
1	BBC[1]	AD7015
2	FLASH-PROM[2]	256 K × 16, 150 ns
1	SRAM[3]	128 K × 8, 120 ns
1	EEPROM[4]	2 K × 8
1	Display Driver	Design Specific

MECHANICAL CONSIDERATIONS

The chipset has been specifically designed to meet not only cost and power consumption requirements but also attention was paid to the physical dimensions. State-of-the-art package technology was used to achieve smallest possible geometries. See Table II for list of main packaging dimensions and consult individual datasheets of the three components for further details.

Table II. Package Dimensions

Parameter	ASP	PLP	BBC	Unit
Package	TQFP	TQFP	TQFP	
Leads	100	176	80	
Pitch	0.5	0.5	0.65	mm
Body	14 × 14	24 × 24	14 × 14	mm
Total Height	1.6	1.7	1.6	mm
Board Area	16 × 16	26 × 26	16 × 16	mm

All three components utilize low profile plastic quad flat packs with lead pitches of 0.5 mm minimum. Special attention was paid to the possible use in PCMCIA cards. Figure 6 gives some impression how well the chipset together with other major components fits on a standard PCMCIA-card.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Power Mixer/AGC/RSSI 3 V Receiver IF Subsystem

AD607

FEATURES

Complete Receiver on a Chip: Monoceiver™ Mixer
- **–15 dBm 1 dB Compression Point**
- **–8 dBm Input Third Order Intercept**
- **500 MHz RF and LO Bandwidths**

Linear IF Amplifier
- **Linear-in-dB Gain Control**
- **MGC or AGC with RSSI Output**

Quadrature Demodulator
- **On-Board Phase-Locked Quadrature Oscillator**
- **Demodulates IFs from 400 kHz to 12 MHz**
- **Can Also Demodulate AM, CW, SSB**

Low Power
- **25 mW at 3 V**
- **CMOS Compatible Power-Down**

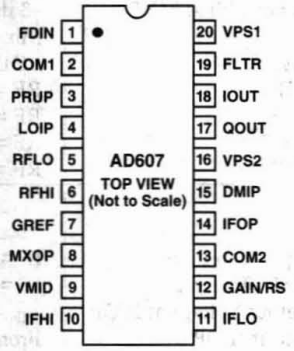
Interfaces to AD7013 and AD7015 Baseband Converters

APPLICATIONS

GSM, CDMA, TDMA, and TETRA Receivers
Satellite Terminals
Battery-Powered Communications Receivers

PIN CONFIGURATION

20-Lead SSOP
(RS Suffix)



GENERAL DESCRIPTION

The AD607 is a 3 V low power receiver IF subsystem for operation at input frequencies as high as 500 MHz and IFs from 400 kHz to 12 MHz. It consists of a mixer, IF amplifiers, I and Q demodulators, a phase-locked quadrature oscillator, AGC detector, and a biasing system with external power-down.

The AD607's low noise, high intercept mixer is a doubly-balanced Gilbert cell type. It has a nominal –15 dBm input referred 1 dB compression point and a –8 dBm input referred third-order intercept. The mixer section of the AD607 also includes a local oscillator (LO) preamplifier, which lowers the required LO drive to –16 dBm.

The gain control input can serve as either a manual gain control (MGC) input or an automatic gain control (AGC) voltage-based RSSI output. In MGC operation, the AD607 accepts an external gain-control voltage input from an external AGC detector or a DAC. In AGC operation, an onboard detector and an external averaging capacitor form an AGC loop that holds the IF output level at ±300 mV. The voltage across this capacitor then provides an RSSI output.

Monoceiver is a trademark of Analog Devices, Inc.

The I and Q demodulators provide inphase and quadrature baseband outputs to interface with Analog Devices' AD7013 (IS54, TETRA, MSAT) and AD7015 (GSM) baseband converters. A quadrature VCO phase-locked to the IF drives the I and Q demodulators. The I and Q demodulators can also demodulate AM; when the AD607's quadrature VCO is phase locked to the received signal, the in-phase demodulator becomes a synchronous product detector for AM. The VCO can also be phase-locked to an external beat-frequency oscillator (BFO), and the demodulator serves as a product detector for CW or SSB reception. Finally, the AD607 can be used to demodulate BPSK using an external Costas Loop for carrier recovery.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD607ARS	–25°C to +85°C for 2.7 V to 5.5 V Operation; –40°C to +85°C for 4.5 V to 5.5 V Operation	20-Pin Plastic SSOP	RS-20

*For outline information see Package Information section.

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AD607–SPECIFICATIONS (@ T_A = +25°C, Supply = 3.0 V, IF = 10.7 MHz, unless otherwise noted)

Model	Conditions	AD607ARS Min	AD607ARS Typ	AD607ARS Max	Units
DYNAMIC PERFORMANCE					
MIXER					
Maximum RF and LO Frequency Range	For Conversion Gain > 20 dB		500		MHz
Maximum Mixer Input Voltage	For Linear Operation; Between RFHI and RFLO		±54		mV
Input 1 dB Compression Point	RF Input Terminated in 50 Ω		–15		dBm
Input Third-Order Intercept	RF Input Terminated in 50 Ω		–5		dBm
Noise Figure	Matched Input, Max Gain, f = 83 MHz, IF = 10.7 MHz		14		dB
	Matched Input, Max Gain, f = 144 MHz, IF = 10.7 MHz		12		dB
Maximum Output Voltage at MXOP	Z_{IF} = 165 Ω, at Input Compression		±1.3		V
Mixer Output Bandwidth at MXOP	–3 dB, Z_{IF} = 165 Ω		45		MHz
LO Drive Level	Mixer LO Input Terminated in 50 Ω		–16		dBm
LO Input Impedance	LOIP to VMID		1		kΩ
Isolation, RF to IF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		30		dB
Isolation, LO to IF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		20		dB
Isolation, LO to RF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		40		dB
Isolation, IF to RF	RF = 240 MHz, IF = 10.7 MHz, LO = 229.3 MHz		70		dB
IF AMPLIFIERS					
Noise Figure	Max Gain, f = 10.7 MHz		17		dB
Input 1 dB Compression Point	IF = 10.7 MHz		–15		dBm
Output Third-Order Intercept	IF = 10.7 MHz		+18		dBm
Maximum IF Output Voltage at IFOP	Z_{IF} = 600 Ω		±560		mV
Output Resistance at IFOP	From IFOP to VMID		15		Ω
Bandwidth	–3 dB at IFOP, Max Gain		45		MHz
GAIN CONTROL	(See Figures 43 and 44)				
Gain Control Range	Mixer + IF Section, GREF to 1.5 V		90		dB
Gain Scaling	GREF to 1.5 V		20		mV/dB
	GREF to General Reference Voltage V_R		$75/V_R$		dB/V
Gain Scaling Accuracy	GREF to 1.5 V, 80 dB Span		±1		dB
Bias Current at GAIN/RSSI			5		μA
Bias Current at GREF			1		μA
Input Resistance at GAIN, GREF			1		MΩ
I AND Q DEMODULATORS					
Required DC Bias at DMIP			VPOS/2		V dc
Input Resistance at DMIP	From DMIP to VMID		50		kΩ
Input Bias Current at DMIP			2		μA
Maximum Input Voltage	IF > 3 MHz		±150		mV
	IF ≤ 3 MHz		±75		mV
Amplitude Balance	IF = 10.7 MHz, Outputs at 600 mV p-p, F = 100 kHz		±0.2		dB
Quadrature Error	IF = 10.7 MHz, Outputs at 600 mV p-p, F = 100 kHz		–1.2		Degrees
Phase Noise in Degrees	IF = 10.7 MHz, F = 10 kHz		–100		dBc/Hz
Demodulation Gain	Sine Wave Input, Baseband Output		18		dB
Maximum Output Voltage	R_L ≥ 20 kΩ		±1.23		V
Output Offset Voltage	Measured from I_{OUT}, Q_{OUT} to VMID		10		mV
Output Bandwidth	Sine Wave Input, Baseband Output		1.5		MHz
PLL					
Required DC Bias at FDIN			VPOS/2		V dc
Input Resistance at FDIN	From FDIN to VMID		50		kΩ
Input Bias Current at FDIN			200		nA
Frequency Range			0.4 to 12		MHz
Required Input Drive Level	Sine Wave Input at Pin 1		400		mV
Acquisition Time to ±3°	IF = 10.7 MHz		16.5		μs
POWER-DOWN INTERFACE					
Logical Threshold	For Power Up on Logical High		2		V dc
Input Current for Logical High			75		μA
Turn-On Response Time	To PLL Locked		16.5		μs
Standby Current			550		μA
POWER SUPPLY					
Supply Range		2.7		5.5	V
Supply Current	Midgain, IF = 10.7 MHz		8.5		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}	Operation to 2.7 V Minimum Supply Voltage	–25		+85	°C
	Operation to 4.5 V Minimum Supply Voltage	–40		+85	°C

Specifications subject to change without notice.

Low Power Mixer/Limiter/RSSI 3 V Receiver IF Subsystem

AD608

FEATURES

Mixer
- **–15 dBm 1 dB Compression Point**
- **–5 dBm IP3**
- **24 dB Conversion Gain**
- **>500 MHz Input Bandwidth**

Logarithmic/Limiting Amplifier
- **80 dB RSSI Range**
- **±3° Phase Stability over 80 dB Range**

Low Power
- **21 mW at 3 V Power Consumption**
- **CMOS-Compatible Power-Down to 300 μW typ**
- **200 ns Enable/Disable Time**

APPLICATIONS

PHS, GSM, TDMA, FM, or PM Receivers
Battery-Powered Instrumentation
Base Station RSSI Measurement

GENERAL DESCRIPTION

The AD608 provides both a low power, low distortion, low noise mixer and a complete, monolithic logarithmic/limiting amplifier using a "successive-detection" technique. It provides both a high speed RSSI (Received Signal Strength Indicator) output with 80 dB dynamic range and a hard-limited output. The RSSI output is from a two-pole post-demodulation low-pass filter and provides a loadable output voltage of +0.2 V to +1.8 V. The AD608 operates from a single 2.7 V to 5.5 V supply at a typical power level of 21 mW at 3 V.

The RF and LO bandwidths both exceed 500 MHz. In a typical IF application, the AD608 will accept the output of a 240 MHz SAW filter and downconvert it to a nominal 10.7 MHz IF with a conversion gain of 24 dB (Z_{IF} = 165 Ω). The AD608's logarithmic/limiting amplifier section handles any IF from LF to as high as 30 MHz.

The mixer is a doubly-balanced "Gilbert-Cell" type and operates linearly for RF inputs spanning –95 dBm to –15 dBm. It has a nominal –5 dBm third-order intercept. An onboard LO preamplifier requires only –16 dBm of LO drive. The mixer's current output drives a reverse-terminated, industry-standard 10.7 MHz 330 Ω filter.

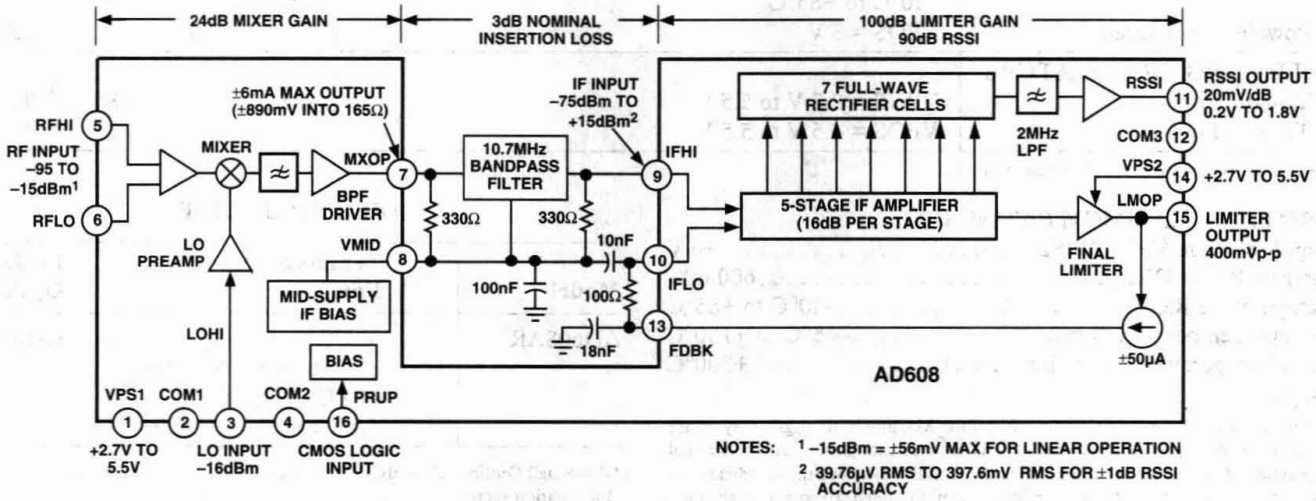
The nominal logarithmic scaling is such that the output is +0.2 V for a sinusoidal input to the IF amplifier of –75 dBm and +1.8 V at an input of +5 dBm; over this range the logarithmic conformance is typically ±1 dB. The logarithmic slope is proportional to the supply voltage. A feedback loop automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD608's limiter output provides a hard-limited signal output at 400 mV p-p. The voltage gain of the limiting amplifier to this output is more than 100 dB. Transition times are 11 ns and the phase is stable to within ±3° at 10.7 MHz for signals from –75 dBm to +5 dBm.

The AD608 is enabled by a CMOS logic-level voltage input, with a response time of 200 ns. When disabled, the standby power is reduced to 300 μW within 400 ns.

The AD608 is specified for the industrial temperature range of –25°C to +85°C for 2.7 V to 5.5 V supplies and –40°C to +85°C for 4.5 V to 5.5 V supplies. It comes in a 16-pin plastic SOIC.

FUNCTIONAL BLOCK DIAGRAM



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AD608—SPECIFICATIONS (@ T_A = +25°C, Supply = 3 V, dBm is referred to 50 Ω, unless otherwise noted)

Model	Conditions[1]	AD608 Min	AD608 Typ	AD608 Max	Units
MIXER PERFORMANCE					
RF and LO Frequency Range			500		MHz
LO Power	Input Terminated in 50 Ω		–16		dBm
Conversion Gain	Driving Doubly-Terminated 330 Ω IF Filter, Z_{IF} = 165 Ω		24		dB
Noise Figure	Matched Input, f_{RF} = 100 MHz		11		dB
	Matched Input, f_{RF} = 240 MHz		16		dB
1 dB Compression Point	Input Terminated in 50 Ω		–15		dBm
Third-Order Intercept	f_{RF} = 240 MHz and 240.02 MHz, f_{LO} = 229.3 MHz		–5		dBm
Input Resistance	f_{RF} = 100 MHz (See Table I)		1.9		kΩ
Input Capacitance	f_{RF} = 100 MHz (See Table I)		3		pF
LIMITER PERFORMANCE					
Gain	Full Temperature and Supply Range		110		dB
Limiting Threshold	3° rms Phase Jitter at 10.7 MHz 280 kHz IF Bandwidth		–75		dBm
Input Resistance			10		kΩ
Input Capacitance			3		pF
Phase Variation	–75 dBm to +5 dBm IF Input Signal at 10.7 MHz		±3		Degree
DC Level	Center of Output Swing (VPOS-1)		2		V
Output Level	Limiter Output Driving 5 kΩ Load		400		mV p-p
Rise and Fall Times	Driving a 5 pF Load		11		ns
Output Impedance			200		Ω
RSSI PERFORMANCE	At 10.7 MHz				
Nominal Slope	At VPOS = 3 V; Proportional to VPOS		20		mV/dB
Nominal Intercept			–85		dBm
Minimum RSSI Voltage	–75 dBm Input Signal		0.2		V
Maximum RSSI Voltage	+5 dBm Input Signal		1.8		V
Logarithmic Linearity Error	–75 dBm to +5 dBm Input Signal at IFHI		±1		dB
RSSI Response Time	90% RF to 50% RSSI		200		ns
Output Impedance	At Midscale		250		Ω
POWER-DOWN INTERFACE					
Logical Threshold	System Active on Logical High		1.5		V
Input Current	For Logical High		75		μA
Power-Up Response Time	Active Limiter Output		200		ns
Power-Down Response Time	To 200 μA Supply Current		400		ns
Power-Down Current			100		μA
POWER SUPPLY					
Operating Range	–25°C to +85°C	2.7		5.5	V
	–40°C to +85°C	4.5		5.5	V
Powered Up Current	VPOS = 3 V		7.3		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}	VPOS = 2.7 V to 5.5 V	–25		+85	°C
T_{MIN} to T_{MAX}	VPOS = 4.5 V to 5.5 V	–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPS1, VPS2 ..... +6 V
Internal Power Dissipation[2] ..... 600 mW
Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering 60 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:
16-Pin SOIC Package: θ_{JA} = 110°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD608AR	–25°C to +85°C, 2.7 V to 5.5 V Supplies; –40°C to +85°C, 4.5 V to 5.5 V Supplies	R-16A*

*R = Small Outline IC (SOIC). For outline information see Package Information section.

ANALOG DEVICES

Low Distortion Mixer

AD831

FEATURES

Doubly-Balanced Mixer
Low Distortion
- **+24 dBm Third Order Intercept (IP3)**
- **+10 dBm 1 dB Compression Point**

Low LO Drive Required: –10 dBm
Bandwidth
- **500 MHz RF and LO Input Bandwidths**
- **250 MHz Differential Current IF Output**
- **DC to >200 MHz Single-Ended Voltage IF Output**

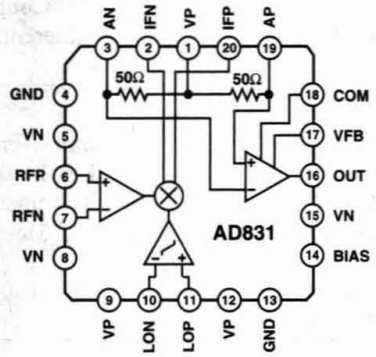
Single or Dual Supply Operation
DC Coupled Using Dual Supplies
- **All Ports May Be DC Coupled**
- **No Lower Frequency Limit—Operation to DC**

User-Programmable Power Consumption

APPLICATIONS

High Performance RF/IF Mixer
Direct to Baseband Conversion
Image-Reject Mixers
I/Q Modulators and Demodulators

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD831 is a low distortion, wide dynamic range, monolithic mixer for use in such applications as RF to IF down conversion in HF and VHF receivers, the second mixer in DMR base stations, direct-to-baseband conversion, quadrature modulation and demodulation, and doppler-shift detection in ultrasound imaging applications. The mixer includes an LO driver and a low-noise output amplifier and provides both user-programmable power consumption and 3rd-order intercept point.

The AD831 provides a +24 dBm third-order intercept point for –10 dBm LO power, thus improving system performance and reducing system cost compared to passive mixers, by eliminating the need for a high power LO driver and its attendant shielding and isolation problems.

The RF, IF, and LO ports may be dc or ac coupled when the mixer is operating from ±5 V supplies or ac coupled when operating from a single supply of 9 V minimum. The mixer operates with RF and LO inputs as high as 500 MHz.

The mixer's IF output is available as either a differential current output or a single-ended voltage output. The differential output is from a pair of open collectors and may be ac coupled via a transformer or capacitor to provide a 250 MHz output bandwidth. In down-conversion applications, a single capacitor connected across these outputs implements a low-pass filter to reduce harmonics directly at the mixer core, simplifying output filtering. When building a quadrature-amplitude modulator or image reject mixer, the differential current outputs of two AD831s may be summed by connecting them together.

An integral low noise amplifier provides a single-ended voltage output and can drive such low impedance loads as filters, 50 Ω amplifier inputs, and A/D converters. Its small signal bandwidth exceeds 200 MHz. A single resistor connected between pins OUT and FB sets its gain. The amplifier's low dc offset allows its use in such direct-coupled applications as direct-to-baseband conversion and quadrature-amplitude demodulation.

The mixer's SSB noise figure is 10.3 dB at 70 MHz using its output amplifier and optimum source impedance. Unlike passive mixers, the AD831 has no insertion loss and does not require an external diplexer or passive termination.

A programmable-bias feature allows the user to reduce power consumption, with a reduction in the 1 dB compression point and third-order intercept. This permits a tradeoff between dynamic range and power consumption. For example, the AD831 may be used as a second mixer in cellular and two-way radio base stations at reduced power while still providing a substantial performance improvement over passive solutions.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD831AP	–40°C to +85°C	20-Lead PLCC	P-20A

*For outline information see Package Information section.

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AD831—SPECIFICATIONS (T_A = +25°C and $\pm V_S$ = ±5 V unless otherwise noted; all values in dBm assume 50 Ω load.)

Parameter	Conditions	Min	Typ	Max	Units
RF INPUT					
Bandwidth	–10 dBm Signal Level, IP3 ≥ +20 dBm 10.7 MHz IF and High Side Injection See Figure 1		400		MHz
1 dB Compression Point			10		dBm
Common-Mode Range				±1	V
Bias Current	DC Coupled		160	500	µA
DC Input Resistance	Differential or Common Mode		1.3		kΩ
Capacitance			2		pF
IF OUTPUT					
Bandwidth	Single-Ended Voltage Output, –3 dB Level = 0 dBm, R_L = 100 Ω		200		MHz
Conversion Gain	Terminals OUT and VFB Connected		0		dB
Output Offset Voltage	DC Measurement; LO Input Switched ±1	–40	15	+40	mV
Slew Rate			300		V/µs
Output Voltage Swing	R_L = 100 Ω, Unity Gain		±1.4		V
Short Circuit Current			75		mA
LO INPUT					
Bandwidth	–10 dBm Input Signal Level 10.7 MHz IF and High Side Injection		400		MHz
Maximum Input Level		–1		+1	V
Common-Mode Range		–1		+1	V
Minimum Switching Level	Differential Input Signal		200		mV p-p
Bias Current	DC Coupled		17	50	µA
Resistance	Differential or Common Mode		500		Ω
Capacitance			2		pF
ISOLATION BETWEEN PORTS					
LO to RF	LO = 100 MHz, R_S = 50 Ω, 10.7 MHz IF		70		dB
LO to IF	LO = 100 MHz, R_S = 50 Ω, 10.7 MHz IF		30		dB
RF to IF	RF = 100 MHz, R_S = 50 Ω, 10.7 MHz IF		45		dB
DISTORTION AND NOISE	LO = –10 dBm, f = 100 MHz, IF = 10.7 MHz				
3rd Order Intercept	Output Referred, ±100 mV LO Input		24		dBm
2rd Order Intercept	Output Referred, ±100 mV LO Input		62		dBm
1 dB Compression Point	R_L = 100 Ω, R_{BIAS} = ∞		10		dBm
Noise Figure, SSB	Matched Input, RF = 70 MHz, IF = 10.7 MHz		10.3		dB
	Matched Input, RF = 150 MHz, IF = 10.7 MHz		14		dB
POWER SUPPLIES					
Recommended Supply Range	Dual Supply	±4.5		±5.5	V
	Single Supply	9		11	V
Quiescent Current[1]	For Best 3rd Order Intercept Point Performance BIAS Pin Open Circuited		100	125	mA

NOTES

[1]Quiescent current is programmable.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage $\pm V_S$ ..... ±5.5 V

Input Voltages

RFHI, RFLO ..... ±3 V

LOHI, LOLO ..... ±1 V

Internal Power Dissipation[2] ..... 1200 mW

Operating Temperature Range

AD831A ..... –40°C to +85°C

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature Range (Soldering 60 sec) ..... +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics:

20-Pin PLCC Package: θ_{JA} = 110°C/Watt; θ_{JC} = 20°C/Watt.

Note that the θ_{JA} = 110°C/W value is for the package measured while suspended in still air; mounted on a PC board, the typical value is θ_{JA} = 90°C/W due to the conduction provided by the AD831's package being in contact with the board, which serves as a heat sink.

ANALOG DEVICES

CMOS DDS Modulator

AD7008

FEATURES
Single +5 V Supply
32-Bit Phase Accumulator
On-Chip COSINE and SINE Look-Up Tables
On-Chip 10-Bit DAC
Frequency, Phase and Amplitude Modulation
Parallel and Serial Loading
Software and Hardware Power Down Options
20 MHz and 50 MHz Speed Grades
44-Pin PLCC

APPLICATIONS
Frequency Synthesizers
Frequency, Phase or Amplitude Modulators
DDS Tuning
Digital Modulation

PRODUCT DESCRIPTION

The AD7008 direct digital synthesis chip is a numerically controlled oscillator employing a 32-bit phase accumulator, sine and cosine look-up tables and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation, frequency modulation, and both in-phase and quadrature amplitude modulation suitable for QAM and SSB generation.

Clock rates up to 20 MHz and 50 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation may be effected by loading registers either through the parallel microprocessor interface or the serial interface. A frequency-select pin permits selection between two frequencies on a per cycle basis.

The serial and parallel interfaces may be operated independently and asynchronously from the DDS clock; the transfer control signals are internally synchronized to prevent metastability problems. The synchronizer can be bypassed to reduce the transfer latency in the event that the microprocessor clock is synchronous with the DDS clock.

A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface) The AD7008 is available in 44-pin PLCC.

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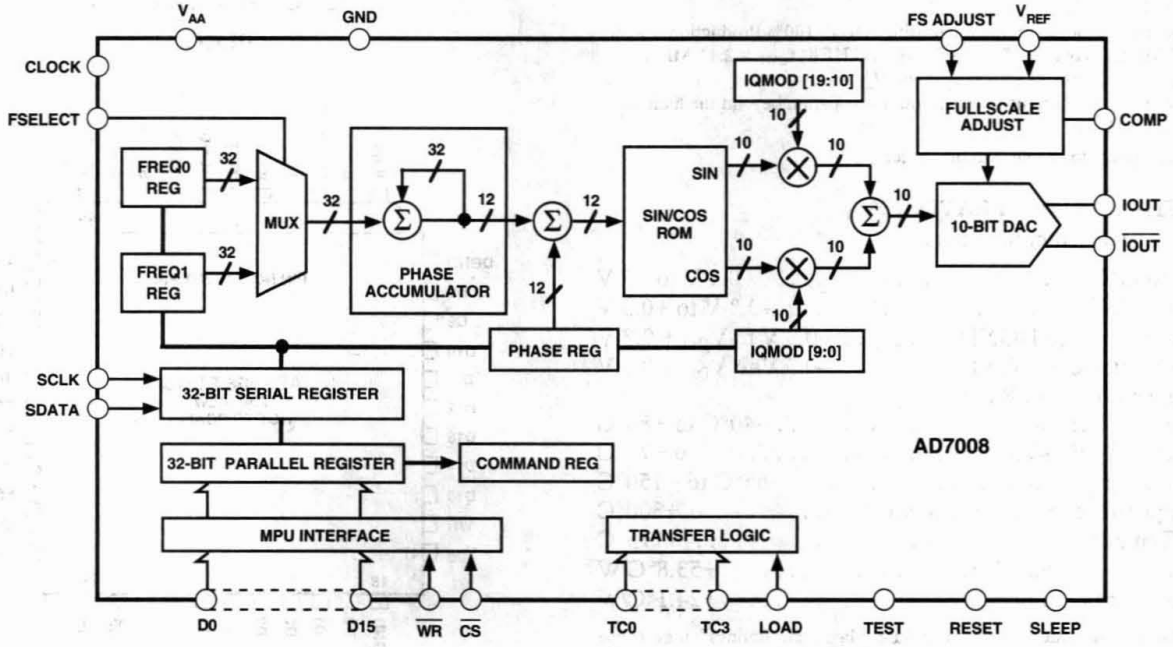
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD7008AP20	–40°C to +85°C	44-Pin PLCC	P-44A
AD7008JP50	0°C to +70°C	44-Pin PLCC	P-44A
AD7008/PCB[2]		1–3.5" Disk	

NOTES
[1]For outline information see Package Information section.
[2]AD7008/PCB DDS Evaluation Kit, assembled and tested. Kit includes an AD7008JP50.

FUNCTIONAL BLOCK DIAGRAM



AD7008–SPECIFICATIONS[1] ($V_{AA} = V_{DD} = +5$ V ± 5%; $T_A = T_{MIN}$ to T_{MAX}, $R_{SET} = 390\ \Omega$, $R_{LOAD} = 1\ \Omega$ for IOUT and $\overline{\text{IOUT}}$, unless otherwise noted)

Parameter	AD7008AP20 Min	AD7008AP20 Typ	AD7008AP20 Max	AD7008JP50 Min	AD7008JP50 Typ	AD7008JP50 Max	Units	Test Conditions/ Comments
SIGNAL DAC SPECIFICATIONS								
Resolution	10			10			Bits	
Update Rate (f_{MAX})			20			50	MSPS	
IOUT Full Scale		20			20		mA	
Output Compliance			1			1	Volts	
DC Accuracy								
Integral Nonlinearity		±1			±1		LSB	
Differential Nonlinearity		±1			±1		LSB	
DDS SPECIFICATIONS[2]								
Update Rate (f_{MAX})			20			50	MSPS	
Dynamic Specifications								
Signal-to-Noise	50			50			dB	$f_{CLK} = f_{MAX}$, f_{OUT} = 2 MHz
Total Harmonic Distortion	–55			–53			dB	$f_{CLK} = f_{MAX}$, f_{OUT} = 2 MHz
Spurious Free Dynamic Range (SFDR)[3]								
Narrow Band (±50 kHz)	–70			–70			dBc	f_{CLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Wide Band (±2 MHz)	–55			–55			dBc	
VOLTAGE REFERENCE								
Internal Reference @ +25°C[4]	1.2	1.27	1.35	1.2	1.27	1.35	Volts	
Reference TC		300			300		ppm/°C	
V_{REF} Overdrive[5]	0	2		0	2		V	
LOGIC INPUTS								
V_{INH}, Input High Voltage	V_{DD} – 0.9			V_{DD} – 0.9			Volts	
V_{INL}, Input Low Voltage			0.9			0.9	Volts	
I_{INH}, Input Current			10			10	µA	
C_{IN}, Input Capacitance			10			10	pF	
POWER SUPPLIES								
V_{DD}	4.75		5.25	4.75		5.25	Volts	
I_{AA}		26			26		mA	$R_{SET} = 390\ \Omega$
I_{DD}		22 + 1.5/MHz			22 + 1.5/MHz		mA	
$I_{AA} + I_{DD}$								
f_{CLK} = Max		80	110		125	160	mA	
Sleep = V_{DD}			10			20	mA	

NOTES

[1]Operating temperature ranges as follows: A Version: –40°C to +85°C; J Version: 0°C to +70°C.

[2]All dynamic specifications are measured using IOUT. 100% Production tested.

[3]f_{CLK} = 6.25 MHz, Frequency Word = 5671C71C HEX, f_{OUT} = 2.11 MHz.

[4]V_{REF} may be externally driven between 0 and V_{DD}.

[5]Do not allow reference current to cause power dissipation beyond the limit of $I_{AA} + I_{DD}$ shown above.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

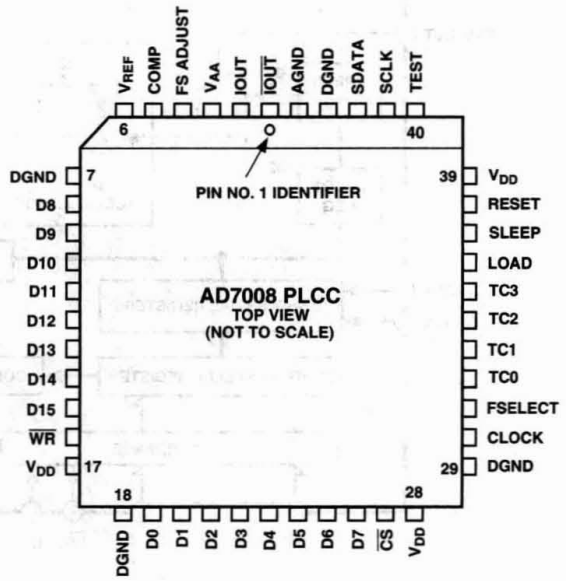
(T_A = +25°C unless otherwise noted)

V_{AA}, V_{DD} to GND ..... –0.3 V to +7 V
AGND to DGND ..... –0.3 V to +0.3 V
Digital I/O Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) ..... –40°C to +85°C
Commercial (J Version) ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Junction Temperature ..... +115°C
PLCC θ_{JA} Thermal Impedance ..... +53.8°C/W
θ_{JC} Thermal Impedance ..... +24.1°C/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION

PLCC



CMOS
JDC π/4 DQPSK Baseband Transmit Port

AD7010

FEATURES

Single +5 V Supply
- **On-Chip π/4 DQPSK Modulator**
- **Root-Raised-Cosine Tx Filters, α = 0.5**
- **Two 10-Bit D/A Converters**
- **4th Order Reconstruction Filters**
- **Differential Analog Outputs**
- **On-Chip Ramp Up/Down Power Control**
- **On-Chip Tx Offset Calibration**
- **Very Low Power Dissipation, 30 mW typ**
- **Power Down Mode < 5 μA**

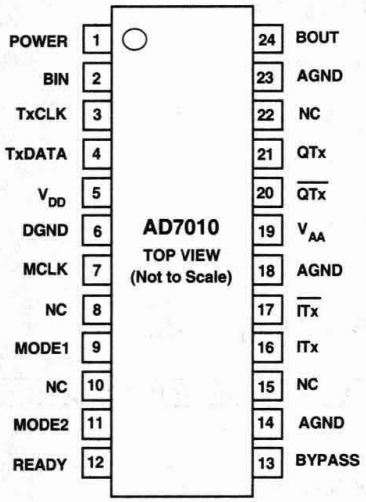
On-Chip Voltage Reference

24-Pin SSOP

APPLICATIONS

Japanese Digital Cellular Telephony

PIN CONFIGURATION



NC = NO CONNECT

GENERAL DESCRIPTION

The AD7010 is a complete low power, CMOS, π/4 DQPSK modulator with single +5 V power supply. The part is designed to perform the baseband conversion of I and Q transmit waveforms in accordance with the Japanese Digital Cellular Telephone system.

The on-chip π/4 Differential Quadrature Phase Shift Keying (DQPSK) digital modulator, which includes the Root Raised Cosine filters, generates I and Q data in response to the transmit data stream. The AD7010 also contains ramp control envelope logic to shape the I and Q output waveforms when ramping up or down at the beginning or end of a transmit burst.

Besides providing all the necessary logic to perform π/4 DQPSK modulation, the part also provides reconstruction filters to smooth the DAC outputs, providing continuous time analog outputs. The AD7010 generates differential analog outputs for both the I and Q signals.

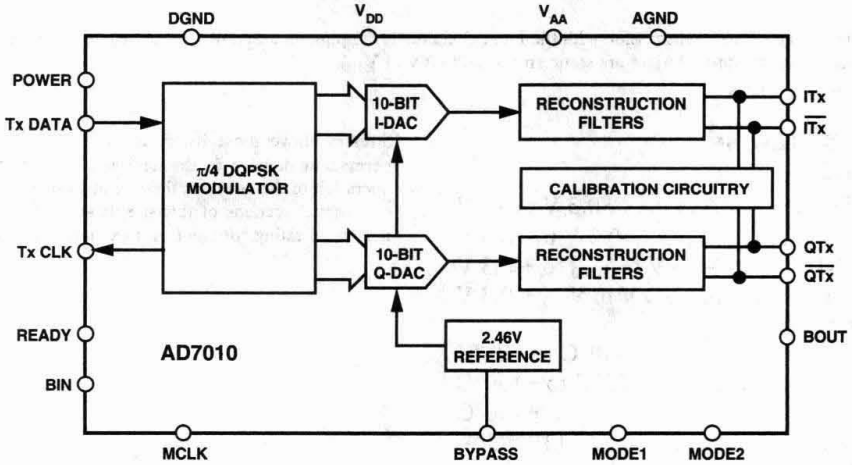
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD7010ARS	–40°C to +85°C	Shrink Small Outline Package	RS-24

*For outline information see Package Information section.

As it is a necessity for all digital mobile systems to use the lowest possible power, the device has power down options. The AD7010 is housed in a space efficient 24-pin SSOP (Shrink Small Outline Package).

FUNCTIONAL BLOCK DIAGRAM



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AD7010–SPECIFICATIONS[1]

($V_{AA} = V_{DD} = +5$ V ± 10%; Test = AGND = DGND = 0 V; $f_{MCLK} = 2.688$ MHz; Power = V_{DD}. All specifications are T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7010ARS	Units	Test Conditions/Comments
DIGITAL MODE TRANSMIT			
No. of Channels	2		(ITx–$\overline{\text{ITx}}$) and (QTx–$\overline{\text{QTx}}$)
Output Signal Range	$V_{REF} \pm V_{REF}/4$	Volts	For Each Analog Output
Differential Output Range	$\pm V_{REF}/2$	Volts	I Channel = (ITx–$\overline{\text{ITx}}$) and Q Channel = (QTx–$\overline{\text{QTx}}$)
Signal Vector Magnitude[2]	0.875 ± 7.5%	Volts max	Measured Differentially
Error Vector Magnitude[2]	1	% rms typ	
	2.5	% rms max	
Offset Vector Magnitude[2]	0.5	% typ	
	2.5	% max	
JDC Spurious Power[2, 3]			
@ 25 kHz	–30	dB typ	
	–25	dB max	
@ 50 kHz	–60	dB typ	
	–55	dB max	
@ 75 kHz	–70	dB typ	
	–65	dB max	
@ 100 kHz, 150 kHz, 200 kHz	–70	dB typ	
	–65	dB max	
REFERENCE & CHANNEL SPECIFICATIONS			
Reference, V_{REF}	2.46	Volts	
Reference Accuracy	±5	%	
I and Q Gain Matching	±0.2	dB max	Measured @ 10 kHz
Power Down Option	Yes		Power = 0 V
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	V_{DD}–0.4	V min	$\lvert I_{OUT} \rvert \le 40$ μA
V_{OL}, Output Low Voltage	0.4	V max	$\lvert I_{OUT} \rvert \le 1.6$ mA
POWER SUPPLIES			
V_{DD}	4.5/5.5	V min/V max	
I_{DD}			
Transmit Section Active	8	mA max	Power = V_{DD}
	6	mA typ	
Transmit Section Powered Down[4]	35	μA max	MCLK Active
	5	μA max	MCLK Inactive

NOTES

[1]Operating temperature ranges as follows: A Version: –40°C to +85°C.

[2]See terminology.

[3]Measured in continuous transmission and Burst transmission with the I and Q channels ramping up and down at the beginning and end of each burst.

[4]Measured while the digital inputs to the transmit interface are static and equal to 0 V or V_{DD}.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} Tx, V_{DD} Rx to AGND . . . . . –0.3 V to +7 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to V_{DD} to + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
SSOP θ_{JA} Thermal Impedance . . . . . +122°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CMOS, ADC π/4 DQPSK Baseband Transmit Port

AD7011

FEATURES

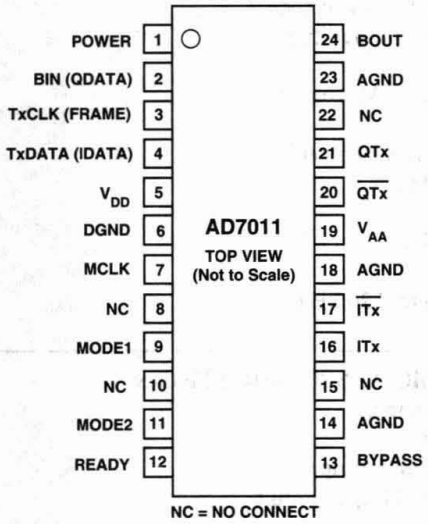
Single +5 V Supply
- **On-Chip π/4 DQPSK Modulator**
- **Modulator Bypass Analog Mode**
- **Root-Raised Cosine Tx Filters, α = 0.35**
- **Two 10-Bit D/A Converters**
- **4th Order Reconstruction Filters**
- **Differential Analog Outputs**
- **On-Chip Ramp Up/Down Power Control**
- **On-Chip Tx Offset Calibration**
- **Dual Mode Operation, Analog and Digital**
- **Very Low Power Dissipation, 30 mW typical**

Power Down Mode < 10 μA
On-Chip Voltage Reference
24-Pin SSOP

APPLICATIONS

American Digital Cellular Telephony
American Analog Cellular Telephony

SSOP PIN CONFIGURATION



NC = NO CONNECT

GENERAL DESCRIPTION

The AD7011 is a complete low power, CMOS, π/4 DQPSK modulator with single +5 V power supply. The part is designed to perform the baseband conversion of I and Q transmit waveforms in accordance with the American Digital Cellular Telephone system (TIA IS-54).

The on-chip π/4 Differential Quadrature Phase Shift Keying (DQPSK) digital modulator, which includes the root raised cosine filters, generates I and Q data in response to the transmit data stream. The AD7011 also contains ramp control envelope logic to shape the I and Q output waveforms when ramping up or down at the beginning or end of a transmit burst.

Besides providing all the necessary logic to perform π/4 DQPSK modulation, the part also provides reconstruction filters to smooth the DAC outputs, providing continuous time analog outputs. The AD7011 generates differential analog outputs for both the I and Q signals.

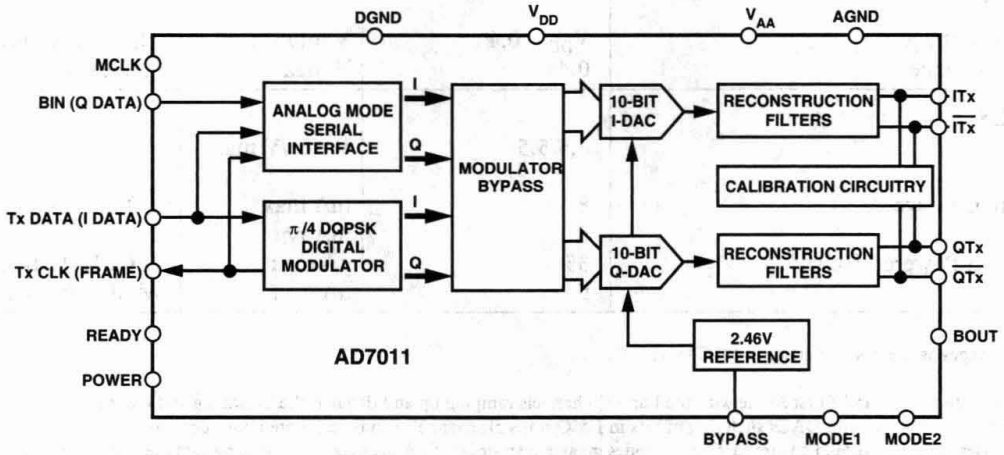
As it is a necessity for all digital mobile systems to use the lowest possible power, the device has transmit and receive power-down options. The AD7011 is housed in a space efficient 24-pin SSOP (Shrink Small Outline Package).

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD7011ARS	–40°C to +85°C	Shrink Small Outline Package	RS-24

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



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AD7011–SPECIFICATIONS[1] ($V_{AA} = V_{DD} = +5$ V ± 10%; Test = AGND = DGND = 0 V; Digital Mode, $f_{MCLK} = 3.1104$ MHz; Analog Mode, $f_{MCLK} = 2.56$ MHz, POWER = V_{DD}. All specifications are T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7011ARS	Units	Test Conditions/Comments
DIGITAL MODE TRANSMIT SPECIFICATIONS			
Number of Channels	2		(ITx – $\overline{\text{ITx}}$) and (QTx – $\overline{\text{QTx}}$)
Output Signal Range	$V_{REF} \pm V_{REF}/4$	Volts	For Each Analog Output
Differential Output Range	$\pm V_{REF}/2$	Volts	I Channel = (ITx – $\overline{\text{ITx}}$) and Q Channel = (QTx – $\overline{\text{QTx}}$)
Signal Vector Magnitude[2]	0.875 ± 7.5%	Volts max	Measured Differentially
Error Vector Magnitude[2]	1	% rms typ	
	2.5	% rms max	
Offset Vector Magnitude[2]	0.5	% typ	
	2.5	% max	
IS-54 Spurious Power[2, 3]			
@ 30 kHz	–35	dB typ	
	–30	dB max	
@ 60 kHz	–70	dB typ	
	–65	dB max	
@ 90 kHz, 120 kHz	–75	dB typ	
	–70	dB max	
ANALOG MODE SPECIFICATIONS			
No. of Channels	2		(ITx – $\overline{\text{Tx}}$) and (QTx – $\overline{\text{QTx}}$)
Resolution	10	Bits	
Output Signal Range	$V_{REF} \pm V_{REF}/3$	Volts	For Each Analog Output
Differential Output Range	$\pm 2V_{REF}/3$	Volts	I Channel = (ITx – $\overline{\text{ITx}}$) and Q Channel = (QTx – $\overline{\text{QTx}}$)
DAC Update Rate	160	kHz	MCLK/16; $f_{MCLK} = 2.56$ MHz
SNR	60	dB typ	Generating a 10 kHz Sine Wave
	55	dB min	
Differential Offset Error	±15	mV max	Post Calibration
Group Delay Matching Between I & Q Outputs	30	ns typ	
Coding	Twos Complement		
Maximum and Minimum DAC Codes[4]	+450/–450	max/min	
REFERENCE & CHANNEL SPECIFICATIONS			
Reference, V_{REF}	2.46	Volts	
Reference Accuracy	±5	%	
I and Q Gain Matching	±0.2	dB max	Measured @ 10 kHz
Power-Down Option	Yes		Power = 0 V
LOGIC INPUTS			
V_{INH}, Input High Voltage	$V_{DD} - 0.9$	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH} Output High Voltage	$V_{DD} - 0.4$	V min	$\lvert I_{OUT} \rvert \leq 40$ μA
V_{OL} Output Low Voltage	0.4	V max	$\lvert I_{OUT} \rvert \leq 1.6$ mA
POWER SUPPLIES			
V_{DD}	4.5/5.5	V min/V max	
I_{DD}			
Transmit Section Active	8	mA max	POWER = V_{DD}
	6	mA typ	
Transmit Section Powered Down[5]	35	μA max	MCLK Active
	5	μA max	MCLK Inactive

NOTES

[1]Operating temperature ranges as follows: A Version: –40°C to +85°C.

[2]See terminology.

[3]Measured in continuous transmission and Burst Mode with the I and Q channels ramping up and down at the beginning and end of a burst.

[4]Headroom must be allowed for the transmit DACs such that offsets in I & Q transmit channels can be calibrated out. Therefore, the full range of the I and Q DACs are not available to the user. The user should ensure that binary codes greater than or less than the maximum or minimum are not loaded into the I or Q DACs.

[5]Measured while the digital inputs to the transmit interface are static and equal to 0 V or V_{DD}.

Specifications subject to change without notice.

CMOS TIA IS-54 Baseband Receive Port

AD7013

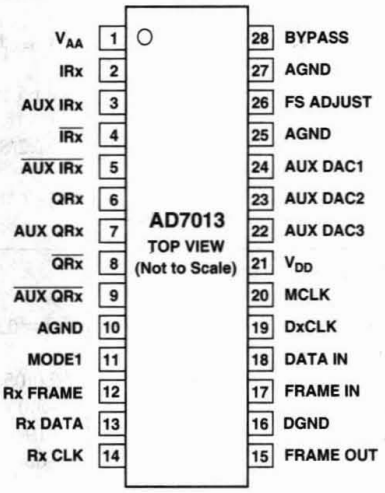
FEATURES

- Single +5 V Supply
- Receive Channel
  - Differential or Single-Ended Analog Inputs
  - Auxiliary Set of Analog I & Q Inputs
  - Two Sigma-Delta A/D Converters
  - Choice of Two Digital FIR Filters
    - Root-Raised-Cosine Rx Filters, $\alpha = 0.35$
    - Brick Wall FIR Rx Filters
  - On-Chip or User Rx Offset Calibration
  - ADC Sampling Vernier
- Three Auxiliary DACs
- On-Chip Voltage Reference
- Low Active Power Dissipation, Typical 45 mW
- Low Sleep Mode Power Dissipation, <50 μW
- 28-Pin SSOP

APPLICATIONS

- American TIA Digital Cellular Telephony
- American Analog Cellular Telephony
- Digital Baseband Receivers

PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7013 is a complete low power, CMOS, TIA IS-54 baseband receive port with single +5 V power supply. The part is designed to perform the baseband conversion of I and Q waveforms in accordance with the American (TIA IS-54) Digital Cellular Telephone system.

The receive path consists of two high performance sigma-delta ADCs, each followed by a FIR digital filter. A primary and auxiliary set of IQ differential analog inputs are provided, where either can be selected as inputs to the sigma-delta ADCs. Also, a choice of two frequency responses are available for the receive FIR filters; a Root-Raised-Cosine filter for digital mode or a brick wall response for analog mode. Differential analog inputs are provided for both I and Q channels. On-chip calibration logic is also provided to remove either on-chip offsets or remove system offsets. A 16-bit serial interface is provided, interfacing easily to most DSPs. The receive path also provides a means to vary the sampling instant, giving a resolution to 1/32 of a symbol interval.

The auxiliary section provides two 8-bit DACs and one 10-bit DAC for functions such as automatic gain control (AGC), automatic frequency control (AFC) and power amplifier control.

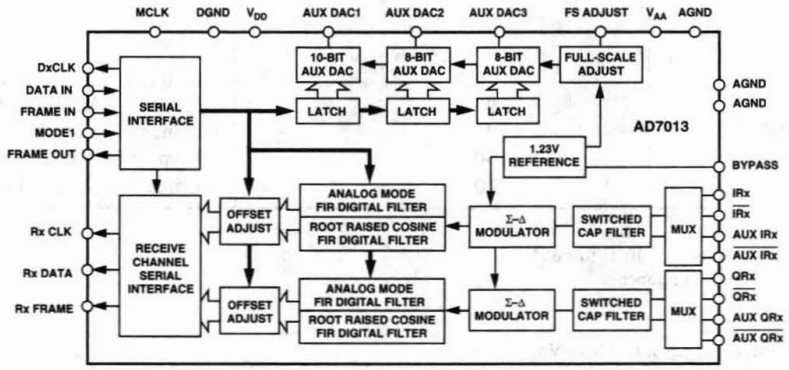
As it is a necessity for all digital mobile systems to use the lowest possible power, the device has receive and auxiliary power down options. The AD7013 is housed in a space efficient 28-pin SSOP (Shrink Small Outline Package).

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7013ARS	–40°C to +85°C	RS-28

*RS = SSOP. For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



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AD7013–SPECIFICATIONS[1] ($V_{AA} = V_{DD} = +5$ V ± 10%; AGND = DGND = 0 V; $f_{MCLK} = 6.2208$ MHz; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	AD7013A	Units	Test Conditions/Comments
RECEIVE SECTION			
ADC SPECIFICATION			
Number of ADC Channels	2		
Resolution	15	Bits	
ADC Signal Range	2.6	Volts p-p	Measured Using an Input Sine Wave of 3 kHz
Differential Signal Range	V_{BIAS} ± 0.65	Volts	For Both Noninverting and Inverting Analog Inputs
Single-Ended Signal Range	V_{BIAS} ± 1.3	Volts	For Noninverting Analog Inputs; Inverting Analog Inputs = V_{BIAS}
V_{BIAS}	0.65 to (V_{AA} – 0.65)	Volts min/max	Differential
	1.3 to (V_{AA} – 1.3)	Volts min/max	Single-Ended
Output Word Rate	97.2/80	kHz	MCLK = 6.2208 MHz/5.12 MHz; 4 × Sampling of the Symbol Rate, MCLK/64
	48.6/40	kHz	MCLK = 6.2208 MHz/5.12 MHz; 2 × Sampling of the Symbol Rate, MCLK/128
RECEIVE DIGITAL FILTERS			
Digital Mode			MCLK = 6.2208 MHz
Root-Raised-Cosine	$\alpha = 0.35$		
Frequency Response			
0–7.8975 kHz	±0.05	dB max	
11.9 kHz	–3.0	dB	
16.4025 kHz	–19	dB	
> 30 kHz	–66	dB max	
Analog Mode			MCLK = 5.12 MHz
Brick Wall Filter			
Frequency Response			
0–8 kHz	0 to –0.5	dB max	
11.4 kHz	–3.0	dB	
15 kHz	–24	dB	
>17 kHz	–68	dB max	
TIA IS-54 RECEIVE SPECIFICATIONS			
Error Vector Magnitude[3]	2	% rms typ	Measured Using a Full-Scale Input
Error Offset Magnitude[3]	1	% rms typ	

AUXILIARY SECTION

	AUX DAC1	AUX DAC2	AUX DAC3		
Resolution	10	8	8	Bits	
DC Accuracy					
Integral	±3	±1	±1	LSBs max	
Differential	–1.5/+4	±1	±1	LSBs max	AUX DAC2 & AUX DAC3 Guaranteed Monotonic

REFERENCE SPECIFICATIONS			
V_{REF}	1.23	Volts typ	
Reference Accuracy	±5	% max	
Reference Impedance	20	kΩ typ	
POWER SUPPLIES			
V_{DD}	4.5/5.5	V_{MIN}/V_{MAX}	
I_{DD}[5]			
All Sections Active	10.5	mA max	CR14 = CR15 = CR16 = CR17 = 1
	9	mA typ	MCLK = 6.2208 MHz
All Sections Powered Down[6]	2	mA max	MCLK = 6.2208 MHz
	30	µA typ	MCLK =100 kHz
	10	µA max	MCLK Inactive, MCLK = 0 V

NOTES

[1]Operating temperature ranges as follows: A version: –40°C to +85°C.

[2]SNR calculation includes noise and distortion components.

[3]See Terminology.

[4]Sampled tested only.

[5]Measured while the digital inputs are static and equal to 0 V or V_{DD}.

[6]With all sections powered down, I_{DD} is proportional to the capacitive load on DxCLK. For example, I_{DD} is typically 1.7 mA with 80 pF load and 600 µA with 10 pF load.

Specifications subject to change without notice.

ANALOG DEVICES

Complete 3 V GSM/DCS1800 Codec

AD7015

FEATURES

+2.7 V to +5.5 V Supply Voltage
Baseband Codec
- **Baseband Serial Port (BSPORT)**
- **Differential IRx, QRx, ITx and QTx**
- **Transmit Channel**
  - **On-Chip Burst Store**
  - **On-Chip GMSK Modulator**
  - **Two 10-Bit D/A Converters**
  - **Analog Reconstruction Filters**
  - **On-Chip Offset Calibration**
  - **Power-Down Mode**
- **Receive Channel**
  - **Two 15-Bit Sigma-Delta A/D Converters**
  - **FIR Digital Filters**
  - **60 dB SNR and THD**
  - **Twos Complement Coding**
  - **On-Chip Offset Calibration**
  - **Power-Down Mode**

Auxiliary D/A Converters
Auxiliary A/D Converter
Auxiliary Serial Port (ASPORT)
On-Chip Ramp-Up/Ramp-Down Envelope RAM
Voiceband Codec
- **Complete Linear Coded Codec**
- **16-Bit Sigma-Delta A/D Converter**
- **16-Bit Sigma-Delta D/A Converter**
- **On-Chip Antialiasing and Anti-Imaging Filters**
- **8 kHz Sampling Rate**
- **Twos Complement Coding**
- **60 dB SNR and 62.5 dB THD**
- **Programmable Gain on DAC and ADC**
- **Voiceband Serial Port (VSPORT)**
- **Full DAI Support**
- **Power-Down Mode**

On-Chip Voltage References
Low Power
Multiple 3 V/5 V Operating Modes
80-Pin TQFP

APPLICATIONS

GSM
DCS1800

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7015AST	–25°C to +85°C	ST-80

*ST = Thin Quad Flatpack (TQFP). For outline information see Package Information section.

GENERAL DESCRIPTION

The AD7015 is a monolithic 3 V/5 V CMOS combined voiceband codec/baseband codec for use in GSM mobile telephones. The chip performs all the data conversion functions needed in a GSM mobile cellular system and DCS1800 networks.

The baseband codec is a complete low power, two-channel, input/output port with signal conditioning. This section is utilized as a baseband digitization subsystem performing signal conversion between the DSP and the IF/RF sections in the Pan-European telephone system (GSM) and DCS1800 networks.

The transmit path consists of an onboard ROM, containing all the code necessary for performing Gaussian Minimum Shift Keying (GMSK) and two high accuracy, fast DACs with output reconstruction filters. The receive path is composed of two high performance sigma-delta ADCs with digital filtering. A common bandgap reference feeds the ADCs and signal DACs. The baseband functions of the AD7015 can be accessed via the baseband serial port (BSPORT) or the auxiliary serial port (ASPORT).

The voiceband codec is a complete analog front-end for high performance voiceband and DSP applications. The voiceband codec's linear-coded DAC and ADC maintain wide dynamic range throughout the transfer function while maintaining far superior SNR and THD in comparison to traditional μ-law and A-law codecs. It includes on-chip antialiasing and anti-imaging filters, 16-bit ADC, 16-bit DAC and programmable gain amplifiers. A serial I/O port (VSPORT) allows easy interfacing to industry standard DSP processors. Data transfers between the DSP and the AD7015 are 16 bits wide. The AD7015 VSPORT also supports the GSM Digital Audio Interface (DAI) standard where 13-bit transfers are used. The voiceband codec can be controlled using any of the three SPORTs.

Three control DACs are included for such functions as AFC, AGC and RF power control signals. A three channel ADC completes the available auxiliary converter functions. The auxiliary functions can be accessed via the auxiliary port (ASPORT) or the baseband port (BSPORT).

As it is a necessity for all GSM and DCS1800 mobile systems to use the lowest power possible, the device has power-down or sleep options for all sections. By setting appropriate bits in the on-chip control registers, power consumption can be reduced to a minimum.

The AD7015 is housed in an 80-pin TQFP.

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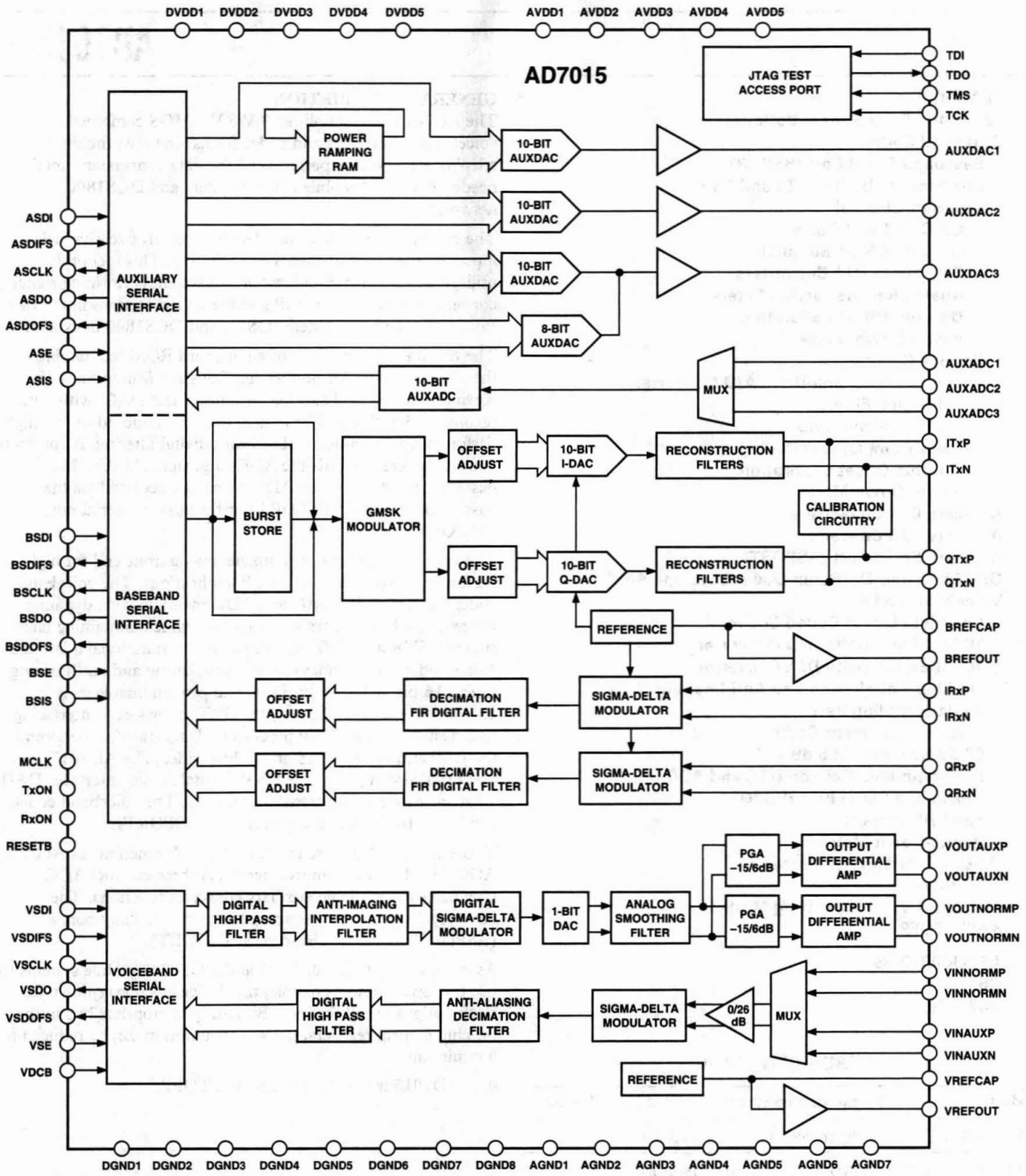
FUNCTIONAL BLOCK DIAGRAM



ANALOG DEVICES

CMOS Complete DDS

AD9830

FEATURES
+5 V Power Supply
50 MHz Speed
On-Chip SINE Look-Up Table
On-Chip 10-Bit DAC
Parallel Loading
Power-Down Option
72 dB SFDR
250 mW Power Consumption
48-Pin TQFP

APPLICATIONS
DDS Tuning
Digital Demodulation

GENERAL DESCRIPTION

This DDS device is a numerically controlled oscillator employing a phase accumulator, a sine look-up table and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 50 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation is effected by loading registers through the parallel microprocessor interface.

A power-down pin allows external control of a power-down mode. The part is available in a 48-pin TQFP package.

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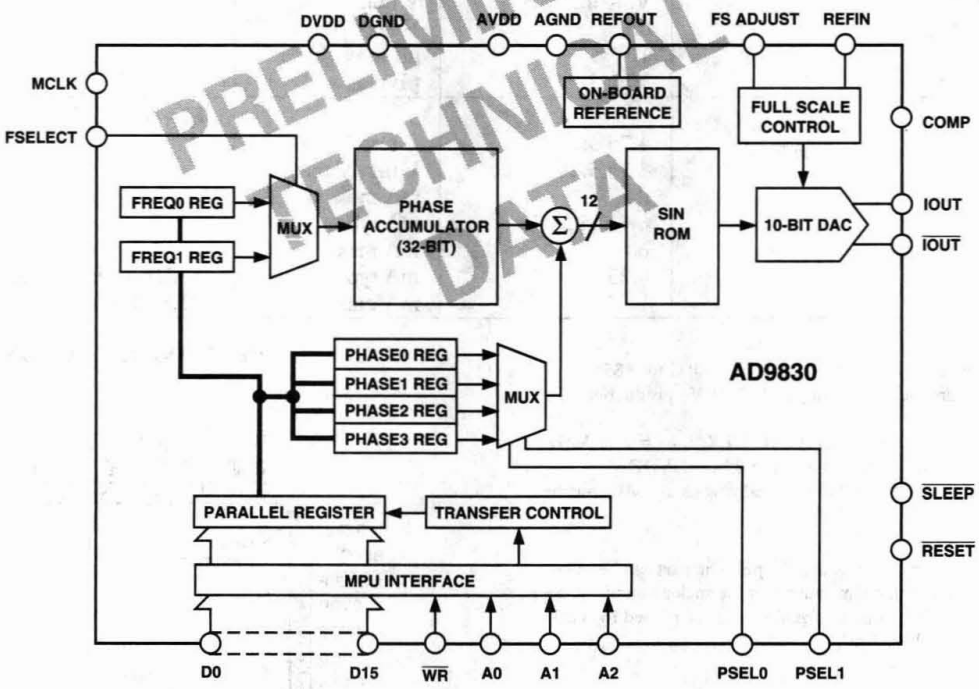
PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



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AD9830–SPECIFICATIONS[1] (V_{DD} = +5 V ± 5%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}; REFIN = REFOUT; R_{SET} = 1 kΩ; R_{LOAD} = 51 Ω for IOUT and $\overline{IOUT}$ unless otherwise noted)

Parameter	AD9830A	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (f_{MAX})	50	MSPS max	
I_{OUT} Full Scale	20	mA max	
Output Compliance	1	V max	
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±0.5	LSB typ	
DDS SPECIFICATIONS[2]			
Dynamic Specifications			
Signal-to-Noise Ratio	50	dB min	f_{MCLK} = f_{MAX} , f_{OUT} = 2 MHz
Total Harmonic Distortion	–53	dBc max	f_{MCLK} = f_{MAX} , f_{OUT} = 2 MHz
Spurious Free Dynamic Range (SFDR)[3]			f_{MCLK} = 6.25 MHz, f_{OUT} = 2.11 MHz
Narrow Band			
(±50 kHz)	–72	dBc min	
(±200 kHz)	–68	dBc min	
Wide Band (±2 MHz)	–50	dBc min	
Clock Feedthrough	–55	dBc typ	
Wake Up Time	1	ms typ	
Power-Down Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ +25°C	1.21	Volts typ	
T_{MIN} to T_{MAX}	1.21 ± 7%	Volts min/max	
REFIN Input Impedance	10	MΩ typ	
Reference TC	100	ppm/°C typ	
REFOUT Impedance	300	Ω typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	μA max	
C_{IN}, Input Capacitance	10	pF max	
POWER SUPPLIES			f_{OUT} = 2 MHz
AVDD	4.75/5.25	V min/V max	
DVDD	4.75/5.25	V min/V max	
I_{AA}	25	mA max	
I_{DD}	6 + 0.5/MHz	mA typ	
I_{AA} + I_{DD}[4]	60	mA max	
Low Power Sleep Mode[5]	0.25	mA typ	1 MΩ Resistor Tied Between
	1	mA max	REFOUT and AGND

PRELIMINARY TECHNICAL DATA

NOTES

[1]Operating temperature range is as follows: A Version: –40°C to +85°C.

[2]All dynamic specifications are measured using IOUT. 100% production tested.

[3]f_{MCLK} = 6.25 MHz, Frequency Word = 5671C71C HEX, f_{OUT} = 2.11 MHz.

[4]Measured with the digital inputs static and equal to 0 V or DVDD.

[5]The Low Power Sleep Mode current is 2 mA typically when a 1 MΩ resistor is not tied from REFOUT to AGND.

The AD9830 is tested with a capacitive load of 50 pF. The part can be operated with higher capacitive loads, but the magnitude of the analog output will be attenuated. For example, a 10 MHz output signal will be attenuated by 3 dB when the load capacitance equals 250 pF.

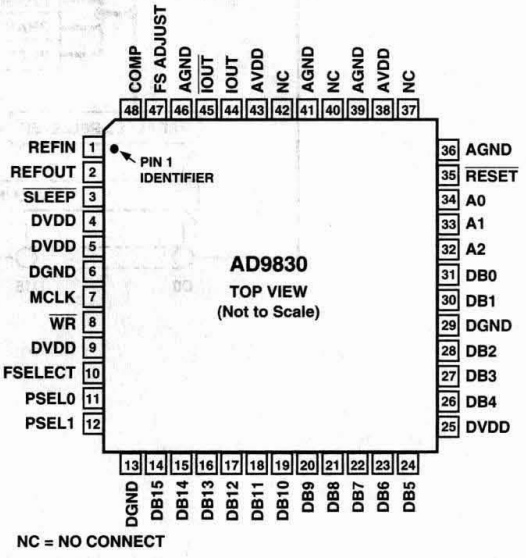
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9830AST	–40°C to +85°C	ST-48

*ST = Thin Quad Flatpack (TQFP). For outline information see Package Information section.

PIN CONFIGURATION



NC = NO CONNECT

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ANALOG DEVICES

CMOS Complete DDS

AD9831

FEATURES
3 V/5 V Power Supply
15 MHz Speed
On-Chip SINE Look-Up Table
On-Chip 10-Bit DAC
Parallel Loading
Powerdown Option
70 dB SFDR
150 mW (5 V) Power Consumption
35 mW (3 V) Power Consumption
48-Pin TQFP

APPLICATIONS
DDS Tuning
Digital Demodulation

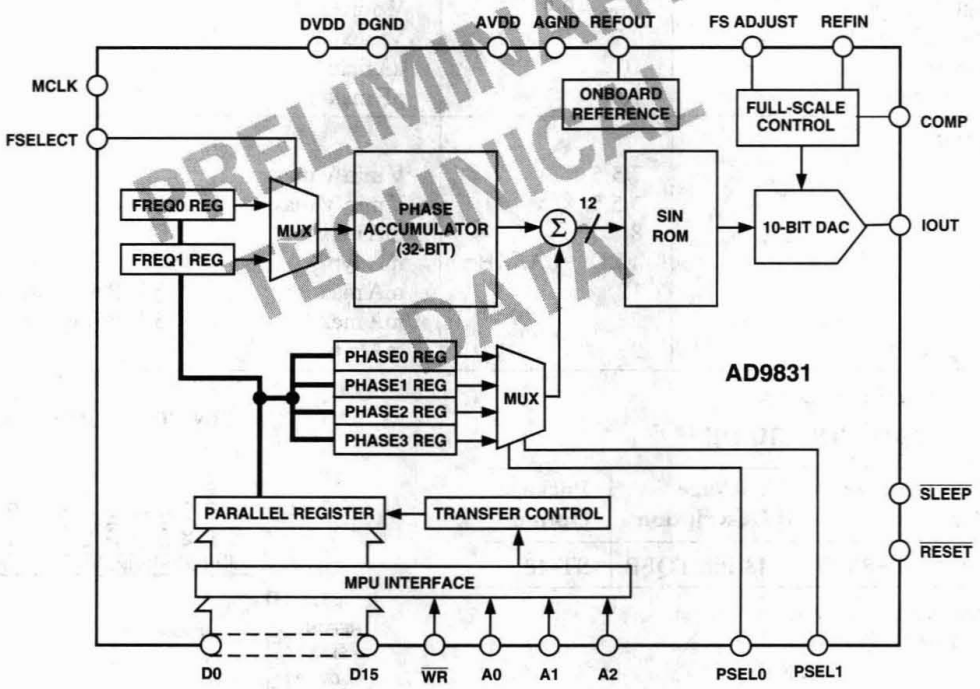
GENERAL DESCRIPTION

This DDS device is a numerically controlled oscillator employing a phase accumulator, a sine look-up table and a 10-bit D/A converter integrated on a single CMOS chip. Modulation capabilities are provided for phase modulation and frequency modulation.

Clock rates up to 15 MHz are supported. Frequency accuracy can be controlled to one part in 4 billion. Modulation is effected by loading registers through the parallel microprocessor interface.

A powerdown pin allows external control of a powerdown mode. The part is available in a 48-pin TQFP package.

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

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AD9831–SPECIFICATIONS

(V_{DD} = +3.3 V ± 10%; +5 V ± 10%; T_A = T_{MIN} to T_{MAX}; REFIN = REFOUT; R_{SET} = 3.9 kΩ; R_{LOAD} = 300 Ω for IOUT unless otherwise noted.)

Parameter	AD9831A	Units	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS			
Resolution	10	Bits	
Update Rate (F_{MAX})	15	MSPS nom	
I_{OUT} Full Scale	4	mA nom	
Output Compliance	TBD	V max	
DC Accuracy			
Integral Nonlinearity	±1	LSB typ	
Differential Nonlinearity	±1	LSB typ	
DDS SPECIFICATIONS[1]			
Dynamic Specifications			
Signal to Noise Ratio	50	dB min	F_{CLK} = 15 MHz, F_{OUT} = 600 MHz
Total Harmonic Distortion	–55	dB max	F_{CLK} = 15 MHz, F_{OUT} = 600 MHz
Spurious Free Dynamic Range (SFDR)			
Narrow Band (±15 kHz)	–70	dB min	F_{CLK} = 1.875 MHz, F_{OUT} = 633 kHz
Wide Band (±600 MHz)	–55	dB min	
Powerdown Option	Yes		
VOLTAGE REFERENCE			
Internal Reference @ 25°C	1.235	Volts typ	
T_{MIN} to T_{MAX}	1.235 ± 7%	Volts min/max	
Reference TC	300	ppm/°C typ	
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD} – 0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
POWER SUPPLIES			
AVDD	3/5.5	V min/V max	
DVDD	3/5.5	V min/V max	
I_{AA}	8	mA max	
I_{DD}	TBD + 0.1/MHz	mA typ	
I_{AA} + I_{DD}	12	mA max	3 V Power Supply
	28	mA max	3 V Power Supply
Low-Power Sleep Mode	2	mA typ	

PRELIMINARY TECHNICAL DATA

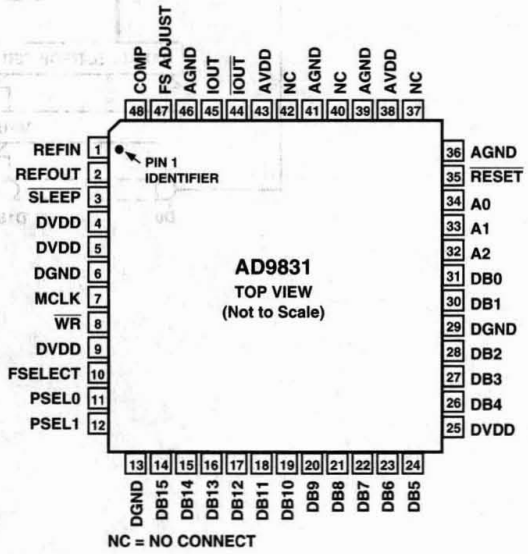
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9831AST	–40°C to +85°C	48-Pin TQFP	ST-48

*For outline information see Package Information section.
ST = Thin Quad Flatpack (TQFP)

PIN CONFIGURATION



NC = NO CONNECT

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

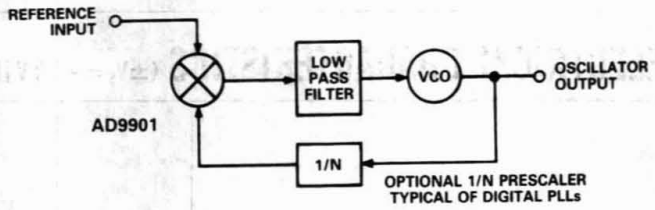
Ultrahigh Speed Phase/Frequency Discriminator

AD9901

FEATURES
Phase and Frequency Detection
ECL/TTL/CMOS Compatible
Linear Transfer Function
No "Dead Zone"
MIL-STD-883 Compliant Versions Available

APPLICATIONS
Low Phase Noise Reference Loops
Fast-Tuning "Agile" IF Loops
Secure "Hopping" Communications
Coherent Radar Transmitter/Receiver Chains

PHASE-LOCKED LOOP



GENERAL DESCRIPTION

The AD9901 is a digital phase/frequency discriminator capable of directly comparing phase/frequency inputs up to 200 MHz. Processing in a high speed trench-oxide isolated process, combined with an innovative design, gives the AD9901 a linear detection range, free of indeterminate phase detection zones common to other digital designs.

With a single +5 V supply, the AD9901 can be configured to operate with TTL or CMOS logic levels; it can also operate with ECL inputs when operated with a –5.2 V supply. The open-collector outputs allow the output swing to be matched to post-filtering input requirements. A simple current setting resistor controls the output stage current range, permitting a reduction in power when operated at lower frequencies.

A major feature of the AD9901 is its ability to compare phase/frequency inputs at standard IF frequencies without prescalers. Excessive phase uncertainty which is common with standard PLL configurations is also eliminated. The AD9901 provides the locking speed of traditional phase/frequency discriminators, with the phase stability of analog mixers.

The AD9901 is available as a commercial temperature range device, 0°C to +70°C, and as a military temperature device, –55°C to +125°C. The commercial versions are packaged in a 14-pin ceramic DIP and a 20-pin PLCC.

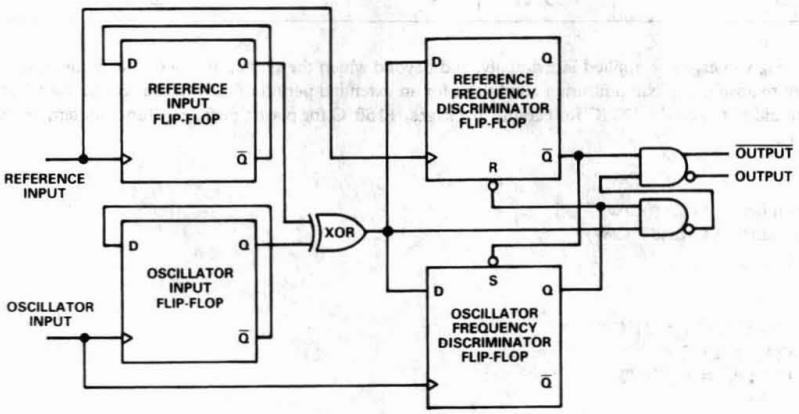
The AD9901 Phase/Frequency Discriminator is available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current AD9901/883B data sheet for specifications.

ORDERING GUIDE

Model	Temperature	Descriptions	Package Option[1]
AD9901KQ	0°C to +70°C	14-Pin Ceramic DIP	Q-14
AD9901KP	0°C to +70°C	20-Pin PLCC	P-20A
AD9901TQ/883[2]	–55°C to +125°C	14-Pin Ceramic DIP	Q-14
AD9901TE/883[2]	–55°C to +125°C	20-Contact Ceramic LCC	E-20A

NOTES
[1]E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Infomation section.
[2]For specifications, refer to Analog Devices *Military Products Databook.*

FUNCTIONAL BLOCK DIAGRAM



AD9901–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage (+V_S for TTL Operation) . . . . . +7 V
Negative Supply Voltage (–V_S for ECL Operation) . . . . . –7 V
Input Voltage Range (TTL Operation) . . . . . 0 V to +5.5 V
Differential Input Voltage (ECL Operation) . . . . . 4.0 V
I_{SET} Current . . . . . 12 mA
Output Current . . . . . 30 mA
Operating Temperature Range
AD9901KQ/KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature[2]
Plastic . . . . . +150°C
Ceramic . . . . . +175°C
Lead Soldering Temperature (l0sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS ($\pm V_S$ = +5.0 V [for TTL] or –5.2 V [for ECL], unless otherwise noted)

	Temp	Test Level	Commercial Temperature 0°C to +70°C AD9901KQ/KP Min	Typ	Max	Units
INPUT CHARACTERISTICS						
TTL Input Logic "1" Voltage	Full	VI	2.0			V
TTL Input Logic "0" Voltage	Full	VI			0.8	V
TTL Input Logic "1" Current[3]	Full	VI			0.6	mA
TTL Input Logic "0" Current[3]	Full	VI			1.6	mA
ECL Differential Switching Volt.	Full	VI	300			mV
ECL Input Current	Full	VI			20	µA
OUTPUT CHARACTERISTICS						
Peak-to-Peak Output Voltage Swing[4]	Full	VI	1.6	1.8	2.0	V
TTL Output Compliance Range	Full	V		3–7		V
ECL Output Compliance Range	Full	V		±2		V
I_{OUT} Range	Full	V		0.9–11		mA
Internal Reference Voltage	Full	VI	0.42	0.47	0.52	V
AC CHARACTERISTICS						
Linear Phase Detection Range[4]						
40 kHz	+25°C	V		360		Degrees
30 MHz	+25°C	V		320		Degrees
70 MHz	+25°C	V		270		Degrees
Functionality @ 70 MHz	+25°C	I		Pass/Fail		
POWER SUPPLY CHARACTERISTICS						
TTL Supply Current (+5.0 V)[5, 6]	+25°C	I		43.5	54.0	mA
	Full	I		43.5	54.0	mA
ECL Supply Current (–5.2 V)[5, 6]	+25°C	I		42.5	52.5	mA
	Full	I		42.5	52.5	mA
Nominal Power Dissipation	+25°C	V		218		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the service ability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Maximum junction temperature should not exceed +175°C for ceramic packages, +150°C for plastic packages. Junction temperature can be calculated by:

$t_J = PD\ (\theta_{JA}) + t_A = PD\ (\theta_{JC}) + t_C$

where:

PD = power dissipation
θ_{JA} = thermal impedance from junction to air (°C/W)
θ_{JC} = thermal impedance from junction to case (°C/W)
t_A = ambient temperature (°C)
t_C = case temperature (°C)

typical thermal impedances:

AD9901 Ceramic DIP = θ_{JA} = 74°C/W; θ_{JC} = 21°C/W
AD9901 LCC = θ_{JA} = 80°C/W; θ_{JC} = 19°C/W
AD9901 PLCC = θ_{JA} = 88.2°C/W; θ_{JC} = 45.2°C/W

[3]V_L = +0.4 V; V_H = +2.4 V.

[4]R_{SET} = 47.5 Ω; R_L = 182 Ω.

[5]Includes load current of 10 mA (load resistors = 182 Ω).

[6]Supply should remain stable within ±5% for normal operation.

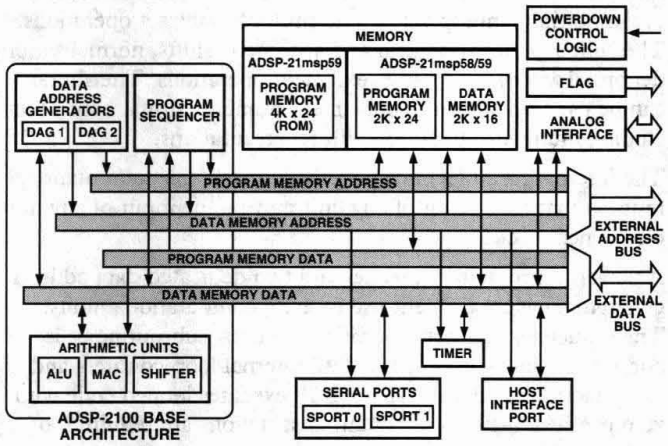
Specifications subject to change without notice.

ADSP-21msp58/59

FEATURES

- 38 ns Instruction Cycle Time (26 MIPS) from 13.00 MHz Crystal
- ADSP-2100 Family Code and Function Compatible with New Instruction Set Enhanced for Bit Manipulation Instructions, Multiplication Instructions, Biased Rounding, and Global Interrupt Masking
- 2K × 24 Words of On-Chip Program Memory RAM
- 2K × 16 Words of On-Chip Data Memory RAM
- 4K × 24 Words of On-Chip Program Memory ROM (ADSP-21msp59 Only)
- 8-Bit Parallel Host Interface Port
- Analog Interface Provides:
  - 16-Bit Sigma-Delta ADC and DAC
  - Programmable Gain Stages
  - On-Chip Anti-Aliasing & Anti-Imaging Filters
  - 8 kHz Sampling Frequency
  - 65 dB ADC, SNR and THD
  - 72 dB DAC, SNR and THD
- 425 mW Typical Power Dissipation @ 5.0 V @ 38 ns
- <1 mW Powerdown Mode with 100 Cycle Recovery
- Dual Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides:
  - Zero Overhead Looping
  - Conditional Instruction Execution
- Two Double-Buffered Serial Ports with Companding Hardware, One Serial Port (SPORT0) has Automatic Data Buffering
- Programmable 16-Bit Interval Timer with Prescaler
- Programmable Wait State Generation
- Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Host Interface Port
- Stand-Alone ROM Execution (ADSP-21msp59 Only)
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- Multifunction Instructions
- Three Edge- or Level-Sensitive External Interrupts
- Low Power Dissipation in Standby Mode
- 100-Lead TQFP

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-21msp58 and ADSP-21msp59 Mixed-Signal Processors (MSProcessor® DSPs) are fully integrated, single-chip DSPs complete with a high performance analog front end. The ADSP-21msp58/59 Family is optimized for voice band applications such as Speech Compression, Speech Processing, Speech Recognition, Text-to Speech, and Speech-to-Text conversion.

The ADSP-21msp58/59 combines the ADSP-2100 base architecture (three computation units, data address generators, and program sequencer) with two serial ports, a host interface port, an analog front end, a programmable timer, extensive interrupt capability, and on-chip program and data memory.

The ADSP-21msp58 provides 2K words (24-bit) of program RAM and 2K words (16-bit) of data memory. The ADSP-21msp59 provides an additional 4K words (24-bit) of program ROM. The ADSP-21msp58/59 integrates a high performance analog codec based on a single chip, voice band codec, the AD28msp02. Powerdown circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-21msp58/59 is available in a 100-pin TQFP package (thin quad flat package).

In addition, the ADSP-21msp58/59 supports new instructions, which include bit manipulations–bit set, bit clear, bit toggle, bit test–new ALU constants, new multiplication instruction (x squared), biased rounding, and global interrupt masking.

MSProcessor is a registered trademark of Analog Devices, Inc.

DIGITAL ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-21msp58/59. The processors contain three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-21msp58/59 executes looped code with zero overhead—no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers to (and from) on-chip memory.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA, DMA) share a single external address bus, allowing memory to be expanded off chip, and the two data buses (PMD, DMD) share a single external data bus. The $\overline{\text{BMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{PMS}}$ signals indicate which memory space the external buses are being used for.

Program memory can store both instructions and data, permitting the ADSP-21msp58/59 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-21msp58/59 can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of the processors' buses with the use of the bus request/grant signals ($\overline{\text{BR}}$ and $\overline{\text{BG}}$). Bus grant has two modes of operation. If GoMode is enabled in the MSTAT register, instruction execution continues from internal memory. If GoMode is disabled, the processor stops instruction execution and waits for deassertion of $\overline{\text{BR}}$.

In addition to the address and data bus for external memory connection, the ADSP-21msp58/59 has a host interface port (HIP) for easy connection to a host processor. The HIP is made up of 8 data/address pins and 10 control pins. The HIP is extremely flexible and provides a simple interface to a variety of host processors. For example, the Motorola 68000 series, the Intel 80C51 series, and the Analog Devices ADSP-2101 can be easily connected to the HIP. The host processor can boot the ADSP-21msp58/59 on-chip memory through the HIP.

The ADSP-21msp58/59 can respond to eleven interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive, and seven internal interrupts generated by the Timer, the Serial Ports (SPORTs), the HIP, the powerdown circuitry, and the analog interface. There is also a master $\overline{\text{RESET}}$ signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

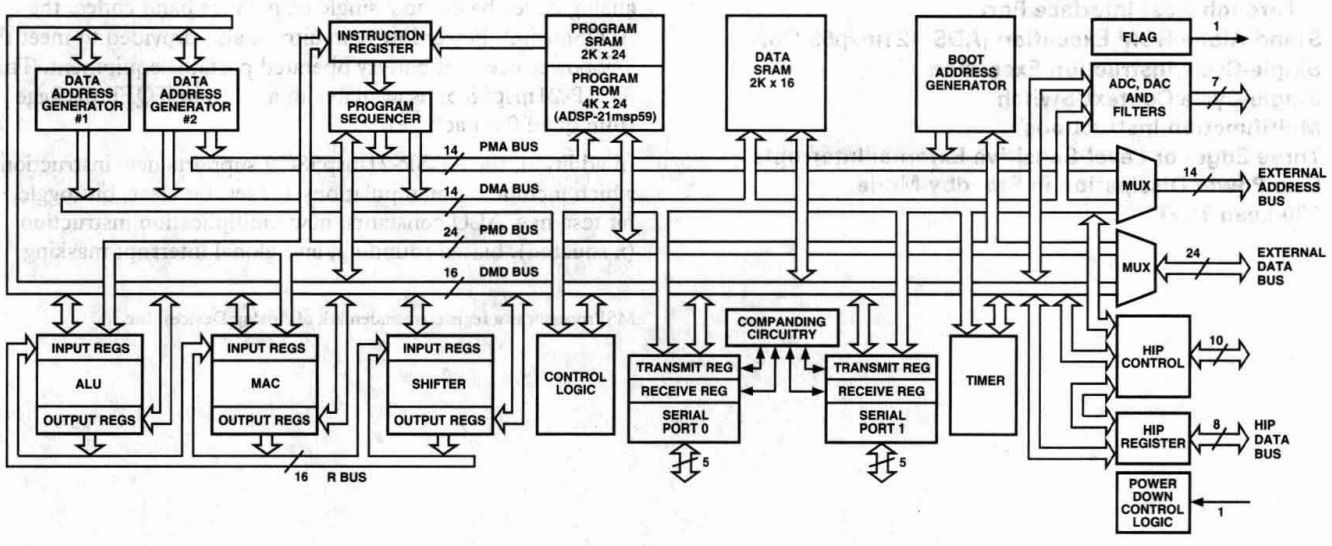


Figure 1. ADSP-21msp58/59 Block Diagram

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Computer & Digital/Audio Circuits–Selection Guides

Stereo & Computer Audio

Linear

Singles

Model	# Bits	# D/As	Over Sample × FS	Power Supply Requirements $+V_{CC}$ Volts	Gain Error % FS	Mid-scale Error max	THD+N @ 1 kHz 0 dB %	SNR dB	Channel Separation dB	# Pins	Page No.	Comments	Fax-code
AD1851J	16	1	16	±5 @ 13 mA	1	±10 mV	0.004	107		16	18–15		1064
AD1861J	18	1	16	±5 @ 15 mA	2	±30 mV	0.008	107		16	18–15		1067
AD1862J	20	1	16	±5–12 @ 15 mA	2	±5 µA	0.0025	110		16	18–21		1068
AD1862K	20	1	16	±5–12 @ 15 mA	2	±5 µA	0.0016	113		16	18–21		1068

Duals

Model	# Bits	# D/As	Over Sample × FS	Power Supply Requirements $+V_{CC}$ Volts	Gain Error % FS	Mid-scale Error max	THD+N @ 1 kHz 0 dB %	SNR dB	Channel Separation dB	# Pins	Page No.	Comments	Fax-code
AD1866J	16	2	8	+5 @ 3 mA	3	±30 mV	0.01	95	108	16	18–25	Single Supply	1071
AD1864J	18	2	8	±5–12 @ 15 mA	1	±15 mV	0.006	102	108	24	*		1069
AD1864K	18	2	8	±5–12 @ 15 mA	1	±15 mV	0.004	102	108	24	*		1069
AD1865J	18	2	16	±5 @ 26 mA	1	±4 mV	0.006	107	110	24	18–23		1070
AD1865K	18	2	16	±5 @ 26 mA	1	±4 mV	0.004	107	110	24	18–23		1070
AD1868N	18	2	8	+5 @ 14 mA	1	±15 mV	0.008	95	108	16	18–27	Single Supply	1072
AD1868N-J	18	2	8	+5 @ 14 mA	1	±15 mV	0.008	95	108	16	18–27	Single Supply	1072

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Sigma-Delta

Model	# Bits	# D/As	Over Sample Rate	Power Supply Requirements $+V_{CC}$ Volts	Serial I/O	THD+N @ 1 kHz 0 dB %	SNR dB	Interpolation Filter Sample Rate	# Pins	Page No.	Comments	Fax-code
AD1859	16/18	2	Variable	+5 @ 60 mA	All	90	94	Variable	28	18–19	On-Chip Async Master Clock, 27 MHz	1853
AD1857	16	2	256/384	+5 @ 60 mA	DSP	90	96.00	128	28	18–17		1988
AD1858	16	2	256/384	+5 @ 60 mA	I^2S	90	96.00	128	28	18–17		1988

Sample Rate Converters

Model	# Bits	Power V_S V	Power I_S mA	Dynamic Range 20 Hz to 20 kHz dB	THD+N 1 kHz FS Input –dB	THD+N 10 kHz FS Input –dB	F_{SAMPLE} Rate kHz	# Pins	Page No.	Comments	Fax-code
AD1890	20	+5	40	120	94	106	8–56	28	18–33	Short/Long Group Delay Modes	1077
AD1891	16	+5	40	96	96	95	8–56	28	18–33		1077
AD1893	16	+3.3	20	96	94	96	8–56	28/44	18–35	4-Wire Serial with Right Justified	1821

Computer & Digital/Audio Circuits–Selection Guides

Mixed Signal Processor

Model	Description	# Pins	Page No.	Comments	Fax-code
AD1812	ADSP-2171 DSP Core and 16-Bit Stereo Codec, ADPCM Compress/Decompress	160	18–5	Compatible with All Sound Standards	1944

SoundPort®

Model	Description	# Pins	Page No.	Comments	Fax-code
AD1847	16-Bit, Serial Port, Sample Rate 5.5 kHz to 49 kHz	44	18–11	Multiple Stereo Inputs	1061
AD1849	16-Bit, Serial Port, Sample Rate 5.5 kHz to 49 kHz	44	18–13	CS4215 Compatible	1063
AD1843	16-Bit, Serial Port, Integrated Speech, Audio and Fax Modem Functions with 1 Hz Resolution Programmable Sample Rate 4 > 54 kHz	80	18–7	Quad D/A	1565
AD1845	16-Bit, Parallel Port, ISA & EISA Bus Compatible	68/100	18–9	CS4248/4231 Compatible	1900

Duals: Audio Sigma-Delta

Model	# Bits	Over Sample Rate	Power Supply Requirements $+V_{CC}$ Volts	THD Plus Noise @ 1 kHz dB	SNR dB	Frequency Response @			# Pins	Page No.	Comments	Fax-code
AD1878	16	256	±/5 @ 13 mA	98	98	21 kHz	25 kHz	26 kHz	28	18–31		1075
AD1877	16	256/384	+5 @ 80 mA	86	90				28	18–29		1074
AD1879	18	64	±/5 @ 13 mA	98	103	0 dB	–30 dB	–120 dB	28	18–31		1076

SoundPort is a registered trademark of Analog Devices, Inc.

ANALOG DEVICES

SoundPort Controller

AD1812

FEATURES

Compatibility with:
- **Sound Blaster Pro***
- **AdLib***
- **Windows* Sound System**

16-Bit ΣΔ Stereo Codec
MPC Level-2+ Mixer
Dual DMA/Full Duplex Operation
On-Chip FIFO Buffers
Sample Rates from 5.5 kHz to 50 kHz
ADPCM Compression/Decompression
Plug and Play Compliant
Compatible MIDI MPU-401 Port
Integrated Game Port
Free Supporting Software:
- **Windows 3.1 Driver**
- **Windows 95 Driver**
- **Control Applets**
- **Diagnostics**

Power Management Modes
Operation from +5 V Supply
16-Bit Parallel Interface to ISA Bus
24 mA Bus Drive Capability

*Sound Blaster Pro is a trademark of Creative Labs, Ltd.
AdLib is a trademark of AdLib Multimedia.
Windows is a trademark and Microsoft is a registered trademark of Microsoft Corp.
SoundPort is a registered trademark of Analog Devices, Inc.

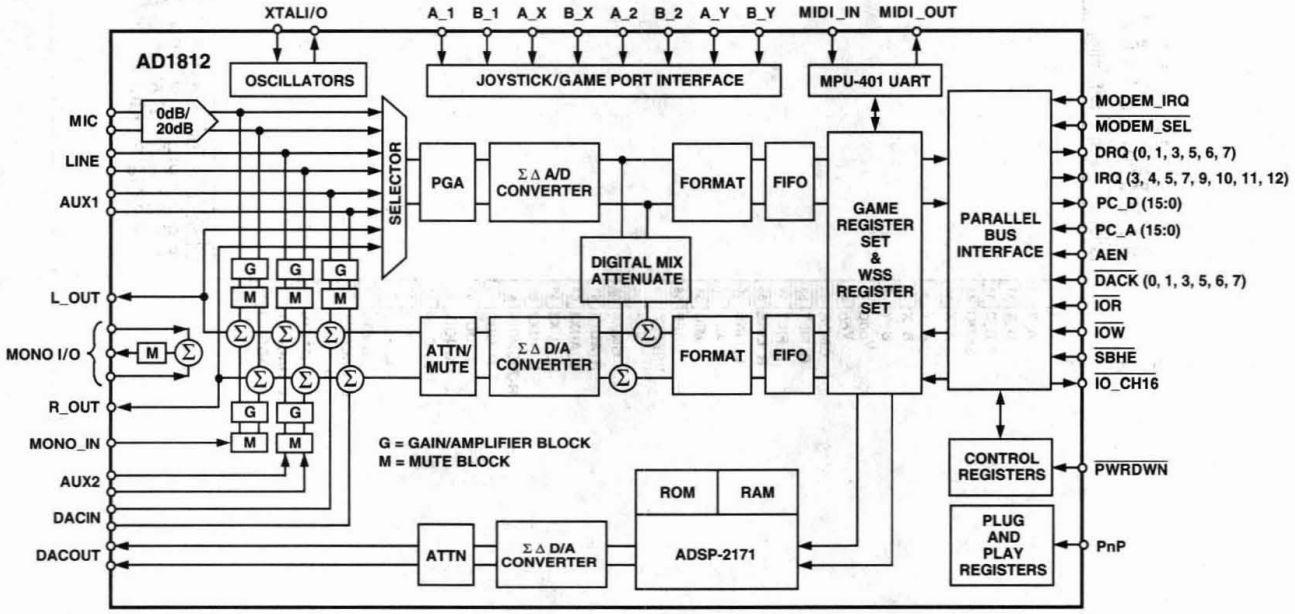
PRODUCT OVERVIEW

The AD1812 SoundPort® Controller is a single chip audio subsystem for adding 16-bit stereo audio to personal computers. The AD1812 is compatible with Sound Blaster Pro, AdLib, and the Microsoft* Windows Sound System. The AD1812 provides an integrated audio solution for enhanced business audio, entertainment sound effects, and multimedia applications.

The AD1812 audio subsystem combines an integrated digital audio controller, a powerful signal processor, a mixer, and a 16-bit ΣΔ stereo codec. The DOS games register set, the Windows Sound System register set, music synthesis hardware, an MPU-401 compatible UART interface, a game port (with timer), and a Plug and Play ISA interface are all contained on chip. The on-chip Plug and Play (PnP) routine provides configuration services for the internal logical devices and an external modem chipset.

The AD1812 can record compress and playback voice, sound and music. The system provides all PC 95 audio conversion and compatibility requirements for a multimedia enabled PC.

FUNCTIONAL BLOCK DIAGRAM

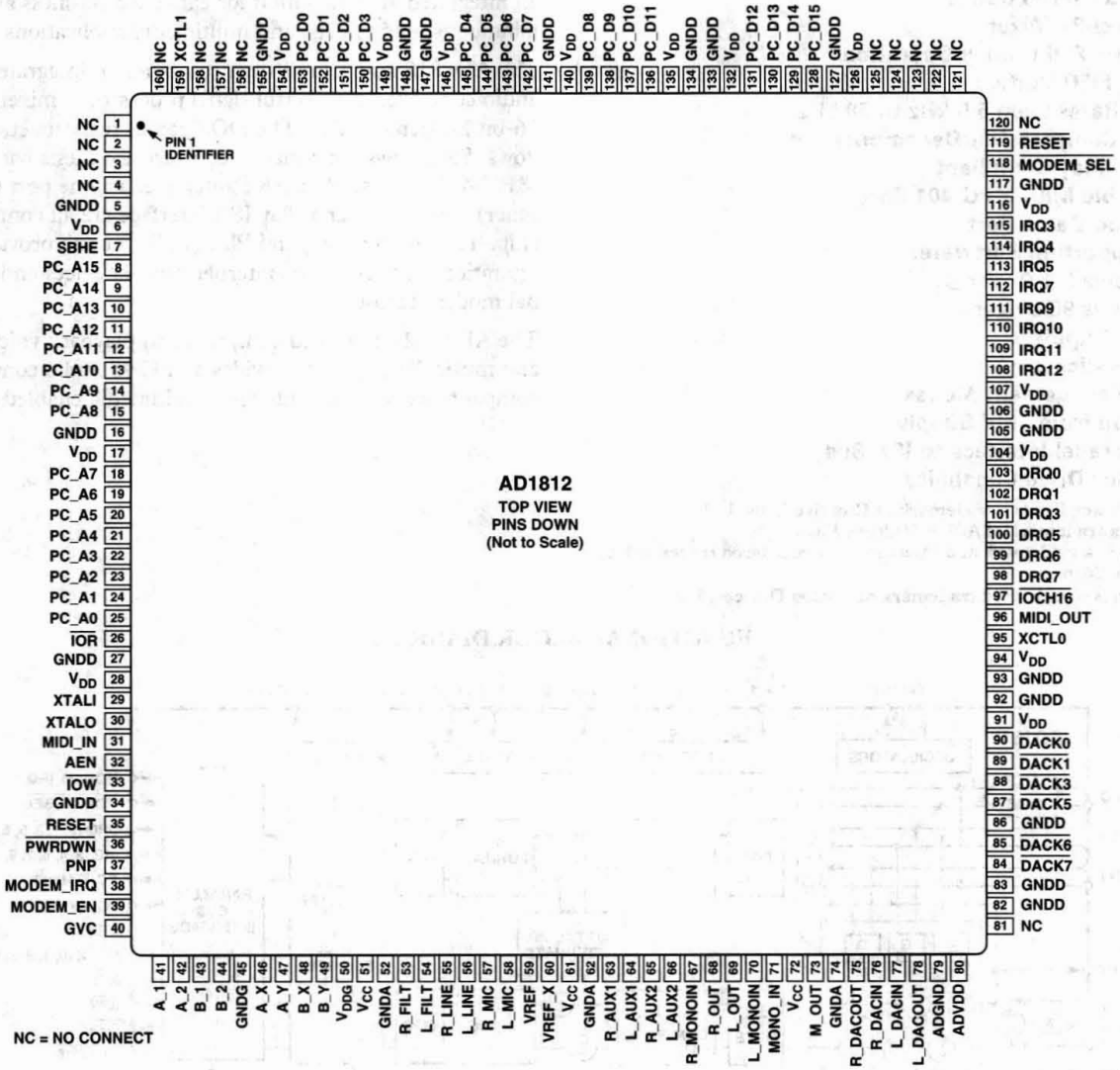


ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1812JS	0°C to +70°C	160-Lead PQFP	S-160
AD1812JST	0°C to +70°C	160-Lead TQFP	ST-160

*For outline information see Package Information section.

PQFP AND TQFP PIN LOCATIONS



Serial-Port 16-Bit SoundComm Codec

AD1843

FEATURES

Single Chip Integrated Speech, Audio, Fax and Modem Codec
Highly Configurable Stereo ΣΔ ADCs and Quad ΣΔ DACs
Supports V.34, V.32bis, and Fallback Modem Standards As Well As Voice Over Data
Dual Digital Resamplers with Programmable Input and Output Phase and Frequency
Three On-Chip Phase Lock Loops for Synchronization to External Signals, Including Video
Thirteen Analog Inputs and Seven Analog Outputs
Advanced Analog and Digital Signal Mixing and Digital-to-Digital Sample Rate Conversion
Programmable Gain, Attenuation and Mute
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low Pass
1 Hz Resolution Programmable Sample Rates from 4 kHz to 54 kHz Derived from a Single Clock Input
80-Lead PQFP and 100-Lead TQFP Packages
Operation from +5 V or Mixed +5 V/+3 V Supplies
FIFO-Buffered Serial Digital Interface Compatible with ADSP-21xx Fixed-Point DSPs
Advanced Power Management
VHDL Model of Serial Port Available; Evaluation Board and MAFE Board Available

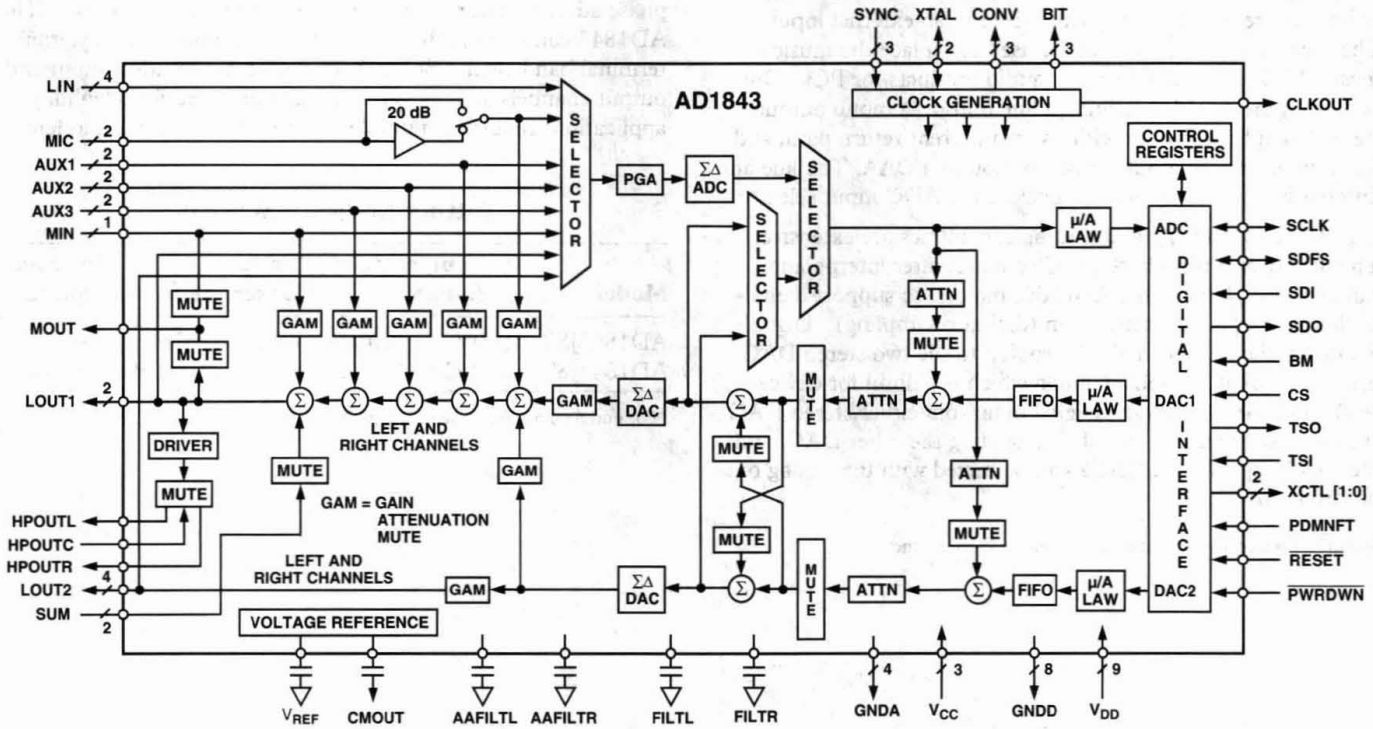
GENERAL PRODUCT DESCRIPTION

The AD1843 SoundComm™ Codec is a complete analog front end for high performance DSP-based telephony and audio applications. The device integrates the real-world analog I/O requirements for many popular functions thereby reducing size, power consumption, and system complexity. The AD1843 SoundComm is the world's first codec which can support four different sample rates simultaneously, without any beat frequency noise issues. This is essential for highly integrated audio/modem/fax products since the sample rates associated with audio are very much distinct from the sample rates associated with telephony-oriented data communication. It is also the first codec to offer on-chip digital phase lock loops for sample rate synchronization to external clock signals. This sample rate flexibility is enabled through Analog Devices' Continuous Time Oversampling (CTO) technology.

The main elements of the AD1843 are its extensive input and mixing section, its two channels of sigma-delta (ΣΔ) analog-to-digital conversion, its four channels of ΣΔ digital-to-analog conversion, its digital filters, and the clock and control circuitry for implementing the device's different modes. The AD1843 permits flexible sample-rate selection through programming and external synchronization, many input and output options, and many mixing options.

SoundComm is a trademark of Analog Devices, Inc.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



The versatility of the device is shown by the following examples of functions it can perform:

- Stereo audio input and/or quad output, simultaneously at different sample rates
- Stereo audio output with simultaneous full duplex modem or fax operation with frequency and phase resampling
- Mono audio input and stereo audio output with simultaneous modem receive and transmit for simultaneous voice and data communications
- Dual independent audio inputs with audio output for echo-cancelling speakerphones

Audio Functional Description

The AD1843 SoundComm codec provides a complete audio solution with very few external components required. Dynamic range of the device exceeds 80 dB over the 20 kHz audio band and sample rates from 4 kHz to 49 kHz are supported (up to 54 kHz for a single channel if other channels are powered down). The audio functionality of this device is a superset of that found in the Analog Devices AD1848 SoundPort® device which has set the business audio standard throughout the computer industry.

Inputs to the device include a stereo microphone pair, a stereo line pair, a stereo CD input pair (AUX1), a stereo synthesized music input pair (AUX2), a dual phone line input (AUX3), a mono input, and a stereo input from an FM synthesizer (SUM). All of these inputs (except SUM) are multiplexed to the two ΣΔ A/D converters and are mixable directly as analog signals with the outputs of the D/A converters. All analog input signals (except SUM) can be amplified, attenuated or muted before mixing with the outputs of the D/A converters.

The device has two pairs of ΣΔ DACs which accept 8- or 16-bit digital data from the serial port. Each DAC pair's independent sampling rate can either be programmed by Control Register (with 1 Hz resolution) or synchronized to an external input. The second pair of DACs can be used to replace the music synthesis DAC pair found on many audio products for PCs. Outputs from the AD1843 include a line output, a mono output, a stereo headphone output with its own current return path, and a differential stereo output for connection to a DAA. The line and differential outputs are looped back to the ADC input selector.

The AD1843's mixing and routing capabilities are extensive. The digital data from both DAC channels after interpolation can be routed back to the ADC decimators, to support digital-to-digital sample rate conversion (digital resampling). Digital data from the ADC can also be routed to the two stereo DAC pairs, for a digital loopback mode which is helpful for device-level and board-level test. Digital data from either stereo DAC can be mixed with the digital data feeding the other DAC, and the analog signal from DAC2 can be mixed with the analog output from DAC1.

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Sample rates are independently programmable in the range of 4 kHz to 54 kHz to a 1 Hz resolution or sample rates can be synchronized to an external source. Up to three different signals can be applied to the device's three digital phase lock loop SYNC inputs for external synchronization.

These SYNC inputs can also be used in a special mode for audio/video synchronization. In this mode, an NTSC or PAL derived clock signal (approximately 15 kHz) is applied to the SYNC inputs and the device produces one of a variety of standard audio sample rates (32 kHz, 44.056 kHz, 44.1 kHz and 48 kHz, and most of these divided by the integers 1 through 8). In this manner, video and audio sample rates which are mathematically unrelated can be locked together.

Data Communications/Telephony Functional Description

The AD1843 includes all data conversion, filtering, and clock generation circuitry needed to implement an echo-cancelling modem with a companion digital signal processor. Software-programmable sample rates and clocking modes support all established modem standards including those for the V.34 standard.

The AD1843 utilizes advanced ΣΔ technology to move the entire echo-cancelling modem implementation into the digital domain. The device maintains 90 dB typical dynamic range throughout all filtering and data conversion across a 9.6 kHz passband. Purely DSP-based echo cancellation algorithms can maintain robust bit error rates under worst-case signal attenuation and echo amplitude conditions. The AD1843's on-chip interpolation filter resamples (both frequency and phase) the received signal after echo cancellation in the DSP, freeing the processor for other voice or data communications tasks.

On-chip bit and baud clock generation circuitry allows either synchronous or asynchronous operation of the transmit (DAC) and receive (ADC) paths. Each path features independent phase advance and retard adjustments via software control. The AD1843 can also synchronize modem operation to an external terminal band clock. Because the device has multiple input and output channels and converters, it is well suited for telephony applications requiring multiple channels for voice and modem.

ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option*
AD1843JS	0°C to +70°C	80-Lead PQFP	S-80
AD1843JST	0°C to +70°C	100-Lead TQFP	ST-100

*For outline information see Package Information section.

Parallel-Port 16-Bit SoundPort Stereo Codec

AD1845

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Microsoft* and Windows* Sound System Compatible
MPC Level-2+ Compliant Mixing
16 mA Bus Drive Capability
Supports Two DMA Channels for Full Duplex Operation
On-Chip Capture and Playback FIFOs
Advanced Power-Down Modes
Programmable Gain and Attenuation
Sample Rates from 4.0 kHz to 50 kHz Derived from a Single Clock or Crystal Input
68-Lead PLCC, 100-Lead TQFP Packages
Operation from +5 V Supplies
Byte-Wide Parallel Interface to ISA and EISA Buses
Pin Compatible with AD1848, AD1846, CS4248, CS4231

PRODUCT OVERVIEW

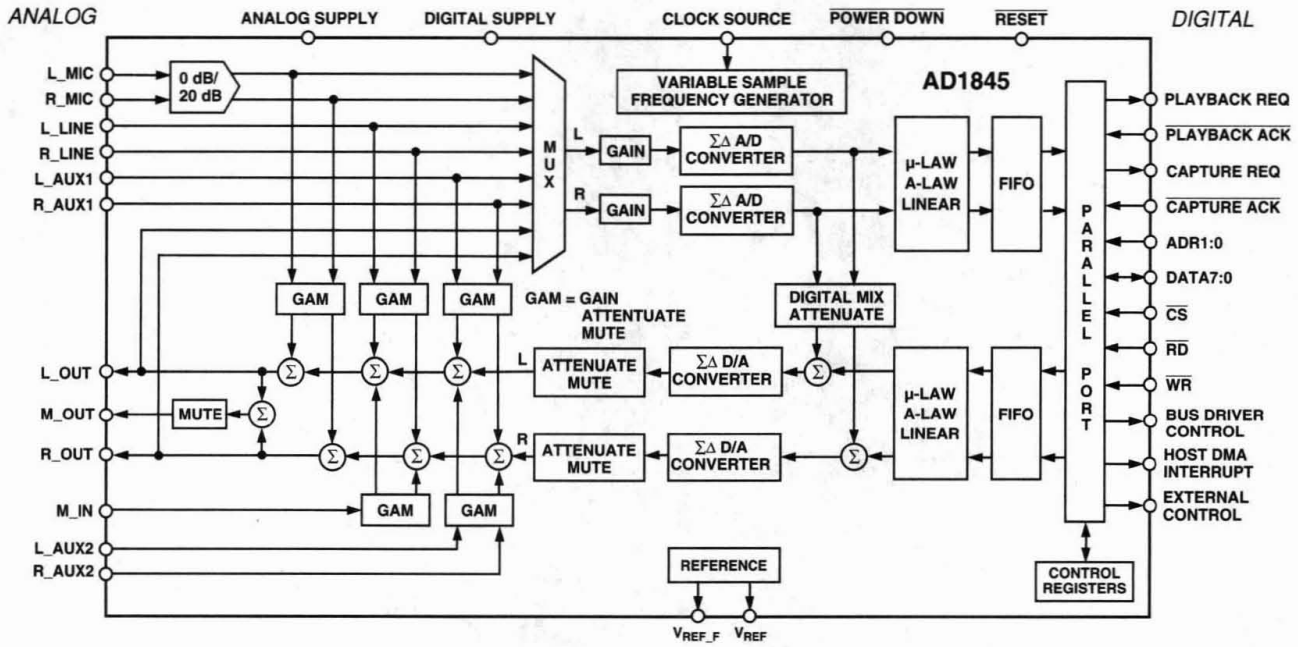
The Parallel Port AD1845 SoundPort® Stereo Codec integrates key audio data conversion and control functions into a single integrated circuit. The AD1845 provides a complete, single chip computer audio solution for business audio and multimedia applications. The codec includes stereo audio converters, complete on-chip filtering, MPC Level-2 compliant analog mixing, programmable gain, attenuation and mute, a variable sample frequency generator, FIFOs, and supports advanced power-down modes. It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card.

The AD1845 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. Two input control lines support mixed direct and indirect addressing of thirty-seven internal control registers over this asynchronous interface. The AD1845 includes dual DMA count registers for full duplex operation enabling the AD1845 to capture data on one DMA channel and play back data on a separate channel. The FIFOs on the AD1845 reduce the risk of losing data when making DMA transfers over the ISA/EISA bus. The FIFOs buffer data transfers and allow for relaxed timing in acknowledging requests for capture and playback data.

External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. Dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 4 kHz to 50 kHz are supported from a single external crystal or clock source.

*Microsoft is a registered trademark of Microsoft Corporation.
Windows is a trademark of Microsoft Corporation.
SoundPort is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



The AD1845 has built-in 8/16 mA (user selectable) bus drivers. If 24 mA drive capability is required, the AD1845 generates enable and direction controls for IC bus buffers such as the 74_245.

The codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. The AD1845 mixer surpasses MPC Level-2 recommendations. Inputs to the ADC can be selected from four stereo pairs of analog signals: line (LINE), microphone (MIC), auxiliary line #1 (AUX1), and post-mixed DAC output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. In addition, the analog mixer allows the mono input (M_IN), MIC, AUX1, LINE and auxiliary line #2 (AUX2) signals to be mixed with the DACs' output. The ADCs' output can be digitally mixed with the DACs' input.

The pair of 16-bit outputs from the ADCs is available over a byte-wide bidirectional interface that also supports 16-bit digital input to the DACs and control information. The AD1845 can accept and generate 16-bit twos complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantized noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters.

The AD1845 supports multiple low power and power-down modes to support notebook and portable computing multimedia applications. The ADC, DAC, and mixer paths can be suspended independently allowing the AD1845 to be used for capture-only or playback-only, lessening power consumption and extending battery life.

The AD1845 includes a variable sample frequency generator, that allows the codec to instantaneously change sample rates with a resolution of 1 Hz without "clicks" and "pops". Additionally, ΣΔ quantization noise is kept out of the 20 kHz audio band regardless of the chosen sample rate. The codec uses the variable sample frequency generator to derive all internal clocks from a single external crystal or clock source.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1845JP	0°C to +70°C	68-Lead PLCC	P-68A
AD1845JST	0°C to +70°C	100-Lead TQFP	ST-100

*For outline information see Package Information section.

Serial-Port 16-Bit SoundPort Stereo Codec

AD1847

FEATURES

- **Single-Chip Integrated ΣΔ Digital Audio Stereo Codec**
- **Supports the Microsoft Windows Sound System***
- **Multiple Channels of Stereo Input**
- **Analog and Digital Signal Mixing**
- **Programmable Gain and Attenuation**
- **On-Chip Signal Filters**
  - **Digital Interpolation and Decimation**
  - **Analog Output Low-Pass**
- **Sample Rates from 5.5 kHz to 48 kHz**
- **44-Lead PLCC and TQFP Packages**
- **Operation from +5 V Supplies**
- **Serial Digital Interface Compatible with ADSP-21xx Fixed-Point DSP**

PRODUCT OVERVIEW

The AD1847 SoundPort® Stereo Codec integrates key audio data conversion and control functions into a single integrated circuit. The AD1847 is intended to provide a complete, low cost, single-chip solution for business, game audio and multimedia applications requiring operation from a single +5 V supply. It provides a serial interface for implementation on a computer motherboard, add-in or PCMCIA card. See Figure 1 for an example system diagram.

SoundPort is a registered trademark of Analog Devices, Inc.
Windows Sound System is a registered trademark of Microsoft Corporation.

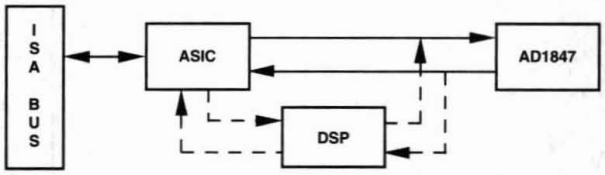


Figure 1. Example System Diagram

External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. Dynamic range exceeds 70 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals.

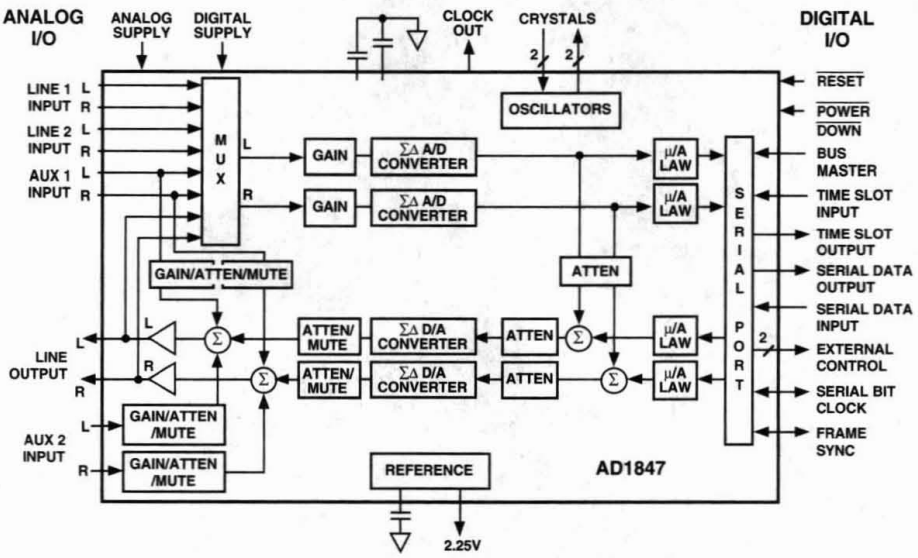
The Codec includes a stereo pair of ΣΔ analog-to-digital converters (ADCs) and a stereo pair of ΣΔ digital-to-analog converters (DACs). Inputs to the ADC can be selected from four stereo pairs of analog signals: line 1, line 2, auxiliary ("aux") line #1, and post-mixed DAC output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The pair of 16-bit outputs from the ADCs is available over a serial interface that also supports 16-bit digital input to the DACs and control/status information. The AD1847 can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output.

The AD1847 serial data interface uses a Time Division Multiplex (TDM) scheme that is compatible with DSP serial ports configured in Multi-Channel Mode with 32 16-bit time slots (i.e., SPORT0 on the ADSP-2101, ADSP-2115, etc.).

FUNCTIONAL BLOCK DIAGRAM



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AUDIO FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1847 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1847 SoundPort Stereo Codec accepts stereo line-level inputs. All inputs should be capacitively coupled (ac-coupled) to the AD1847. LINE1, LINE2, and AUX1, and post-mixed DAC output analog stereo signals are multiplexed to the internal programmable gain amplifier (PGA) stage.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left-channel inputs appearing at both channel outputs.

Analog Mixing

AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary analog input can be independently gained/attenuated from +12 dB to –34.5 dB in –1.5 dB steps or completely muted. The post-mixed DAC output is available on L_OUT and R_OUT external and as an input to the ADCs.

Even if the AD1847 is not playing back data from its DACs, the analog mix function can still be active.

Analog-to-Digital Datapath

The ΣΔ ADCs incorporate a proprietary fourth-order modulator. A single pole of passive filtering is all that is required for antialiasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include digital decimation filters that low-pass filter the input to $0.4 \times F_S$. ("F_S" is the word rate or "sampling frequency.") ADC input overrange conditions will cause status bits to be set that can be read.

Digital-to-Analog Datapath

The ΣΔ DACs contain a programmable attenuator and a low-pass digital interpolation filter. The anti-imaging interpolation filter oversamples and digitally filters the higher frequency images. The attenuator allows independent control of each DAC channel from 0 dB to –94.5 dB in 1.5 dB steps plus full mute. The DACs' ΣΔ noise shapers also oversample and convert the signal to a single-bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. These filters remove the very high frequency components of the DAC bitstream output. No external components are required.

Changes in DAC output attenuation take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise on playback. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 8 milliseconds at a 48 kHz sampling rate and 48 milliseconds at an 8 kHz sampling rate. (Time-out [ms] ≈ 384 ÷ F_S [kHz]).

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1847JP	0°C to +70°C	44-Lead PLCC	P-44A
AD1847JST	0°C to +70°C	44-Lead TQFP	ST-44

*P = PLCC; ST = TQFP. For outline information see Package Information section.

Serial-Port 16-Bit SoundPort Stereo Codec

AD1849K

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Multiple Channels of Stereo Input and Output
Digital Signal Mixing
On-Chip Speaker and Headphone Drive Capability
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
44-Lead PLCC
Operation from +5 V and Mixed +5 V/+3.3 V Supplies
Serial Interface Compatible with ADSP-21xx Fixed-Point DSμPs
Compatible with CS4215 (See Text)

PRODUCT OVERVIEW

The Serial-Port AD1849K SoundPort® Stereo Codec integrates the key audio data conversion and control functions into a single integrated circuit. The AD1849K is intended to provide a complete, single-chip audio solution for multimedia applications requiring operation from a single +5 V supply. External signal path circuit requirements are limited to three low tolerance capacitors for line level applications; anti-imaging filters are incorporated on-chip. The AD1849K includes on-chip monaural speaker and stereo headphone drive circuits that require no additional external components. Dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals, from an external clock, or from the serial interface bit clock.

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The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Analog signals can be input at line levels or microphone levels. A software controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The left and right channel 16-bit outputs from the ADCs are available over a single bidirectional serial interface that also supports 16-bit digital input to the DACs and control information. The AD1849K can accept and generate 8-bit μ-law or A-law companded digital data.

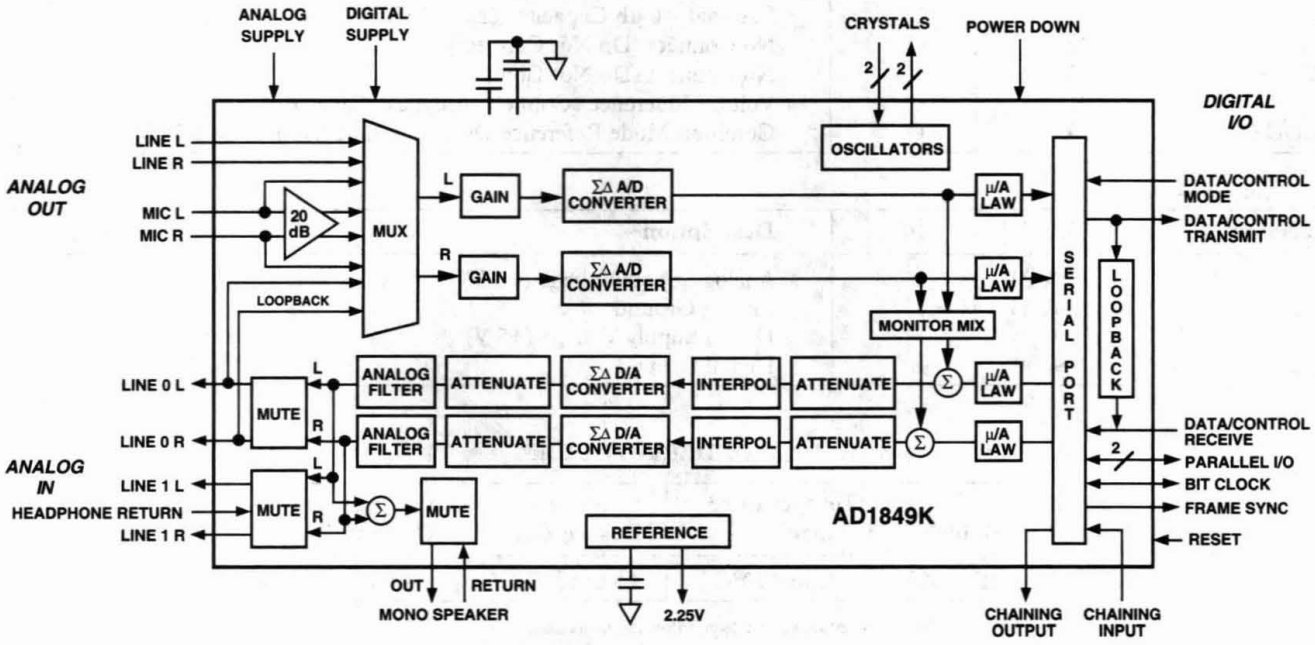
The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantization noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two independent stereo pairs of line-level (or one line-level and one headphone) outputs are generated, as well as drive for a monaural (mono) speaker.

SERIAL INTERFACE

A single serial interface on the AD1849K provides for the transfer of both data and control information. This interface is similar to AT&T's Concentrated Highway Interface (CHI), allowing simple connection with ISDN and other telecommunication devices. The AD1849K's implementation also allows a no-glue direct connection to members of Analog Devices' family of fixed-point DSP processors, including the ADSP-2101, the ADSP-2105, the ADSP-2111, and the ADSP-2115.

18

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Digital Signals

Pin Name	PLCC	I/O	Description
SDRX	1	I	Receive Serial Data Pin
SDTX	44	O	Transmit Serial Data Pin
SCLK	43	I/O	Bidirectional Serial Bit Clock
FSYNC	42	O	Frame Sync Output Signal
TSOUT	41	O	Chaining Word Output
TSIN	40	I	Chaining Word Input
D/$\overline{C}$	35	I	Data/Control Select Input
CIN1	6	I	Crystal 1 Input
COUT1	7	O	Crystal 1 Output
CIN2	10	I	Crystal 2 Input
COUT2	11	O	Crystal 2 Output
CLKIN	4	I	External Sample Clock Input ($256 \times F_S$)
CLKOUT	5	O	External Sample Clock Output ($256 \times F_S$)
PDN	13	I	Power Down Input (Active HI)
$\overline{RESET}$	12	I	Reset Input (Active LO)
PIO1	37	I/O	Parallel Input/Output Bit 1
PIO0	36	I/O	Parallel Input/Output Bit 0

Analog Signals

Pin Name	PLCC	I/O	Description
LINL	18	I	Left Channel Line Input
LINR	16	I	Right Channel Line Input
MINL	17	I	Left Channel Microphone Input (–20 dB from Line Level if MB = 0 or Line Level if MB = 1)
MINR	15	I	Right Channel Microphone Input (–20 dB from Line Level if MB = 0 or Line Level if MB = 1)
LOUT0L	32	O	Left Channel Line Output 0
LOUT0R	33	O	Right Channel Line Output 0
LOUT1L	31	O	Left Channel Line Output 1
LOUT1R	29	O	Right Channel Line Output 1
LOUT1C	30	I	Common Return Path for Large Current from External Headphones
MOUT	27	O	Mono Speaker Output
MOUTR	28	I	Mono Speaker Output Return
C0	14	O	External 1.0 µF Capacitor (±10%) Connection
C1	20	O	External 1.0 µF Capacitor (±10%) Connection
N/C	26		No Connect (Do Not Connect)
N/C	34		No Connect (Do Not Connect)
V_{REF}	21	O	Voltage Reference (Connect to Bypass Capacitor)
CMOUT	19	O	Common Mode Reference Datum Output (Nominally 2.25 V)

Power Supplies

Pin Name	PLCC	I/O	Description
V_{CC}	23 & 24	I	Analog Supply Voltage (+5 V)
GNDA	22 & 25	I	Analog Ground
V_{DD}	3, 8, 38	I	Digital Supply Voltage (+5 V)
GNDD	2, 9, 39	I	Digital Ground

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1849KP	0°C to +70°C	44-Lead PLCC	P-44A

*For outline information see Package Information section.

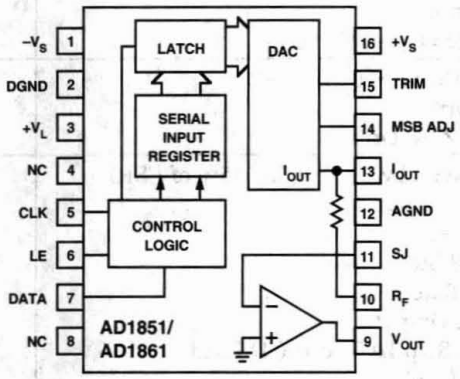
16-Bit/18-Bit, 16 × F_S PCM Audio DACs

AD1851/AD1861

FEATURES
110 dB SNR
Fast Settling Permits 16× Oversampling
±3 V Output
Optional Trim Allows Super-Linear Performance
±5 V Operation
16-Pin Plastic DIP and SOIC Packages
Pin-Compatible with AD1856 & AD1860 Audio DACs
2s Complement, Serial Input

APPLICATIONS
High-End Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD1851/AD1861 is a monolithic PCM audio DAC. The AD1851 is a 16-bit device, while the AD1861 is an 18-bit device. Each device provides a voltage output amplifier, DAC, serial-to-parallel register and voltage reference. The digital portion of the AD1851/AD1861 is fabricated with CMOS logic elements that are provided by Analog Devices' 2 µm ABCMOS process. The analog portion of the AD1851/AD1861 is fabricated with bipolar and MOS devices as well as thin-film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser-trimming of the linearity error affords low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small, contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3 V signal at load currents up to 8 mA. When used in current output mode, the AD1851/AD1861 provides a ±1 mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The AD1851 input clock can support a 12.5 MHz data rate, while the AD1861 input clock can support a 13.5 MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4×, 8× and 16× sampling frequencies.

The critical specifications of THD+N and signal-to-noise ratio are 100% tested for all devices.

The AD1851/AD1861 operates with ±5 V power supplies, making it suitable for home use markets. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided. Power dissipation is 100 mW typical.

The AD1851/AD1861 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Both packages incorporate the industry standard pinout found on the AD1856 and AD1860 PCM audio DACs. As a result, the AD1851/AD1861 is a drop-in replacement for designs where ±5 V supplies have been used with the AD1856/AD1860. Operation is guaranteed over the temperature range of –25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. AD1851 16-bit resolution provides 96 dB dynamic range. AD1861 18-bit resolution provides 108 dB dynamic range.
2. No external components are required.
3. Operates with ±5 V supplies.
4. Space saving 16-pin SOIC and plastic DIP packages.
5. 100 mW power dissipation.
6. High input clock data rates and 1.5 µs settling time permits 2×, 4×, 8× and 16× oversampling.
7. ±3 V or ±1 mA output capability.
8. THD + Noise and SNR are 100% tested.
9. Pin-compatible with AD1856 & AD1860 PCM audio DACs.

ORDERING GUIDE

Model	Resolution	THD + N	Package Option*
AD1851N	16 Bits	0.008%	N-16
AD1851N-J	16 Bits	0.004%	N-16
AD1851R	16 Bits	0.008%	R-16
AD1851R-J	16 Bits	0.004%	R-16
AD1861N	18 Bits	0.008%	N-16
AD1861N-J	18 Bits	0.004%	N-16
AD1861R	18 Bits	0.008%	R-16
AD1861R-J	18 Bits	0.004%	R-16

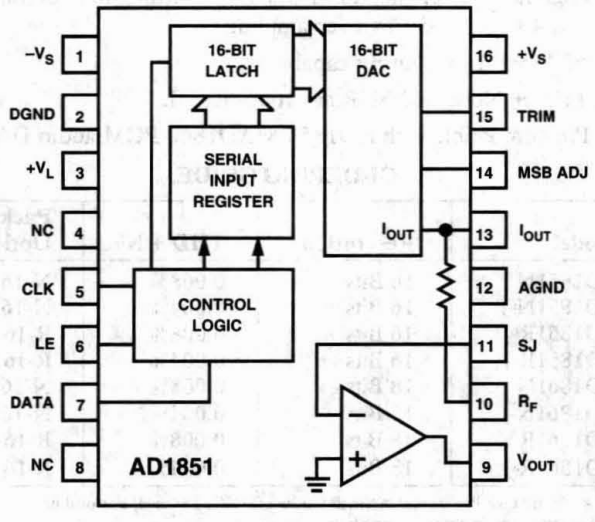
*N = Plastic DIP Package; R = Small Outline (SOIC) Package. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD1851/AD1861–SPECIFICATIONS (T_A @ +25°C and ±5 V supplies, unless otherwise noted)

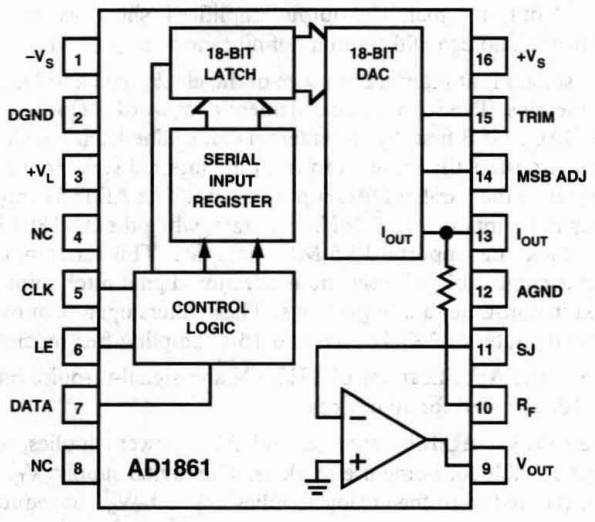
	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			**1.0**	µA
I_{IL}, $V_{IL} = 0.4$			**–10**	µA
ACCURACY				
Gain Error		±1		%
Midscale Output Voltage		±10		mV
DRIFT (0°C to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (To ±0.0015% of FSR)				
Voltage Output				
6 V Step		1.5		µs
1 LSB Step		1.0		µs
Slew Rate		9		V/µs
Current Output				
1 mA Step 10 Ω to 100 Ω Load		350		ns
1 kΩ Load		350		ns
OUTPUT				
Voltage Output Configuration				
Bipolar Range	**±2.88**	±3.0	**±3.12**	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage				
$+V_L$ and $+V_S$	4.75		5.25	V
$-V_S$	–5.25		–4.75	V
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	–25		+70	°C
Storage	–60		+100	°C
WARM-UP TIME	1			min

Specifications subject to change without notice.



NC = NO CONNECT

AD1851 Functional Block Diagram



NC = NO CONNECT

AD1861 Functional Block Diagram

Stereo, Single Supply 16-/18-Bit Sigma-Delta DACs

AD1857/AD1858

FEATURES

Low Cost, High Performance Stereo DACs
128 Times Oversampling Interpolation Filter
Multibit ΣΔ Modulator with Triangular PDF Dither
Discrete Time and Continuous Time Analog Reconstruction Filters
Buffered Outputs with 2 kΩ Output Load Drive
96 dB Dynamic Range, –90 dB THD+N Performance
Digital De-emphasis and Mute
±0.1° Maximum Phase Linearity Deviation
Continuously Variable Sample Rate Support
Power-Down Mode
16 and 18 Bit I^2S-Justified, Left-Justified Modes Offered on AD1857
16 Bit Right-Justified and DSP Serial Port Modes Offered on AD1858
Single +5 V Supply
20-Pin SSOP Package

APPLICATIONS

Digital Cable TV and Direct Broadcast Satellite Set-Top Decoder Boxes
Video Laser Disk, Video CD and CD-I Players
High Definition Televisions, Digital Audio Broadcast Receivers
CD, CD-R, DAT, DCC and MD Players
Digital Audio Workstations, Computer Multimedia Products

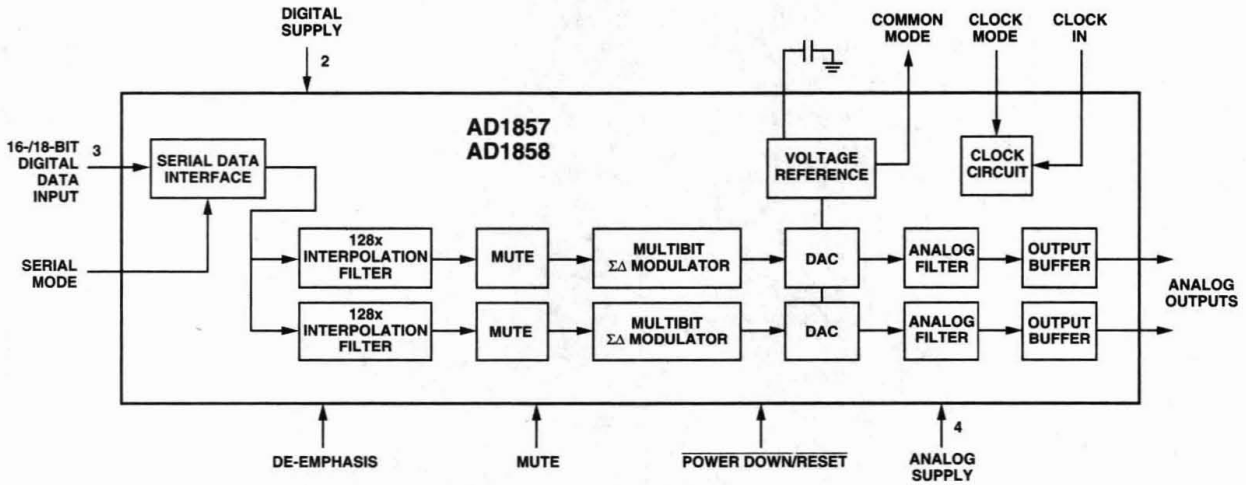
PRODUCT OVERVIEW

The AD1857/AD1858 are complete single-chip stereo digital audio playback components. They each comprise an advanced digital interpolation filter, a revolutionary "linearity-compensated" multibit sigma-delta (ΣΔ) modulator with dither, a jitter-tolerant DAC, switched capacitor and continuous time analog filters, and analog output drive circuitry. Other features include digital de-emphasis processing and mute. The AD1857/AD1858 support continuously variable sample rates with essentially linear phase response, and support 50/15 μs digital de-emphasis intended for "Redbook" 44.1 kHz sample frequency playback from Compact Discs. The user must provide a master clock that is synchronous with left/right clock, at 256 or 384 times the intended sample frequency.

The AD1857/AD1858 have a simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The AD1857 serial data input port can be configured in either 16-bit or 18-bit left-justified or I^2S-justified modes. The AD1858 serial data input port can be configured in either 16-bit right-justified or DSP serial port compatible modes. The AD1857/AD1858 accept serial audio data in MSB-first, twos-complement format. A power-down mode is offered to minimize power consumption when the device is inactive. The AD1857/AD1858 operate from a single +5 V power supply. They are fabricated on a single monolithic integrated circuit using a 0.6 μm CMOS double polysilicon, double metal process, and are housed in 20-pin SSOP packages for operation over the temperature range 0°C to +70°C.

PRELIMINARY TECHNICAL DATA

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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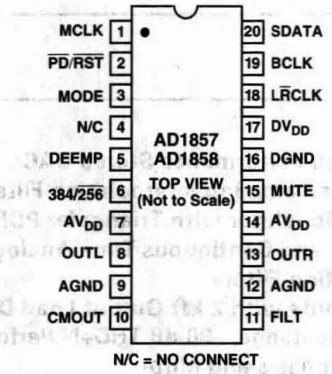
ORDERING GUIDE

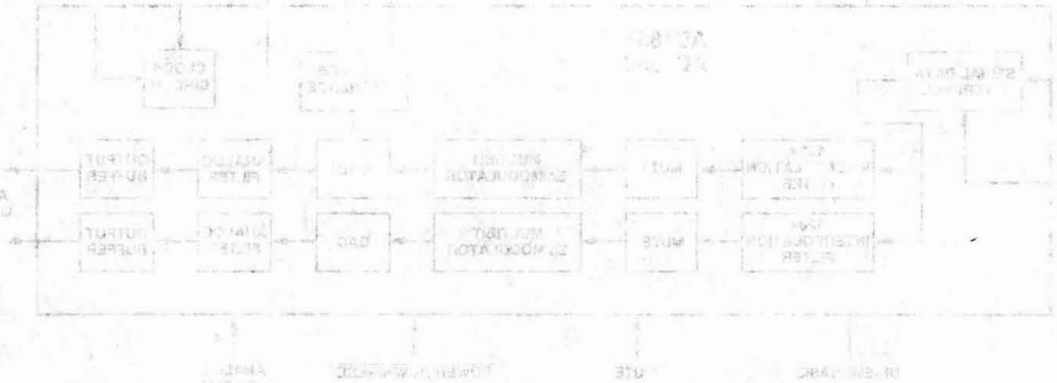
Model	Temperature	Package Description	Package Option*
AD1857JRS	0°C to +70°C	20-Lead SSOP	RS-20
AD1858JRS	0°C to +70°C	20-Lead SSOP	RS-20

*For outline information see Package Information section.

PIN CONFIGURATION



PRELIMINARY TECHNICAL DATA



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ANALOG DEVICES

Stereo, Single-Supply 18-Bit Integrated ΣΔ DAC

AD1859

FEATURES

Complete, Low Cost Stereo DAC System in a Single Die Package
Variable Rate Oversampling Interpolation Filter
Multibit ΣΔ Modulator with Triangular PDF Dither
Discrete and Continuous Time Analog Reconstruction Filters
Extremely Low Out-of-Band Energy
64 Step (1 dB/Step) Analog Attenuator with Mute
Buffered Outputs with 2 kΩ Output Load Drive
Rejects Sample Clock Jitter
94 dB Dynamic Range, –88 dB THD+N Performance
Option for Analog De-emphasis Processing with External Passive Components
±0.1° Maximum Phase Linearity Deviation
Continuously Variable Sample Rate Support
Digital Phase Locked Loop Based Asynchronous Master Clock
On-Chip Master Clock Oscillator, Only External Crystal Is Required
Power-Down Mode
Flexible Serial Data Port (I^2S-Justified, Left-Justified, Right-Justified and DSP Serial Port Modes)
SPI* Compatible Serial Control Port
Single +5 V Supply
28-Pin SOIC and SSOP Packages

APPLICATIONS

Digital Cable TV and Direct Broadcast Satellite Set-Top Decoder Boxes
Digital Video Disc, Video CD and CD-I Players
High Definition Televisions, Digital Audio Broadcast Receivers
CD, CD-R, DAT, DCC, ATAPI CD-ROM and MD Players
Digital Audio Workstations, Computer Multimedia Products

*SPI is a registered trademark of Motorola, Inc.

PRODUCT OVERVIEW

The AD1859 is a complete 16-/18-bit single-chip stereo digital audio playback subsystem. It comprises a variable rate digital interpolation filter, a revolutionary multibit sigma-delta (ΣΔ) modulator with dither, a jitter-tolerant DAC, switched capacitor and continuous time analog filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port.

The key differentiating feature of the AD1859 is its asynchronous master clock capability. Previous ΣΔ audio DACs required a high frequency master clock at 256 or 384 times the intended audio sample rate. The generation and management of this high frequency synchronous clock is burdensome to the board level designer. The analog performance of conventional single bit ΣΔ DACs is also dependent on the spectral purity of the sample and master clocks. The AD1859 has a digital Phase Locked Loop (PLL) which allows the master clock to be asynchronous, and which also strongly rejects jitter on the sample clock (left/right clock). The digital PLL allows the AD1859 to be clocked with a single frequency (27 MHz for example) while the sample frequency (as determined from the left/right clock) can vary over a wide range. The digital PLL will lock to the new sample rate in approximately 100 ms. Jitter components 15 Hz above and below the sample frequency are rejected by 6 dB per octave. This level of jitter rejection is unprecedented in audio DACs.

The AD1859 supports continuously variable sample rates with essentially linear phase response, and with an option for external analog de-emphasis processing. The clock circuit includes an on-chip oscillator, so that the user need only provide an external crystal. The oscillator may be overdriven, if desired, with an external clock source.

The AD1859 has a simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The serial data input port can be configured in left-justified, I^2S-justified, right-justified and DSP serial port compatible modes. The AD1859 accepts 16- or 18-bit serial audio data in MSB-first, twos-complement format. A power-down mode is offered to minimize power consumption when the device is inactive. The AD1859 operates from a single +5 V power supply. It is fabricated on a single monolithic integrated circuit using a 0.6 μM CMOS double polysilicon, double metal process, and is housed in 28-pin SOIC and SSOP packages for operation over the temperature range –40°C to +105°C.

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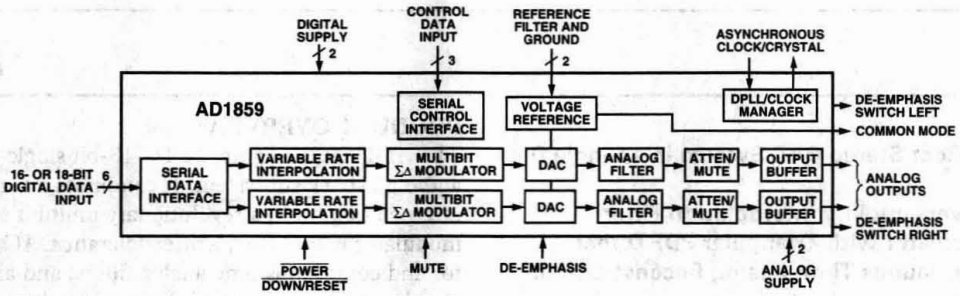
FUNCTIONAL BLOCK DIAGRAM

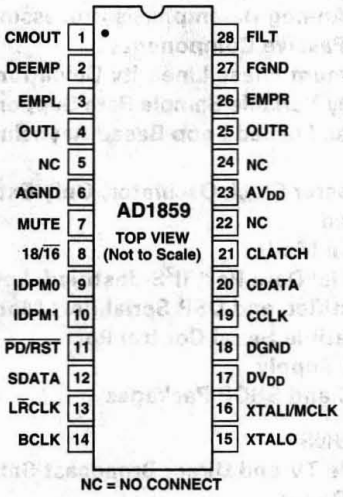


ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1859JR	0°C to +70°C	28-Lead SOIC	R-28
AD1859JRS	0°C to +70°C	28-Lead SSOP	RS-28

*For outline information see Package Information section.

PIN CONNECTIONS



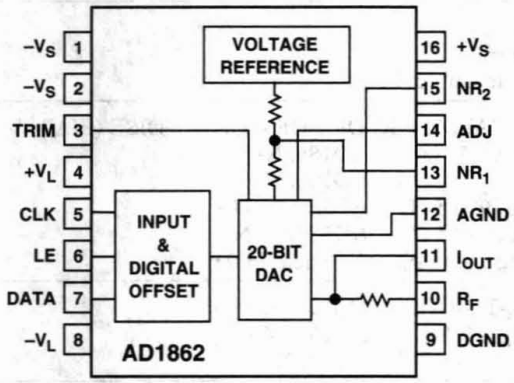
Ultralow Noise 20-Bit Audio DAC

AD1862*

FEATURES
119 dB Signal-to-Noise Ratio
102 dB D-Range Performance
±1 dB Gain Linearity
±1 mA Output Current
16-Pin DIP Package
0.0012% THD + N

APPLICATIONS
High Performance Compact Disc Players
Digital Audio Amplifiers
Synthesizer Keyboards
Digital Mixing Consoles
High Resolution Signal Processing

FUNCTIONAL BLOCK DIAGRAM



18

PRODUCT DESCRIPTION

The AD1862 is a monolithic 20-bit digital audio DAC. Each device provides a 20-bit DAC, 20-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1862 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1862 is fabricated with bipolar and MOS devices as well as thin-film resistors.

New design, layout and packaging techniques all combine to produce extremely high performance audio playback. The design of the AD1862 incorporates a digital offset circuit which improves low-level distortion performance. Low stress packaging techniques are used to minimize stress-induced parametric shifts. Stress-sensitive circuit elements are located in die areas which are least affected by packaging stress. Laser-trimming of initial linearity error affords extremely low total harmonic distortion. Output glitch is also small, contributing to the overall high level of performance.

The noise performance of the AD1862 is excellent. When used with the recommended two external noise-reduction capacitors, it achieves 119 dB signal-to-noise ratio.

The serial input port consists of the clock, data and latch enable pins. A serial 20-bit, 2s complement data word is clocked into the DAC, MSB first, by the external data clock. A latch-enable signal transfers the input word from the internal serial input register to the DAC input register. The data clock can function at 17 MHz, allowing $16 \times F_S$ operation. The serial input port is compatible with second-generation digital filter chips for consumer audio products such as the NPC SM5813 and SM5818.

The AD1862 operates with ±5 V to ±12 V supplies for the digital power supplies and ±12 V supplies for the analog supplies. The digital and analog supplies can be separated for reduced digital crosstalk. Separate analog and digital common pins are also provided. The AD1862 typically dissipates less than 300 mW.

The AD1862 is packaged in a 16-pin plastic DIP. The operating range is guaranteed to be –25°C to +70°C.

PRODUCT HIGHLIGHTS

1. 119 dB signal-to-noise ratio. (typical)
2. 102 dB D-Range performance. (minimum)
3. ±1 dB gain linearity @ –90 dB amplitude.
4. 20-bit resolution provides 120 dB of dynamic range.
5. $16 \times F_S$ operation.
6. 0.0012% THD+N @ 0 dB signal amplitude. (typical)
7. Space saving 16-pin DIP package.
8. ±1 mA output current.

***Protected by U.S. Patent Numbers: 4,349,811; 4,857,862; 4,855,618; 3,961,326; 4,141,004; 4,902,959.**

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AD1862–SPECIFICATIONS (T_A at +25°C and ±12 V supplies, see Figure 10 for test circuit schematic)

		Min	Typ	Max	Units
RESOLUTION		20			Bits
DIGITAL INPUTS	V_{IH}	2.0	**4.0**		V
	V_{IL}		**0.4**	0.8	V
	I_{IH} @ V_{IH} = 4.0 V			**1.0**	µA
	I_{IL} @ V_{IL} = 0.4 V			**–10**	µA
Maximum Clock Input Frequency		17			MHz
ACCURACY					
Gain Error				**±2**	%
Midscale Output Error			±2	**±5**	µA
TOTAL HARMONIC DISTORTION + NOISE (EIAJ)[1]					
0 dB, 990.5 Hz	AD1862N-J		–98 (0.0012)	**–96 (0.0016)**	dB (%)
	AD1862N		–94 (0.0019)	**–92 (0.0025)**	dB (%)
–20 dB, 990.5 Hz	AD1862N, N-J		–84 (0.0063)	**–80 (0.01)**	dB (%)
–60 dB, 990.5 Hz	AD1862N, N-J		–45 (0.56)	**–42 (0.8)**	dB (%)
D-Range, –60 dB,	A-Weight Filter	**102**			dB
SIGNAL-TO-NOISE RATIO[2]: (EIAJ)[1]					
A-Weight Filter	AD1862N-J	**113**	119		dB
	AD1862N	**110**	119		dB
GAIN LINEARITY					
@ –90 dB	AD1862N-J		±1		dB
	AD1862N		±1		dB
OUTPUT CURRENT					
Bipolar Range			±1		mA
Tolerance			±1	**±2**	%
Output Impedance (±30%)			2.1		kΩ
Settling Time			350		ns
FEEDBACK RESISTOR					
Value			3		kΩ
Tolerance			±1	**±2**	%
POWER SUPPLY					
Voltage	V_L and $-V_L$	4.75	**12.0**	13.2	±V
Voltage	V_S and $-V_S$	10.8	**12.0**	13.2	±V
Current	+I, V_L and V_S = 12 V, 17 MHz Clock		11	**15**	mA
	–I, $-V_L$ and $-V_S$ = –12 V, 17 MHz Clock		13	**16**	mA
POWER DISSIPATION					
V_L and V_S = 12 V, $-V_L$ and $-V_S$ = –12 V, 17 MHz Clock			288	372	mW
TEMPERATURE RANGE					
Specification			**+25**		°C
Operation		–25		+70	°C
Storage		–60		+100	°C

NOTES

[1]Test Method complies with EIAJ Standard CP-307.

[2]The signal-to-noise measurement includes noise contributed by the SE5534A op amp used in the test fixture but does not include the noise contributed by the low pass filter used in the test fixture.

Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Operating Temperature Range	THD+N @ FS	SNR	Package Option*
AD1862N	–25°C to +70°C	–92 dB, 0.0025%	110 dB	N-16
AD1862N-J	–25°C to +70°C	–96 dB, 0.0016%	113 dB	N-16

*N = Plastic DIP. For outline information see Package Information section.

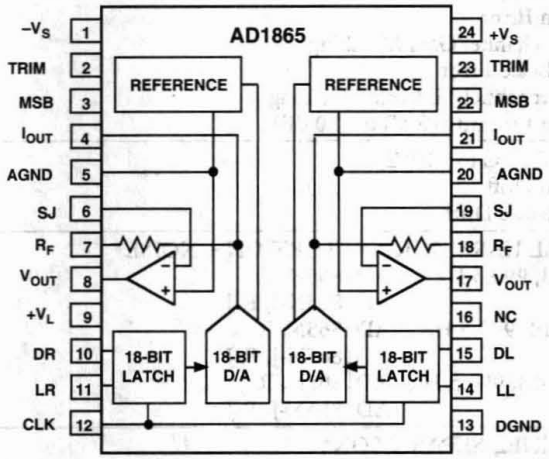
Complete Dual 18-Bit 16 × F_S Audio DAC

AD1865*

FEATURES
- Dual Serial Input, Voltage Output DACs
- No External Components Required
- 110 dB SNR
- 0.003% THD+N
- Operates at 16 × Oversampling per Channel
- ±5 Volt Operation
- Cophased Outputs
- 116 dB Channel Separation
- Pin Compatible with AD1864
- DIP or SOIC Packaging

APPLICATIONS
- Multichannel Audio Applications
- Compact Disc Players
- Multivoice Keyboard Instruments
- DAT Players and Recorders
- Digital Mixing Consoles
- Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM
(DIP Package)



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD1865 is a complete, dual 18-bit DAC offering excellent THD+N and SNR while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1865 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices' ABCMOS process.

The DACs on the AD1865 chip employ a partially segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1865 provides two ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1865 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout. At the same time, both channels of the AD1865 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

*Protected by U.S. Patents Nos.: RE 30,586; 3,961,326; 4,141,004; 4,349,811; 4,855,618; 4,857,862.

A versatile digital interface allows the AD1865 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1865 operates with ±5 V power supplies. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1865 typically dissipates only 225 mW, with a maximum power dissipation of 260 mW.

The AD1865 is packaged in both a 24-pin plastic DIP and a 28-pin SOIC package. Operation is guaranteed over the temperature range of –25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. The AD1865 is a complete dual 18-bit audio DAC.
2. 110 dB signal-to-noise ratio for low noise operation.
3. THD+N is typically 0.003%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 16 × F_S.
8. Low Power—only 225 mW typ, 260 mW max.
9. Five-wire interface for individual DAC control.
10. 24-pin DIP or 28-pin SOIC packages available.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD1865–SPECIFICATIONS (T_A = +25°C, $+V_L$ = $+V_S$ = +5 V and $-V_S$ = –5 V, F_S = 705.6 kHz, no MSB adjustment or deglitcher)

Parameter		Min	Typ	Max	Unit
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.0		$+V_L$	V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = $+V_L$			**1.0**	µA
	I_{IL}, V_{IL} = 0.4 V			**–10**	µA
Clock Input Frequency		**13.5**			MHz
ACCURACY					
Gain Error			0.2	**1.0**	% of FSR
Interchannel Gain Matching			0.3	**0.8**	% of FSR
Midscale Error			4		mV
Interchannel Midscale Matching			5		mV
Gain Linearity (0 dB to –90 dB)			<2		dB
DRIFT (0°C to +70°C)					
Gain Drift			±25		ppm of FSR/°C
Midscale Drift			±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*					
0 dB, 990.5 Hz	AD1865N, R		0.004	**0.006**	%
	AD1865N-J, R-J		0.003	**0.004**	%
20 dB, 990.5 Hz	AD1865N, R		0.010	**0.040**	%
	AD1865N-J, R-J		0.010	**0.020**	%
–60 dB, 990.5 Hz	AD1865N, R		1.0	**4.0**	%
	AD1865N-J, R-J		1.0	**2.0**	%
CHANNEL SEPARATION*					
0 dB, 990.5 Hz		**110**	116		dB
SIGNAL-TO-NOISE RATIO* (20 Hz to 30 kHz)		**107**	110		dB
D-RANGE* (With A-Weight Filter)					
–60 dB, 990.5 Hz	AD1865N, R	**88**	100		dB
	AD1865N-J, R-J	**94**	100		dB
OUTPUT					
Voltage Output Configuration					
Output Range (±1%)		**±2.94**	±3.0	**±3.06**	V
Output Impedance			0.1		Ω
Load Current		±8			mA
Short Circuit Duration		Indefinite to Common			
Current Output Configuration					
Bipolar Output Range (±30%)			±1		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
$+V_L$ and $+V_S$		4.75	**5.0**	5.25	V
$-V_S$		–5.25	**–5.0**	–4.75	V
+I, $+V_L$ and $+V_S$ = +5 V			22	**26**	mA
–I, $-V_S$ = –5 V			–23	**–26**	mA
POWER DISSIPATION, $+V_L$ = $+V_S$ = +5 V, $-V_S$ = –5 V			225	**260**	mW
TEMPERATURE RANGE					
Specification		0	**+25**	+70	°C
Operation		–25		+70	°C
Storage		–60		+100	°C
WARMUP TIME		1			min

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.

*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	THD+N @ FS	Package Option*
AD1865N	–25°C to +70°C	0.006%	N-24A
AD1865N-J	–25°C to +70°C	0.004%	N-24A
AD1865R	–25°C to +70°C	0.006%	R-28
AD1865R-J	–25°C to +70°C	0.004%	R-28

*N = Plastic DIP, R = Small Outline IC Package. For outline information see Package Information section.

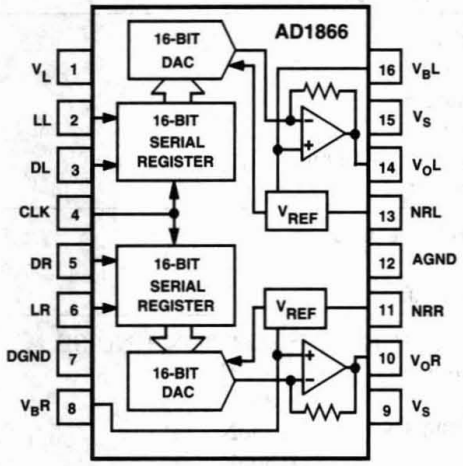
Single Supply Dual 16-Bit Audio DAC

AD1866*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 Volt Supply
0.005% THD+N
Low Power –50 mW
115 dB Channel Separation
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Multimedia Workstations
PC Audio Add-In Boards
Portable CD and DAT Players
Automotive CD and DAT Players
Noise Cancellation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1866 is a complete dual 16-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements and laser trimmed, thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation and low power dissipation.

The DACs on the AD1866 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into 7 elements. The 13 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1866 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. The 2.5 V reference voltages eliminate the need for "false ground" networks.

A versatile digital interface allows the AD1866 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 16 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S = 44.1 kHz) for each channel. The digital input pins of the AD1866 are TTL and +5 V CMOS compatible.

The AD1866 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1866 dissipates 50 mW.

The AD1866 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of –35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single supply operation @ +5 V.
2. 50 mW power dissipation.
3. THD+N is 0.005% (typical).
4. Signal-to-Noise Ratio is 95 dB (typical).
5. 115 dB channel separation (typical).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

***Protected by U.S. Patent Nos: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.**

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD1866–SPECIFICATIONS (T_A = +25°C and +5 V supplies unless otherwise noted)

		Min	Typ	Max	Unit
RESOLUTION			16		Bits
DIGITAL INPUTS	V_{IH}	**2.4**			V
	V_{IL}			**0.8**	V
	I_{IH}, V_{IH} = V_L		1.0		µA
	I_{IL}, V_{IL} = DGND		–10.0		µA
Maximum Clock Input Frequency		**13.5**			MHz
ACCURACY					
Gain Error			±3		% of FSR
Gain Matching			±3		% of FSR
Midscale Error			±30		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to +70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			–130		µV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1866N		0.005	**0.01**	%
	AD1866R		0.005	**0.01**	%
–20 dB, 990.5 Hz	AD1866N		0.02		%
	AD1866R		0.02		%
–60 dB, 990.5 Hz	AD1866N		2.0		%
	AD1866R		2.0		%
CHANNEL SEPARATION (1 kHz, 0 dB)		**108**	115		dB
SIGNAL-TO-NOISE RATIO (With A-Weight Filter)			95		dB
D-RANGE (With A-Weight Filter)			90		dB
OUTPUT					
Voltage Output Pins (V_{OL}, V_{OR})					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_{BL}, V_{BR})					
Output Range			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		**4.75**	5	**5.25**	V
Operation, V_L and V_S		**3.5**		**5.25**	V
+I, V_L and V_S = 5 V			10	**14**	mA
POWER DISSIPATION			50	70	mW
TEMPERATURE RANGE					
Operation		–35		**85**	°C
Storage		–60		**100**	°C

Specifications subject to change without notice.
Specifications in **boldface** are tested on all production units at final electrical.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1866N	–35°C to +85°C	Plastic DIP	N-16
AD1866R	–35°C to +85°C	SOIC	R-16
AD1866R-REEL	–35°C to +85°C	SOIC	R-16

*For outline information see Package Information section.

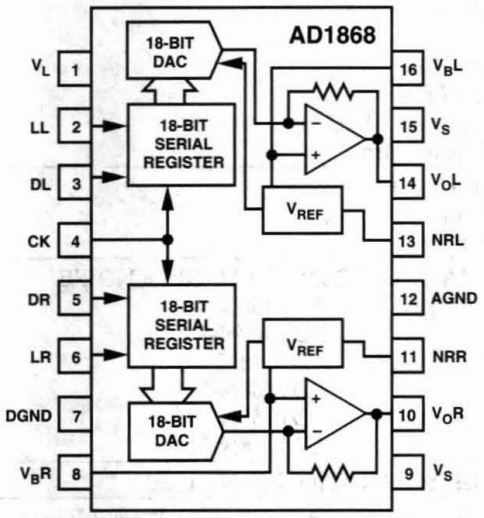
Single Supply Dual 18-Bit Audio DAC

AD1868*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 V Supply
0.004% THD+N (typ)
Low Power: 50 mW (typ)
108 dB Channel Separation (min)
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Portable Compact Disc Players
Portable DAT Players and Recorders
Automotive Compact Disc Players
Automotive DAT Players
Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1868 is a complete dual 18-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation, and low power dissipation.

The DACs on the AD1868 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into seven elements. The 15 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1868 requires no deglitcher or trimming circuitry. Low noise is achieved through the use of two noise-reduction capacitors.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. Reference voltages of 2.5 V are provided, eliminating the need for "False Ground" networks.

A versatile digital interface allows the AD1868 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 13.5 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency for each channel. The digital input pins of the AD1868 are TTL and +5 V CMOS compatible.

***Protected by U.S. Patent Numbers: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.**

The AD1868 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1868 dissipates 50 mW.

The AD1868 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of –35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single-supply operation @ +5 V.
2. 50 mW power dissipation (typical).
3. THD+N is 0.004% (typical).
4. Signal-to-Noise Ratio is 97.5 dB (typical).
5. 108 dB channel separation (minimum).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

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AD1868–SPECIFICATIONS (typical at T_A = +25°C and +5 V supplies unless otherwise noted)

		Min	Typ	Max	Units
RESOLUTION			18		Bit
DIGITAL INPUTS	V_{IH}	2.4			V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = V_L		1.0		µA
	I_{IL}, V_{IL} = DGND		1.0		µA
Maximum Clock Input Frequency		13.5			MHz
ACCURACY					
Gain Error			±1		% of FSR
Gain Matching			±1		% of FSR
Midscale Error			±15		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to +70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			±100		µV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1868N		0.004	0.008	%
	AD1868N-J		0.004	0.006	%
–20 dB, 990.5 Hz	AD1868N		0.020	0.08	%
	AD1868N-J		0.020	0.08	%
–60 dB, 990.5 Hz	AD1868N		2.0	5.0	%
	AD1868N-J		2.0	5.0	%
CHANNEL SEPARATION 1 kHz, 0 dB		108	NIL*		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)		95	97.5		dB
D-RANGE (with A-Weight Filter)		86	92		dB
OUTPUT					
Voltage Output Pins (V_OL, V_OR)					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_BL, V_BR)					
Output Voltage			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		4.75	5	5.25	V
Operation, V_L and V_S		3.5		5.25	V
+I, V_L and V_S = 5 V			10	14	mA
POWER DISSIPATION			50	70	mW
TEMPERATURE RANGE					
Specification		0	25	70	°C
Operation		–35		85	°C
Storage		–60		100	°C

*Above 115 dB.

Specifications subject to change without notice.

ORDERING GUIDE

Model	THD + N @ F_S	SNR	Package Option*
AD1868N	0.008%	95 dB	N-16
AD1868R	0.008%	95 dB	R-16
AD1868N-J	0.006%	95 dB	N-16
AD1868R-J	0.006%	95 dB	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

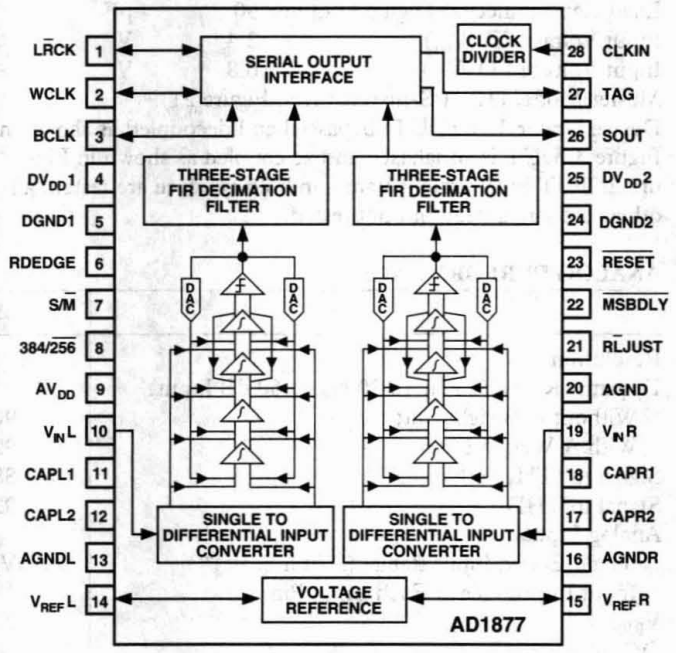
Single-Supply 16-Bit ΣΔ Stereo ADC

AD1877*

FEATURES
- Single +5 V Power Supply
- Single-Ended Dual-Channel Analog Inputs
- 92 dB (typ) Dynamic Range
- 90 dB (typ) S/(THD+N)
- 0.006 dB Decimator Passband Ripple
- Fourth-Order, 64-Times Oversampling ΣΔ Modulator
- Three-Stage, Linear-Phase Decimator
- 256 × F_S or 384 × F_S Input Clock
- Less than 100 μW (typ) Power-Down Mode
- Input Overrange Indication
- On-Chip Voltage Reference
- Flexible Serial Output Interface
- 28-Pin SOIC Package

APPLICATIONS
- Consumer Digital Audio Receivers
- Digital Audio Recorders, Including Portables
  - CD-R, DCC, MD and DAT
- Multimedia and Consumer Electronic Equipment
- Sampling Music Synthesizers
- Digital Karaoke Systems

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The AD1877 is a stereo, 16-bit oversampling ADC based on Sigma Delta (ΣΔ) technology intended primarily for digital audio bandwidth applications requiring a single +5 V power supply. Each single-ended channel consists of a fourth-order one-bit noise shaping modulator and a digital decimation filter. An on-chip voltage reference, stable over temperature and time, defines the full-scale range for both channels. Digital output data from both channels are time-multiplexed to a single, flexible serial interface. The AD1877 accepts a 256 × F_S or a 384 × F_S input clock (F_S is the sampling frequency) and operates in both serial port "master" and "slave" modes. In slave mode, all clocks must be externally derived from a common source.

Input signals are sampled at 64 × F_S onto internally buffered switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The on-chip single-ended to differential signal converters save the board designer from having to provide them externally. The AD1877's internal differential architecture provides increased dynamic range and excellent power supply rejection characteristics. The AD1877's proprietary fourth-order differential switched-capacitor ΣΔ modulator architecture shapes the one-bit comparator's quantization noise out of the audio passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the AD1877 to very low levels. Because its modulator is single-bit, AD1877 is inherently monotonic and has no mechanism for producing differential linearity errors.

The input section of the AD1877 uses autocalibration to correct any dc offset voltage present in the circuit, provided that the inputs are ac coupled. The single-ended dc input voltage can swing between 0.7 V and 3.8 V typically. The AD1877 antialias input circuit requires four external 470 pF NPO ceramic chip filter capacitors, two for each channel. No active electronics are needed. Decoupling capacitors for the supply and reference pins are also required.

The dual digital decimation filters are triple-stage, finite impulse response filters for effectively removing the modulator's high frequency quantization noise and reducing the 64 × F_S single-bit output data rate to an F_S word rate. They provide linear phase and a narrow transition band that properly digitizes 20 kHz signals at a 44.1 kHz sampling frequency. Passband ripple is less than 0.006 dB, and stopband attenuation exceeds 90 dB.

The flexible serial output port produces data in twos-complement, MSB-first format. The input and output signals are TTL compatible. The port is configured by pin selections. Each 16-bit output word of a stereo pair can be formatted within a 32-bit field of a 64-bit frame as either right-justified, I^2S-compatible, Word Clock controlled or left-justified positions. Both 16-bit samples can also be packed into a 32-bit frame, in left-justified and I^2S-compatible positions.

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD1877JR	0°C to +70°C	SOIC	R-28

*For outline information see Package Information section.

*Protected by U.S. Patent Numbers 5055843, 5126653, and others pending.

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AD1877–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	+5.0	V
Ambient Temperature	25	°C
Input Clock (F_{CLKIN}) [256 × F_S]	12.288	MHz
Input Signal	991.768	Hz
	–0.5	dB Full Scale
Measurement Bandwidth	23.2 Hz to 19.998 kHz	
Load Capacitance on Digital Outputs	50	pF
Input Voltage HI (V_{IH})	2.4	V
Input Voltage LO (V_{IL})	0.8	V

Master Mode, Data I^2S-Justified (ref. Figure 21).
Device Under Test (DUT) bypassed and decoupled as shown in Figure 3. DUT is antialiased and ac coupled as shown in Figure 2. DUT is calibrated. Values in bold typeface are tested, all others are guaranteed but not tested.

ANALOG PERFORMANCE

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)				
Without A-Weight Filter	90	92		dB
With A-Weight Filter	92	94		dB
Signal to (THD + Noise)	88	90		dB
Signal to THD	92	94		dB
Analog Inputs				
Single-Ended Input Range (± Full Scale)*	V_{REF} – 1.55	V_{REF}	V_{REF} + 1.55	V
Input Impedance at Each Input Pin		32		kΩ
V_{REF}	**2.05**	2.25	**2.55**	V
DC Accuracy				
Gain Error		±0.5	**±2.5**	%
Interchannel Gain Mismatch		0.01		dB
Gain Drift		115		ppm/°C
Midscale Offset Error (After Calibration)		±3	**±20**	LSBs
Midscale Drift		15		ppm/°C
Crosstalk (EIAJ Method)	**–90**	–99		dB

*V_{IN} p-p = V_{REF} × 1.333.
Specifications subject to change without notice.

PIN DESCRIPTION

Pin	Input/ Output	Pin Name	Description
1	I/O	$\overline{LR}$CK	Left/$\overline{Right}$ Clock
2	I/O	WCLK	Word Clock
3	I/O	BCLK	Bit Clock
4	I	$DV_{DD}1$	+5 V Digital Supply
5	I	DGND1	Digital Ground
6	I	RDEDGE	Read Edge Polarity Select
7	I	S/$\overline{M}$	Slave/$\overline{Master}$ Select
8	I	384/$\overline{256}$	Clock Mode
9	I	AV_{DD}	+5 V Analog Supply
10	I	V_{IN}L	Left Channel Input
11	O	CAPL1	Left External Filter Capacitor 1
12	O	CAPL2	Left External Filter Capacitor 2
13	I	AGNDL	Left Analog Ground
14	O	V_{REF}L	Left Reference Voltage Output
15	O	V_{REF}R	Right Reference Voltage Output
16	I	AGNDR	Right Analog Ground
17	O	CAPR2	Right External Filter Capacitor 2
18	O	CAPR1	Right External Filter Capacitor 1
19	I	V_{IN}R	Right Channel Input
20	I	AGND	Analog Ground
21	I	R$\overline{L}$JUST	Right/$\overline{Left}$ Justify
22	I	$\overline{MSBDLY}$	Delay MSB One BCLK Period
23	I	$\overline{RESET}$	Reset
24	I	DGND2	Digital Ground
25	I	$DV_{DD}2$	+5 V Digital Supply
26	O	SOUT	Serial Data Output
27	O	TAG	Serial Overrange Output
28	I	CLKIN	Master Clock

ANALOG DEVICES

High Performance 16-/18-Bit ΣΔ Stereo ADCs

AD1878/AD1879*

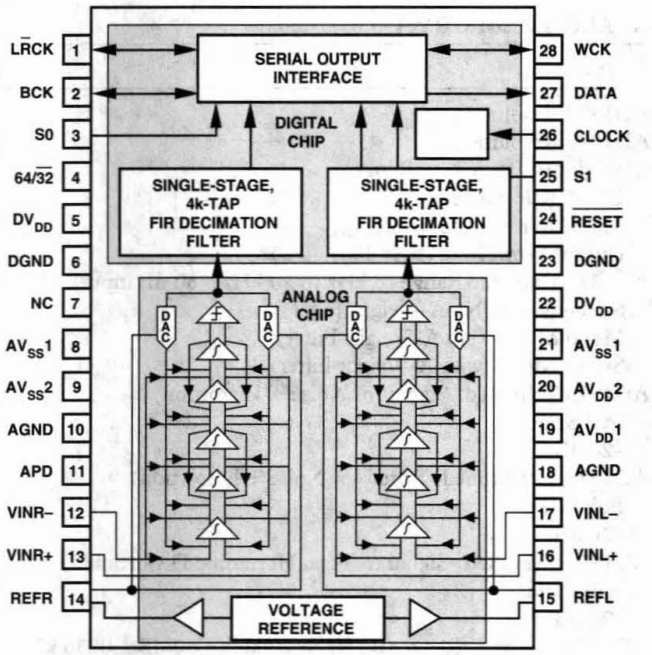
FEATURES

Fully Differential Dual Channel Analog Inputs
103 dB Signal-to-Noise (AD1879 typ)
–98 dB THD+N (AD1879 typ)
0.001 dB Passband Ripple and 115 dB Stopband Attenuation
Fifth-Order, 64 Times Oversampling ΣΔ Modulator
Single Stage, Linear Phase Decimator
256 × F_S Input Clock

APPLICATIONS

Digital Tape Recorders
Professional, DCC, and DAT
A/V Digital Amplifiers
CD-R
Sound Reinforcement

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The AD1879 is a two-channel, 18-bit oversampling ADC based on ΣΔ technology and intended primarily for digital audio applications. The AD1878 is identical to the 18-bit AD1879 except that it outputs 16-bit data words. Statements in this data sheet should be read as applying to both parts unless otherwise noted.

Each input channel of these ADCs is fully differential. Each data conversion channel consists of a fifth order one-bit noise shaping modulator and a digital decimation filter. An on-chip voltage reference provides a voltage source to both channels stable over temperature and time. Digital output data from both channels is time-multiplexed to a single, flexible serial interface. The AD1878/AD1879 accepts a 256 × F_S input master clock.

Input signals are sampled at 64 × F_S on switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The AD1878/AD1879's proprietary fifth-order differential switched-capacitor modulator architecture shapes the one-bit comparator's quantization noise out of the audio passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the AD1878/AD1879 to very low levels. The AD1878/AD1879's differential architecture provides increased dynamic range and excellent common-mode rejection characteristics. Because its modulator is single-bit, AD1878/AD1879 is inherently monotonic and has no mechanism for producing differential linearity errors.

The digital decimation filters are single-stage, 4095-tap finite impulse response filters for filtering the modulator's high frequency quantization noise and reducing the 64 × F_S single-bit output data rate to a F_S word rate. They provide linear phase and a narrow transition band that permits the digitization of 20 kHz signals while preventing aliasing into the passband even when using a 44.1 kHz sampling frequency. Passband ripple is less the 0.001 dB, and stopband attenuation exceeds 115 dB.

The flexible serial output port produces data in twos-complement, MSB-first format. Input and output signals are to TTL and CMOS-compatible logic levels. The port is configured by pin selections. The AD1878/AD1879 can operate in either master or slave mode. Each 16-/18-bit output word of a stereo pair can be formatted within a 32-bit field as either right-justified, I^2S-compatible, or at user-selected positions. The output can also be truncated to 16-bits by formatting into a 16-bit field.

The AD1878/AD1879 consists of two integrated circuits in a single ceramic 28-pin DIP package. The modulators and reference are fabricated in a BiCMOS process; the decimator and output port, in a 1.0 μm CMOS process. Separating these functions reduces digital crosstalk to the analog circuitry. Analog and digital supply connections are separated to further isolate the analog circuitry from the digital supplies.

The AD1878/AD1879 operates from ±5 V power supplies over the temperature range of –25°C to +70°C.

*Protected by U.S. Patent Numbers 5055843, 5126653, and others pending.

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AD1878/AD1879–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	±5	V
Ambient Temperature	25	°C
Input Clock (F_{CLOCK})	12.288	MHz
Input Signal	974	Hz
	–0.5	dB Full Scale

All minimums and maximums tested except as noted.

ANALOG PERFORMANCE

	Min	Typ	Max	Units
AD1879 Resolution		18		Bits
AD1878 Resolution		16		Bits
Clock Input Frequency Range				
CLOCK Input (F_{CLOCK})	0.01	12.288	14.286	MHz
Modulator Sample Rate ($F_{CLOCK}/4$)	0.0025	3.072	3.5715	MHz
Output Word Rate ($F_S = F_{CLOCK}/256$)	0.039	48	55.8	kHz
AD1879 Dynamic Range (0 kHz to 20 kHz, –60 dB input)				
Stereo Mode (No A-Weight Filter)	100	103		dB
Mono Mode[1] (No A-Weight Filter)		106		dB
Stereo Mode (with A-Weight Filter)		105		dB
AD1879 Trimmed[2] Signal to (Noise + Distortion)				
Full Scale	93	98		dB
–20 dB		83		dB
AD1879 Untrimmed[3] Signal to (Noise + Distortion)				
Full Scale	91	96		dB
–20 dB		83		dB
AD1879 Trimmed[2] Signal to Total Harmonic Distortion				
Full Scale		98		dB
–20 dB		100		dB
AD1878 Dynamic Range (0 kHz to 20 kHz, –60 dB 1.0936 kHz Input Dithered with a –10 dB 21.873 kHz Sine Wave)				
Stereo Mode (No A-Weight Filter)	95	97		dB
AD1878 Trimmed[2] Signal to (Noise + Distortion)				
Full Scale	93	95		dB
–20 dB		77		dB
AD1878 Untrimmed[3] Signal to (Noise + Distortion)				
Full Scale	91	94		dB
–20 dB		77		dB
AD1878 Trimmed[2] Signal to Total Harmonic Distortion				
Full Scale		98		dB
–20 dB		100		dB
Analog Inputs				
Differential Input Range[4]	±5.985	±6.3	±6.615	V
Input Impedance at Each Input Pin		7.0		kΩ
DC Accuracy				
Gain Error		±1	±5	%
Interchannel Gain Mismatch		0.05	0.15	dB
Gain Drift		150		ppm/°C
AD1879 Midscale Offset Error		±200	±750	18-Bit LSBs
AD1878 Midscale Offset Error		±50	±200	16-Bit LSBs
Midscale Drift		13		ppm/°C
Voltage Reference	2.4	2.86	3.2	V
Crosstalk (EIAJ Method)	100	105		dB
Interchannel Phase Deviation		±0.001		Degrees

NOTES

[1]Both channels connected together for mono operations as described below in "How to Extend SNR."

[2]Differential gain imbalance manually trimmed to eliminate second harmonic. See "Applications Issues" below.

[3]Test performed without part-to-part trimming.

[4]The differential input range is twice the range seen at each input pin. The input range corresponds to the full-scale digital output range.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD1878JD	–25°C to +70°C	Ceramic DIP	D-28
AD1879JD	–25°C to +70°C	Ceramic DIP	D-28

*For outline information see Package Information section.

SamplePort Stereo Asynchronous Sample Rate Converters

AD1890/AD1891

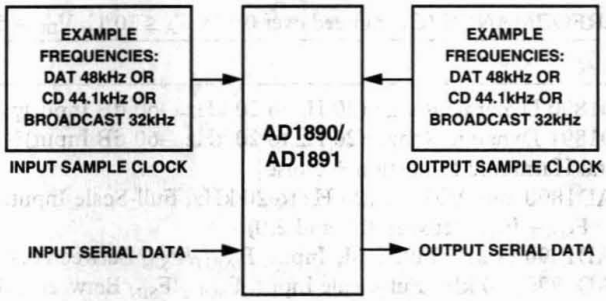
FEATURES

- Automatically Sense Sample Frequencies—No Programming Required
- Tolerant of Sample Clock Jitter
- Smooth Transition When Sample Clock Frequencies Cross
- Accommodate Dynamically Changing Asynchronous Sample Clocks
- 8 kHz to 56 kHz Sample Clock Frequency Range
- 1:2 to 2:1 Ratio Between Sample Clocks
- –106 dB THD+N at 1 kHz (AD1890)
- 120 dB Dynamic Range (AD1890)
- Optimal Clock Tracking Control
  - –Short/Long Group Delay Modes
  - –Slow/Fast Settling Modes
- Linear Phase in All Modes
- Equivalent of 4 Million 22-Bit FIR Filter Coefficients Stored On-Chip
- Automatic Output Mute
- Flexible Four Wire Serial Interfaces
- Low Power

APPLICATIONS

- Digital Mixing Consoles and Digital Audio Workstations
- CD-R, DAT, DCC and MD Recorders
- Multitrack Digital Audio and Video Tape Recorders
- Studio to Transmitter Links
- Digital Audio Signal Routers/Switches
- Digital Audio Broadcast Equipment
- High Quality D/A Converters
- Digital Tape Recorder Varispeed Applications
- Computer Communication and Multimedia Systems

SYSTEM DIAGRAM


EXAMPLE FREQUENCIES: DAT 48kHz OR CD 44.1kHz OR BROADCAST 32kHz
INPUT SAMPLE CLOCK
AD1890/ AD1891
EXAMPLE FREQUENCIES: DAT 48kHz OR CD 44.1kHz OR BROADCAST 32kHz
OUTPUT SAMPLE CLOCK
INPUT SERIAL DATA
OUTPUT SERIAL DATA

PRODUCT OVERVIEW

The AD1890 and AD1891 SamplePorts™ are fully digital, stereo Asynchronous Sample Rate Converters (ASRCs) that solve sample rate interfacing and compatibility problems in digital audio equipment. Conceptually, these converters interpolate the input data up to a very high internal sample rate with a time resolution of 300 ps, then decimate down to the desired output sample rate. The AD1890 is intended for 18- and 20-bit professional applications, and the AD1891 is intended for 16-bit lower cost applications where large dynamic sample-rate changes are not encountered. These devices are asynchronous because the frequency and phase relationships between the input and output sample clocks (both are inputs to the AD1890/AD1891 ASRCs) are arbitrary and need not be related by a simple integer ratio. There is no need to explicitly select or program the input and output sample clock frequencies, as the AD1890/AD1891 automatically sense the relationship between the two clocks. The input and output sample clock frequencies can nominally range from 8 kHz to 56 kHz, and the ratio between them can vary from 1:2 to 2:1.

The AD1890/AD1891 use multirate digital signal processing techniques to construct an output sample stream from the input sample stream. The input word width is 4 to 20 bits for the AD1890 or 4 to 16 bits for the AD1891. Shorter input words are automatically zero-filled in the LSBs. The output word width for both devices is 24 bits. The user can receive as many of the output bits as desired. Internal arithmetic is performed with 22-bit coefficients and 27-bit accumulation. The digital samples are processed with unity gain.

The input and output control signals allow for considerable flexibility for interfacing to a variety of DSP chips, AES/EBU receivers and transmitters and for I^2S compatible devices. Input and output data can be independently justified to the left/right clock edge, or delayed by one bit clock from the left/right clock edge. Input and output data can also be independently justified to the word clock rising edge or delayed by one bit clock from the word clock rising edge. The bit clocks can also be independently configured for rising edge active or falling edge active operation.

The AD1890/AD1891 SamplePort™ ASRCs have on-chip digital coefficients that correspond to a highly oversampled 0 kHz to 20 kHz low-pass filter with a flat passband, a very narrow transition band, and a high degree of stopband attenuation. A subset of these filter coefficients are dynamically chosen on the basis of the filtered instantaneous ratio between the input sample clock ($L\overline{R}\_I$) and the output sample clock ($L\overline{R}\_O$), and these coefficients are used in an FIR convolver to perform the sample rate conversion. Refer to the "Theory of Operation" section of this data sheet for a more thorough functional description. The low-pass filter has been designed so that full 20 kHz bandwidth is maintained when the input and output sample clock frequencies are as low as 44.1 kHz. If the output sample rate drops below the input sample rate, the bandwidth of the input signal is

(*continued on next page*)

SamplePort and SamplePorts are trademarks of Analog Devices, Inc.

AD1890/AD1891–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltage	+5.0	V
Ambient Temperature	25	°C
MCLK	20	MHz
Load Capacitance	100	pF

All minimums and maximums tested except as noted.

PERFORMANCE (Guaranteed over 0°C ≤ T_A ≤ 70°C, V_{DD} = 5.0 V ± 10%, 8 MHz ≤ MCLK ≤ 20 MHz)

	Min	Max	Units
AD1890 Dynamic Range (20 Hz to 20 kHz, –60 dB Input)†	120		dB
AD1891 Dynamic Range (20 Hz to 20 kHz, –60 dB Input)†	96		dB
Total Harmonic Distortion + Noise†			dB
AD1890 and AD1891 (20 Hz to 20 kHz, Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.5 and 2.0)		–94	dB
AD1890 (1 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		–106	dB
AD1890 (10 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		–100	dB
AD1891 (1 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		–96	dB
AD1891 (10 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		–95	dB
Interchannel Phase Deviation†		0	Degrees
Input and Output Sample Clock Jitter† (For ≤ 1 dB Degradation in THD+N with 10 kHz Full-Scale Input, Slow-Settling Mode)	10		ns

Specifications subject to change without notice.

PRODUCT OVERVIEW (Continued)

automatically limited to avoid alias distortion on the output signal. The AD1890/AD1891 dynamically alter the low-pass filter cutoff frequency smoothly and slowly, so that real-time variations in the sample rate ratio are possible without degradation of the audio quality.

The AD1890/AD1891 have a pin selectable slow- or fast-settling mode. This mode determines how quickly the ASRCs adapt to a change in either the input sample clock frequency (F_{SIN}) or the output sample clock frequency (F_{SOUT}). In the slow-settling mode, the control loop which computes the ratio between F_{SIN} and F_{SOUT} settles in approximately 800 ms and begins to reject jitter above 3 Hz. The slow-settling mode offers the best signal quality and the greatest jitter rejection. In the fast-settling mode, the control loop settles in approximately 200 ms and begins to reject jitter above 12 Hz. The fast-settling mode allows rapid, real time sample rate changes to be tracked without error, at the expense of some narrow-band noise modulation products on the output signal.

The AD1890 also has a pin selectable, short or long group delay mode. This pin determines the depth of the First-In, First-Out (FIFO) memory which buffers the input data samples before they are processed by the FIR convolver. In the short mode, the group delay is approximately 700 µs. The ASRC is more sensitive to sample rate changes in this mode (i.e., the pointers which manage the FIFO are more likely to cross and become momentarily invalid during a sample rate step change), but the group delay is minimized. In the long mode, the group delay is approximately 3 ms. The ASRC is tolerant of large dynamic sample rate changes in this mode, and it should be used when the device is required to track fast sample rate changes, such as in varispeed applications. The AD1891 features the short group delay mode only. In either device, if the read and write pointers that manage the FIFO cross (indicating underflow or overflow), the ASRC asserts the mute output (MUTE_O) pin HI for 128 output clock cycles. If MUTE_O is connected to the mute input (MUTE_I) pin, as it normally should be, the serial output will be muted (i.e., all bits zero) during this transient event.

The AD1890/AD1891 are fabricated in a 0.8 µm single poly, double metal CMOS process and are packaged in a 0.6" wide 28-pin plastic DIP and a 28-pin PLCC. The AD1890/AD1891 operate from a +5 V power supply over the temperature range of 0°C to +70°C.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1890JN	0°C to +70°C	Plastic DIP	N-28
AD1890JP	0°C to +70°C	PLCC	P-28A
AD1891JN	0°C to +70°C	Plastic DIP	N-28
AD1891JP	0°C to +70°C	PLCC	P-28A

*For outline information see Package Information section.

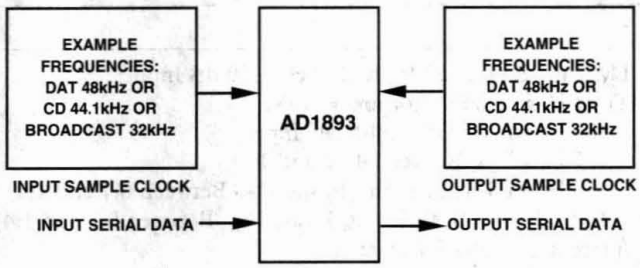
Low Cost Sample-Rate Converter
16-Bit Stereo Asynchronous Sample Rate Converter

AD1893

FEATURES
- Low Cost
- TQFP and PDIP Packages
- 3 V Supply Performance Specified—Very Low Power
- Automatically Senses Sample Frequencies—No Programming Required
- Rejects Sample Clock Jitter
- Accommodates Dynamically Changing Asynchronous Sample Clocks
- 8 kHz to 56 kHz Sample Clock Frequency Range
- Approximately 1:2 to 2:1 Ratio Between Sample Clocks
- –96 dB THD+N at 1 kHz
- 96 dB Dynamic Range
- Optimal Clock Tracking Control –Slow/Fast Settling Modes
- Linear Phase in All Modes
- Automatic Output Mute
- Flexible Four Wire Serial Interfaces with Right-Justified Mode
- Power-Down Mode
- On-Chip Oscillator

APPLICATIONS
- Consumer CD-R, DAT, DCC, MD and 8 mm Video Tape Recorders Including Portables
- Digital Audio Communication/Network Systems
- Computer Multimedia Systems

SYSTEM DIAGRAM


EXAMPLE FREQUENCIES: DAT 48kHz OR CD 44.1kHz OR BROADCAST 32kHz
AD1893
EXAMPLE FREQUENCIES: DAT 48kHz OR CD 44.1kHz OR BROADCAST 32kHz
INPUT SAMPLE CLOCK
OUTPUT SAMPLE CLOCK
INPUT SERIAL DATA
OUTPUT SERIAL DATA

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PRODUCT OVERVIEW

The AD1893 SamplePort® is a fully digital, stereo Asynchronous Sample Rate Converter (ASRC) that solves sample rate interfacing and compatibility problems in digital audio equipment. Conceptually, this converter interpolates the input data up to a very high internal sample rate with a time resolution of 300 ps, then decimates down to the desired output sample rate. The AD1893 is intended for 16-bit low cost, non-varispeed applications where low voltage, low power (i.e., battery-powered) operation is required. Refer to the AD1890/AD1891 data sheet for other products in the SamplePort family. This device is asynchronous because the frequency and phase relationships between the input and output sample clocks (both are inputs to the AD1893 ASRC) are arbitrary and need not be related by a simple integer ratio. There is no need to explicitly select or program the input and output sample clock frequencies, as the AD1893 automatically senses the relationship between the two clocks. The input and output sample clock frequencies can nominally range from 8 kHz to 56 kHz, and the ratio between them can vary from approximately 1:2 to 2:1.

SamplePort is a registered trademark of Analog Devices, Inc.

The AD1893 uses multirate digital signal processing techniques to construct an output sample stream from the input sample stream. The input word width is 4 to 16 bits for the AD1893. Shorter input words are automatically zero-filled in the LSBs. The output word width is 24 bits. The user can receive as many of the output bits as desired. Internal arithmetic is performed with 22-bit coefficients and 27-bit accumulation. The digital samples are processed with unity gain.

The input and output control signals allow for considerable flexibility for interfacing to a variety of DSP chips, AES/EBU receivers and transmitters and for I²S compatible devices. Input and output data can be independently right- or left- (with or without a one bit clock delay) justified to the left/right clock edge. In the right-justified mode, the MSB is delayed 16 bit clock periods from the left/right clock edge transition. Input and output data can also be independently justified to the word clock rising edge. The data justification options are encoded on two mode pins for both the input port and the output port. The bit clocks can also be independently configured for rising edge active or falling edge active operation.

The AD1893 SamplePort ASRC has on-chip digital coefficients that correspond to a highly oversampled 0 Hz to 20 kHz low-pass filter with a flat passband, a very narrow transition band, and a high degree of stopband attenuation. A subset of these filter coefficients are dynamically chosen on the basis of the filtered ratio between the input sample clock ($\overline{LR}$_I) and the output sample clock ($\overline{LR}$_O), and these coefficients are then used in an FIR convolver to perform the sample rate conversion. Refer to the "Theory of Operation" section of this data sheet for a more thorough functional description. The low-pass filter has been designed so that full 20 kHz bandwidth is maintained when the input and output sample clock frequencies are as low as 44.1 kHz. If the output sample rate drops below the input sample rate, the bandwidth of the input signal is automatically

(continued on next page)

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AD1893–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltage	+3.0	V
Ambient Temperature	25	°C
Crystal Frequency	16	MHz
Load Capacitance	100	pF

All minimums and maximums tested except as noted.

PERFORMANCE* (Guaranteed for V_{DD} = +3.3 V to +5.0 V ± 10%)

	Min	Max	Units
Dynamic Range (20 Hz to 20 kHz, –60 dB Input)	96		dB
Total Harmonic Distortion + Noise			
(20 Hz to 20 kHz, Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.51 and 1.99)		–94	dB
(1 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		–96	dB
(10 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		–95	dB
Interchannel Phase Deviation		0	Degrees
Input and Output Sample Clock Jitter (For ≤1 dB Degradation in THD+N with 10 kHz Full-Scale Input, Slow-Settling Mode)	10		ns

*Guaranteed, Not Tested.

Specifications subject to change without notice.

PRODUCT OVERVIEW (Continued)

limited to avoid alias distortion on the output signal. The AD1893 dynamically alters the low-pass filter cutoff frequency smoothly and slowly, so that real-time variations in the sample rate ratio are possible without degradation of the audio quality.

The AD1893 has a pin selectable slow- or fast-settling mode. This mode determines how quickly the ASRC adapts to a change in either the input sample clock frequency (F_{SIN}) or the output sample clock frequency (F_{SOUT}). In the slow-settling mode, the control loop which computes the ratio between F_{SIN} and F_{SOUT} settles in approximately 800 ms and begins to reject jitter above 3 Hz. The slow-settling mode offers the best signal quality and the greatest jitter rejection. In the fast-settling mode, the control loop settles in approximately 200 ms and begins to reject jitter above 12 Hz. The fast-settling mode allows rapid, real time sample rate changes to be tracked without error, at the expense of some narrow-band noise modulation products on the output signal.

The AD1893 features short group delay processing. This feature relates to the depth of the First-In, First-Out (FIFO) memory which buffers the input data samples before they are processed by the FIR convolver. In the AD1893, the group delay is approximately 700 µs. If the read and write pointers that manage the FIFO cross (indicating underflow or overflow), the AD1893 asserts the mute output (MUTE_O) pin HI for 128 output clock cycles. If MUTE_O is connected to the mute input (MUTE_I) pin, as it normally should be, the serial output will be muted (i.e., all bits zero) during this transient event.

The AD1893 includes an on-chip oscillator which only requires that the user provide an external crystal. By removing the need for an external oscillator, the AD1893 lowers the total cost of ownership to the end user. The AD1893 also includes a power-down mode, which is invoked with the PWRDWN pin. Asserting this control signal HI will place the AD1893 into a very low power dissipation in active and standby condition.

The AD1893 is fabricated in a 0.8 µm single poly, double metal CMOS process and are packaged in a 0.6" wide 28-pin plastic DIP and a 10 mm by 10 mm body size 44-pin TQFP. The AD1893 operates from a +3 V to +5 V power supply over the temperature range of 0°C to +70°C.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1893JN	0°C to +70°C	Plastic DIP	N-28
AD1893JST	0°C to +70°C	TQFP	ST-44

*For outline information see Package Information section.

High Speed Networks & RS-xxx Interface Products
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AD7306 – +5 V Powered RS-232/RS-422 Transceiver	19–11
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ADM207E/ADM208E/ADM211E/ADM213E – EMI/EMC Compliant, ±15 kV ESD Protected, RS-232 Line Drivers/Receivers	19–15
ADM222/ADM232A/ADM242 – High Speed, +5 V, 0.1 µF CMOS RS-232 Drivers/Receivers	19–17
ADM223/ADM230L–ADM241L – +5 V Powered CMOS RS-232 Drivers/Receivers	19–19
ADM485 – +5 V Low Power EIA RS-485 Transceiver	19–21
ADM560/ADM561 – Ultralow Power, +3.3 V, RS-232 Notebook PC Serial Port Drivers/Receivers	19–23
ADM1485 – +5 V Low Power EIA RS-485 Transceiver	19–25
ADM5170 – Octal, RS-232/RS-423 Line Driver	19–27
ADM5180 – Octal, RS-232/RS-423 Line Receiver	19–29

High Speed Networks & RS-xxx Interface Products–Selection Guides

Nonregeneration Applications

Model	Standards Supported	VCO MHz	VCO Int/Ext	Tracking Range MBPS Min	Tracking Range MBPS Max	Received Clock Skew ns Min	Received Clock Skew ns Max	Jitter Tolerance Unit Interval p-p	Page No.	Comments	Fax-code
AD800-45	DS-3	44.736	Int	43	45.5	0.2	1	0.47 @ 1 MHz	19–5		1395
AD800-25	STS-1	51.84	Int	49	53	0.2	1	0.47 @ 20 kHz	19–5		1395
AD802-155	STS-3, STM-1	155.52	Int	155	156	0.2	1	NS	19–5		1395

Regeneration Applications

Model	Standards Supported	VCO MHz	VCO Int/Ext	Tracking Range MBPS Min	Tracking Range MBPS Max	Received Clock Skew ns Min	Received Clock Skew ns Max	Jitter Tolerance Unit Interval p-p	Page No.	Comments	Fax-code
AD803	PONs	20.48	Int	19.1	20.5	1.95	13.6	0.95 @ 10 kHz	*		1398
AD805	G.958 Type A or B	155.52	Ext	±7.7 kHz		0.2	1.1	0.65 @ 1 MHz	*		1399
AD807	G.958 Type A	155.52	Int	155	156	NS	NS	0.45 @ 1 MHz	19–7	With On-Chip Quantizer	1904

Frequency Synthesizer, 9.72 MHz or 19.44 MHz Input

Model	Standards Supported	VCO MHz	VCO Int/Ext	Tracking Range MBPS Min	Tracking Range MBPS Max	Received Clock Skew ns Min	Received Clock Skew ns Max	Jitter Tolerance Unit Interval p-p	Page No.	Comments	Fax-code
AD809	SDH, SONET	155.52		9.719	9.721				19–9	9.719 MHz Mode	1935
AD809	SDH, SONET	155.52		19.44	19.442				19–9	19.442 MHz Mode	1935

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Model	Power Supply #1 Volts	# Drivers	# Receivers	kBPS min	Ext Cap	Shutdown SD	# RCV Active	Three State Enable $\overline{EN}$	# Pins N/R	Page No.	Comments	Fax-code
RS-232 Fast, 15 kV ESD, Low EMI Emissions/Immunity, 0.1 µF Caps												
ADM207E	+5	5	3	100	4	No	0	No	24	19–15		1991
ADM208E	+5	4	4	100	4	No	0	No	24	19–15		1991
ADM209E	+5	3	5	100	2	No	0	$\overline{EN}$	24	*	V_{IN} # 2, +9 V–+13.2 V	1991
ADM211E	+5	4	5	100	4	$\overline{SD}$	0	$\overline{EN}$	28	19–15		1991
ADM213E	+5	4	5	100	4	$\overline{SD}$	2	EN	28	19–15		1991
RS-232 Low Power, 1 µF Caps												
ADM230L	+5	5	0	100	4	SD	0	No	20	19–19		1540
ADM231L	+5	2	2	100	2	No	0	No	14/16	19–19	V_{IN} # 2, +7.5 V–+13.2 V	1540
ADM232L	+5	2	2	100	4	No	0	No	16	19–19		1540
ADM234L	+5	4	0	100	4	No	0	No	16	19–19		1540
ADM236L	+5	4	3	100	4	SD	0	$\overline{EN}$	24	19–19		1540
ADM237L	+5	5	3	100	4	No	0	No	24	19–19		1540
ADM238L	+5	4	4	100	4	No	0	No	24	19–19		1540
ADM239L	+5	3	5	100	2	No	0	$\overline{EN}$	24	19–19	V_{IN} # 2, +7.5 V–+13.2 V	1540
ADM241L	+5	4	5	100	4	SD	0	$\overline{EN}$	28	19–19		1540
ADM205L	+5	2	2	100	0	No	0	No	20	*	No Capacitors Required	1540
RS-232 Fast, 0.1 µF Caps												
ADM202	+5	2	2	120	4	No	0	No	16	19–13		1528
ADM206	+5	4	3	100	4	SD	0	$\overline{EN}$	24	*		1530
ADM207	+5	5	3	100	4	No	0	No	24	*		1530
ADM208	+5	4	4	100	4	No	0	No	24	*		1530
ADM209	+5	3	5	100	2	No	0	$\overline{EN}$	24	*	V_{IN} # 2, +9 V–+13.2 V	1530
ADM211	+5	4	5	100	4	$\overline{SD}$	0	$\overline{EN}$	28	*		1530
ADM213	+5	4	5	100	4	$\overline{SD}$	2	EN	28	*		1530
ADM222	+5	2	2	200	4	SD	0	No	18	19–17		1539
ADM223	+5	4	5	100	4	SD	2	$\overline{EN}$	28	19–19		1540
ADM232A	+5	2	2	200	4	No	0	No	16	19–17		1539
ADM242	+5	2	2	200	4	SD	0	$\overline{EN}$	18	19–17		1539
ADM203	+5	2	2	120	0	No	0	No	20	19–13	No Capacitors Required	1528

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

High Speed Networks & RS-xxx Interface Products–Selection Guides

RS-232 & EIA-562

Model	Power Supply #1 Volts	# Drivers	# Receivers	kBPS min	Ext Cap	Shutdown SD	# RCV Active	Three State Enable $\overline{EN}$	# Pins N/R	Page No.	Comments	Fax-code
ADM560	+3.3	4	5	116	4	SD	2	EN	28	19–23		1556
ADM561	+3.3	4	5	116	4	SD	0	$\overline{EN}$	28	19–23		1556

RS-232 or RS-423A, Mode Control, Programmable Slew Rate

Model	Power Supply #1 Volts	# Drivers	# Receivers	kBPS min	Ext Cap	Shutdown SD	# RCV Active	Three State Enable $\overline{EN}$	# Pins N/R	Page No.	Comments	Fax-code
ADM5170	±10	8	0	116	N/A	SD	0	$\overline{EN}$	28	19–27		1554
ADM5180	+5	0	8	200	N/A	SD	0	Fail-Safe Function	28	19–29		1555

Programmable, RS-232 and RS-422

Model	Power Supply #1 Volts	# Drivers	# Receivers	kBPS min	Ext Cap	Shutdown SD	# RCV Active	Three State Enable $\overline{EN}$	# Pins N/R	Page No.	Comments	Fax-code
AD7306	+5	1/1	2/1	100	4	No	0	No	24	19–11	Configured as RS-232	1273
AD7306	+5	1/1	1/2	5000	4	No	0	No	24	19–11	Configured as RS-422	1273

RS-485

Model	Power Supply #1 Volts	# Drivers	# Receivers	kBPS min	Ext Cap	Shutdown SD	# RCV Active	Three State Enable $\overline{EN}$	# Pins N/R	Page No.	Comments	Fax-code
ADM485	+5	1	1	5000	N/A	No	0	No	8	19–21		1553
ADM1485	+5	1	1	30000	N/A	No	0	No		19–25		1527

Clock Recovery and Data Retiming Phase-Locked Loop

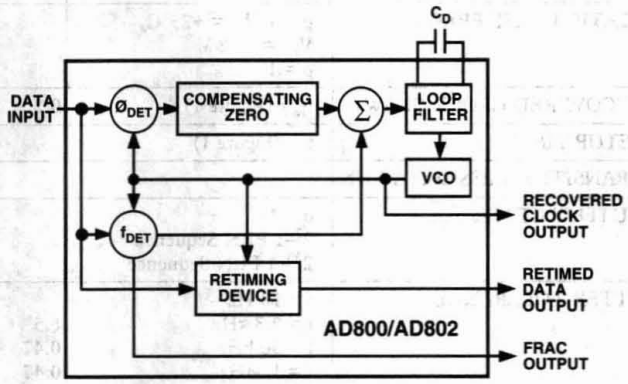
AD800/AD802*

FEATURES

Standard Products
- **44.736 Mbps—DS-3**
- **51.84 Mbps—STS-1**
- **155.52 Mbps—STS-3 or STM-1**

Accepts NRZ Data, No Preamble Required
Recovered Clock and Retimed Data Outputs
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Random Jitter: 20° Peak-to-Peak
Pattern Jitter: Virtually Eliminated
10KH ECL Compatible
Single Supply Operation: –5.2 V or +5 V
Wide Operating Temperature Range: –40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD800 and AD802 employ a second order phase-locked loop architecture to perform clock recovery and data retiming on Non-Return to Zero, NRZ, data. This architecture is capable of supporting data rates between 20 Mbps and 160 Mbps. The products described here have been defined to work with standard telecommunications bit rates. 45 Mbps DS-3 and 52 Mbps STS-1 are supported by the AD800-45 and AD800-52 respectively. 155 Mbps STS-3 or STM-1 are supported by the AD802-155.

Unlike other PLL-based clock recovery circuits, these devices do not require a preamble or an external VCXO to lock onto input data. The circuit acquires frequency and phase lock using two control loops. The frequency acquisition control loop initially acquires the clock frequency of the input data. The phase-lock loop then acquires the phase of the input data, and ensures that the phase of the output signals track changes in the phase of the input data. The loop damping of the circuit is dependent on the value of a user selected capacitor; this defines jitter peaking performance and impacts acquisition time. The devices exhibit 0.08 dB jitter peaking, and acquire lock on random or scrambled data within 4×10^5 bit periods when using a damping factor of 5.

During the process of acquisition the frequency detector provides a Frequency Acquisition (FRAC) signal which indicates that the device has not yet locked onto the input data. This signal is a series of pulses which occur at the points of cycle slip between the input data and the synthesized clock signal. Once the circuit has acquired frequency lock no pulses occur at the FRAC output.

The inclusion of a precisely trimmed VCO in the device eliminates the need for external components for setting center frequency, and the need for trimming of those components. The VCO provides a clock output within ±20% of the device center frequency in the absence of input data.

The AD800 and AD802 exhibit virtually no pattern jitter, due to the performance of the patented phase detector. Total loop jitter is 20° peak-to-peak. Jitter bandwidth is dictated by mask programmable fractional loop bandwidth. The AD800, used for data rates < 90 Mbps, has been designed with a nominal loop bandwidth of 0.1% of the center frequency. The AD802, used for data rates in excess of 90 Mbps, has a loop bandwidth of 0.08% of center frequency.

All of the devices operate with a single +5 V or –5.2 V supply.

ORDERING GUIDE

Device	Center Frequency	Fractional Loop Bandwidth	Description	Operating Temperature	Package Options*
AD800-45BQ	44.736 MHz	0.1%	20-Pin Cerdip	–40°C to +85°C	Q-20
AD800-52BR	51.84 MHz	0.1%	20-Pin Plastic SOIC	–40°C to +85°C	R-20
AD802-155BR	155.52 MHz	0.08%	20-Pin Plastic SOIC	–40°C to +85°C	R-20
AD802-155KR	155.52 MHz	0.08%	20-Pin Plastic SOIC	0°C to +70°C	R-20

*For outline information see Package Information section.

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AD800/AD802–SPECIFICATIONS

(V_{EE} = V_{MIN} to V_{MAX}, V_{CC} = GND, T_A = T_{MIN} to T_{MAX}, Loop Damping Factor = 5, unless otherwise noted)

Parameter[1]	Condition	AD800-45BQ Min	AD800-45BQ Typ	AD800-45BQ Max	AD800-52BR Min	AD800-52BR Typ	AD800-52BR Max	AD802-155KR/BR Min	AD802-155KR/BR Typ	AD802-155KR/BR Max	Units
NOMINAL CENTER FREQUENCY			44.736			51.84			155.52		MHz
OPERATING TEMPERATURE RANGE (T_{MIN} to T_{MAX})	K Grade							0		70	°C
	B Grade	–40		85	–40		85	–40		85	°C
TRACKING RANGE		43		45.5	49		53	155		156	Mbps
CAPTURE RANGE		43		45.5	49		53	155		156	Mbps
STATIC PHASE ERROR	ρ = 1, T_A = +25°C, V_{EE} = –5.2 V		2	10		2	10		14	30	Degrees
	ρ = 1		3	11.5		3	11.5		18	37	Degrees
RECOVERED CLOCK SKEW	t_{RCS} (Figure 1)	0.2	0.6	1	0.2	0.6	1	0.2	0.8	1	ns
SETUP TIME	t_{SU} (Figure 1)							2.06	2.37		ns
TRANSITIONLESS DATA RUN				240			240			240	Bit Periods
OUTPUT JITTER	ρ = 1		2			2			3.5		Degrees rms
	2^7–1 PRN Sequence		2.5	4.7		2.5	4.7		5.4	9.7	Degrees rms
	2^{23}–1 PRN Sequence		2.5	4.7		2.5	4.7		5.4	9.7	Degrees rms
JITTER TOLERANCE	f = 10 Hz		2,500			2,500			3,000		Unit Intervals
	f = 2.3 kHz	6.5									Unit Intervals
	f = 30 kHz	0.47									Unit Intervals
	f = 1 MHz	0.47									Unit Intervals
	f = 30 Hz				830						Unit Intervals
	f = 300 Hz				83						Unit Intervals
	f = 2 kHz				7.4						Unit Intervals
	f = 20 kHz				0.47						Unit Intervals
	f = 6.5 kHz							2.0	7.6		Unit Intervals
	f = 65 kHz							0.26	0.9		Unit Intervals
JITTER TRANSFER											
Damping Factor Capacitor, C_D											
ζ = 1, Nominal			8.2			6.8			2.2		nF
ζ = 5, Nominal			0.22			0.15			0.047		µF
ζ = 10, Nominal			0.82			0.68			0.22		µF
Peaking											
ζ = 1, Nominal	T_A = +25°C, V_{EE} = –5.2 V		2			2			2		dB
ζ = 5, Nominal	T_A = +25°C, V_{EE} = –5.2 V		0.08			0.08			0.08		dB
ζ = 10, Nominal	T_A = +25°C, V_{EE} = –5.2 V		0.02			0.02			0.02		dB
Bandwidth			45			52			130		kHz
ACQUISITION TIME											
ρ = 1/2	ζ = 1		1×10^4			1×10^4			1.5×10^4		Bit Periods
T_A = +25°C	ζ = 5		3×10^5	8×10^5		3×10^5	8×10^5		4×10^5	8×10^5	Bit Periods
V_{EE} = –5.2 V	ζ = 10		8×10^5			8×10^5			1.4×10^6		Bit Periods
POWER SUPPLY											
Voltage (V_{MIN} to V_{MAX})	T_A = +25°C	–4.5	–5.2	–5.5	–4.5	–5.2	–5.5	–4.5	–5.2	–5.5	Volts
Current	T_A = +25°C, V_{EE} = –5.2 V		125	170		125	170		140	180	mA
				180			180			205	mA
INPUT VOLTAGE LEVELS	T_A = +25°C										
Input Logic High, V_{IH}		–1.084		–0.72	–1.084		–0.72	–1.084		–0.72	Volts
Input Logic Low, V_{IH}		–1.95		–1.594	–1.95		–1.594	–1.95		–1.594	Volts
OUTPUT VOLTAGE LEVELS	T_A = +25°C										
Output Logic High, V_{OH}		–1.084		–0.72	–1.084		–0.72	–1.084		–0.72	Volts
Output Logic Low, V_{OL}		–1.95		–1.60	–1.95		–1.60	–1.95		–1.60	Volts
INPUT CURRENT LEVELS	T_A = +25°C										
Input Logic High, I_{IH}				125			125			125	µA
Input Logic Low, I_{IL}				80			80			80	µA
OUTPUT SLEW TIMES	T_A = +25°C										
Rise Time (t_R)	20%–80%		0.75	1.5		0.75	1.5		0.75	1.5	ns
Fall Time (t_F)	80%–20%		0.75	1.5		0.75	1.5		0.75	1.5	ns
SYMMETRY	ρ = 1/2, T_A = +25°C										
Recovered Clock Output	V_{EE} = –5.2 V	45		55	45		55	45		55	%

NOTES

[1]Refer to Glossary for parameter definition.

Specifications subject to change without notice.

Fiber Optic Receiver with Quantizer and Clock Recovery and Data Retiming

AD807

FEATURES

Meets CCITT G.958 Requirements for STM-1 Regenerator—Type A
Meets Bellcore TR-NWT-000253 Requirements for OC-3
Output Jitter: 2.0 Degrees RMS
155 Mbps Clock Recovery and Data Retiming
Accepts NRZ Data, No Preamble Required
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Quantizer Sensitivity: 2 mV
Level Detect Range: 2.0 mV to 30 mV
Single Supply Operation: +5 V or –5.2 V
Low Power: 140 mW
10 KH ECL/PECL Compatible Output
Package: 16-Pin Narrow 150 mil SOIC

PRODUCT DESCRIPTION

The AD807 provides the receiver functions of data quantization, signal level detect, and clock recovery and data retiming for 155 Mbps NRZ data. The device, together with a PIN diode/preamplifier combination, can be used for a highly integrated, low cost, low power SONET OC-3 or SDH STM-1 fiber optic receiver.

The receiver front end signal level detect circuit indicates when the input signal level has fallen below a user adjustable threshold. The threshold is set with a single external resistor. The signal level detect circuit 3 dB optical hysteresis prevents chatter at the signal level detect output.

The PLL has a factory trimmed VCO center frequency and a frequency acquisition control loop that combine to guarantee frequency acquisition without false lock. This eliminates a reliance on external components, like a crystal or a SAW filter, to aid frequency acquisition.

The AD807 acquires frequency and phase lock on input data using two control loops that work without requiring external control. The frequency acquisition control loop initially acquires the frequency of the input data, acquiring frequency lock on random or scrambled data without the need for a preamble. At frequency lock, the frequency error is zero, and the frequency detector has no further effect. The phase acquisition control loop then works to ensure that the output phase tracks the input phase. Pattern jitter is virtually eliminated through the AD807 due to a patented phase detector.

The device VCO uses a ring oscillator architecture and patented low noise design techniques. Jitter is 2.0 degrees rms. This low jitter results from using a fully differential signal architecture, Power Supply Rejection Ratio circuitry, and the use of a dielectrically isolated process that provides immunity from extraneous signals on the IC. The device can withstand hundreds of millivolts of power supply noise without an effect on jitter performance.

The user sets the jitter peaking and acquisition time of the PLL by choosing a damping factor capacitor whose value determines loop damping. CCITT G.958 Type A jitter transfer requirements can easily be met with a damping factor of 5 or greater.

Device design guarantees that the clock output frequency will drift by less than 20% in the absence of input data transitions. Shorting the damping factor capacitor, C_D, brings the clock output frequency to the VCO center frequency.

The AD807 consumes 140 mW and operates from a single power supply at either +5 V or –5.2 V.

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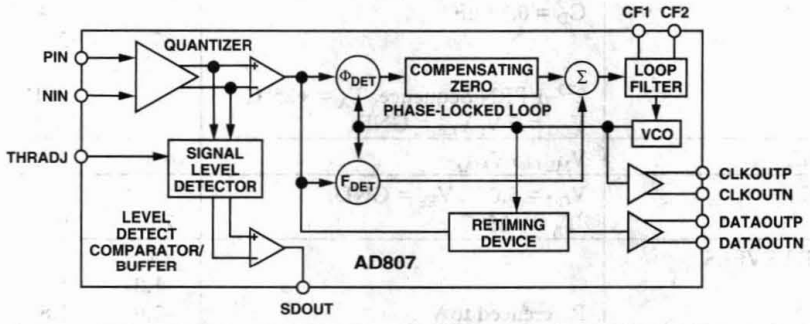
FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD807-155BR	–40°C to +85°C	16-Pin Narrowbody SOIC	R-16A
AD807-155BR-REEL7	–40°C to +85°C	750 Pieces, 7" Reel	R-16A

*For outline information see Package Information section.

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AD807–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = V_{MIN}$ to V_{MAX}, C_D = 0.1 µF, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
QUANTIZER–DC CHARACTERISTICS					
Input Voltage Range	@ P_{IN} or N_{IN}	2.5		V_S	V
Input Sensitivity, V_{SENSE}	P_{IN}–N_{IN}, Figure 1, BER = ≤ 1×10^{-10}	2			mV
Input Overdrive, V_{OD}	Figure 1, BER = ≤ 1×10^{-10}	0.001		2.5	V
Input Offset Voltage			50	500	µV
Input Current			5	10	µA
Input RMS Noise	BER = ≤ 1×10^{-10}		50		µV
Input Pk-Pk Noise	BER = ≤ 1×10^{-10}		650		µV
QUANTIZER–AC CHARACTERISTICS					
Upper –3 dB Bandwidth			180		MHz
Input Resistance			1		MΩ
Input Capacitance			2		pF
Pulse Width Distortion			100		ps
LEVEL DETECT					
Level Detect Range	R_{THRESH} = INFINITE	0.8	2	2.2	mV
	R_{THRESH} = 49.9 kΩ	4	5	7.4	mV
	R_{THRESH} = 3.4 kΩ	14	20	25	mV
Response Time	DC Coupled	0.1		1.5	µs
Hysteresis (Electrical)	R_{THRESH} = INFINITE	2.3	4.0	10.0	dB
	R_{THRESH} = 49.9 kΩ	3.0	5.0	9.0	dB
	R_{THRESH} = 3.4 Ω	3.0	7.0	10.0	dB
SDOUT Output Logic High	Load = +4 mA	3.6			V
SDOUT Output Logic Low	Load = –1.2 mA			0.4	V
PHASE-LOCKED LOOP NOMINAL CENTER FREQUENCY			155.52		MHz
CAPTURE RANGE		155		156	MHz
TRACKING RANGE		155		156	MHz
STATIC PHASE ERROR	2^7–1 PRN Sequence		4	20	Degrees
SETUP TIME (t_{SU})	Figure 2	3.0	3.2	3.5	ns
HOLD TIME (t_H)	Figure 2	3.0	3.1	3.3	ns
PHASE DRIFT	240 Bits, No Transitions			40	Degrees
JITTER	2^7–1 PRN Sequence		2.0		Degrees RMS
	2^{23}–1 PRN Sequence		2.0	2.7	Degrees RMS
JITTER TOLERANCE	f = 10 Hz		3000		Unit Intervals
	f = 6.5 kHz	4.5	7.6		Unit Intervals
	f = 65 kHz	0.45	1.0		Unit Intervals
	f = 1.3 MHz	0.45	0.67		Unit Intervals
JITTER TRANSFER					
Peaking (Figure 20)	C_D = 0.15 µF		0.08		dB
	C_D = 0.33 µF		0.04		dB
Bandwidth		65	92	130	kHz
Acquisition Time					
C_D = 0.1 µF	2^{23}–1 PRN Sequence, T_A = +25°C		4×10^5	2×10^6	Bit Periods
C_D = 0.33 µF	V_{CC} = 5 V, V_{EE} = GND		2×10^6		Bit Periods
POWER SUPPLY VOLTAGE	V_{MIN} to V_{MAX}	4.5		5.5	Volts
POWER SUPPLY CURRENT	V_{CC} = 5.0 V, V_{EE} = GND, T_A = +25°C	25	30	37	mA
PECL OUTPUT VOLTAGE LEVELS					
Output Logic High, V_{OH}		–1.2	–1.0	–0.7	Volts
Output Logic Low, V_{OL}	Referenced to V_{CC}	–2.0	–1.8	–1.7	Volts
SYMMETRY (Duty Cycle)	ρ = 1/2, T_A = +25°C,				
Recovered Clock Output, Pin 5	V_{CC} = 5 V, V_{EE} = GND	50.1		54.1	%
OUTPUT RISE / FALL TIMES					
Rise Time (t_R)	20%–80%		1.1	1.5	ns
Fall Time (t_F)	80%–20%		1.1	1.5	ns

Specifications subject to change without notice.

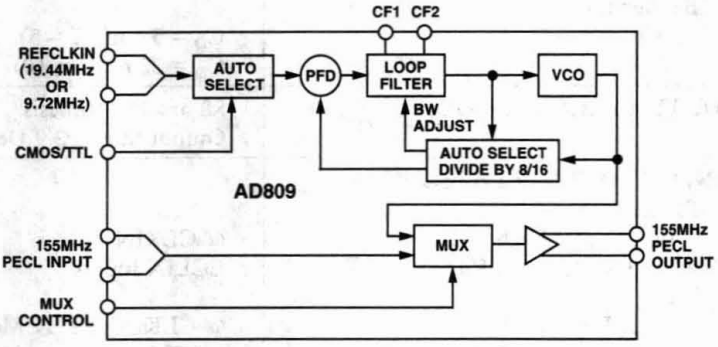
ANALOG DEVICES

155.52 MHz Frequency Synthesizer

AD809

FEATURES
Frequency Synthesis to 155.52 MHz
19.44 MHz or 9.72 MHz Input
Reference Signal Select Mux
Single Supply Operation: +5 V or –5.2 V
Output Jitter: 2.0 Degrees RMS
Low Power: 90 mW
10 KH ECL/PECL Compatible Output
10 KH ECL/PCL/TTL/CMOS Compatible Input
Package: 16-Pin Narrow 150 Mil SOIC

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

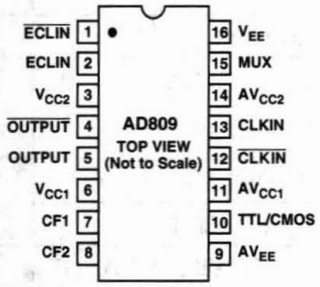
The AD809 provides a 155.52 MHz ECL/PECL output clock from either a 19.44 MHz or a 9.72 MHz TTL/CMOS/ECL/PECL reference frequency. The AD809 functionality supports a distributed timing architecture, allowing a backplane or PCB 19.44 MHz or 9.72 MHz timing reference signal to be distributed to multiple 155.52 Mbps ports. The AD809 can be applied to create the transmit bit clock for one or more ports.

An input signal multiplexer supports loop-timed applications where a 155.52 MHz transmit bit clock is recovered from the 155.52 Mbps received data.

The low jitter VCO, low power, and wide operating temperature range make the device suitable for generating a 155.52 MHz bit clock for SONET/SDH/Fiber in the Loop systems.

The device has a low cost, on-chip VCO that locks to either 8× or 16× the frequency at the 19.44 MHz or 9.72 MHz input. No external components are needed for frequency synthesis, however the user can adjust loop dynamics through selection of a damping factor capacitor whose value determines loop damping.

PIN CONFIGURATION



The AD809 design guarantees that the clock output frequency will drift low (by roughly 20%) in the absence of a signal at the REFCLKIN input.

The AD809 consumes 90 mW and operates from a single power supply at either +5 V or –5.2 V.

AD809–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = V_{MIN}$ to V_{MAX}, C_D = 22 nF, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
TRACKING AND CAPTURE RANGE[1]	×8 Synthesis	19.42		19.46	MHz
	×16 Synthesis	9.71		9.73	MHz
OUTPUT JITTER	×8 Synthesis		1.6	2.9	Degrees RMS
	×16 Synthesis		1.6	2.9	Degrees RMS
JITTER TRANSFER					
Bandwidth			200		kHz
Peaking	C_D = 5.6 nF (ζ = 5)		0.08		dB
	C_D = 22 nF (ζ = 10)		0.02		dB
DUTY CYCLE TOLERANCE	×8 or ×16 Synthesis				
	Output Jitter ≤ 2.9 Degrees RMS	15		85	%
INPUT VOLTAGE LEVELS					
PECL					
Input Logic High, V_{IH}	@ CLKIN &	3.8		V_{CC}	Volts
Input Logic Low, V_{IL}	ECLIN Inputs	3.1		3.6	Volts
TTL					
Input Logic High, V_{IH}	@ CLKIN, TTL/CMOS and	2.0			Volts
Input Logic Low, V_{IL}	MUX Inputs			0.8	Volts
OUTPUT VOLTAGE LEVELS	Referenced to V_{CC}				
PECL					
Output Logic High, V_{OH}		–1.2	–1.0	–0.7	Volts
Output Logic Low, V_{OL}		–2.0	–1.8	–1.7	Volts
SYMMETRY (Duty Cycle)	×8 Synthesis or ×16 Synthesis	46	52	62	%
OUTPUT RISE/FALL TIMES					
Rise Time (t_R)	20%–80%		1.1	1.5	ns
Fall Time (t_F)	80%–20%		1.1	1.5	ns
POWER SUPPLY VOLTAGE	V_{MIN} to V_{MAX}	4.5		5.5	Volts
POWER SUPPLY CURRENT			17	26	mA
OPERATING TEMPERATURE RANGE	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES

[1]Device design is guaranteed for operation over Capture Ranges and Tracking Ranges, however the device has wider capture and tracking ranges (for both ×8 and ×16 synthesis).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +12 V
Input Voltage (Pin 12 or Pin 13) . . . . . V_{CC} + 0.6 V
Maximum Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
ESD Rating (Human Body Model) . . . . . 500 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics:
16-Pin Narrow Body SOIC Package: θ_{JA} = 110°C/W.

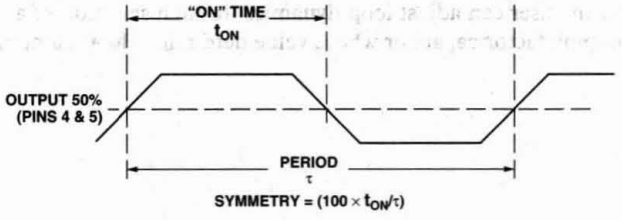


Figure 1. Symmetry

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD809BR	–40°C to +85°C	16-Pin Narrow Body SOIC	R-16A
AD809BR-REEL7	–40°C to +85°C	750 Pieces, 7" Reel	R-16A

*For outline information see Package Information section.

+5 V Powered RS-232/RS-422 Transceiver

AD7306

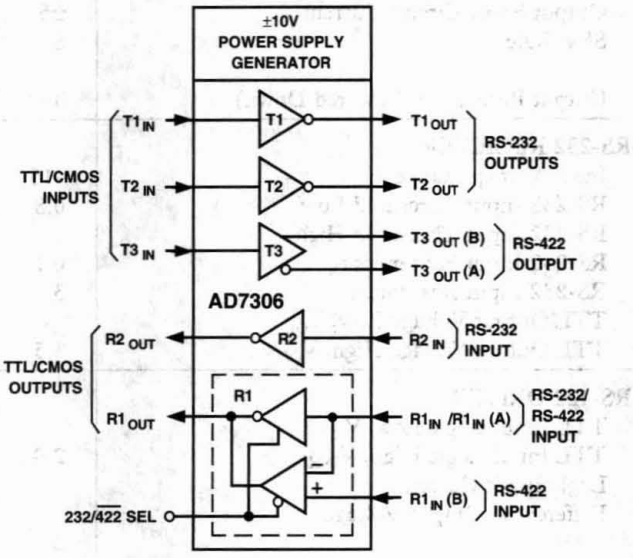
FEATURES

RS-232 and RS-422 on One Chip
Single +5 V Supply
0.1 µF Capacitors
Short Circuit Protection
Excellent Noise Immunity
Low Power BiCMOS Technology
High Speed, Low Skew RS-422 Operation
–40°C to +85°C Operations

APPLICATIONS

DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7306 line driver/receiver is a 5 V monolithic product which provides an interface between TTL signal levels and dual standard EIA RS-232/RS-422 signal levels. The part contains two RS-232 drivers, one RS-422 driver, one RS-232 receiver, and one receiver path which can be configured either as RS-232 or as RS-422.

An internal charge pump voltage converter facilitates operation from a single +5 V power supply. The internal charge pump generates ±10 V levels allowing RS-232 output levels to be developed without the need for external bipolar power supplies.

A highly efficient charge pump design allows operation using non polarized, miniature 0.1 µF capacitors. This gives a considerable saving in printed circuit board space over conventional products which can use up to 10 µF capacitors. The charge pump output voltages may also be used to power external circuitry which requires dual supplies.

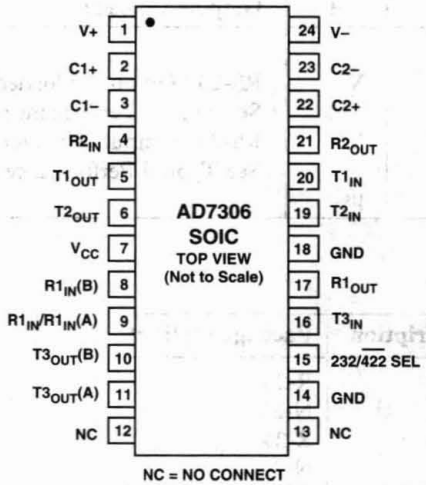
The RS-232 channels are suitable for communications rates up to 100 kHz and the RS-422 channels are suitable for high speed communications up to 5 MHz. The RS-422 transmitter complementary outputs are closely matched and feature low timing skew between the complementary outputs. This is often an essential requirement to meet tight system timing specifications.

All inputs feature ESD protection, all driver outputs feature high source and sink current capability and are internally protected against short circuits on the outputs. An epitaxial layer is used to guard against latch-up.

The part is available in a 24-lead SOIC and 24-pin plastic DIP package.

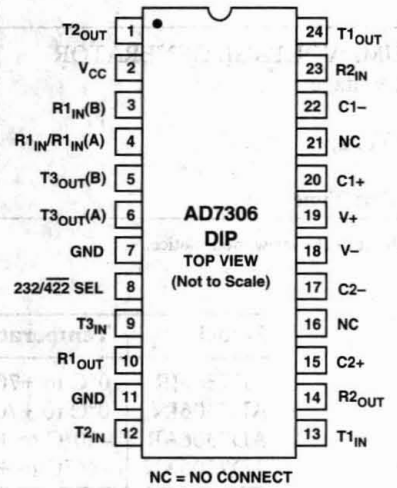
PIN CONFIGURATIONS

SOIC



NC = NO CONNECT

DIP



NC = NO CONNECT

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AD7306–SPECIFICATIONS (V_{CC} = +5 V ± 5%, C1 = C2 = C3 = C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RS-232 DRIVER					
TTL Input Logic Low, V_{INL}			0.8	V	
TTL Input Logic High, V_{INH}	2.0			V	
Input Logic Current		0.1	±10	µA	V_{IN} = 0 V to V_{CC}
RS-232 High Level Output Voltage	5.0	7.3		V	R_L = 3 kΩ
RS-232 Low Level Output Voltage	–5.0	–6.5		V	R_L = 3 kΩ
Output Short Circuit Current	±5	±12		mA	V_{OUT} = 0 V, T_A = 0°C to +70°C
Slew Rate	8	20	30	V/µs	C_L = 50 pF, R_L = 3 kΩ
		4		V/µs	C_L = 2500 pF, R_L = 3 kΩ
Output Resistance (Powered Down)	300	10M		Ω	V_{CC} = 0 V, V_{OUT} = ±3 V
RS-232 RECEIVER					
Input Voltage Range	–15		+15	V	
RS-232 Input Threshold Low	0.8	1.3		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.1	0.4	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = +4 mA
TTL Output Voltage High, V_{OH}	3.5	4.8		V	I_{OUT} = –4 mA
RS-422 DRIVER					
TTL Input Logic Low, V_{INL}			0.8	V	
TTL Input Logic High, V_{INH}	2.0			V	
Logic Input Current		0.1	±10	µA	V_{IN} = 0 V to V_{CC}
Differential Output Voltage			5.0	V	V_{CC} = 5 V, R_L Diff = ∞; Figure 3
	2			V	R_L Diff = 100 Ω; Figure 3
Common-Mode Output Voltage			3	V	
$\Delta\lvert V_{OUT}\rvert$ for Complementary O/P States			0.2	V	R_L Diff = 100 Ω
Output Short Circuit Current	35		150	mA	0 V ≤ V_{CMR} ≤ +7 V
RS-422 RECEIVER					
Common-Mode Voltage Range			±7	V	Typical RS-422 Input Voltage <5 V
Differential Input Threshold Voltage	–0.2		+0.2	V	
Input Voltage Hysteresis		70		mV	V_{CM} = 0 V
Input Resistance	3	5	7	kΩ	
TTL Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = +4.0 mA
TTL Output Voltage High, V_{OH}	3.5	4.8		V	I_{OUT} = –4.0 mA
232/$\overline{422}$ SEL Input					
Input Logic Low, V_{INL}			0.8	V	
Input Logic High, V_{INH}	2.0			V	
Logic Input Current		0.1	±10	µA	V_{IN} = 0 V to V_{CC}
POWER SUPPLY CURRENT					
I_{CC}		10	15	mA	Outputs Unloaded
CHARGE PUMP VOLTAGE GENERATOR					
V+ Output Voltage		9		V	RS-232 Output Unloaded; See Typical Performance Curves
V– Output Voltage		–9		V	RS-232 Outputs Unloaded; See Typical Performance Curves
Generator Rise Time		200		µs	

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD7306JR	0°C to +70°C	24-Lead SOIC	R-24
AD7306JN	0°C to +70°C	24-Pin DIP	N-24
AD7306AR	–40°C to +85°C	24-Lead SOIC	R-24
AD7306AN	–40°C to +85°C	24-Pin DIP	N-24

*For outline information see Package Information section.

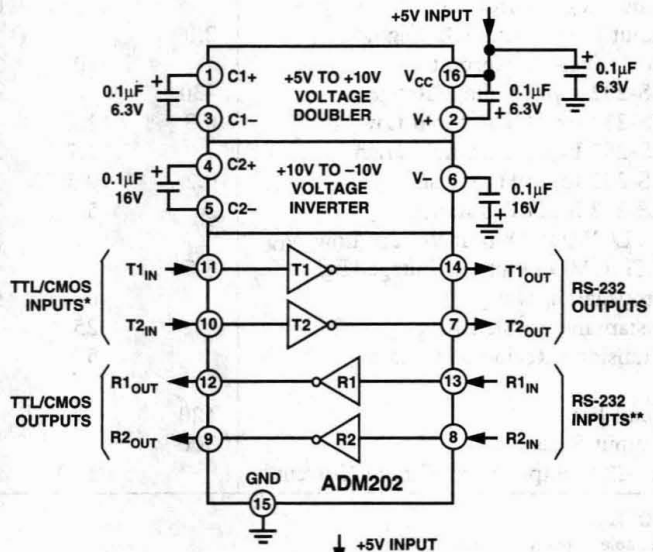
High Speed, +5 V, 0.1 µF CMOS RS-232 Driver/Receiver

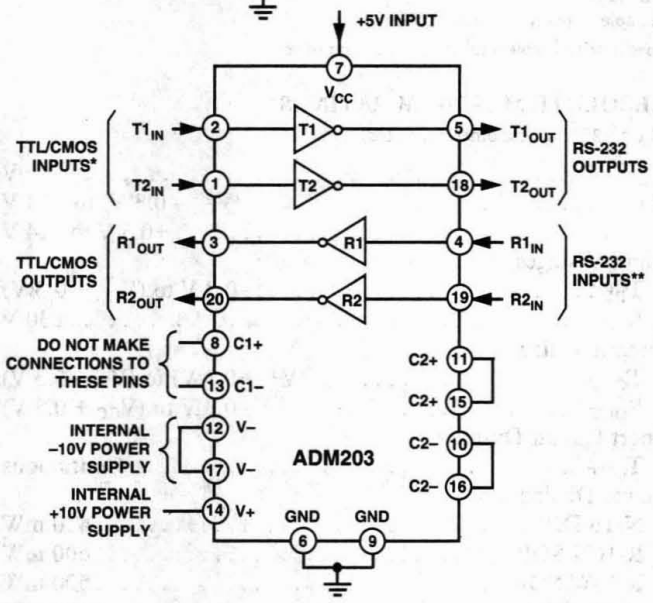
ADM202/ADM203

FEATURES
120 kB Transmission Rate
ADM202: Small (0.1 µF) Charge Pump Capacitors
ADM203: No External Capacitors Required
Single 5 V Power Supply
Meets EIA-232-E and V.28 Specifications
Two Drivers and Two Receivers
On-Board DC-DC Converters
±9 V Output Swing with +5 V Supply
Low Power BiCMOS: 2.0 mA I_{CC}
±30 V Receiver Input Levels

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

FUNCTIONAL BLOCK DIAGRAMS





*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

GENERAL DESCRIPTION

The ADM202/ADM203 is a two-channel RS-232 line driver/receiver pair designed to operate from a single +5 V power supply. A highly efficient on-chip charge pump design permits RS-232 levels to be developed using charge pump capacitors as small as 0.1 µF. The capacitors are internal to the package on the ADM203 so no external capacitors are required. These converters generate ±10 V RS-232 output levels.

The ADM202/ADM203 meets or exceeds the EIA-232-E and V.28 specifications. Fast driver slew rates permit operation up to 120 kB while high drive currents allows for extended cable lengths.

An epitaxial BiCMOS construction minimizes power consumption to 10 mW and also guards against latch-up. Overvoltage protection is provided allowing the receiver inputs to withstand continuous voltages in excess of ±30 V. In addition, all pins contain ESD protection to levels greater than 2 kV.

The ADM202 is available in 16-lead DIP and both narrow and wide SOIC packages. The ADM203 is available in a 20-pin DIP package.

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ADM202/ADM203–SPECIFICATIONS (V_{CC} = +5 V ± 10%, (ADM202 C1–C4 = 0.1 µF). All Specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Conditions/Comments
Output Voltage Swing	±5	±9		V	V_{CC} = 5 V ± 5%, $T1_{OUT}$, $T2_{OUT}$ Loaded with 3 kΩ to GND
Output Voltage Swing	±5	±9		V	V_{CC} = 5 V ± 10%, T_A = +25°C, $T1_{OUT}$, $T2_{OUT}$ Loaded with 3 kΩ to GND
V_{CC} Power Supply Current		1.5	2	mA	No Load, $T1_{IN}$, $T2_{IN}$ = V_{CC}
		3.0	4	mA	No Load, $T1_{IN}$, $T2_{IN}$ = GND
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}
Logic Pull-Up Current		10	25	µA	T_{IN} = 0 V
RS-232 Input Voltage Range	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
Propagation Delay		0.5	5	µs	RS-232 to TTL
Instantaneous Slew Rate[1]		25	30	V/µs	C_L = 10 pF, R_L = 3–7 kΩ, T_A = +25°C
Transition Region Slew Rate		5		V/µs	R_L = 3 kΩ, C_L= 2500 pF Measured from +3 V to –3 V or –3 V to +3 V
Baud Rate	120			kB	R_L = 3 kΩ, C_L = 1 nF
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10	±60	mA	

NOTE
[1]Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{CC} ..... +6 V
V+ ..... (V_{CC} – 0.3 V) to +14 V
V– ..... +0.3 V to –14 V
Input Voltages
  T_{IN} ..... –0.3 V to (V_{CC} + 0.3 V)
  R_{IN} ..... ±30 V
Output Voltages
  T_{OUT} ..... (V+, +0.3 V) to (V–, – 0.3 V)
  R_{OUT} ..... –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} ..... Continuous
Power Dissipation
  N-16 DIP ..... 470 mW
  R-16N SOIC ..... 600 mW
  R-16W SOIC ..... 500 mW
  N-20 DIP ..... 890 mW
Thermal Impedance
  N-16 DIP ..... 135°C/W
  R-16N SOIC ..... 105°C/W
  R-16W SOIC ..... 105°C/W
  N-20 DIP ..... 125°C/W
Operating Temperature Range
  Commercial (J Version) ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Soldering
  Vapor Phase (60 sec) ..... +215°C
  Infrared (15 sec) ..... +220°C
ESD Rating ..... >2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM202JN	0°C to +70°C	N-16
ADM202JRN	0°C to +70°C	R-16N
ADM202JRW	0°C to +70°C	R-16W
ADM203JN	0°C to +70°C	N-20

*For outline information see Package Information section.

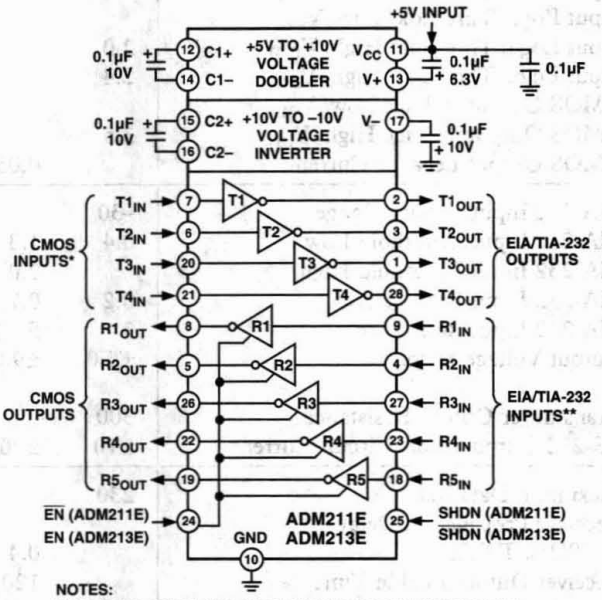
EMI/EMC Compliant, ±15 kV ESD Protected, RS-232 Line Drivers/Receivers

ADM207E/ADM208E/ADM211E/ADM213E

FEATURES
- Complies with 89/336/EEC EMC Directive
- ESD Protection to IEC1000-4-2 (801.2)
- ±8 kV: Contact Discharge
- ±15 kV: Air-Gap Discharge
- ±15 kV: Human Body Model
- Fast Transient Burst (EFT) Immunity (IEC1000-4-4)
- Low EMI Emissions (EN55022)
- Eliminates Costly TranZorbs*
- 230 kbits/s Data Rate Guaranteed
- Single +5 V Power Supply
- Shutdown Mode 1 μW
- Plug-In Upgrade for MAX2xxE
- Space Saving TSSOP Package Available

APPLICATIONS
- Laptop Computers
- Notebook Computers
- Printers
- Peripherals
- Modems

FUNCTIONAL BLOCK DIAGRAM



NOTES:
* INTERNAL 400kΩ PULL-UP RESISTOR ON EACH CMOS INPUT
** INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

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GENERAL DESCRIPTION

The ADM2xxE is a family of robust RS-232 and V.28 interface devices which operates from a single +5 V power supply. These products are suitable for operation in harsh electrical environments and are compliant with the EU directive on EMC (89/336/EEC). Both the level of emissions and immunity are in compliance. EM immunity includes ESD protection in excess of ±15 kV on all I-O lines (1000-4-2), Fast Transient Burst protection (1000-4-4) and Radiated Immunity (1000-4-3). EM emissions include radiated and conducted emissions as required by Information Technology Equipment EN55022, CISPR22.

All devices fully conform to the EIA-232E and CCITT V.28 specifications and operate at data rates up to 230 kbps.

Shutdown and Enable control pins are provided on some of the products. Please refer to Table I.

The shutdown function on the ADM211E disables the charge pump and all transmitters and receivers. On the ADM213E the charge pump, all transmitters, and three of the five receivers are disabled. The remaining two receivers remain active thereby allowing monitoring of peripheral devices. This feature allows the device to be shut down until a peripheral device begins communication. The active receivers can alert the processor which can then take the ADM213E out of the shutdown mode.

Operating from a single +5 V supply, four external 0.1 μF capacitors are required.

The ADM207E and ADM208E are available in 24-pin DIP, SO, SSOP and TSSOP packages. The ADM211E and ADM213E are available in 28-pin SO, SSOP and TSSOP packages.

All products are backward compatible with earlier ADM2xx products facilitating easy upgrading of older designs.

*TranZorb is a registered trademark of General Semiconductor Industries, Inc.

Table I. Selection Table

Model	Supply Voltage	Drivers	Receivers	ESD Protection	Shutdown	$\overline{\text{Enable}}$	Packages
ADM207E	+5 V	5	3	±15 kV	No	No	N, R, RS, RU-24
ADM208E	+5 V	4	4	±15 kV	No	No	N, R, RS, RU-24
ADM211E	+5 V	4	5	±15 kV	Yes	Yes	R, RS, RU-28
ADM213E	+5 V	4	3	±15 kV	Yes ($\overline{\text{SD}}$)*	Yes (EN)	R, RS, RU-28

*Two receivers active.

ADM207E/ADM208E/ADM211E/ADM213E–SPECIFICATIONS

(V_{CC} = +5.0 V ± 10%, C1–C4 = 0.1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Operating Voltage Range	+4.5	+5.0	+5.5	Volts	
V_{CC} Power Supply Current		3.5	6	mA	No Load
Shutdown Supply Current		0.2	5	µA	
Input Pull-Up Current		10	25	µA	T_{IN} = GND
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, EN, $\overline{EN}$, SHDN, $\overline{SHDN}$,
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}
Input Logic Threshold High, V_{INH}	2.4			V	EN, $\overline{EN}$, SHDN, $\overline{SHDN}$
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –40 µA
CMOS Output Leakage Current		0.05	±5	µA	$\overline{EN}$ = V_{CC}, EN = GND, 0 V ≤ R_{OUT} ≤ V_{CC}
EIA-232 Input Voltage Range	–30		+30	V	
EIA-232 Input Threshold Low	0.4	1.3		V	
EIA-232 Input Threshold High		2.0	2.4	V	
EIA-232 Input Hysteresis	0.2	0.7	1.0	V	
EIA-232 Input Resistance	3	5	7	kΩ	
Output Voltage Swing	±5.0	±9.0		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
Transmitter Output Resistance	300			Ω	V_{CC} = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current	±10	±20	±60	mA	
Maximum Data Rate	230			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 2500 pF
Receiver Propagation Delay TPHL, TPLH		0.4	2	µs	C_L = 150 pF
Receiver Output Enable Time, t_{ER}		120		ns	
Receiver Output Disable Time, t_{DR}		120		ns	
Transmitter Propagation Delay TPHL, TPLH		1		µs	R_L = 3 kΩ, C_L = 2500 pF
Transition Region Slew Rate	3	10	30	V/µs	R_L = 3 kΩ, C_L = 50 pF to 2500 pF Measured from +3 V to –3 V or –3 V to +3 V
ESD Protection (I-O Pins)		±15		kV	Human Body Model
		±15		kV	IEC1000-4-2 Air Discharge
		±8		kV	IEC1000-4-2 Contact Discharge
ESD Protection (All Other Pins)		±2.5		kV	Human Body Model, MIL-STD-883B
EFT Protection (I-O Pins)		±2		kV	IEC1000-4-4
EMI Immunity		10		V/m	IEC1000-4-3

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} ..... –0.3 V to +6 V
V+ ..... (V_{CC} – 0.3 V) to +14 V
V– ..... +0.3 V to –14 V
Input Voltages
  T_{IN} ..... –0.3 V to (V+, +0.3 V)
  R_{IN} ..... ±30 V
Output Voltages
  T_{OUT} ..... ±15 V
  R_{OUT} ..... –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} ..... Continuous
Power Dissipation
  N-24 DIP (Derate 13.5 mW/°C Above +70°C) .. 1000 mW
  R-24 SOIC (Derate 12 mW/°C Above +70°C) ... 900 mW
  RS-24 SSOP (Derate 12 mW/°C Above +70°C) .... 850 mW
  RU-24 TSSOP (Derate 12 mW/°C Above +70°C) .. 900 mW
  R-28 SOIC (Derate 12 mW/°C Above +70°C) ..... 900 mW
  RS-28 SSOP (Derate 10 mW/°C Above +70°C) .... 900 mW
  RU-24 TSSOP (Derate 12 mW/°C Above +70°C) .. 900 mW
Operating Temperature Range
  Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
ESD Rating (MIL-STD-883B) (I-O Pins) ..... ±15 kV
ESD Rating (MIL-STD-883B) (Except I-O) ..... ±2.5 kV
ESD Rating (IEC1000-4-2 Air) (I-O Pins) ..... ±15 kV
ESD Rating (IEC1000-4-2 Contact) (I-O Pins) ..... ±8 kV
EFT Rating (IEC1000-4-4) (I-O Pins) ..... ±2 kV

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

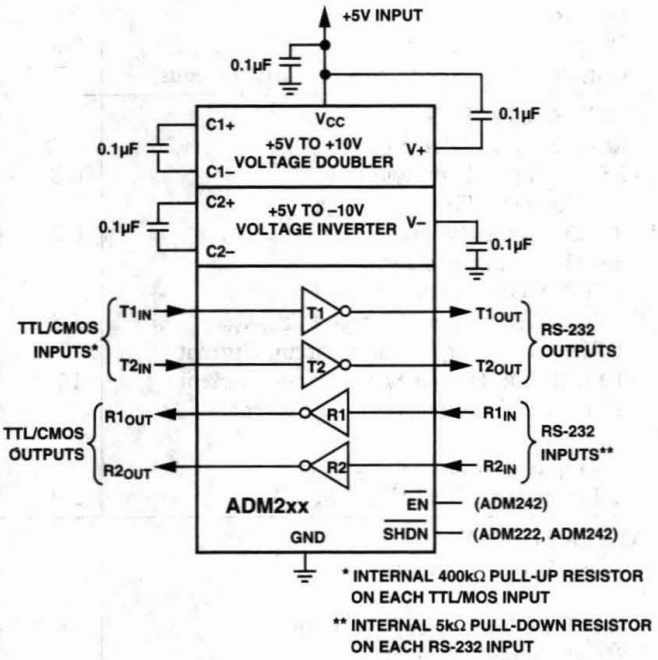
High Speed, +5 V, 0.1 µF CMOS RS-232 Drivers/Receivers

ADM222/ADM232A/ADM242*

FEATURES
200 kB/s Transmission Rate
Small (0.1 µF) Charge Pump Capacitors
Single 5 V Power Supply
Meets All EIA-232-E and V.28 Specifications
Two Drivers and Two Receivers
On-Board DC-DC Converters
±9 V Output Swing with +5 V Supply
±30 V Receiver Input Levels
Pin Compatible with MAX222/MAX232A/MAX242

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM222, ADM232A, ADM242 are a family of high speed RS-232 line drivers/receivers offering transmission rates up to 200 kB/s. Operating from a single +5 V power supply, a highly efficient on-chip charge pump using small (0.1 µF) external capacitors allows RS-232 bipolar levels to be developed. Two RS-232 drivers and two RS-232 receivers are provided on each device.

The devices are fabricated on BiCMOS, an advanced mixed technology process which combines low power CMOS with high speed bipolar circuitry. This allows for transmission rates up to 200 kB/s yet minimizes the quiescent power supply current to under 5 mA.

The ADM232A is a pin-compatible, high speed upgrade for the AD232 and for the ADM232L. It is available in 16-pin DIP and in both narrow and wide surface mount (SOIC) packages.

The ADM222 contains an additional shutdown ($\overline{SHDN}$) function which may be used to disable the device thereby reducing the supply current to 0.1 µA. During shutdown, all transmit/receive functions are disabled. The ADM222 is available in 18-pin DIP and in a wide surface mount (SOIC) package.

The ADM242 combines both shutdown ($\overline{SHDN}$) and enable ($\overline{EN}$) functions. The shutdown function reduces the supply curent to 0.1 mA. During shutdown, the transmitters are disabled but the receivers continue to operate normally. The enable function allows the receiver outputs to be disabled thereby facilitating sharing a common bus. The ADM242 is available in 18-pin DIP and in a wide surface mount (SOIC) package.

***Protected by U.S. Patent No. 5,237,209.**

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM222AN	–40°C to +85°C	N-18
ADM222AR	–40°C to +85°C	R-18W
ADM232AAN	–40°C to +85°C	N-16
ADM232AARN	–40°C to +85°C	R-16N
ADM232AARW	–40°C to +85°C	R-16W
ADM242AN	–40°C to +85°C	N-18
ADM242AR	–40°C to +85°C	R-18W

*For outline information see Package Information section.

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ADM222/ADM232A/ADM242–SPECIFICATIONS (V_{CC} = +5 V ± 10%, C1–C4 = 0.1 µF; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
RS-232 TRANSMITTERS					
Output Voltage Swing	±5	±9		V	All Transmitter Outputs Loaded with 3 kΩ to Ground
Input Logic Threshold Low, V_{INL}		1.4	0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.0	1.4		V	T_{IN}
Logic Pullup Current		5	40	µA	T_{IN} = 0 V
Data Rate	200			kB/s	
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
Output Short Circuit Current (Instantaneous)	±7	±22		mA	
RS-232 RECEIVERS					
RS-232 Input Voltage Range	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.3		V	
RS-232 Input Threshold High		1.8	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	V_{CC} = 5 V
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}		0.2	0.4	V	I_{OUT} = 3.2 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
TTL/CMOS Output Short-Circuit Current	–2	–10		mA	Source Current (V_{OUT} = GND)
TTL/CMOS Output Short-Circuit Current	10	30		mA	Sink Current (V_{OUT} = V_{CC})
TTL/CMOS Output Leakage Current		±0.05	±10	µA	$\overline{SHDN}$ = GND/$\overline{EN}$ = V_{CC} 0 V ≤ V_{OUT} ≤ V_{CC}
$\overline{EN}$ Input Threshold Low, V_{INL}		1.4	0.8	V	
$\overline{EN}$ Input Threshold High, V_{INH}	2.0	1.4		V	
POWER SUPPLY					
Power Supply Current		4	8	mA	No Load
		15		mA	3 kΩ Load on Both Outputs
Shutdown Power Supply Current		0.1	10	µA	
$\overline{SHDN}$ Input Leakage Current			±1	µA	
$\overline{SHDN}$ Input Threshold Low, V_{INL}		1.4	0.8	V	
$\overline{SHDN}$ Input Threshold High, V_{INH}	2.0	1.4		V	
AC CHARACTERISTICS					
Transition Region Slew Rate	6	12	30	V/µs	C_L = 50 pF to 2500 pF, R_L = 3 kΩ to 7 kΩ Measured from +3 V to –3 V or –3 V to +3 V
Transmitter Propagation Delay TTL to RS-232		0.7	3.5	µs	t_{PHLT}
		0.7	3.5	µs	t_{PLHT}
Receiver Propagation Delay RS-232 to TTL		0.2	0.5	µs	t_{PHLR}
		0.3	0.5	µs	t_{PLHR}
Receiver Output Enable Time		125	500	ns	t_{ER}
Receiver Output Disable Time		160	500	ns	t_{DR}
Transmitter Output Enable Time		250		µs	$\overline{SHDN}$ Goes high
Transmitter Output Disable Time		3.5		µs	$\overline{SHDN}$ Goes low
Transmitter + to – Propagation Delay Difference		300		ns	
Receiver + to – Propagation Delay Difference		100		ns	

Specifications subject to change without notice.

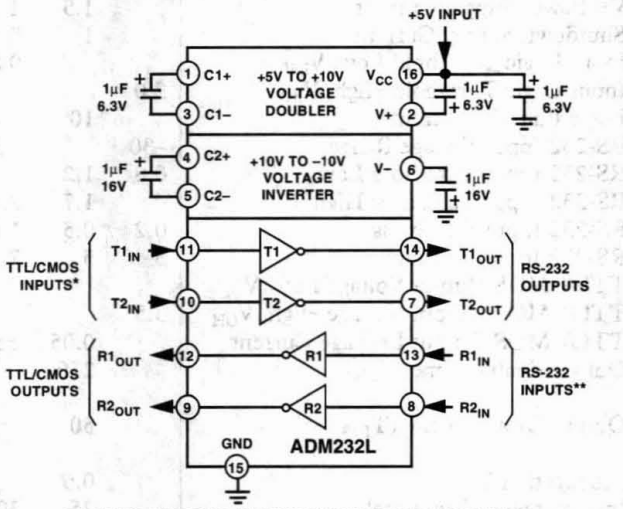
+5 V Powered CMOS RS-232 Drivers/Receivers

ADM223/ADM230L–ADM241L

FEATURES
Single 5 V Power Supply
Meets All EIA-232-E and V.28 Specifications
120 kB/s Data Rate
On-Board DC-DC Converters
±9 V Output Swing with +5 V Supply
Small 1 µF Capacitors
Low Power Shutdown ≤1 µA
Receivers Active in Shutdown (ADM223)
ESD > 2 kV
±30 V Receiver Input Levels
Latch-Up FREE
Plug-In Upgrade for MAX223/230-241
Plug-In Upgrade for AD230–AD241

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

ADM232L TYPICAL OPERATING CIRCUIT



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

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GENERAL DESCRIPTION

The ADM2xx family of line drivers/receivers is intended for all EIA-232-E and V.28 communications interfaces, especially in applications where ±12 V is not available. The ADM223, ADM230L, ADM235L, ADM236L and ADM241L feature a low power shutdown mode which reduces power dissipation to less than 5 µW making them ideally suited for battery powered equipment. Two receivers remain enabled during shutdown on the ADM223. The ADM233L and ADM235L do not require any external components and are particularly useful in applications where printed circuit board space is critical.

All members of the ADM230L family, except the ADM231L and the ADM239L, include two internal charge pump voltage converters which allow operation from a single +5 V supply. These converters convert the +5 V input power to the ±10 V required for RS-232 output levels. The ADM231L and ADM239L are designed to operate from +5 V and +12 V supplies. An internal +12 V to –12 V charge pump voltage converter generates the –12 V supply.

The ADM2xxL is an enhanced upgrade for the AD2xx family featuring lower power consumption, faster slew rate and operation with smaller (1 µF) capacitors.

Table I. Selection Table*

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Pins
ADM223	+5 V	4	5	4	Yes ($\overline{SD}$)	Yes (EN)	28
ADM230L	+5 V	5	0	4	Yes	No	20
ADM231L	+5 V & +7.5 V to +13.2 V	2	2	2	No	No	14
ADM232L	+5 V	2	2	4	No	No	16
ADM233L	+5 V	2	2	None	No	No	20
ADM234L	+5 V	4	0	4	No	No	16
ADM235L	+5 V	5	5	None	Yes	Yes	24
ADM236L	+5 V	4	3	4	Yes	Yes	24
ADM237L	+5 V	5	3	4	No	No	24
ADM238L	+5 V	4	4	4	No	No	24
ADM239L	+5 V & +7.5 V to +13.2 V	3	5	2	No	Yes	24
ADM241L	+5 V	4	5	4	Yes	Yes	28

*For outline information see Package Information section.

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ADM223/ADM230L–ADM241L–SPECIFICATIONS

(V_{CC} = +5 V ± 10% (ADM223, 31L, 32L, 34L, 36L, 38L, 39L, 41L); V_{CC} = +5 V ± 5% (ADM230L, 33L, 35L, 37L); V+ = 7.5 V to 13.2 V (ADM231L & ADM239L); C1–C4 = 1.0 µF Ceramic. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	±5	±9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		2	3.0	mA	No Load, All T_{INS} = V_{CC} (Except ADM223)
		3.5	6	mA	No Load, All T_{INS} = GND
		0.4	1	mA	ADM231L, ADM239L
V+ Power Supply Current		1.5	4	mA	No Load, V+ = 12 V ADM231L & ADM239L Only
Shutdown Supply Current		1	5	µA	
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$
Logic Pull-Up Current		10	25	µA	T_{IN} = 0 V
RS-232 Input Voltage Range	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.7	2.4	V	
RS-232 Input Hysteresis	0.2	0.5	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
TTL/CMOS Output Leakage Current		0.05	±5	µA	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		250		ns	ADM223, ADM235L, ADM236L, ADM239L, ADM241L (Figure 25. C_L = 150 pF)
Output Disable Time (T_{DIS})		50		ns	ADM223, ADM235L, ADM236L, ADM239L, ADM241L (Figure 25. R_L = 1 kΩ)
Propagation Delay		0.5		µs	RS-232 to TTL
Instantaneous Slew Rate[1]		25	30	V/µs	C_L = 10 pF, R_L = 3-7 kΩ, T_A = +25°C
Transition Region Slew Rate		5		V/µs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to –3 V or –3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10		mA	

NOTE
[1]Sample tested to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} ..... –0.3 V to +6 V
V+ ..... (V_{CC} – 0.3 V) to +14 V
V– ..... +0.3 V to –14 V
Input Voltages
  T_{IN} ..... –0.3 V to (V_{CC} + 0.3 V)
  R_{IN} ..... ±30 V
Output Voltages
  T_{OUT} ..... (V+, + 0.3 V) to (V–, – 0.3 V)
  R_{OUT} ..... –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} ..... Continuous
Power Dissipation
  N-14 DIP (Derate 10 mW/°C above +70°C) ..... 800 mW
  N-16 DIP (Derate 10.5 mW/°C above +70°C) ..... 840 mW
  N-20 DIP (Derate 11 mW/°C above +70°C) ..... 890 mW
  N-24 DIP (Derate 13.5 mW/°C above +70°C) ..... 1000 mW
  N-24A DIP (Derate 13.5 mW/°C above +70°C) ..... 500 mW
  R-16 SOIC (Derate 9 mW/°C above +70°C) ..... 760 mW
  R-20 SOIC (Derate 9.5 mW/°C above +70°C) ..... 800 mW
  R-24 SOIC (Derate 12 mW/°C above +70°C) ..... 850 mW
  R-28 SOIC (Derate 12.5 mW/°C above +70°C) ..... 900 mW
  RS-28 SSOP (Derate 10 mW/°C above +70°C) ..... 900 mW
  Q-14 Cerdip (Derate 10 mW/°C above +70°C) ..... 720 mW
  Q-16 Cerdip (Derate 10 mW/°C above +70°C) ..... 800 mW
  Q-20 Cerdip (Derate 11.2 mW/°C above +70°C) ..... 890 mW
  Q-24 Cerdip (Derate 12.5 mW/°C above +70°C) ..... 1000 mW
  D-24 Ceramic (Derate 20 mW/°C above +70°C) ..... 1000 mW

Thermal Impedance, θ_{JA}
  N-14 DIP ..... 140°C/W
  N-16 DIP ..... 135°C/W
  N-20 DIP ..... 125°C/W
  N-24 DIP ..... 120°C/W
  N-24A DIP ..... 110°C/W
  R-16 SOIC ..... 105°C/W
  R-20 SOIC ..... 105°C/W
  R-24 SOIC ..... 85°C/W
  R-28 SOIC ..... 80°C/W
  RS-28 SSOP ..... 100°C/W
  Q-14 Cerdip ..... 105°C/W
  Q-16 Cerdip ..... 100°C/W
  Q-20 Cerdip ..... 100°C/W
  Q-24 Cerdip ..... 55°C/W
  D-24 Ceramic ..... 50°C/W
Operating Temperature Range
  Commercial (J Version) ..... 0 to +70°C
  Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to + 150°C
Lead Temperature, Soldering ..... +300°C
  Vapour Phase (60 sec) ..... +215°C
  Infrared (15 sec) ..... +220°C
ESD Rating ..... >2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operaion secuons of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

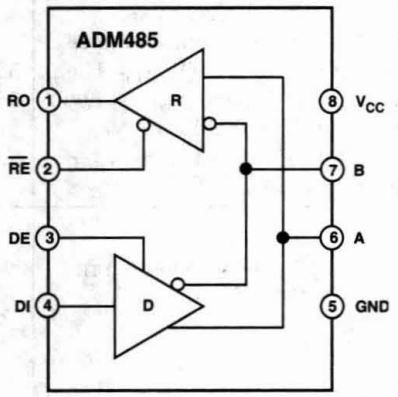
+5 V Low Power EIA RS-485 Transceiver

ADM485

FEATURES
Meets EIA RS-485 Standard
5 Mb/s Data Rate
Single +5 V Supply
–7 V to +12 V Bus Common-Mode Range
High Speed, Low Power BiCMOS
Thermal Shutdown Protection
Short Circuit Protection
Zero Skew Driver
Driver Propagation Delay: 10 ns
Receiver Propagation Delay: 25 ns
High Z Outputs with Power Off
Superior Upgrade for LTC485

APPLICATIONS
Low Power RS-485 Systems
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The ADM485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are tristated.

The ADM485 operates from a single +5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if during fault conditions a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM485 driver features high output impedance when disabled and also when powered down. This minimizes the loading effect when the transceiver is not being utilized. The high impedance driver output is maintained over the entire common-mode voltage range from –7 V to +12 V.

The receiver contains a fail safe feature which results in a logic high output state if the inputs are unconnected (floating).

The ADM485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 5 Mbits/s while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in an 8-pin DIL/SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM485JN	0°C to +70°C	N-8
ADM485JR	0°C to +70°C	R-8
ADM485AN	–40°C to +85°C	N-8
ADM485AR	–40°C to +85°C	R-8
ADM485AQ	–40°C to +85°C	Q-8

*For outline information see Package Information section.

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ADM485–SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	R = ∞, Figure 1
	2.0		5.0	V	V_{CC} = 5 V, R = 50 Ω (RS-422), Figure 1
	1.5		5.0	V	R = 27 Ω (RS-485), Figure 1
V_{OD3}	1.5		5.0	V	V_{TST} = –7 V to +12 V, Figure 2
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Figure 1
Common-Mode Output Voltage V_{OC}			3	V	R = 27 Ω or 50 Ω, Figure 1
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω
Output Short Circuit Current (V_{OUT} = High)	35		250	mA	–7 V ≤ V_O ≤ +12 V
Output Short Circuit Current (V_{OUT} = Low)	35		250	mA	–7 V ≤ V_O ≤ +12 V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI)			±1.0	µA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	–0.2		+0.2	V	–7 V ≤ V_{CM} ≤ +12 V
Input Voltage Hysteresis, ΔV_{TH}		70		mV	V_{CM} = 0 V
Input Resistance	12			kΩ	–7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			+1	mA	V_{IN} = 12 V
			–0.8	mA	V_{IN} = –7 V
Logic Enable Input Current ($\overline{RE}$)			±1	µA	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +4.0 mA
CMOS Output Voltage High, V_{OH}	4.0			V	I_{OUT} = –4.0 mA
Short Circuit Output Current	7		85	mA	V_{OUT} = GND or V_{CC}
Tristate Output Leakage Current			±1.0	µA	0.4 V ≤ V_{OUT} ≤ +2.4 V
POWER SUPPLY CURRENT					
I_{CC} (Outputs Enabled)		1.35	2.2	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}
I_{CC} (Outputs Disabled)		0.7	1	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}

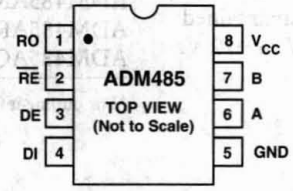
Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	2	10	15	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver O/P to $\overline{O/P}$ T_{SKEW}		0	5	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Rise/Fall Time T_R, T_F		2	10	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Enable to Output Valid		10	25	ns	
Driver Disable Timing		10	25	ns	
RECEIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	18	25	40	ns	C_L = 15 pF, Figure 5
Skew $\|T_{PLH}–T_{PHL}\|$		0	5	ns	
Receiver Enable T_{EN1}		15	25	ns	Figure 6
Receiver Disable T_{EN2}		15	25	ns	Figure 6

Specifications subject to change without notice.

PIN CONFIGURATION



Ultralow Power, +3.3 V, RS-232 Notebook PC Serial Port Drivers/Receivers

ADM560/ADM561

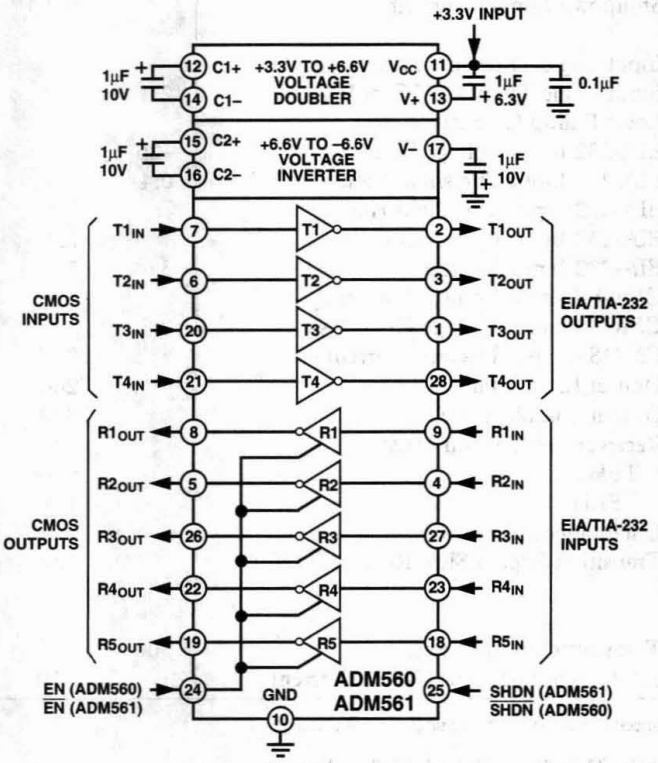
FEATURES

RS-232 Compatible
Operates with 3 V or 5 V Logic
Ultralow Power CMOS: 1.3 mA Operation
Low Power Shutdown: 0.2 μA
Suitable for Serial Port Mice
116 kbits/s Data Rate
1 μF Charge Pump Capacitors
Single +3 V to +3.6 V Power Supply
Two Receivers Active in Shutdown (ADM560)

APPLICATIONS

Laptop Computers
Palmtop Computers
Notebook Computers
Peripherals
Modems
Printers
Battery Operated Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM560/ADM561 are four driver/five receiver interface devices designed to meet the EIA-232 standard while operating with a single +3.3 V power supply. The devices feature an on-board dc-to-dc converter, eliminating the need for dual ±5 V power supplies. This dc-dc converter contains a voltage doubler and voltage inverter which internally generates ±6.6 V from the input +3.3 V power supply.

The ADM560 and ADM561 consume only 5 mW making them ideally suited for battery and other power-sensitive applications. A shutdown facility is also provided which reduces the power to 0.66 μW.

The ADM560 contains active low shutdown and active high receiver enable signals. In shutdown mode, two receivers remain active thereby allowing monitoring of peripheral devices. This feature allows the device to be shut down until a peripheral device begins communication. The active receivers can alert the processor which can then take the ADM560 out of the shutdown mode.

The ADM561 features active high shutdown and an active low receiver enable. In this device all receivers are disabled in shutdown.

The ADM560/ADM561 is fabricated using CMOS technology for minimal power consumption. It features a high level of overvoltage protection and latch-up immunity. The receiver inputs can withstand up to ±25 V levels. The transmitter inputs can be driven from either 3 V or 5 V logic levels. This allows operation in mixed 3 V/5 V power supply systems.

The ADM560/ADM561 is packaged in a 28-pin SO and a 28-pin SSOP package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM560JR	0°C to +70°C	R-28
ADM560JRS	0°C to +70°C	RS-28
ADM561JR	0°C to +70°C	R-28
ADM561JRS	0°C to +70°C	RS-28

*For outline information see Package Information section.

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ADM560/ADM561–SPECIFICATIONS (V_{CC} = +3.3 V ±10%, C1–C4 = 1 µF. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	±5.0	±5.5		Volts	V_{CC} = 3.3 V, Three Transmitter Outputs Loaded with 3 kΩ to Ground
	±4	±4.5		Volts	V_{CC} = 3.0 V, All Transmitter Outputs Loaded into 3 kΩ to Ground
V_{CC} Power Supply Current		1.3	2	mA	No Load, T_{IN} = V_{CC}
		2.2	3.0	mA	No Load, T_{IN} = GND
Shutdown Supply Current		0.2	5	µA	$\overline{SHDN}$ = GND (ADM560); SHDN = V_{CC} (ADM561), T_{IN} = V_{CC}
Input Logic Threshold Low, V_{INL}			0.4	V	T_{IN}, EN, $\overline{EN}$, SHDN, $\overline{SHDN}$,
Input Logic Threshold High, V_{INH}	2.4			V	T_{IN}, EN, $\overline{EN}$, SHDN, $\overline{SHDN}$
Logic Pullup Current		3	20	µA	T_{IN} = GND
EIA-232 Input Voltage Range	–25		+25	V	
EIA-232 Input Threshold Low	0.4	0.8		V	
EIA-232 Input Threshold High		1.1	2.4	V	
EIA-232 Input Hysteresis		0.3		V	
EIA-232 Input Resistance	3	5	7	kΩ	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
CMOS Output Voltage High, V_{OH}	2.8			V	I_{OUT} = –40 µA
CMOS Output Leakage Current		0.05	±5	µA	$\overline{EN}$ = V_{CC}, EN = GND, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time		200		ns	
Output Disable Time		300		ns	
Receiver Propagation Delay					
TPHL		0.4	1	µs	
TPLH		1.3	2	µs	
Instantaneous Slew Rate			30	V/µs	C_L = 50 pF, R_L = 3 kΩ–7 kΩ
Transition Region Slew Rate		5.0		V/µs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to –3 V or –3 V to +3 V
Transmitter Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10		mA	

Specifications subject to change without notice.

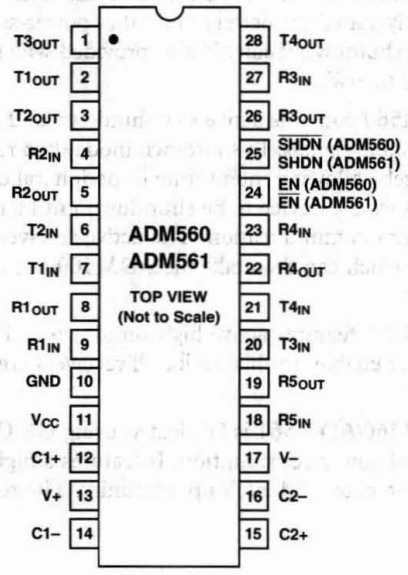
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} ..... –0.3 V to +6 V
V+ ..... (V_{CC} –0.3 V) to +14 V
V– ..... +0.3 V to –14 V
Input Voltages
T_{IN} ..... –0.3 V to (V+, +0.3 V)
R_{IN} ..... ±25 V
Output Voltages
T_{OUT} ..... (V+, +0.3 V) to (V–, –0.3 V)
R_{OUT} ..... –0.3 V to (V_{CC} +0.3 V)
Short Circuit Duration
T_{OUT} ..... Continuous
Power Dissipation
SSOP ..... 900 mW
SOIC ..... 900 mW
Operating Temperature Range
Commercial (J Version) ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
ESD Rating ..... >2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

PIN CONFIGURATIONS



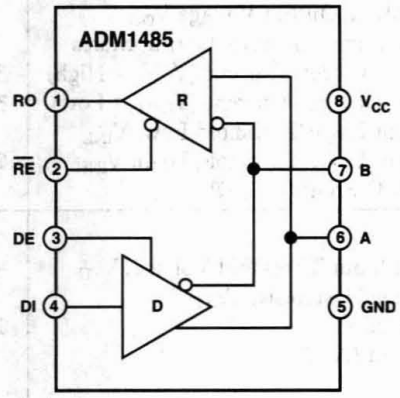
+5 V Low Power EIA RS-485 Transceiver

ADM1485

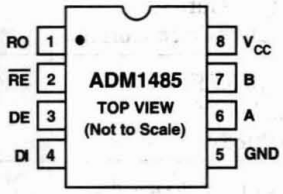
FEATURES
Meets EIA RS-485 Standard
30 Mb/s Data Rate
Single +5 V Supply
–7 V to +12 V Bus Common-Mode Range
High Speed, Low Power BiCMOS
Thermal Shutdown Protection
Short Circuit Protection
Zero Skew Driver
Driver Propagation Delay: 10 ns
Receiver Propagation Delay: 25 ns
High Z Outputs with Power Off
Superior Upgrade for LTC1485

APPLICATIONS
Low Power RS-485 Systems
DTE-DCE Interface
Packet Switching
Local Area Networks
Data Concentration
Data Multiplexers
Integrated Services Digital Network (ISDN)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



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GENERAL DESCRIPTION

The ADM1485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both EIA Standards RS-485 and RS-422. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are tristated.

The ADM1485 operates from a single +5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if during fault conditions a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important therefore that the remaining disabled drivers do not load the bus. To ensure this, the ADM1485 driver features high output impedance when disabled and also when powered down.

This minimizes the loading effect when the transceiver is not being utilized. The high impedance driver output is maintained over the entire common-mode voltage range from –7 V to +12 V.

The receiver contains a fail safe feature which results in a logic high output state if the inputs are unconnected (floating).

The ADM1485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM1485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 30 Mbits/s while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in an 8-pin DIL/SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM1485JN	0°C to +70°C	N-8
ADM1485JR	0°C to +70°C	R-8
ADM1485AN	–40°C to +85°C	N-8
ADM1485AR	–40°C to +85°C	R-8
ADM1485AQ	–40°C to +85°C	Q-8

*For outline information see Package Information section.

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ADM1485–SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Differential Output Voltage, V_{OD}			5.0	V	R = ∞, Figure 1
	2.0		5.0	V	V_{CC} = 5 V, R = 50 Ω (RS-422), Figure 1
	1.5		5.0	V	R = 27 Ω (RS-485), Figure 1
V_{OD3}	1.5		5.0	V	V_{TST} = –7 V to +12 V, Figure 2
$\Delta\|V_{OD}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω, Figure 1
Common-Mode Output Voltage V_{OC}			3	V	R = 27 Ω or 50 Ω, Figure 1
$\Delta\|V_{OC}\|$ for Complementary Output States			0.2	V	R = 27 Ω or 50 Ω
Output Short Circuit Current (V_{OUT} = High)	35		250	mA	–7 V ≤ V_O ≤ +12 V
Output Short Circuit Current (V_{OUT} = Low)	35		250	mA	–7 V ≤ V_O ≤ +12 V
CMOS Input Logic Threshold Low, V_{INL}			0.8	V	
CMOS Input Logic Threshold High, V_{INH}	2.0			V	
Logic Input Current (DE, DI)			±1.0	µA	
RECEIVER					
Differential Input Threshold Voltage, V_{TH}	–0.2		+0.2	V	–7 V ≤ V_{CM} ≤ +12 V
Input Voltage Hysteresis, ΔV_{TH}		70		mV	V_{CM} = 0 V
Input Resistance	12			kΩ	–7 V ≤ V_{CM} ≤ +12 V
Input Current (A, B)			+1	mA	V_{IN} = 12 V
			–0.8	mA	V_{IN} = –7 V
Logic Enable Input Current ($\overline{RE}$)			±1	µA	
CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = +4.0 mA
CMOS Output Voltage High, V_{OH}	4.0			V	I_{OUT} = –4.0 mA
Short Circuit Output Current	7		85	mA	V_{OUT} = GND or V_{CC}
Three-State Output Leakage Current			±1.0	µA	0.4 V ≤ V_{OUT} ≤ +2.4 V
POWER SUPPLY CURRENT					
I_{CC} (Outputs Enabled)		1.35	2.2	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}
I_{CC} (Outputs Disabled)		0.7	1	mA	Outputs Unloaded, Digital Inputs = GND or V_{CC}

Specifications subject to change without notice.

TIMING SPECIFICATIONS (V_{CC} = +5 V ± 5%. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DRIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	2	10	15	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver O/P to $\overline{O/P}$ T_{SKEW}		0	5	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Rise/Fall Time T_R, T_F		2	10	ns	R_L Diff = 54 Ω C_{L1} = C_{L2} = 100 pF, Figure 3
Driver Enable to Output Valid		10	25	ns	
Driver Disable Timing		10	25	ns	
RECEIVER					
Propagation Delay Input to Output T_{PLH}, T_{PHL}	18	25	40	ns	C_L = 15 pF, Figure 5
Skew $\|T_{PLH}–T_{PHL}\|$		0	5	ns	
Receiver Enable T_{EN1}		15	25	ns	Figure 6
Receiver Disable T_{EN2}		15	25	ns	Figure 6

Specifications subject to change without notice.

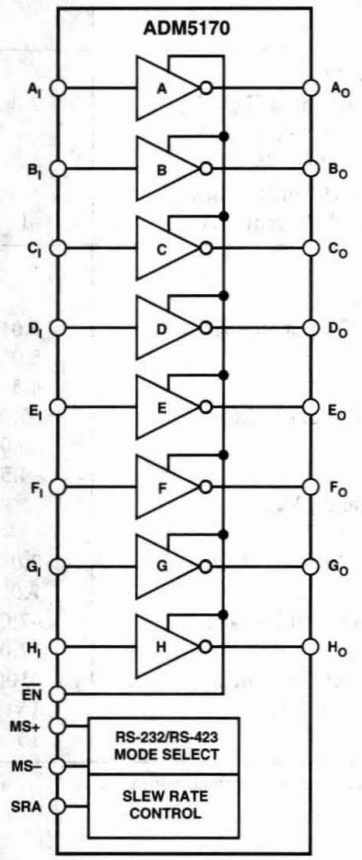
Octal, RS-232/RS-423 Line Driver

ADM5170

FEATURES
Eight Single Ended Line Drivers in One Package
Meets EIA Standard RS-232E, RS-423A and CCITT V.10/X.26
Resistor Programmable Slew Rate
Wide Supply Voltage Range
Low Power CMOS
3-State Outputs
TTL/CMOS Compatible Inputs
Output Short Circuit Protection
Available in 28-Pin DIP/PLCC
Low Power Replacement for UC5170C

APPLICATIONS
High Speed Communication
Computer I-O Ports Peripherals
High Speed Modems
Printers
Logic Level Translation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM5170 is an octal line driver suitable for digital communication systems with data rates up to 116 kB/s. Input TTL or CMOS signal levels are inverted and translated into either EIA RS-232E or RS-423A signal levels depending on the status of the Mode Select inputs MS+ and MS–. With both Mode Select inputs at GND, RS-423 operation is selected while with MS+ connected to V_{DD} and MS– connected to V_{SS}, RS-232 operation is selected.

The output slew rates may be controlled using an external resistor connected between the SRA (Slew Rate Adjust) pin and GND. Resistor values between 2 kΩ and 10 kΩ may be selected giving a slew rate which can be adjusted from 10 V/µs to 2.2 V/µs. This adjustment of the slew rate allows tailoring of the output characteristics to suit the interface cable being used.

The outputs may be disabled using the $\overline{EN}$ (Enable Input). This feature permits sharing of a common output line.

The ADM5170 is fabricated on an advanced CMOS process featuring low power consumption. In the disabled state the power consumption reduces from 500 mW to 40 mW. The ADM5170 is available in both 28-pin DIP and 28-lead PLCC packages.

Truth Table

Inputs $\overline{EN}$	Data	Outputs EIA RS-232E*	RS-423A
0	0	(V_{DD} – 3 V)	5 V to 6 V
0	1	(V_{SS} – 3 V)	–5 V to –6 V
1	X	High Z	High Z

*Minimum Output Level

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM5170JN	0°C to +70°C	N-28
ADM5170AN	–40°C to +85°C	N-28
ADM5170JP	0°C to +70°C	P-28A
ADM5170AP	–40°C to +85°C	P-28A

*For outline information see Package Information section.

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ADM5170–SPECIFICATIONS

(V_{DD} = +10 V ± 10%, V_{SS} = –10 V ± 10% V, MS+ = MS– = 0 V, R_{SRA} = 10 kΩ. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD} Range	9		15	V	
V_{SS} Range	–9		–15	V	
I_{DD} (Disabled)		2	4	mA	$\overline{EN}$ = High
I_{DD} (Enabled)		25	36	mA	R_L = ∞, $\overline{EN}$ = 0 V
I_{SS} (Disabled)		–2	–4	mA	$\overline{EN}$ = High
I_{SS} (Enabled)		–23	–36	mA	R_L = ∞, $\overline{EN}$ = 0 V
DIGITAL INPUTS					
Input Logic Threshold High, V_{INH}	2.0			V	
Input Logic Threshold Low, V_{INL}			0.8	V	
Input Clamp Voltage, V_{INK}		–1.1	–1.8	V	I_{IN} = –15 mA
Input High Level Current, I_{INH}			1	μA	V_{INH} = 2.4 V
Input Low Level Current, I_{INL}	–1			μA	V_{INL} = 0.4 V
OUTPUTS					
RS-423A Outputs					$\overline{EN}$ = 0.8 V, MS+ = MS– = 0 V
High Level Output Voltage	5.0	5.3	6.0	V	R_L = ∞, V_{IN} = 0.8 V
	5.0	5.3	6.0	V	R_L = 3 kΩ, V_{IN} = 0.8 V
	4.5	5.2	6.0	V	R_L = 450 Ω, V_{IN} = 0.8 V
Low Level Output Voltage	–5.0	–5.3	–6.0	V	R_L = ∞, V_{IN} = 2.0 V
	–5.0	–5.6	–6.0	V	R_L = 3 kΩ, V_{IN} = 2.0 V
	–4.5	–5.4	–6.0	V	R_L = 450 Ω, V_{IN} = 2.0 V
Output Balance, V_{BAL}		0.05	0.4	V	R_L = 450 Ω, V_{BAL} = V_{OH} – V_{OL}
RS-232 Outputs					$\overline{EN}$ = 0.8 V, MS+ = V_{DD}, MS– = V_{SS}
High Level Output Voltage	7.0	7.6	V_{DD}	V	R_L = ∞, V_{IN} = 0.8 V
	7.0	7.6	V_{DD}	V	R_L = 3 kΩ, V_{IN} = 0.8 V
Low Level Output Voltage	–7.0	–7.7	V_{SS}	V	R_L = ∞, V_{IN} = 2.0 V
	–7.0	–7.7	V_{SS}	V	R_L = 3 kΩ, V_{IN} = 2.0 V
Off-State Output Current, I_{OZ}	–100		100	μA	$\overline{EN}$ = 2.0 V, V_O = ±6 V, V_{DD} = 15 V, V_{SS} = –15 V
Short Circuit Current, I_{OS}	15	50	100	mA	V_{IN} = 0 V, $\overline{EN}$ = 0 V
	15	40	100	mA	V_{IN} = 5 V, $\overline{EN}$ = 0 V

Specifications subject to change without notice.

TIMING CHARACTERISTICS

(V_{DD} = +10 V ± 10%, V_{SS} = –10 V ± 10%, MS+ = MS– = 0 V. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Slew Rate					Fig 1, Fig 2. R_{SRA} = 2 kΩ, R_L = 450 Ω, C_L = 50 pF
	6.65	10	14	V/μs	Rising/Falling Edge, t_R, t_F
Output Slew Rate					Fig 1, Fig 2. R_{SRA} = 10 kΩ, R_L = 450 Ω, C_L = 50 pF
	1.33	2.0	3	V/μs	Rising/Falling Edge, t_R , t_F
Output to Hi-Z Propagation Delay (Disable)					Fig 1, Fig 3. R_{SRA} = 10 kΩ, R_L = 450 Ω, C_L = 50 pF
		0.3	1.0	μs	t_{HZ}
		0.5	1.0	μs	t_{LZ}
Hi-Z to Valid Output Propagation Delay (Enable)					Fig 1, Fig 3. R_{SRA} = 10 kΩ, R_L = 450Ω, C_L = 50 pF
		6.0	15	μs	t_{ZH}
		7.0	15	μs	t_{ZL}

Specifications subject to change without notice.

ANALOG DEVICES

Octal, RS-232/RS-423 Line Receiver

ADM5180

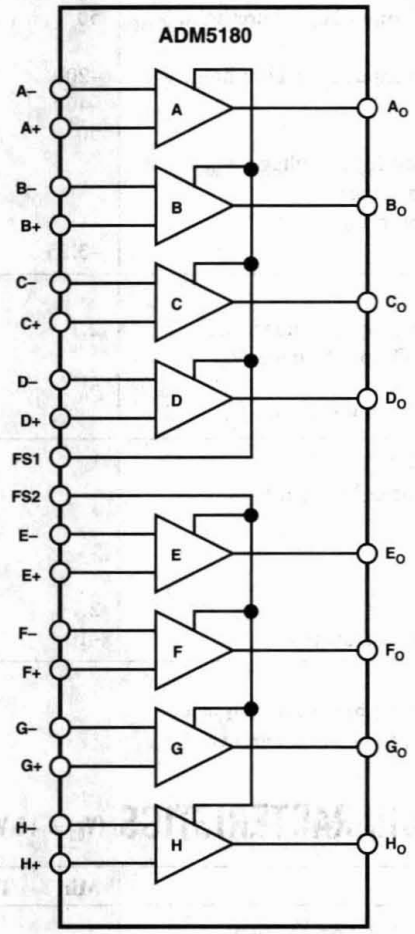
FEATURES

Eight Differential Line Receivers in One Package
Meets EIA Standard EIA-232E, 423A, 422A and CCITT V.10, V.11, V.28
Single +5 V Supply
Differential Inputs Withstand ±25 V
Internal Hysteresis
Low Power CMOS –3.5 mA Supply Current
TTL/CMOS Compatible Outputs
Available in 28-Pin DIP and PLCC Packages
Low Power Replacement for UC5180C/NE5180

APPLICATIONS

High Speed Communication
Computer I-O Ports
Peripherals
High Speed Modems
Printers
Logic Level Translation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM5180 is an octal differential line receiver suitable for a wide range of digital communication systems with data rates up to 200 kB/s. Input signals conforming to EIA Standards 232-E, 422A and CCITT V.10, V.11, V.28, X.26, and X.27 are accepted and translated into TTL /CMOS output signal levels.

The ADM5180 is a superior upgrade for the UC5180C and the NE5180. It is fabricated on an advanced BiCMOS process, allowing high speed bipolar circuitry to be combined with low power CMOS. This minimizes the power consumption to less than 25 mW.

A failsafe function ensures a known output state under a variety of input fault conditions as defined in RS-422A and RS-423A. The failsafe function is controlled by FS1 and FS2. Each controls four receivers. With FS = Low and a fault condition the output is forced low while if FS = High, the output is forced high.

The device is available in both 28-pin DIP and 28-lead PLCC packages.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM5180JN	0°C to +70°C	N-28
ADM5180AN	–40°C to +85°C	N-28
ADM5180JP	0°C to +70°C	P-28A
ADM5180AP	–40°C to +85°C	P-28A

For outline information see Package Information section.

Truth Table

Differential Input (+) - (–)	Failsafe Input FS1, FS2	Receiver Logic Output
>200 mV	X	H
<–200 mV	X	L
O/C	L	L
S/C	L	L
O/C	H	H
S/C	H	H

ADM5180–SPECIFICATIONS (V_{DD} = +5 V ± 5%, Input Common-Mode Range = ±7 V. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	4.75		5.25	V	
I_{DD}		3.5	5	mA	
INPUTS					
Input Resistance, R_{IN}	3		7	kΩ	3 V ≤ |V_{IN}| ≤ 25 V
Differential Input High Threshold, V_{TH}	50		200	mV	R_S = 0 Ω, V_{OUT} = 2.7 V, I_{OUT} = –440 µA, See Figure 1
			400	mV	R_S = 500 Ω, V_{OUT} = 2.7 V, I_{OUT} = –440 µA, See Figure 1
Differential Input Low Threshold, V_{TL}	–200		–50	mV	R_S = 0 Ω, V_{OUT} = 0.45 V, I_{OUT} = 8 mA, See Figure 1
	–400			mV	R_S = 500 Ω, V_{OUT} = 0.45 V, I_{OUT} = 8 mA, See Figure 1
Hysteresis, V_H	50		140	mV	FS1, FS2 = 0 V or V_{DD}, See Figure 1
Open Circuit Input Voltage, V_{IOC}			60	mV	
Input Capacitance			20	pF	
Input Current, I_{IN}			3.25	mA	V_{IN} = +10 V
	–3.25			mA	V_{IN} = –10 V
OUTPUTS					
High Level Output Voltage, V_{OH}	2.7			V	V_{ID} = 1.0 V, I_{OUT} = –440 µA
Low Level Output Voltage , V_{OL}			0.4	V	V_{ID} = –1.0 V, I_{OUT} = 4 mA
			0.45	V	V_{ID} = –1.0 V, I_{OUT} = 8 mA, T_A = 0°C to +70°C
Short Circuit O/P Current, I_{OS}			100	mA	Note 1
FAILSAFE FUNCTION					
Failsafe Output Voltage, V_{OFS}					Inputs Open or Shorted Together or One Input Open and One Grounded
			0.40	V	0 ≤ I_{OUT} ≤ 4 mA; FS1, FS2 = 0 V
			0.45	V	0 ≤ I_{OUT} ≤ 8 mA, T_A = 0°C to +70°C; FS1, FS2 = 0 V
	2.7			V	0 ≥ I_{OUT} ≥ –400 µA; FS1, FS2 = V_{DD}
FS1, FS2 Input Current	–10		+10	µA	

NOTE
[1]Only one output may be shorted at any time.

Specifications subject to change without notice.

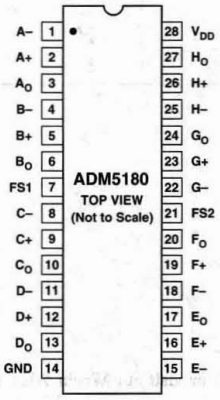
TIMING CHARACTERISTICS (V_{DD} = +5 V ± 5%. All Specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Propagation Delay–Low to High			550	ns	C_L = 50 pF, V_{IN} = ±500 mV
Propagation Delay–High to Low			550	ns	C_L = 50 pF, V_{IN} = ±500 mV
Acceptable Input Frequency			0.1	MHz	Unused Input Grounded, V_{IN} = ±200 mV
Rejectable Input Frequency	5.5			MHz	Unused Input Grounded, V_{IN} = ±500 mW

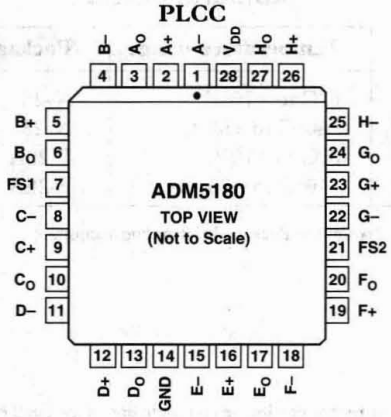
Specifications subject to change without notice.

PIN CONFIGURATIONS

DIP



PLCC



Power Management Circuits
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Power Management Circuits–Selection Guides

Micropower Linear Voltage Regulators

Dual Mode, +5 V, or Adjustable +1.6 V to +16 V

Model	Input Voltage Range Volts Min	Max	Nominal Output Voltage Volts Min	Max	I_{OUT} mA	I_Q @ I_{OUT} max mA	V_{BATT} Detect	I_{OUT} Sense	V_{TEMP} Output	Dropout Voltage mV @ I_{MAX}	# Pins	Page No.	Comments	Fax-code
ADP3367	+2.5	+16.5	+4.75	+5.25	200	14	Yes	No	No	250	8	20–37	6 kV ESD Protection	1913
ADP667	+3.5	+16.5	+4.8	+5.2	200	20	Yes	No	No	250	8	20–11		1917
ADM663	+2	+16.5	+4.75	+5.25	40	12	No	Yes	Yes	NS	8	*		1558
ADM666	+2	+16.5	+4.75	+5.25	40	12	Yes	No	No	NS	8	*		1558
ADP3301	+2.7–5	+22	See Comments		100	2	No	No	No	100	8	20–33	2, 7, 3, 3.2, 3.3, 5 V	
ADP3302	+2.7–5	+25	See Comments		100	8	No	Yes	No	100	8	20–35	2, 7, 3, 3.2, 3.3, 5 V	

Trimode, +3 V, +5 V or Adjustable +1.3 V to +16 V

Model	Input Voltage Range Volts Min	Max	Nominal Output Voltage Volts Min	Max	I_{OUT} mA	I_Q @ I_{OUT} max mA	V_{BATT} Detect	I_{OUT} Sense	V_{TEMP} Output	Dropout Voltage mV @ I_{MAX}	# Pins	Page No.	Comments	Fax-code
V_{SET} = LOW ADM663A	+2	+16.5	+4.75	+5.25	100	12	No	Yes	Yes	100	8	20–9		1559
V_{SET} = HIGH ADM663A	+2	+16.5	+3.135	+3.465	100	12	No	Yes	Yes	100	8	20–9		1559
V_{SET} = LOW ADM666A	+2	+16.5	+4.75	+5.25	100	12	Yes	No	No	100	8	20–9		1559
V_{SET} = HIGH ADM666A	+2	+16.5	+3.135	+3.465	100	12	Yes	No	No	100	8	20–9		1559

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

Micropower Switching Regulators†

Model	Input Voltage Range Volts Min	Max	Nominal Output Voltage Volts Min	I_{OUT} mA	I_Q @ I_{OUT} max	V_{BATT} Detect	Oscillator Frequency kHz	Duty Cycle %	T_{ON} µs	# Pins	Page No.	Comments	Fax-code
ADP1073	+1.0	+12.6	+3.3, 5, 12	40	125 µA‡	Yes	19	72	38	8	20–13	Step-Up, Step-Down	2015
ADP1173	+2.0	+30	+3.3, 5, 12	80	150 µA‡	Yes	24	55	23	8	20–29	Step-Up, Step-Down	2016
ADP1108	+2	+12.6	+3.3, 5, 12	150	100 µA‡	Yes	19	70	36	8	20–15	Step-Up, Step-Down	2017
ADP1109	+3	NS	+3.3, 5, 12	100	550 µA‡	No	120	50	4.2	8	20–17	Step-Up	2018
ADP1110	+1.15	+12.6	+3.3, 5, 12	NS	300 µA‡	Yes	72	65	7	8	20–19	Step-Down	2019
ADP1111	+2	+12.6	+3.3, 5, 12	100	400 µA‡	Yes	70	69	38	8	20–21	Step-Up, Step-Down	2020
ADP3000	+2	+30	+3.3, 5, 12	100	500 µA‡	No	400	90	2	8	20–31	With Internal Switch	2028

†All available with adjustable outputs.
‡In Standby mode.

Power Management Circuits–Selection Guides

DC-to-DC Converters

Unregulated Switched Cap Voltage

Model	V dc Input Volts	Oscillator Frequency kHz	V dc Out Volts	I_{OUT} mA	With Shutdown	# Pins	Page No.	Comments	Fax-code
ADM660	+1.5–+7	25–120	–1.5––7	100	No	8	20–7	Voltage Inverter Configuration	1934
ADM660	+2.5–+7	25–120	+5–+14		No	8	20–7	Voltage Doubler Configuration	1934
ADM8660	+1.5–+7	25–120	–1.5––7	100	Yes	8	20–7	With Shutdown, I_Q = 0.3 µA	1934

Regulated Switched Cap Voltage

Model	V dc Input Volts	Oscillator Frequency kHz	V dc Out Volts	I_{OUT} mA	With Shutdown	Pins	Page No.	Comments	Fax-code
ADP3603	+4.5–+6	240	–2.7––3.3	50	Yes	8	20–39	Output Ohms/Ripple = 12 Ω/25 mV	1982
ADP3604	+4.5–+6	240	–2.7––3.3	120	Yes	8	20–41	Output Ohms/Ripple = 8 Ω/25 mV	1982

High Efficiency Step-Down Switching Regulator Controller

Model	V dc Input Volts	Oscillator Frequency kHz	V dc Out Volts	I_{OUT} mA	# Pins	Page No.	Comments	Fax-code
ADP1147-3.3	3.5–20	400	3.0	700	8	20–23	P-Channel Drive	2022
ADP1147-5	3.5–20	400	5.0	700	8	20–23	P-Channel Drive	2022
ADP1148-3.3†	3.5–20	250	3.0	700	14	20–25	N- & P-Channel Drive	2023
ADP1148-5†	3.5–20	250	5.0	700	14	20–25	N- & P-Channel Drive	2023
ADP1149-3.3†	3.3–48	250	3.0	700	16	20–27	N- & P-Channel Drive	2024
ADP1149-5†	3.3–48	250	5.0	700	16	20–27	N- & P-Channel Drive	2024

†Synchronous operation.

High Power, High Efficiency

Model	V dc Input Volts	Integral EMI Filter	V dc Out Volts	I_{OUT} Amps	Watts max	# Pins	Page No.	Comments	Fax-code
ADDC02805S	16–50	Yes	5	20	100	17	20–5	See Notes	1947

NOTES
1. All products are manufactured in a hermetically sealed, molybdenum hybrid package. Typ weight for each product is 85 grams.
2. All products are available in three screening/price levels: industrial, ruggedized industrial, 883B/SMD.
3. Contact factory for modified standard versions and for information on lower power product line in development.

28 V/100 W DC/DC Converter with Integral EMI Filter

ADDC02805S

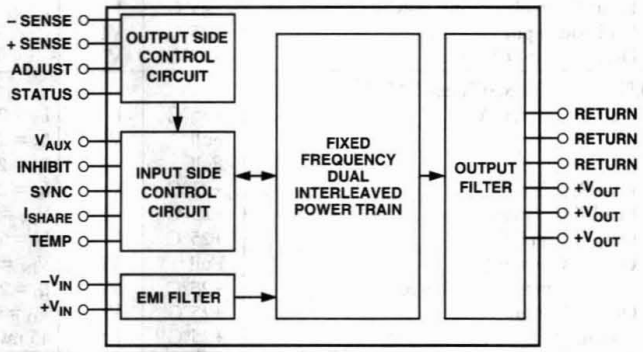
FEATURES

28 V dc Input, 5 V dc @ 20 A, 100 W Output
Integral EMI Filter Designed to Meet MIL-STD-461D
Low Weight: 80 Grams
NAVMAT Derated
Many Protection and System Features

APPLICATIONS

Commercial and Military Airborne Electronics
Missile Electronics
Space-Based Antennae and Vehicles
Mobile/Portable Ground Equipment
Distributed Power Architecture for Active Array Radar

FUNCTIONAL BLOCK DIAGRAM



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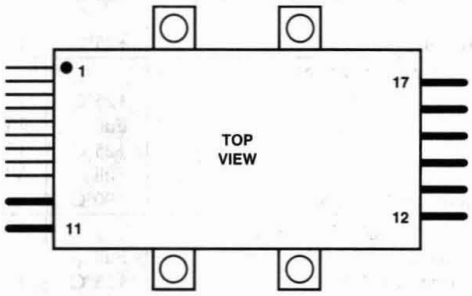
GENERAL DESCRIPTION

The ADDC02805S hybrid dc/dc converter with integral EMI filter offers the highest power density of any dc/dc converter with its features and in its power range available today. The converter with integral EMI filter is a fixed frequency, 1 MHz, square wave switching dc/dc power supply. It is not a variable frequency resonant converter. In addition to many protection features, this converter has system level features that allow it to be used as a component in larger systems as well as a stand-alone power supply. The unit is designed for high reliability and high performance applications where saving space and/or weight are critical.

The ADDC02805S is available in three screening grades; all grades use a hermetically sealed, molybdenum based hybrid package. Contact factory for MIL-STD-883 device availability.

PIN CONFIGURATION



ORDERING INFORMATION

Device	Operating Temperature Range (Case)	Description
ADDC02805SAKV	–40°C to +85°C	Hermetic Package
ADDC02805SATV	–55°C to +90°C	Hermetic Package
ADDC02805SATV/883B*	–55°C to +125°C	Hermetic Package

*Contact factory.

ADDC02805S–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (T_C = +25°C, V_{IN} = 28 V dc ±0.5 V dc, unless otherwise noted; full temperature range is –55°C to +90°C; all temperatures are case and T_C is the temperature measured at the center of the package bottom.)

Parameter	Case Temp	Test Level	Conditions	ADDC02805S Min	Typ	Max	Units
INPUT CHARACTERISTICS							
Steady State Operating Input Voltage Range[1]	Full	VI	I_O = 2 A to 20 A	18	28	40	V
Abnormal Operating Input Voltage Range (Per MIL-STD-704D)[1]	Full	VI	I_O = 2 A to 16 A	16		50	V
Input Overvoltage Shutdown	+25°C	I		50	52.5	55	V
No Load Input Current	+25°C	VI			82	90	mA
Disabled Input Current	+25°C	VI			4	5	mA
OUTPUT CHARACTERISTICS[2, 3]							
Output Voltage (V_O)	+25°C	I	I_O = 2 A to 20 A, V_{IN} = 18 V to 40 V dc	5.00	5.025	5.05	V
	Full	VI	I_O = 2 A to 20 A, V_{IN} = 18 V to 40 V dc	4.90		5.10	V
	Full	VI	I_O = 2 A to 16 A, V_{IN} = 16 V to 50 V dc	4.90		5.10	V
Line Regulation	+25°C	VI	I_O = 20 A, V_{IN} = 18 V to 40 V dc		1	10	mV
Load Regulation	+25°C	VI	V_{IN} = 28 V dc, I_O = 2 A to 20 A		1	10	mV
Output Ripple/Noise[4]	+25°C	I	I_O = 20 A, 5 kHz – 2 MHz BW		15	50	mV p-p
Output Current (I_O)	Full	VI	V_{IN} = 18 V to 40 V dc	2		20	A
Output Overvoltage Protection	+25°C	V	I_O = 20 A, Open Remote Sense Connection		125		% V_O Nom
Output Current Limit	+25°C	V	V_O = 90% V_{OUT} Nom		130		% I_O max
Output Short Circuit Current	+25°C	I	45 mΩ ≤ R_{SHORT} Circuit ≤ 60 mΩ			30	A
ISOLATION CHARACTERISTICS							
Isolation Resistance	+25°C	I	Input to Output or Any Pin to Case at 500 V dc	100			MΩ
DYNAMIC CHARACTERISTICS[4]							
Maximum Output Voltage Deviation Due to Step Change in Load	+25°C	I	I_O = 10 A to 20 A or 20 A to 10 A di/dt = 0.5 A/µs		445	575	mV
Response Time Due to Step Change in Load	+25°C	I	I_O = 10 A to 20 A or 20 A to 10 A, di/dt = 0.5 A/µs, Time for V_{OUT} to Return within 2% of Final Value		125	170	µs
Soft Start Turn-On Time	+25°C	I	I_O = 20 A, From Inhibit High to Status High		7	20	ms
THERMAL CHARACTERISTICS							
Efficiency	+25°C	I	I_O = 12 A	78	80		%
	Full	VI	I_O = 12 A	76			%
	+25°C	I	I_O = 20 A	78	79		%
	Full	VI	I_O = 20 A	76			%
Hottest Junction Temperature[5]	+90°C	V	I_O = 20 A		110		°C
CONTROL CHARACTERISTICS							
Clock Frequency	Full	VI	I_O = 2 A	0.87		1.03	MHz
ADJUST (Pin 3) V ADJ	+25°C	I		1.97	2.04	2.10	V
STATUS (Pin 4)							
V_{OH}	+25°C	I	I_{OH} = 400 µA	2.4	4.0		V
V_{OL}	+25°C	I	I_{OL} = 1 mA		0.15	0.7	V
V_{AUX} (Pin 5)							
V_O (nom)	+25°C	I	I_{AUX} = 5 mA, Load Current = 20 A	14.5	14.7	15.0	V
INHIBIT (Pin 6)							
V_{IL}	+25°C	I				0.5	V
I_{IL}	+25°C	I	V_{IL} = 0.5 V			1.2	mA
V_I (Open Circuit)	+25°C	I				15	V
SYNC (Pin 7)[6]							
V_{IH}	+25°C	I		4.0			V
I_{IH}	+25°C	I	V_{IH} = 7.0 V			150	µA
I_{SHARE} (Pin 8)	+25°C	I	I_O = 20 A	2.78	2.82	2.88	V
TEMP (Pin 9)	+25°C	V			3.90		V

NOTES

[1]50 V dc upper limit rated for transient condition of up to 50 ms. 16 V dc lower limit rated for continuous operation during emergency condition. Steady state and abnormal input voltage range require source impedance sufficient to insure input stability at low line. See sections entitled System Instability Considerations and Input Voltage Range.

[2]Measured at the remote sense points.

[3]Unit regulates output voltage to zero load.

[4]C_{LOAD} = 0.

[5]Refer to section entitled Thermal Characteristics for more information.

[6]Unit has internal pull-down; refer to section entitled Pin 7 (SYNC).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

INHIBIT	50 V dc, –0.5 V dc
SYNC	8.0 V dc, –0.5 V dc
I_{SHARE}	6 V dc, –0.5 V dc
TEMP	12 V dc, –0.3 V dc
Common-Mode Voltage, Input to Output	500 V dc
Lead Soldering Temp (10 sec)	+300°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	+150°C
Maximum Case Operating Temperature	+125°C

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

CMOS Switched-Capacitor Voltage Converters

ADM660/ADM8660

FEATURES
ADM660: Inverts or Doubles Input Supply Voltage
ADM8660: Inverts Input Supply Voltage
100 mA Output Current
Shutdown Function (ADM8660)
2.2 µF or 10 µF Capacitors
0.3 V Drop at 30 mA Load
+1.5 V to +7 V Supply
Low Power CMOS: 600 µA Quiescent Current
Selectable Charge Pump Frequency (25 kHz/120 kHz)
Pin Compatible Upgrade for MAX660, MAX665, ICL7660

APPLICATIONS
Handheld Instruments
Portable Computers
Remote Data Acquisition
Op Amp Power Supplies

GENERAL DESCRIPTION

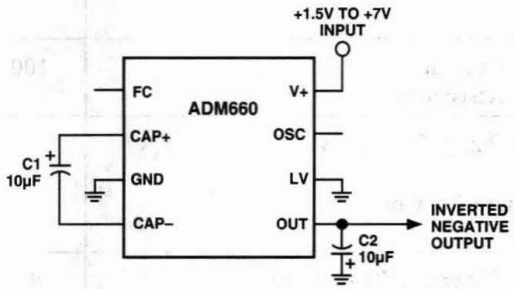
The ADM660/ADM8660 is a charge-pump voltage converter that can be used to either invert the input supply voltage giving $V_{OUT} = -V_{IN}$ or double it (ADM660 only) giving $V_{OUT} = 2 \times V_{IN}$.

Input voltages ranging from +1.5 V to +7 V can be inverted into a negative –1.5 V to –7 V output supply. This inverting scheme is ideal for generating a negative rail in single power-supply systems. Only two small external capacitors are needed for the charge pump. Output currents up to 50 mA with greater than 90% efficiency are achievable, while 100 mA achieves greater than 80% efficiency.

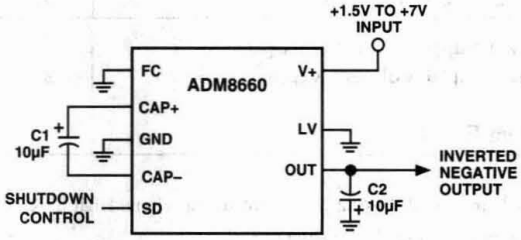
A Frequency Control (FC) input pin is used to select either 25 kHz or 120 kHz charge-pump operation. This is used to optimize capacitor size and quiescent current. With 25 kHz selected, a 10 µF external capacitor is suitable, while with 120 kHz, the capacitor may be reduced to 2.2 µF. The oscillator frequency on the ADM660 can also be controlled with an external capacitor connected to the OSC input or by driving this input with an external clock. In applications where a higher supply voltage is desired it is possible to use the ADM660 to double the input voltage. With input voltages from 2.5 V to 7 V, output voltages from 5 V to 14 V are achievable with up to 100 mA output current.

The ADM8660 features a low power shutdown (SD) pin instead of the external oscillator (OSC) pin. This can be used to disable the device and reduce the quiescent current to 300 nA.

TYPICAL CIRCUIT CONFIGURATIONS



Voltage Inverter Configuration (ADM660)



Voltage Inverter Configuration with Shutdown (ADM8660)

The ADM660 is a pin compatible upgrade for the MAX660, MAX665, ICL7660 and LTC1046.

The ADM660/ADM8660 is available in 8-pin DIP and narrow-body SOIC.

ADM660/ADM8660 Options

Option	ADM660	ADM8660
Inverting Mode	Y	Y
Doubling Mode	Y	N
External Oscillator	Y	N
Shutdown	N	Y
Package Options		
SO-8	Y	Y
N-8	Y	Y

ADM660/ADM8660–SPECIFICATIONS

(V+ = +5 V, C1, C2 = 10 µF,[1] $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V+					R_L = 1 kΩ
	3.5		7.0	V	Inverting Mode, LV = Open
	1.5		7.0	V	Inverting Mode, LV = GND
	2.5		7.0	V	Doubling Mode, LV = OUT
Supply Current					No Load
		0.6	1	mA	FC = Open (ADM660), GND (ADM8660)
		2.5	4.5	mA	FC = V+, LV = Open
Output Current	100			mA	
Output Resistance		9	15	Ω	I_L = 100 mA
Charge-Pump Frequency		25		kHz	FC = Open (ADM660), GND (ADM8660)
		120		kHz	FC = V+
OSC Input Current		±5		µA	FC = Open (ADM660), GND (ADM8660)
		±25		µA	FC = V+
Power Efficiency (FC = Open)	90	94		%	R_L = 1 kΩ Connected from V+ to OUT
	90	93		%	R_L = 500 Ω Connected from OUT to GND
		81.5		%	I_L = 100 mA to GND
Voltage Conversion Efficiency	99	99.96		%	No Load
Shutdown Supply Current, I_{SHDN}		0.3	5	µA	ADM8660, SHDN = V+
Shutdown Input Voltage, V_{SHDN}	2.4			V	SHDN High = Disabled
			0.8	V	SHDN Low = Enabled
Shutdown Exit Time		500		µs	I_L = 100 mA

NOTES

[1]C1 and C2 are low ESR (<0.2 Ω) electrolytic capacitors. High ESR will degrade performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

Input Voltage (V+ to GND, GND to OUT) ..... +7.5 V
LV Input Voltage ..... (OUT – 0.3 V) to (V+, +0.3 V)
FC and OSC Input Voltage
..... (OUT – 0.3 V) or (V+, –6 V) to (V+, +0.3 V)
OUT, V+ Output Current (Continuous) ..... 120 mA
Output Short Circuit Duration to GND ..... 10 secs
Power Dissipation, N-8 ..... 625 mW
(Derate 8.3 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 120°C/W
Power Dissipation R-8 ..... 450 mW
(Derate 6 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 170°C/W
Operating Temperature Range
Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD Rating ..... >2000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADM660AN	–40°C to +85°C	N-8
ADM660AR	–40°C to +85°C	SO-8
ADM8660AN	–40°C to +85°C	N-8
ADM8660AR	–40°C to +85°C	SO-8

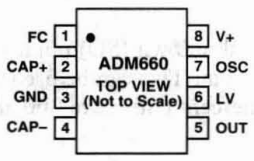
NOTES

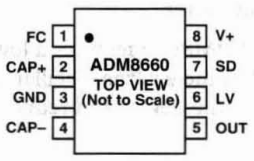
[1]N = Plastic DIP; R = SOIC.

[2]For outline information see Package Information section.

PIN CONNECTIONS

8-Pin





Tri-Mode: +3.3 V, +5 V, Adjustable Micropower Linear Voltage Regulators

ADM663A/ADM666A*

FEATURES

Tri-Mode Operation
3.3 V, 5 V Fixed or +1.3 V to +16 V Adjustable
Low Power CMOS: 9 μA max Quiescent Current
High Current 100 mA Output
Low Dropout Voltage
Upgrade for ADM663/ADM666
"Small" 0.1 μF Output Capacitor (0805 Style)
+2 V to +16.5 V Operating Range
Low Battery Detector ADM666A
No Overshoot on Power-Up
Thermal Shutdown

APPLICATIONS

Handheld Instruments
LCD Display Systems
Pagers
Battery Operated Equipment

GENERAL DESCRIPTION

The ADM663A/ADM666A are precision linear voltage regulators featuring a maximum quiescent current of 9 μA. They can be used to give a fixed +3.3 V or +5 V output with no additional external components or can be adjusted from 1.3 V to 16 V using two external resistors. Fixed or adjustable operation is automatically selected via the V_{SET} input. The low quiescent current makes these devices especially suitable for battery powered systems. The input voltage range is 2 V to 16.5 V, and an output current up to 100 mA is provided. Current limiting may be set using a single external resistor. For additional safety, an internal thermal shutdown circuit monitors the internal die temperature.

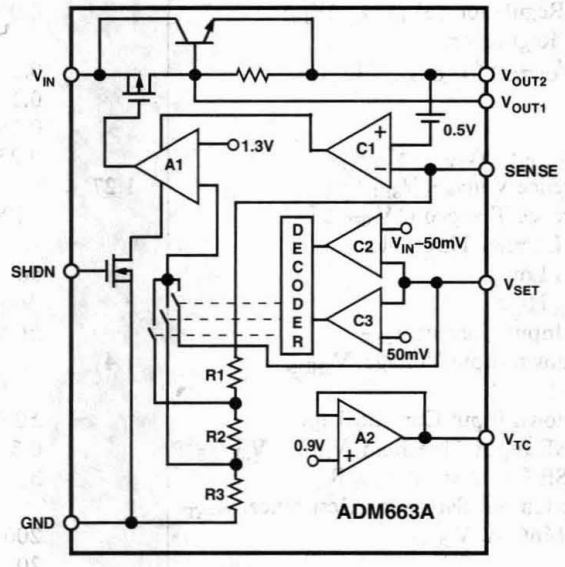
The ADM666A features additional low battery monitoring circuitry to detect for low battery voltages.

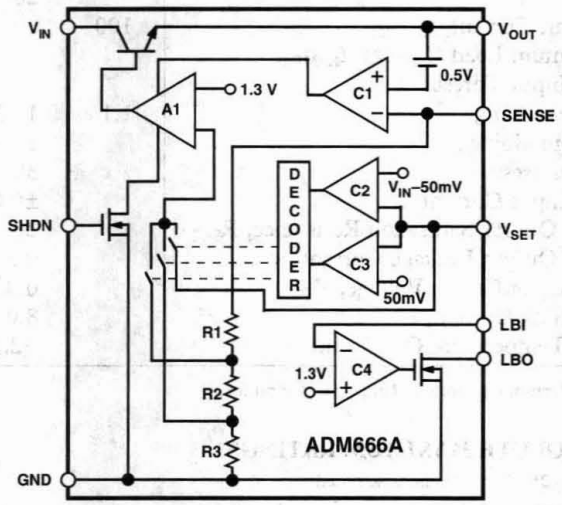
The ADM663A/ADM666A are pin compatible enhancements for the ADM663/ADM666. Improvements include an additional 3.3 V output range, higher output current, and operation with a small output capacitor.

The ADM663A/ADM666A are available in an 8-pin DIP and narrow surface mount (SOIC) packages.

*Patent pending.

FUNCTIONAL BLOCK DIAGRAMS





ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM663AAN	–40°C to +85°C	N-8
ADM663AAR	–40°C to +85°C	R-8
ADM666AAN	–40°C to +85°C	N-8
ADM666AAR	–40°C to +85°C	R-8

*For outline information see Package Information section.

ADM663A/ADM666A–SPECIFICATIONS (V_{IN} = +9 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	2.0		16.5	V	
Quiescent Current, I_Q		6	9	µA	No Load, V_{IN} = +16.5 V
Output Voltage, $V_{OUT(2)}$ (+5 V Mode)	4.75	5.0	5.25	V	V_{SET} = GND
Output Voltage, $V_{OUT(2)}$ (+3.3 V Mode)	3.135	3.3	3.465	V	V_{SET} = V_{IN}
Dropout Voltage, V_{DO}		0.75	0.9	V	I_{OUT} = 40 mA, V_{OUT} = +14.5 V
Dropout Voltage, V_{DO}		1.0	1.2	V	I_{OUT} = 100 mA, V_{OUT} = +14.5 V
Line Regulation ($\Delta V_{OUT(2)}/\Delta V_{IN}$)		0.03	0.35	%/V	+2 V ≤ V_{IN} ≤ +15 V, V_{OUT} = V_{REF}
Load Regulation					V_{IN} = (V_{OUT} +3 V), 1 mA ≤ $I_{OUT(2)}$ ≤ 100 mA
$\Delta V_{OUT(2)}$; ($\Delta V_{OUT(2)}/\Delta I_{OUT(2)}$)		0.3	1.0	Ω	V_{SET} = GND (Fixed +5 V Output)
		0.15	0.35	Ω	V_{SET} = V_{IN} (Fixed +3.3 V Output)
		0.15	0.30	Ω	V_{SET} = Resistive Divider (Adjustable Output)
ΔV_{OUT1}; ($\Delta V_{OUT1}/\Delta I_{OUT1}$)		0.25	1.2	Ω	ADM663A, 50 µA ≤ I_{OUT1} ≤ 10 mA
Reference Voltage, V_{SET}	1.27		1.33	V	T_A = +25°C, V_{OUT} = V_{SET}
Reference Tempco ($\Delta V_{SET}/\Delta T$)		±100		ppm/°C	
V_{SET} Internal Threshold					
$V_{F/A}$ Low		50		mV	V_{SET} < $V_{F/A}$ Low for +5 V Output
$V_{F/A}$ High		V_{IN} – 50		mV	V_{SET} > $V_{F/A}$ High for +3.3 V Output
V_{SET} Input Current, I_{SET}		±0.01	±10	nA	
Shutdown Input Voltage, V_{SHDN}	1.4			V	V_{SHDN} High = Output Off
			0.3	V	V_{SHDN} Low = Output On
Shutdown Input Current, I_{SHDN}		±0.01	±10	nA	
SENSE Input Threshold, V_{OUT} – V_{SENSE}		0.5		V	Current Limit Threshold
SENSE Input Resistance, R_{SENSE}		3		MΩ	
Input-Output Saturation Resistance, R_{SAT}					
ADM663A, V_{OUT1}		200	400	Ω	V_{IN} = +2 V, I_{OUT} = 1 mA
		20	40	Ω	V_{IN} = +9 V, I_{OUT} = 10 mA
		20	30	Ω	V_{IN} = +15 V, I_{OUT} = 10 mA
Output Current, $I_{OUT(2)}$	100			mA	+3 V ≤ V_{IN} ≤ +16.5 V, V_{IN} – V_{OUT} = +1.5 V
Minimum Load Current, $I_{L\ (MIN)}$			1.0	µA	
LBI Input Threshold					
Low Going	1.1	1.26		V	ADM666A
High Going		1.29	1.42	V	ADM666A
Hysteresis		30		mV	ADM666A
LBI Input Current, I_{LBI}		±0.01	±10	nA	ADM666A
LBO Output Saturation Resistance, R_{SAT}		20	30	Ω	ADM666A, I_{SAT} = 2 mA
LBO Output Leakage Current		0.2		nA	ADM666A, LBI = 1.4 V
V_{TC} Open Circuit Voltage, V_{TC}		0.9		V	ADM663A
V_{TC} Sink Current, I_{TC}		8.0	2.0	mA	ADM663A
V_{TC} Temperature Coefficient		+2.5		mV/°C	ADM663A

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

Input Voltage, V_{IN} . . . . . +18 V
Terminal Voltage
(ADM663A) Pins 1, 3, 5, 6, 7
. . . . . (GND – 0.3 V) to (V_{IN} + 0.3 V)
(ADM666A) Pins 1, 2, 3, 5, 6
. . . . . (GND – 0.3 V) to (V_{IN} + 0.3 V)
(ADM663A) Pin 2 . . . . . (GND – 0.3 V) to (V_{OUT1} + 0.3 V)
(ADM666A) Pin 7 . . . . . (GND – 0.3 V) to +16.5 V
Output Source Current
(ADM663A, ADM666A) Pin 2 . . . . . 100 mA
(ADM663A) Pin 3 . . . . . 25 mA
Output Sink Current, Pin 7 . . . . . –20 mA
Power Dissipation, N-8 . . . . . 800 mW
(Derate 8.3 mW/°C above +30°C)
θ_{JA}, Thermal Impedance . . . . . 120°C/W
Power Dissipation, R-8 . . . . . 570 mW
(Derate 6 mW/°C above +30°C)
θ_{JA}, Thermal Impedance . . . . . 170°C/W
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . >5000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

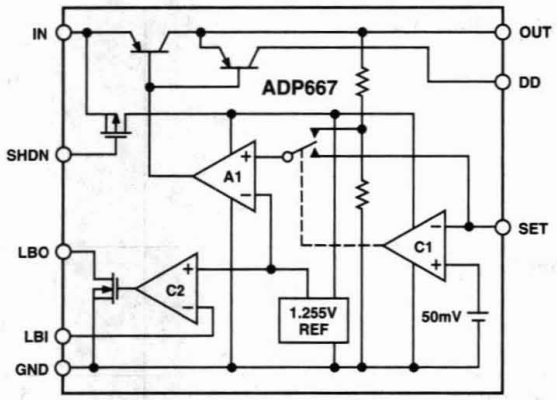
+5 V Fixed, Adjustable Low-Dropout Linear Voltage Regulator

ADP667

FEATURES
Low Dropout: 150 mV @ 200 mA
Low Power CMOS: 20 μA Quiescent Current
Shutdown Mode: 0.2 μA Quiescent Current
250 mA Output Current
Pin Compatible with MAX667
Stable with 10 μF Load Capacitor
Low Battery Detector
Fixed +5 V or Adjustable Output
+3.5 V to +16.5 V Input Range
Dropout Detector Output

APPLICATIONS
Handheld Instruments
Cellular Telephones
Battery Operated Devices
Portable Equipment
Solar Powered Instruments
High Efficiency Linear Power Supplies

FUNCTIONAL BLOCK DIAGRAM



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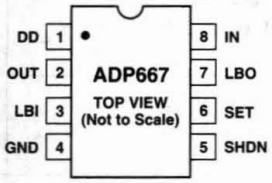
DIP & SOIC PIN CONFIGURATION

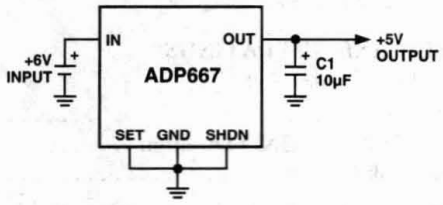


ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADP667AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
ADP667AR	–40°C to +85°C	8-Lead SOIC	SO-8

*For outline information see Package Information section.

TYPICAL OPERATING CIRCUIT



GENERAL DESCRIPTION

The ADP667 is a low-dropout precision voltage regulator that can supply up to 250 mA output current. It can be used to give a fixed +5 V output with no additional external components or can be adjusted from +1.3 V to +16 V using two external resistors. Fixed or adjustable operation is automatically selected via the SET input. The low quiescent current (20 μA) in conjunction with the standby or shutdown mode (0.2 μA) makes this device especially suitable for battery powered systems. The dropout voltage when supplying 100 μA is only 5 mV allowing operation with minimal headroom and prolonging the battery useful life. At higher output current levels the dropout remains low increasing to just 150 mV when supplying 200 mA. A wide input voltage range from 3.5 V to 16.5 V is allowable.

Additional features include a dropout detector and a low supply/battery monitoring comparator. The dropout detector can be used to signal loss of regulation, while the low battery detector can be used to monitor the input supply voltage.

The ADP667 is a pin-compatible replacement for the MAX667. It is specified over the industrial temperature range –40°C to +85°C and is available in an 8-pin DIP and in narrow surface mount (SOIC) packages.

ADP667–SPECIFICATIONS

(V_{IN} = +9 V, GND = 0 V, V_{OUT} = +5 V, C_L = 10 µF, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	3.5		16.5	V	
Output Voltage, V_{OUT}	4.8	5.0	5.2	V	V_{SET} = 0 V, V_{IN} = 6 V, I_{OUT} = 10 mA
Maximum Output Current	250			mA	V_{IN} = +6 V, +4.5 V < V_{OUT} < +5.5 V
Quiescent Current					
I_{GND}: Shutdown Mode		0.2	1	µA	V_{SHDN} = 2 V, T_A = +25°C
			2	µA	T_A = T_{MIN} to T_{MAX}
I_{GND}: Normal Mode					V_{SHDN} = 0 V, V_{SET} = 0 V, T_A = +25°C
		20	25	µA	I_{OUT} = 0 µA
		20	30	µA	I_{OUT} = 100 µA
		5	15	mA	I_{OUT} = 200 mA
					T_A = T_{MIN} to T_{MAX}
			35	µA	I_{OUT} = 0 µA
			50	µA	I_{OUT} = 100 µA
			20	mA	I_{OUT} = 200 mA
Dropout Voltage		5	60	mV	I_{OUT} = 100 µA, T_A = +25°C
			75	mV	T_A = T_{MIN} to T_{MAX}
		150	250	mV	I_{OUT} = 200 mA, T_A = +25°C
			350	mV	T_A = T_{MIN} to T_{MAX}
Load Regulation		50	100	mV	I_{OUT} = 10 mA–200 mA, V_{IN} = 6 V, T_A = +25°C
			250	mV	T_A = T_{MIN} to T_{MAX}
Line Regulation		5	10	mV	V_{IN} = 6 V to 10 V, I_{OUT} = 10 mA, T_A = +25°C
			15	mV	T_A = T_{MIN} to T_{MAX}
SET Reference Voltage, V_{SET}	1.23	1.255	1.28	V	
SET Input Leakage Current, I_{SET}		±0.01	±10	nA	V_{SET} = 1.5 V, T_A = +25°C
			±1000	nA	T_A = T_{MIN} to T_{MAX}
Output Leakage Current, I_{OUT}		0.1	1	µA	V_{SHDN} = 2 V
Short-Circuit Current, I_{OUT}			400	mA	T_A = +25°C
			450	mA	T_A = T_{MIN} to T_{MAX}
Low Battery Detector Input Threshold, V_{LBI}	1.215	1.255	1.295	V	
LBI Input Leakage Current, I_{LBI}		±0.01	±10	nA	V_{LBI} = 1.5 V, T_A = +25°C
			±1000	nA	T_A = T_{MIN} to T_{MAX}
Low Battery Detector Output Voltage, V_{LBO}			0.25	V	V_{LBI} < 1.215 V, I_{LBO} = 10 mA, T_A = +25°C
			0.40	V	T_A = T_{MIN} to T_{MAX}
Shutdown Input Threshold Voltage, V_{SHDN}	1.5			V	
Shutdown Input Leakage Current, I_{SHDN}		±0.01	±10	nA	V_{SHDN} = 0 V to V_{IN}, T_A = +25°C
			±1000	nA	T_A = T_{MIN} to T_{MAX}
Dropout Detector Output Voltage			0.25	V	(V_{SET} = 0 V, V_{SHDN} = 0 V, R_{DD} = 100 kΩ
					V_{IN} = 7 V, I_{OUT} = 10 mA)
	4.0				(V_{SET} = 0 V, V_{SHDN} = 0 V, R_{DD} = 100 kΩ
					V_{IN} = 4.5 V, I_{OUT} = 10 mA)

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

Input Voltage, V_{IN} ..... +18 V
Output Short Circuit to GND Duration ..... 1 sec
LBO Output Sink Current ..... 50 mA
LBO Output Voltage ..... GND to V_{OUT}
SHDN Input Voltage ..... –0.3 V (V_{IN} + 0.3 V)
LBI, SET Input Voltage ..... –0.3 V (V_{IN} + 0.3 V)
Power Dissipation, N-8 ..... 625 mW
(Derate 8.3 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 120°C/W
Power Dissipation, SO-8 ..... 450 mW
(Derate 6 mW/°C above +50°C)
θ_{JA}, Thermal Impedance ..... 170°C/W
Operating Temperature Range
Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C
ESD Rating ..... > 6000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Micropower DC-DC Converter Adjustable and Fixed 5 V, 12 V

ADP1073

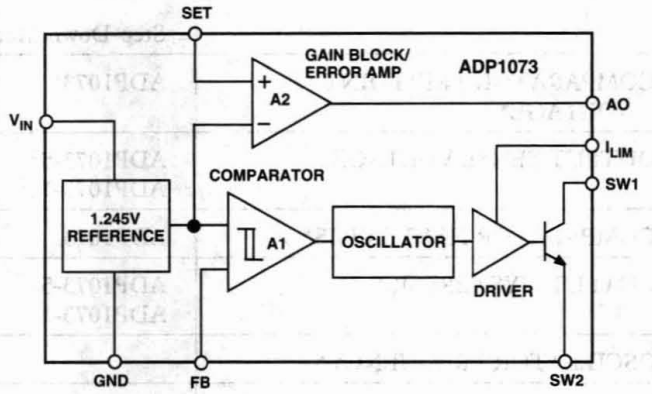
FEATURES

Operates at Supply Voltages from 1.0 V to 30 V
Ground Current: 95 μA
Works in Step-Up or Step-Down Mode
Very Few External Components Required
Low-Battery Detector On Chip
User-Adjustable Current Limit
Internal 1 A Power Switch
Fixed and Adjustable Output Voltage Versions
8-Pin DIP or SO-8 Package

APPLICATIONS

Single-Cell to 5 V Converters
Laptop and Palmtop Computers
Pagers
Cameras
Battery Backup Supplies
Cellular Telephones
Portable Instruments
4 mA–20 mA Loop Powered Instruments
Hand-Held Inventory Computers
Battery-Powered α, β, γ Particle Detectors

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option*
ADP1073AN	ADJ	PDIP	N-8
ADP1073AR	ADJ	SOIC	SO-8
ADP1073AN-5	5 V	PDIP	N-8
ADP1073AR-5	5 V	SOIC	SO-8
ADP1073AN-12	12 V	PDIP	N-8
ADP1073AR-12	12 V	SOIC	SO-8

*For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP1073 is part of a family of step-up/step-down switching regulators which operates from an input supply voltage of as little as 1.0 V. This extremely low input voltage allows the ADP1073 to be used in applications that require using a single cell battery as the primary power source.

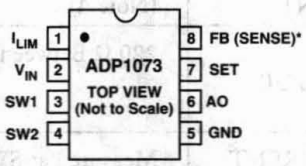
The ADP1073 can be configured to operate in either step-up or step-down mode; but for input voltages greater than 3 V, the ADP1173 is recommended.

An auxiliary gain amplifier can serve as a low-battery detector or linear regulator. Quiescent current on the ADP1073-5 is only 135 μA unloaded, making it ideal for systems where long battery life is required.

The ADP1073 can deliver 40 mA at 5 V from an input voltage range as low as 1.25 V, or 10 mA at 5 V from a 1.0 V input. Current limiting is available by adding an external resistor. Battery protection circuitry keeps reverse currents to safe levels at reverse supply voltages of up to 1.6 V.

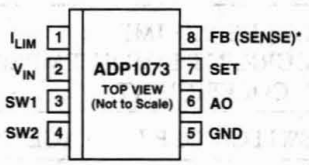
PIN CONFIGURATIONS

Plastic DIP Package (N-8)



*FIXED VERSIONS

Small Outline Package (SO-8)



*FIXED VERSIONS

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ADP1073–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 1.5 V, unless otherwise noted)

Model	Conditions[1]	V_S	ADP1073 Min	ADP1073 Typ	ADP1073 Max	Units
QUIESCENT CURRENT*	Switch Off	I_Q		95	130	µA
QUIESCENT CURRENT, STEP-UP MODE CONFIGURATION	No Load, ADP1073-5 ADP1073-12	I_Q		135 250		µA
INPUT VOLTAGE*	Step-Up Mode Step-Down Mode	V_{IN}	1.15 1.0		12.6 12.6 30	V V V
COMPARATOR TRIP POINT VOLTAGE*	ADP1073[1]		202	212	222	mV
OUTPUT SENSE VOLTAGE*	ADP1073-5[2] ADP1073-12[2]	V_{OUT}	4.75 11.4	5.00 12.00	5.25 12.6	V V
COMPARATOR HYSTERESIS*	ADP1073			5	10	mV
OUTPUT HYSTERESIS*	ADP1073-5 ADP1073-12			125 300	250 600	mV mV
OSCILLATOR FREQUENCY*		f_{OSC}	15	19	23	kHz
DUTY CYCLE*	Full Load ($V_{FB} < V_{REF}$)	DC	65	72	80	%
SWITCH ON TIME*		t_{ON}	30	38	50	µs
FEEDBACK PIN BIAS CURRENT*	ADP1073 V_{FB} = 0 V	I_{FB}		10	50	nA
SET PIN BIAS CURRENT*	$V_{SET} = V_{REF}$	I_{SET}		60	120	nA
AO OUTPUT LOW*	I_{AO} = 100 µA	V_{AO}		0.15	0.4	V
REFERENCE LINE REGULATION*	1.0 V ≤ V_{IN} ≤ 1.5 V 1.5 V ≤ V_{IN} ≤ 12 V			0.35 0.05	1.0 0.1	%/V %/V
SWITCH SATURATION VOLTAGE* STEP-UP MODE	V_{IN} = 1.5 V, I_{SW} = 400 mA V_{IN} = 1.5 V, I_{SW} = 500 mA V_{IN} = 5 V, I_{SW} = 1 A	V_{CESAT}		300 400 700	400 600 550 750 1000 1500	mV mV mV mV mV mV
A2 ERROR AMP GAIN*	R_L = 100 kΩ[3]	A_V	400	1000		V/V
REVERSE BATTERY CURRENT	(Note 4)	I_{REV}		750		mA
CURRENT LIMIT CURRENT LIMIT TEMPERATURE COEFFICIENT	220 Ω Between I_{LIM} and V_{IN}			400 –0.3		mA %/°C
SWITCH OFF LEAKAGE CURRENT	Measured at SW1 Pin	I_{LEAK}		1	10	µA
MAXIMUM EXCURSION BELOW GND	I_{SW1} ≤ 10 µA, Switch Off	V_{SW2}		–400	–350	mV

NOTES

*Denotes the specifications that apply over the full operating temperature range.

[1]This specification guarantees that both the high and low trip point of the comparator fall within the 210 mV to 230 mV range.

[2]This specification guarantees that the output voltage of the fixed versions will always fall within the specified range. The waveform at the sense pin will exhibit a sawtooth shape due to the comparator hysteresis.

[3]100 kΩ resistor connected between a 5 V source and the AO pin.

[4]The ADP1110 is guaranteed to withstand continuous application of +1.6 V applied to the GND and SW2 pins while V_{IN}, I_{LIM}, and SW1 pins are grounded.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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Micropower, DC-DC Converter Adjustable and Fixed 3.3 V, 5 V, 12 V

ADP1108

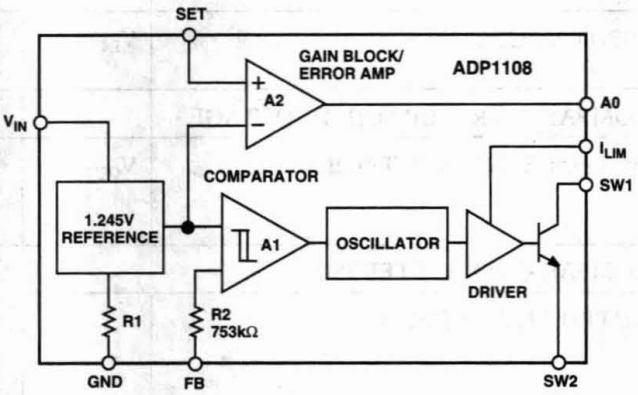
FEATURES

Operates at Supply Voltages From 2.0 V to 30 V
Consumes Only 110 μA Supply Current
Step-Up or Step-Down Mode Operation
Minimum External Components Required
Low Battery Detector Comparator On Chip
User-Adjustable Current Limit
Internal 1A Power Switch
Fixed or Adjustable Output Voltage Versions
8-Pin DIP or SO-8 Package

APPLICATIONS

Notebook/Palmtop Computers
3 V to 5 V, 5 V to 12 V Converters
9 V to 5 V, 12 V to 5 V Converters
LCD Bias Generators
Peripherals and Add-On Cards
Battery Backup Supplies
Cellular Telephones
Portable Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP1108 is a highly versatile micropower switch-mode dc-dc converter that operates from an input voltage supply as low as 2.7 V and typically starts up from 1.8 V.

The ADP1108 can be programmed into a step-up or step-down dc-to-dc converter with only three external components. The fixed outputs are 3.3 V, 5.0 V, and 12 V; an adjustable version is also available. In step-up mode, supply voltage range is 2.0 V to 12 V, and 30 V in step-down mode. The ADP1108 can deliver 150 mA at 5 V from a 2AA cell input and 5 V at 300 mA from a 9 V in step-down mode. Switch current limit can be programmed with a single resistor.

For battery operated and power-conscious applications, the ADP1108 offers a very low power consumption of less than 110 μA.

The auxiliary gain block available in ADP1108 can be used as a low battery detector, linear post regulator, under voltage lockout circuit or error amplifier.

PRELIMINARY TECHNICAL DATA

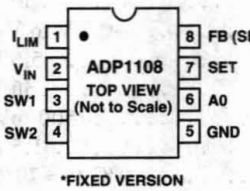
ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option*
ADP1108AN-3.3	3.3 V	PDIP	N-8
ADP1108AR-3.3	3.3 V	SOIC	SO-8
ADP1108AN-5	5 V	PDIP	N-8
ADP1108AR-5	5 V	SOIC	SO-8
ADP1108AN-12	12 V	PDIP	N-8
ADP1108AR-12	12 V	SOIC	SO-8
ADP1108AN	ADJ	PDIP	N-8
ADP1108AR	ADJ	SOIC	SO-8

*For outline information see Package Information section.

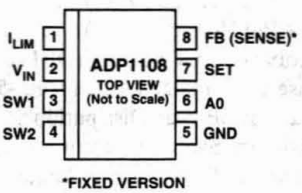
PIN CONFIGURATIONS

8-Lead Plastic DIP (N-8)



*FIXED VERSION

8-Lead SOIC (SO-8)



*FIXED VERSION

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ADP1108–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 3.0 V, unless otherwise noted)

Parameter	Symbol	Conditions[1]	Min	Typ	Max	Units
QUIESCENT CURRENT	I_Q	Switch Off*		110	150	µA
QUIESCENT CURRENT, BOOST MODE CONFIGURATION	I_Q	No Load ADP1108-3 ADP1108-5 ADP1108-12		 100 135 250		
INPUT VOLTAGE	V_{IN}	Step-Up Mode* Step-Down Mode*	2.0		12.6 30	V V
COMPARATOR TRIP POINT VOLTAGE		ADP1108*[1]	1.20	1.245	1.30	V
OUTPUT SENSE VOLTAGE	V_{OUT}	ADP1108-3 ADP1108-5*[2] ADP1108-12*[2]	3.13 4.75 11.4	3.3 5.00 12.0	3.46 5.25 12.6	V V V
COMPARATOR HYSTERESIS		ADP1108*		5	10	mV
OUTPUT HYSTERESIS		ADP1108-3 ADP1108-5* ADP1108-12*		13 20 50	 40 100	mV mV mV
OSCILLATOR FREQUENCY			14	19	25	kHz
DUTY CYCLE		Full Load	63	70	78	%
SWITCH ON TIME	t_{ON}	I_{LIM} Tied to V_{IN}	28	36	48	µs
FEEDBACK PIN BIAS CURRENT		VFB = 0 V*		10	50	nA
SET PIN BIAS CURRENT		$V_{SET} = V_{REF}$*		20	100	nA
GAIN BLOCK OUTPUT LOW	V_{OL}	I_{SINK} = 100 µA, V_{SET} = 1.00 V*		0.15	0.4	V
REFERENCE LINE REGULATION		2.0 V ≤ V_{IN} ≤ 5 V* 5 V ≤ V_{IN} ≤ 30 V*		0.2 0.02	0.4 0.075	%/V %/V

PRELIMINARY TECHNICAL DATA

NOTES
*Denotes the specifications that apply over the full operating temperature range.
[1]This specification guarantees that both the high and low trip points of the comparator fall within the 1.20 V to 1.30 V range.
[2]The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) . . . . . 36 V
SW1 Pin Voltage (V_{SW1}) . . . . . 50 V
SW2 Pin Voltage (V_{SW2}) . . . . . –0.5 V to V_{IN}
Feedback Pin Voltage (ADP1108) . . . . . 5.5 V
Sense Pin Voltage (ADP1108, -5, -12) . . . . . 36 V
Maximum Power Dissipation . . . . . 500 mW
Maximum Switch Current . . . . . 1.5 A
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

This information applies to a product under development. Its characteristics and specifications are subject to change without notice Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Micropower; Low Cost; Fixed 5 V, 12 V and Adjustable DC-to-DC Converter

ADP1109

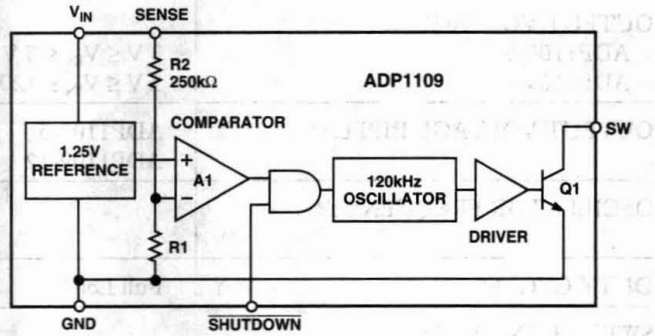
FEATURES

Operates at Supply Voltages 2 V to 12 V
Fixed 5 V, 12 V and Adjustable Output
Minimum External Components Required
Ground Current 320 μA
120 kHz Oscillator Frequency
Logic Shutdown
8-Pin DIP and SO Package

APPLICATIONS

Cellular Telephones
Single-Cell to 5 V Converters
Laptop and Palmtop Computers
Pagers
Cameras
Battery Backup Supplies
Portable Instruments
Laser Diode Drivers
Hand-Held Inventory Computers

FUNCTIONAL BLOCK DIAGRAM



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PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP1109 is a versatile step-up switching regulator. The device requires only minimal external components to operate as a complete switching regulator.

The ADP1109-5 can deliver 100 mA at 5 V from a 3 V input, and ADP1109-12 can deliver 60 mA at 12 V from a 5 V input. The device also features a logic controlled shutdown capability that when a logic low is applied it will shut the oscillator down. The 120 kHz operating frequency allows for the use of small surface mount components.

The gated oscillator capability eliminates the need for frequency compensation.

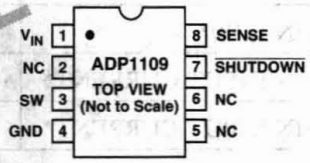
ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option*
ADP1109AN	ADJ	PDIP	N-8
ADP1109AR	ADJ	SOIC	SO-8
ADP1109AN-5	5 V	PDIP	N-8
ADP1109AR-5	5 V	SOIC	SO-8
ADP1109AN-12	12 V	PDIP	N-8
ADP1109AR-12	12 V	SOIC	SO-8

For outline information see Package Information section.

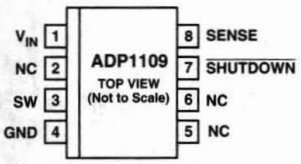
PIN CONFIGURATIONS

8-Lead Plastic DIP
(N-8 Package)



NC = NO CONNECT

8-Lead SOIC
(SO-8 Package)



NC = NO CONNECT

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ADP1109–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 3 V, unless otherwise noted)

Parameter	Conditions[1]	V_S	ADP1109 Min	ADP1109 Typ	ADP1109 Max	Units
QUIESCENT CURRENT*	Switch Off	I_Q		320	550	µA
INPUT VOLTAGE*		V_{IN}	3			V
COMPARATOR TRIP POINT VOLTAGE*	ADP1109		1.20	1.25	1.30	V
OUTPUT VOLTAGE*						
ADP1109-5	3 V ≤ V_{IN} ≤ 5 V	V_{OUT}	4.75	5.00	5.25	V
ADP1109-12	3 V ≤ V_{IN} ≤ 12 V		11.45	12.00	12.55	V
OUTPUT VOLTAGE RIPPLE*	ADP1109-5			25	50	mV
	ADP1109-12			60	120	mV
OSCILLATOR FREQUENCY*		f_{OSC}	100	120	140	kHz
			90		150	kHz
DUTY CYCLE*	Full Load	DC	45	50	60	%
SWITCH ON TIME*		t_{ON}	3.3	4.2	5.3	µs
			3.0		5.5	µs
SWITCH SATURATION VOLTAGE*	I_{SW} = 500 mA	V_{CESAT}		0.4	0.7	
ADP1109-5	V_{IN} = 3 V			0.5	0.8	V
ADP1109-12	V_{IN} = 5 V			0.5	0.8	V
SWITCH LEAKAGE CURRENT	V_{SW} = 12 V			1	10	µA
SHUTDOWN PIN HIGH*		V_{IH}	2.0			V
SHUTDOWN PIN LOW*		V_{IL}			0.8	V
SHUTDOWN PIN INPUT CURRENT*	$V_{SHUTDOWN}$ = 4 V	I_{IH}			10	µA
SHUTDOWN PIN INPUT CURRENT*	$V_{SHUTDOWN}$ = 0 V	I_{IL}			20	µA

NOTES
*Denotes the specifications that apply over the full operating temperature range.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

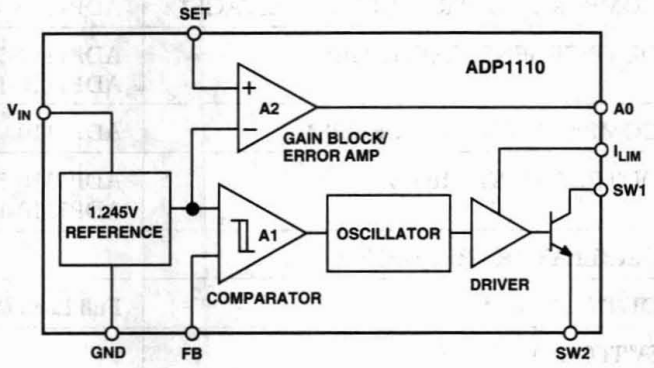
Micropower, Step-Up/Step-Down Switching Regulator Adjustable and Fixed 5 V, 12 V

ADP1110

FEATURES
- Operates at Supply Voltages from 1.0 V to 30 V
- Step-Up or Step-Down Mode
- Minimal External Components Required
- Low Battery Detector
- User-Adjustable Current Limiting
- Fixed or Adjustable Output Voltage Versions
- 8-Pin Plastic DIP or SO-8 Package

APPLICATIONS
- Cellular Telephones
- Single-Cell to 5 V Converters
- Laptop and Palmtop Computers
- Pagers
- Cameras
- Battery Backup Supplies
- Portable Instruments
- Laser Diode Drivers
- Hand-Held Inventory Computers

FUNCTIONAL BLOCK DIAGRAM



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PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option*
ADP1110AN	ADJ	PDIP	N-8
ADP1110AR	ADJ	SOIC	SO-8
ADP1110AN-5	5 V	PDIP	N-8
ADP1110AR-5	5 V	SOIC	SO-8
ADP1110AN-12	12 V	PDIP	N-8
ADP1110AR-12	12 V	SOIC	SO-8

*For outline information see Package Information section.

GENERAL DESCRIPTION

The ADP1110 is part of a family of step-up/step-down switching regulators that operate from an input voltage supply of as little as 1.0 V. This very low input voltage allows the ADP1110 to be used in applications that use a single cell as the primary power source.

The ADP1110 can be configured to operate in either step-up or step-down mode, but for input voltages greater than 3 V, the ADP1111 would be a more effective solution.

An auxiliary gain amplifier can serve as a low battery detector as well as a linear regulator.

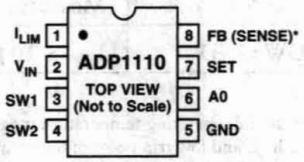
The quiescent current of 300 µA makes the ADP1110 useful in remote or battery powered applications.

The 70 kHz frequency operation also allows for the use of surface mount external capacitors and inductors.

Battery protection circuitry limits the effect of reverse current to safe levels at reverse voltages up to 1.6 V.

PIN CONFIGURATIONS

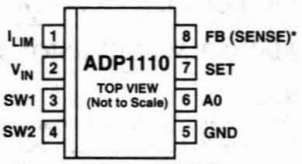
8-Lead Plastic DIP (N-8)



T_{JMAX} = 90°, θ_{JA} = 130°C/W

*FIXED VERSIONS

8-Lead SOIC (SO-8)



T_{JMAX} = 90°, θ_{JA} = 150°C/W

*FIXED VERSIONS

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ADP1110–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 1.5 V, unless otherwise noted)

Parameter	Conditions[1]	V_S	ADP1110 Min	Typ	Max	Units
QUIESCENT CURRENT*	Switch Off	I_Q		300		µA
INPUT VOLTAGE*	Step-Up Mode	V_{IN}	1.15		12.6	V
			1.0		12.6	V
	Step-Down Mode				30	V
COMPARATOR TRIP POINT VOLTAGE*	ADP1110[1]		210	220	230	mV
OUTPUT SENSE VOLTAGE*	ADP1110-5[2]	V_{OUT}	4.75	5.00	5.25	V
	ADP1110-12[2]		11.4	12.00	12.6	V
COMPARATOR HYSTERESIS*	ADP1110			4	8	mV
OUTPUT HYSTERESIS*	ADP1110-5			90	180	mV
	ADP1110-12			200	400	mV
OSCILLATOR FREQUENCY*		f_{OSC}	52	70	90	kHz
DUTY CYCLE*	Full Load ($V_{FB} < V_{REF}$)	DC	62	69	78	%
SWITCH ON TIME*		t_{ON}	7.5	10	12.5	µs
FEEDBACK PIN BIAS CURRENT*	ADP1110 V_{FB} = 0 V	I_{FB}		70	150	nA
SET PIN BIAS CURRENT*	$V_{SET} = V_{REF}$	I_{SET}		100	300	nA
A0 OUTPUT LOW*	I_{AO} = 300 µA V_{SET} = 150 mV	V_{AO}		0.15	0.4	V
REFERENCE LINE REGULATION*	1.0 V ≤ V_{IN} ≤ 1.5 V			0.35	1.0	%/V
	1.5 V ≤ V_{IN} ≤ 12 V			0.05	0.1	%/V
SWITCH SATURATION VOLTAGE* STEP-UP MODE	V_{IN} = 1.5 V, I_{SW} = 400 mA	V_{CESAT}		300	400	mV
					600	mV
	V_{IN} = 1.5 V, I_{SW} = 500 mA			400	550	mV
					750	mV
	V_{IN} = 5 V, I_{SW} = 1 A			700	1000	mV
A2 ERROR AMP GAIN*	R_L = 100 kΩ[3]	A_V	1000	5000		V/V
REVERSE BATTERY CURRENT	(Note 4)	I_{REV}		750		mA
CURRENT LIMIT	220 Ω Between I_{LIM} and V_{IN}			400		mA
CURRENT LIMIT TEMPERATURE COEFFICIENT				–0.3		%/°C
SWITCH-OFF LEAKAGE CURRENT	Measured at SW1 Pin	I_{LEAK}		1	10	µA
MAXIMUM EXCURSION BELOW GND	I_{SW1} ≤ 10 µA, Switch Off	V_{SW2}		–400	–350	mV

NOTES

*Denotes the specifications that apply over the full operating temperature range.

[1]This specification guarantees that both the high and low trip point of the comparator fall within the 210 mV to 230 mV range.

[2]This specification guarantees that the output voltage of the fixed versions will always fall within the specified range. The waveform at the sense pin will exhibit a saw-tooth shape due to the comparator hysteresis.

[3]100 kΩ resistor connected between a 5 V source and the A0 pin.

[4]The ADP1110 is guaranteed to withstand continuous application of +1.6 V applied to the GND and SW2 pins while V_{IN}, I_{LIM}, and SW1 pins are grounded.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

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ANALOG DEVICES

Micropower, Step-Up/Step-Down SW Regulator Adjustable and Fixed 5 V, 12 V

ADP1111

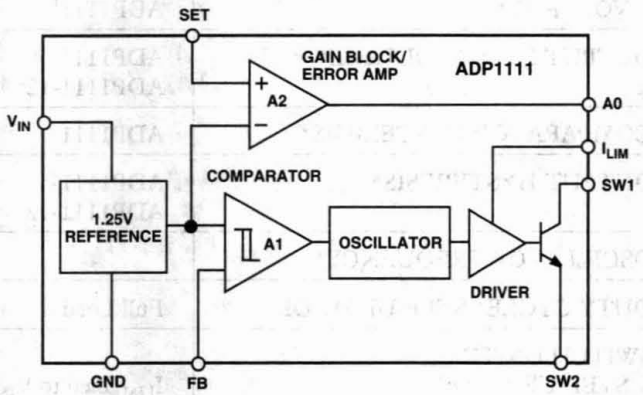
FEATURES

- Operates from 2 V to 30 V Input Voltage Range
- 72 kHz Frequency Operation
- Utilizes Surface Mount Inductors
- Very Few External Components Required
- Operates in Step-Up/Step-Down or Inverting Mode
- Low Battery Detector
- User Adjustable Current Limit
- Internal 1 A Power Switch
- Fixed or Adjustable Output Voltage
- 8-Pin DIP or SO-8 Package

APPLICATIONS

- 3 V to 5 V, 5 V to 12 V Step-Up Converters
- 9 V to 5 V, 12 V to 5 V Step-Down Converters
- Laptop and Palmtop Computers
- Cellular Telephones
- Flash Memory VPP Generators
- Remote Controls
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Uninterruptible Supplies
- Portable Instruments

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Model	Output Voltage	Package Description	Package Options*
ADP1111AN	ADJ	PDIP	N-8
ADP1111AR	ADJ	SOIC	SO-8
ADP1111AN-5	5 V	PDIP	N-8
ADP1111AR-5	5 V	SOIC	SO-8
ADP1111AN-12	12 V	PDIP	N-8
ADP1111AR-12	12 V	SOIC	SO-8

*For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP1111 is part of a family of step-up/step-down switching regulators that operates from an input voltage supply of 2 V to 12 V in step-up mode and up to 30 V in step-down mode. The ADP1111 can be programmed to operate in step-up/step-down or inverting applications with only three external components.

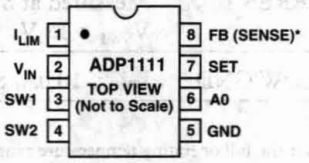
The fixed outputs are 3.3 V, 5 V and 12 V; an adjustable version is also available. The ADP1111 can deliver 100 mA at 5 V from a 3 V input in step-up mode, or it can deliver 200 mA at 5 V from a 12 V input in step-down mode.

Maximum switch current can be programmed with a single resistor. An open collector gain block can be arranged in multiple configuration for low battery detection as a post linear regulator, under voltage lockout, or as an error amplifier.

If input voltages are lower than 2 V, see the ADP1110.

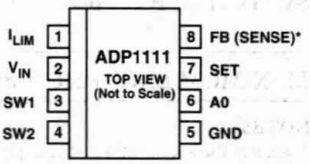
PIN CONFIGURATIONS

8-Lead Plastic DIP (N-8)



*FIXED VERSIONS

8-Lead SOIC (SO-8)



*FIXED VERSIONS

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ADP1111–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 3 V, unless otherwise noted)

Parameter	Conditions[1]	V_S	ADP1111 Min	ADP1111 Typ	ADP1111 Max	Units
QUIESCENT CURRENT*	Switch Off	I_Q		300	400	µA
INPUT VOLTAGE*	Step-Up Mode Step-Down Mode	V_{IN}	2.0		12.6 30.0	V V
COMPARATOR TRIP POINT VOLTAGE*	ADP1111[1]		1.20	1.25	1.30	V
OUTPUT SENSE VOLTAGE*	ADP1111-5[2] ADP1111-12[2]	V_{OUT}	4.75 11.40	5.00 12.00	5.25 12.60	V V
COMPARATOR HYSTERESIS*	ADP1111			8	12.5	mV
OUTPUT HYSTERESIS*	ADP1111-5 ADP1111-12			32 75	50 120	mV mV
OSCILLATOR FREQUENCY*		f_{OSC}	54	72	88	kHz
DUTY CYCLE* STEP-UP MODE	Full Load	DC	43	50	59	%
SWITCH ON TIME* STEP-UP MODE	I_{LIM} Tied to V_{IN}	t_{ON}	5	7	9	µs
SW SATURATION VOLTAGE STEP-UP MODE STEP-DOWN MODE	V_{IN} = 3.0 V, I_{SW} = 650 mA V_{IN} = 5.0 V, I_{SW} = 1 A V_{IN} = 12 V, I_{SW} = 650 mA	V_{SAAT}		0.5 0.8 1.1	0.65 1.0 1.5	V V V
FEEDBACK PIN BIAS CURRENT*	ADP1111 V_{FB} = 0 V	I_{FB}		70	120	nA
SET PIN BIAS CURRENT*	V_{SET} = V_{REF}	I_{SET}		70	300	nA
GAIN BLOCK OUTPUT LOW*	I_{SINK} = 300 µA V_{SET} = 1.00 mV	V_{OL}		0.15	0.4	V
REFERENCE LINE REGULATION*	5 V ≤ V_{IN} ≤ 30 V			0.02	0.075	%/V
GAIN BLOCK GAIN*	R_L = 100 kΩ[3]	A_V	1000	6000		V/V
CURRENT LIMIT	220 Ω from I_{LIM} to V_{IN}	I_{LIM}		400		mA
CURRENT LIMIT TEMPERATURE COEFFICIENT*				–0.3		%/°C
SWITCH OFF LEAKAGE CURRENT	Measured at SW1 Pin V_{SW1} = 12 V			1	10	µA
MAXIMUM EXCURSION BELOW GND	I_{SW1} ≤ 10 µA, Switch Off			–400	–350	mV

NOTES
*Denotes the specifications that apply over the full operating temperature range.
[1]This specification guarantees that both the high and low trip point of the comparator fall within the 1.20 V to 1.30 V range.
[2]The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.
[3]100 kΩ resistor connected between a 5 V source and the AO pin.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

High Efficiency, Step-Down Switching Regulator Controller

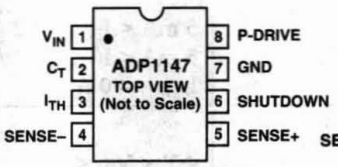
ADP1147

FEATURES
- Over 95% Efficiency
- Current Mode Operation Resulting in Good Line and Load Transient Response
- Low Shutdown Current: 22 μA max
- Input Voltage Range: 3.5 V to 20 V
- Standby Current: 160 μA typ
- Short Circuit Protection
- 8-Pin Plastic DIP and SOIC Package

APPLICATIONS
- Notebook and Palmtop Computers
- Cellular Telephones
- Modems
- Portable Instruments
- GPS Systems

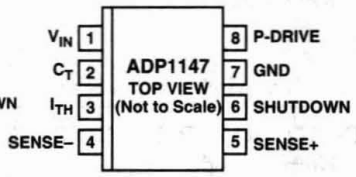
PIN CONFIGURATIONS

8-Lead Plastic DIP (N-8)



T_{JMAX} = 125°C, θ_{JA} = 110°C/W

8-Lead SOIC (SO-8)



T_{JMAX} = 125°C, θ_{JA} = 150°C/W

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PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP1147 is a family of step-down switching regulators featuring automatic sleep mode to maintain high efficiency at low output currents. These regulators drive an external P-channel MOSFET at frequencies up to 250 kHz using constant off-time current mode architecture.

Input supply voltages vary from 3.5 V to 20 V maximum. The constant off-time architecture maintains constant ripple current in the inductor easing the design of wide input range regulators.

Low dropout regulation is limited only by the combination of the R_{DS} (on) of the external MOSFET and resistance of the inductor and current sense resistor.

The ADP1147 family incorporates automatic sleep mode operation to help reduce losses due to switching when load currents drop below the required continuous operation level. In sleep mode standby power is reduced to only 2 mW at V_{IN} = 10 V For even greater efficiencies refer to the ADP1148.

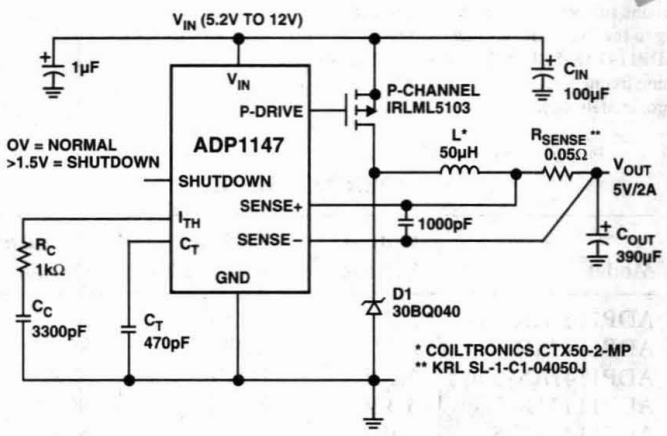

Figure 1. High Efficiency Step-Down Converter

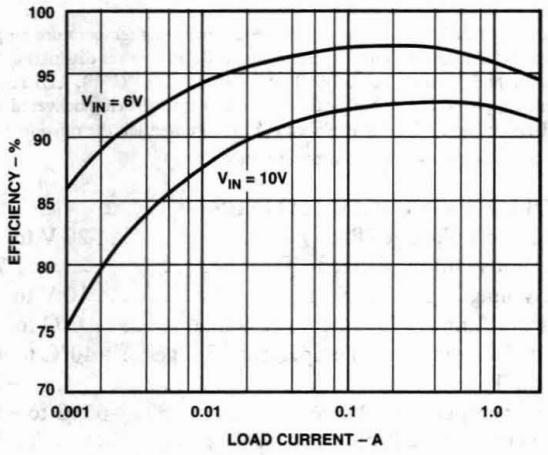

Figure 2. ADP1147-5 Typical Efficiency

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ADP1147–SPECIFICATIONS ($@ T_A = +25°C, V_{IN} = 10 V, V_{SHUTDOWN} = 0 V$, unless otherwise noted)

Parameter	Conditions	V_S	ADP1147 Min	Typ	Max	Units
REGULATED OUTPUT VOLTAGE	V_{IN} = 9 V	V_{OUT}				
ADP1147-3.3*	I_{LOAD} = 700 mA		3.23	3.33	3.43	V
ADP1147-5*	I_{LOAD} = 700 mA		4.90	5.05	5.20	V
OUTPUT VOLTAGE LINE REGULATION	V_{IN} = 7 V to 12 V, I_{LOAD} = 50 mA	ΔV_{OUT}	–40	0	40	mV
OUTPUT VOLTAGE LOAD REGULATION						
ADP1147-3.3*	5 mA < I_{LOAD} < 2 A	ΔV_{OUT}		40	65	mV
ADP1147-5*	5 mA < I_{LOAD} < 2 A			60	100	mV
Sleep Mode Output Ripple	I_{LOAD} = 0 A			50		mV p-p
INPUT DC SUPPLY CURRENT[2]						
Normal Mode	4 V < V_{IN} < 18 V	I_Q		1.6	2.3	mA
Sleep Mode (ADP1147-3.3)	4 V < V_{IN} < 18 V			160	250	µA
Sleep Mode (ADP1147-5)	5 V < V_{IN} < 18 V			160	250	µA
Shutdown	$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 18 V			10	22	µA
CURRENT SENSE THRESHOLD VOLTAGE						
ADP1147-3.3	$V_{SENSE-} = V_{OUT}^+$ 100 mV (Forced)	$V_5–V_4$		25		mV
*	$V_{SENSE-} = V_{OUT}^-$ 100 mV (Forced)		130	150	170	mV
ADP1147-5	$V_{SENSE-} = V_{OUT}^+$ 100 mV (Forced)			25		mV
*	$V_{SENSE-} = V_{OUT}^-$ 100 mV (Forced)		130	150	170	mV
SHUTDOWN PIN THRESHOLD		V_6	0.6	0.8	2	V
SHUTDOWN PIN INPUT CURRENT	0 V < $V_{SHUTDOWN}$ < 8 V, V_{IN} = 16 V	I_6		1.2	5	µA
C_T PIN DISCHARGE CURRENT	V_{OUT} in Regulation,		50	70	90	µA
	$V_{SENSE-} = V_{OUT}$, V_{OUT} = 0 V	I_2		2	10	µA
OFF-TIME*[3]	C_T = 390 pF, I_{LOAD} = 700 mA	t_{OFF}	4	5	6	µs
DRIVER OUTPUT TRANSITION TIMES	C_L = 3000 pF (Pin 8) V_{IN} = 6 V	t_r, t_f		100	200	ns

NOTES

*Denotes specifications that apply over the full operating temperature range. Specifications subject to change without notice.

[1]T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
ADP1147AN-3.3, ADP1147AN-5: $T_J = T_A + (P_D \times 110°C/W)$. ADP1147AR-3.3, ADP1147AR-5: $T_J = T_A + (P_D \times 150°C/W)$.

[2]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

[3]In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 1) . . . . . 20 V to –0.3 V
Continuous Output Current (Pin 8) . . . . . 50 mA
Sense Voltages (Pins 4, 5) . . . . . 10 V to –0.3 V
Operating Ambient Temperature Range . . . . . 0°C to +70°C
Extended Commercial Temperature Range . . –40°C to +85°C
Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C

ORDERING GUIDE

Model	Output Voltage	Package Description	Package Option*
ADP1147AN	ADJ	P-DIP	N-8
ADP1147AR	ADJ	SOIC	SO-8
ADP1147AN-3.3	3.3 V	P-DIP	N-8
ADP1147AR-3.3	3.3 V	SOIC	SO-8
ADP1147AN-5	5 V	P-DIP	N-8
ADP1147AR-5	5 V	SOIC	SO-8

*For outline information see Package Information section.

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High Efficiency, Synchronous Step-Down Switching Regulators

ADP1148/1148-3.3/1148-5

FEATURES

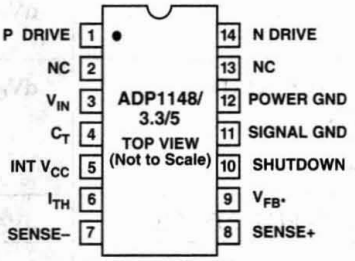
- Operation From 3.5 V to 20 V Input Voltage
- Ultrahigh Efficiency > 95%
- Shutdown Current I_Q = 20 μA
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Wide Current Range
- Logic Controlled Micropower Shutdown
- Short Circuit Protection
- Very Low Dropout Operation
- Synchronous FET Switching for High Efficiency
- Adaptive Nonoverlap Gate Drives

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies
- GPS Systems
- Cellular Telephones

PIN CONFIGURATIONS

14-Lead Plastic DIP
14-Lead Plastic SO



NC = NO CONNECT

*FIXED OUTPUT VERSIONS = SD1

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GENERAL DESCRIPTION

The ADP1148 is a family of synchronous step-down switching regulator controllers featuring automatic-sleep mode to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250 kHz using a constant off-time current-mode architecture.

The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The ADP1148 incorporates automatic power saving sleep mode operation when load currents drop below the level required for continuous operation. In sleep mode, standby power is reduced to only about 2 mV at V_{IN} = 10 V. In shutdown, both MOSFETs are turned off.

PRELIMINARY TECHNICAL DATA

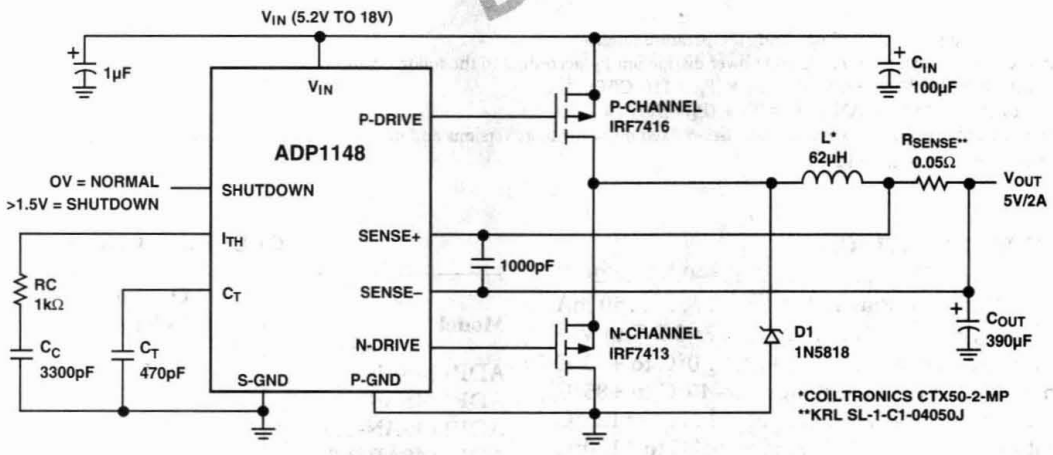

Figure 1. Typical Application

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ADP1148/1148-3.3/1148-5–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 12 V, $V_{SHUTDOWN}$ = 0 V, unless otherwise noted)

Parameter	Symbol	Conditions[1]	Min	Typ	Max	Units
FEEDBACK VOLTAGE						
ADP1148 Only*	V_{10}	V_{IN} = 9 V	1.21	1.25	1.29	V
FEEDBACK CURRENT						
ADP1148 Only*	I_{10}			0.2	1.0	µA
REGULATED OUTPUT VOLTAGE	V_{OUT}	V_{IN} = 9 V				
ADP1148-3.3*		I_{LOAD} = 700 mA	3.23	3.33	3.43	V
ADP1148-5*		I_{LOAD} = 700 mA	4.9	5.05	5.2	V
OUTPUT VOLTAGE LINE REGULATION	dV_{OUT}	V_{IN} = 7 V to 12 V, I_{LOAD} = 50 mA	–40		+40	mV
OUTPUT VOLTAGE LOAD REGULATION	dV_{OUT}					
ADP1148-3.3*		5 mA < I_{LOAD} < 2 A		40	65	mV
ADP1148-5.0*		5 mA < I_{LOAD} < 2 A		60	100	mV
SLEEP MODE OUTPUT RIPPLE*	dV_{OUT}	I_{LOAD} = 0 A		50		mV p-p
INPUT DC SUPPLY CURRENT*[2]	I_Q					
Normal Mode		V_{IN} = 4 V < V_{IN} < 18 V		1.6	2.3	mA
Sleep Mode (ADP1148-3)		V_{IN} = 4 V < V_{IN} < 18 V		160	250	µA
Sleep Mode (ADP1148-5)		V_{IN} = 4 V < V_{IN} < 18 V		160	250	µA
Shutdown		$V_{SHUTDOWN}$ = 2.1 V, 4 V < V_{IN} < 20 V		10	22	µA
CURRENT SENSE THRESHOLD VOLTAGE	V_8–V_7					
ADP1148 Only		V_9 = V_{OUT}/4 + 25 mV (Forced), V_8 = 5 V		25		mV
		V_9 = V_{OUT}/4 – 25 mV (Forced), V_8 = 5 V	130	150	170	mV
ADP1148-3.3		V_{SENSE} = V_{OUT} + 100 mV (Forced)		25		mV
		V_{SENSE} = V_{OUT} – 100 mV (Forced)	130	150	170	mV
ADP1148-5.0		V_{SENSE} = V_{OUT} + 100 mV (Forced)		25		mV
		V_{SENSE} = V_{OUT} – 100 mV (Forced)	130	150	170	mV

PRELIMINARY TECHNICAL DATA

NOTES

*Denotes specifications that apply over the full operating temperature range.

[1]T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
ADP1148AR, ADP1148AR-3, ADP1148AR-5: $T_J = T_A + (P_D \times 110°C/W)$
ADP1148AN, ADP1148AN-3, ADP1148AN-5: $T_J = T_A + (P_D \times 70°C/W)$

[2]Pin 10 is a shutdown pin on the ADP1148-3.3 and ADP1148-5 fixed output voltage versions and must be at ground potential for testing.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 3) . . . . . –0.3 V to 20 V
Continuous Output Currents (Pins 1, 14) . . . . . 50 mA
Sense Voltages (Pins 7, 8) . . . . . –0.3 V to V_{CC}
Operating Temperature Range . . . . . 0°C to +70°C
Extended Commercial Temperature Range . . –40°C to +85°C
Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

ORDERING GUIDE

Model	Output Voltage	Package Option*
ADP1148AN	ADJ	PDIP
ADP1148AR	ADJ	SOIC
ADP1148AN-3.3	3.3 V	PDIP
ADP1148AR-3.3	3.3 V	SOIC
ADP1148AN-5	5 V	PDIP
ADP1148AR-5	5 V	SOIC

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

High Efficiency, Synchronous Step-Down Switching Regulators

ADP1149/1149-3.3/1149-5

FEATURES

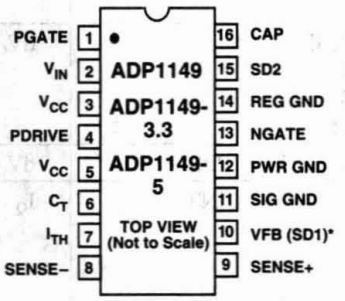
- Operation to 48 V Input Voltage
- Ultrahigh Efficiency (Up to 95%)
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Wide Current Range
- Logic Controlled Micropower Shutdown
- Short Circuit Protection
- Very Low Dropout Operation
- Synchronous FET Switching for High Efficiency
- Adaptive Nonoverlap Gate Drives

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

PIN CONFIGURATIONS

16-Lead Plastic DIP
16-Lead Plastic SO



*FIXED OUTPUT VERSIONS = SD1

20

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP1149 is a family of synchronous step-down switching regulator controllers featuring automatic-sleep mode to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250 kHz using a constant off-time current-mode architecture.

Special onboard regulation and level-shift circuitry allow operation at input voltages from dropout to 48 V (60 V absolute maximum). The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The ADP1149 incorporates automatic power saving sleep mode operation when load currents drop below the level required for continuous operation. In sleep mode, standby power is reduced to only about 8 mW at V_{IN} = 12 V. In shutdown, both MOSFETs are turned off.

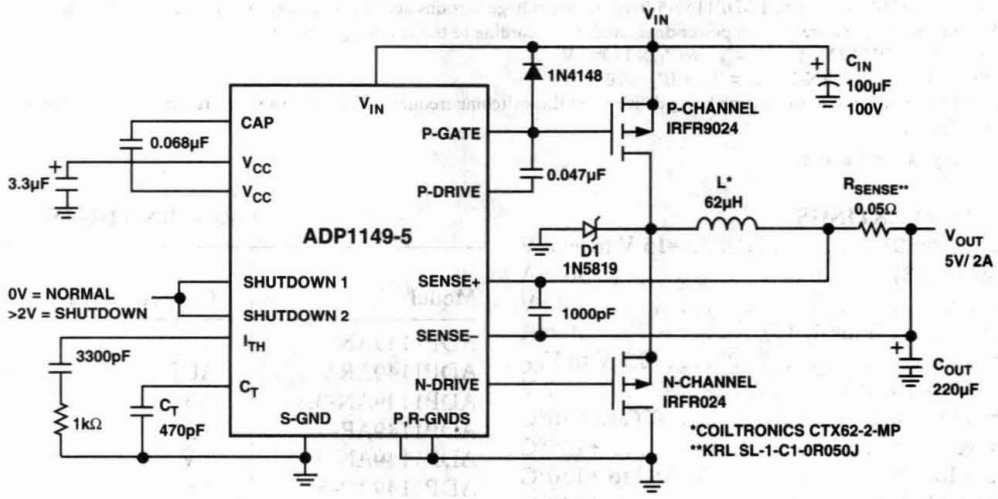


Figure 1. Typical Application

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ADP1149/1149-3.3/1149-5–SPECIFICATIONS

(@ T_A = +25°C, V_{IN} = 12 V, V_{10} = 0 V,[1] unless otherwise noted)

Parameter	Symbol	Conditions[2]	Min	Typ	Max	Units
FEEDBACK VOLTAGE						
ADP1149 Only*	V_{10}	V_{IN} = 9 V	1.21	1.25	1.29	V
FEEDBACK CURRENT						
ADP1149 Only*	I_{10}			0.2	1.0	µA
REGULATED OUTPUT VOLTAGE	V_{OUT}	V_{IN} = 9 V				
ADP1149-3.3*		I_{LOAD} = 700 mA	3.23	3.33	3.43	V
ADP1149-5*		I_{LOAD} = 700 mA	4.9	5.05	5.2	V
OUTPUT VOLTAGE LINE REGULATION	dV_{OUT}	V_{IN} = 9 V to 48 V, I_{LOAD} = 700 mA	–40		+40	mV
OUTPUT VOLTAGE LOAD REGULATION	dV_{OUT}					
ADP1149-3.3*		5 mA < I_{LOAD} < 2 A		40	65	mV
ADP1149-5.0*		5 mA < I_{LOAD} < 2 A		60	100	mV
SLEEP MODE OUTPUT RIPPLE*	dV_{OUT}	I_{LOAD} = 0 A		50		mV p-p
INPUT DC SUPPLY CURRENT*[3]	I_Q					
Normal Mode		V_{IN} = 12 V		2	2.8	mA
		V_{IN} = 48 V		2.2	3.0	mA
Sleep Mode		V_{IN} = 12 V		0.6	0.9	mA
		V_{IN} = 48 V		0.8	1.1	mA
Shutdown		V_{IN} = 12 V, V_{15} = 2 V		135	170	µA
		V_{IN} = 48 V, V_{15} = 2 V		300	390	µA
INTERNAL REGULATOR VOLTAGE* (Sets MOSFET Gate Drive Levels)	V_{CC}	V_{IN} = 12 V to 48 V, I_S = 20 mA	9.75	10.25	11	V
V_{CC} DROPOUT VOLTAGE	V_2–V_3	V_{IN} = 5 V, I_3 = 10 mA		200	250	mV
P GATE TO SOURCE VOLTAGE (OFF)	V_{IN}–V_1	V_{IN} = 12 V*	–0.2	0		V
		V_{IN} = 48 V*	–0.2	0		V
CURRENT SENSE THRESHOLD VOLTAGE	V_9–V_8					
ADP1149 Only		V_8 = 5 V, V_{10} = 1.32 V (Forced)		25		mV
		V_8 = 5 V, V_{10} = 1.1 V* (Forced)	130	150	170	mV
ADP1149-3.3		V_8 = 3.5 V (Forced)		25		mV
		V_8 = 2.9 V (Forced)*	130	150	170	mV
ADP1149-5.0		V_8 = 5.3 V (Forced)		25		mV
		V_8 = 4.4 V (Forced)*	130	150	170	mV

PRELIMINARY TECHNICAL DATA

NOTES

*Denotes specifications that apply over the full operating temperature range.

[1]Pin 10 is a shutdown pin on the ADP1149-3.3 and ADP1149-5 fixed output voltage versions and must be at ground potential for testing.

[2]T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
ADP1149AR, ADP1149AR-3, ADP1149AR-5: $T_J = T_A + (P_D \times 110°C/W)$
ADP1149AN, ADP1149AN-3, ADP1149AN-5: $T_J = T_A + (P_D \times 70°C/W)$

[3]Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) . . . . . –15 V to +60 V
V_{CC} Output Current (Pin 3) . . . . . 50 mA
V_{CC} Input Voltage (Pin 5) . . . . . 20 V
Continuous Output Current (Pins 4, 13) . . . . . 50 mA
Sense Voltages (Pins 10, 15) . . . . . –0.3 V to V_{CC}
Shutdown Voltages (Pins 10, 15) . . . . . 7 V
Operating Temperature Range . . . . . 0°C to +70°C
Junction Temperature . . . . . +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

ORDERING GUIDE

Model	Output Voltage	Package Description*
ADP1149AN	ADJ	PDIP
ADP1149AR	ADJ	SO-16
ADP1149AN-3.3	3.3 V	PDIP
ADP1149AR-3.3	3.3 V	SO-16
ADP1149AN-5	5 V	PDIP
ADP1149AR-5	5 V	SO-16

*For outline information see Package Information section.

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ANALOG DEVICES

Micropower DC-DC Converter

ADP1173

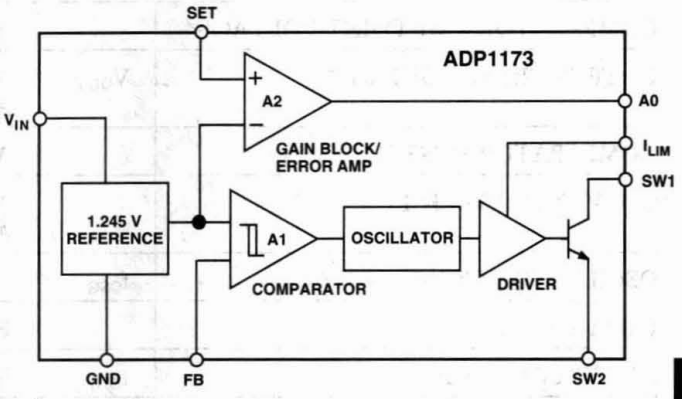
FEATURES

Operates From 2.0 V to 30 V Input Voltages
Typical Only 110 μA Supply Current
Step-Up or Step-Down Mode Operation
Very Few External Components Required
Low Battery Detector On Chip
User-Adjustable Current Limit
Internal 1 A Power Switch
Fixed or Adjustable Output Voltage Versions
8-Pin Plastic DIP or SO-8 Package

APPLICATIONS

Notebook and Palmtop Computers
Cellular Telephones
Flash Memory V p-p Generators
3 V to 5 V, 5 V to 12 V Converters
9 V to 5 V, 12 V to 5 V Converters
Portable Instruments
LCD Bias Generators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP1173 is part of a family of step-up/step-down switching regulators that operates from an input supply voltage of as little as 2 V to 12 V in step-up mode and to 30 V in step-down mode.

The ADP1173 consumes as little as 110 μA in standby mode making it ideal for applications that need low quiescent current. An auxiliary gain amplifier can serve as a low battery detector or linear regulator, under voltage lockout, or error amplifier. The ADP1173 can deliver 80 mA at 5 V from a 3 V input in step-up configuration or 100 mA at 5 V from a 12 V input in step-down configuration. For input voltages of less than 2 V use the ADP1073.

PRELIMINARY TECHNICAL DATA

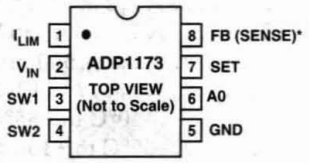
ORDERING GUIDE

Model	Output Voltage	Package Description*
ADP1173AN	ADJ	PDIP
ADP1173AR	ADJ	SO-8
ADP1173AN-5	5 V	PDIP
ADP1173AR-5	5 V	SO-8
ADP1173AN-12	12 V	PDIP
ADP1173AR-12	12 V	SO-8

*For outline information see Package Information section.

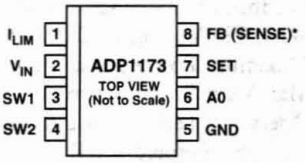
PIN CONFIGURATIONS

8-Lead Plastic DIP



*FIXED VERSIONS

8-Lead SOIC



*FIXED VERSIONS

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ADP1173–SPECIFICATIONS (@ T_A = +25°C, V_{IN} = 3 V, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
QUIESCENT CURRENT*	I_Q	Switch Off		110	150	µA
QUIESCENT CURRENT, BOOST MODE CONFIGURATION	I_Q	No Load ADP1173-5 No Load ADP1173-12		135 250		µA µA
INPUT VOLTAGE*	V_{IN}	Step-Up Mode Step-Down Mode	2.0		12.6 30	V V
COMPARATOR TRIP POINT VOLTAGE*		ADP1173[1]	1.20	1.245	1.30	V
OUTPUT SENSE VOLTAGE*	V_{OUT}	ADP1173-5[2] ADP1173-12[2]	4.75 11.4	5.00 12.0	5.25 12.6	V V
COMPARATOR HYSTERESIS*		ADP1173		5	10	mV
OUTPUT HYSTERESIS*		ADP1173-5 ADP1173-12		20 50	40 100	mV mV
OSCILLATOR FREQUENCY*	f_{OSC}		18	24	30	kHz
DUTY CYCLE*		Full Load	47	55	63	%
SWITCH ON TIME*	t_{ON}	I_{LIM} Tied to V_{IN}	17	23	32	µs
FEEDBACK PIN BIAS CURRENT*		ADP1173, V_{FB} = 0 V		10	50	nA
SET PIN BIAS CURRENT*		$V_{SET} = V_{REF}$		20	100	nA
GAIN BLOCK OUTPUT LOW*	V_{OL}	I_{SINK} = 100 µA, V_{SET} = 1.00 V		0.15	0.4	V
REFERENCE LINE REGULATION*		2.0 V ≤ V_{IN} ≤ 5 V 5 V ≤ V_{IN} ≤ 30 V		0.2 0.02	0.4 0.075	V %/V

NOTES

*Denotes the specifications that apply over the full operating temperature range.

[1]This specification guarantees that both the high and low trip points of the comparator fall within the 1.20 V to 1.30 V range.

[2]The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.

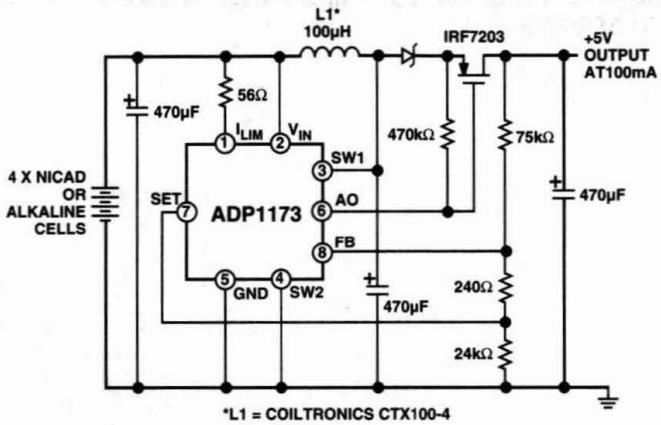
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) . . . . . 36 V
SW1 Pin Voltage (V_{SW1}) . . . . . 50 V
SW2 Pin Voltage (V_{SW2}) . . . . . –0.5 V to V_{IN}
Feedback Pin Voltage (ADP1173) . . . . . 5 V
Sense Pin Voltage (ADP1173, -5, -12) . . . . . 36 V
Maximum Power Dissipation . . . . . 500 mW
Maximum Switch Current . . . . . 1.5 A
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature, (Soldering, 10 sec) . . . . . +300°C

TYPICAL APPLICATION



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Micropower; Step-Up/Step-Down; Fixed 3.3 V, 5 V, 12 V and Adjustable High Frequency SW Regulator

ADP3000

FEATURES

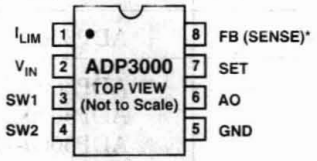
- Operates at Supply Voltages from 2 V to 30 V
- Ground Current: 500 μA
- Works in Step-Up or Step-Down Mode
- Very Few External Components Required
- High Frequency Operation: 400 kHz
- Low Battery Detector on Chip
- User Adjustable Current Limit
- Fixed and Adjustable Output Voltage
- 8-Pin DIP and SO-8 Package
- Ultralow Output Ripple <40 mV p-p @ 3.3 V

APPLICATIONS

- Notebook, Palmtop Computers
- Cellular Telephones
- Hard Disk Drives
- Portable Instruments
- Pagers

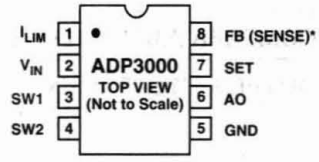
PIN CONFIGURATIONS

8-Lead Plastic DIP (N-8 Package)



*FIXED VERSIONS

8-Lead SOIC (SO-8 Package)



*FIXED VERSIONS

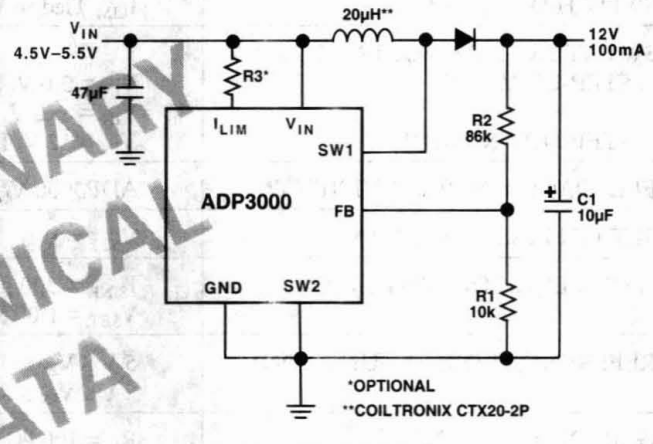


Figure 1. Step-Up DC/DC Converter

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP3000 is a versatile step-up/step-down switching regulator that operates from an input supply voltage of 2 V to 12 V in step-up mode, and up to 30 V in step-down mode.

The ADP3000 consumes only 500 μA making it highly suitable for applications that require low quiescent current.

The ADP3000 can deliver a minimum of 120 mA at 3.3 V from a 5 V input in step-down configuration and 80 mA at 5 V from a 3 V input in step-up configuration.

The auxiliary gain amplifier can be used as a low battery detector, linear regulator under voltage lockout or error amplifier. The ADP3000 operates at 400 kHz and allows for the use of small external components making the device very suitable for space constrained designs.

ORDERING GUIDE

Model	Output Voltage	Package Description	Package Options*
ADP3000AN-3.3	3.3 V	P-DIP	N-8
ADP3000AR-3.3	3.3 V	SOIC	SO-8
ADP3000AN-5	5 V	P-DIP	N-8
ADP3000AR-5	5 V	SOIC	SO-8
ADP3000AN-12	12 V	P-DIP	N-8
ADP3000AR-12	12 V	SOIC	SO-8
ADP3000AN	Adjustable	P-DIP	N-8
ADP3000AR	Adjustable	SOIC	SO-8

*For outline information see Package Information section.

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ADP3000–SPECIFICATIONS (@ V_{IN} = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Conditions[1]	Symbol	ADP3000 Min	ADP3000 Typ	ADP3000 Max	Units
INPUT VOLTAGE*	Step-Up Mode Step-Down Mode	V_{IN}	2.0		12.6 30.0	V V
COMPARATOR TRIP POINT VOLTAGE*	ADP3000[1]		1.20	1.25	1.30	V
OUTPUT SENSE VOLTAGE	ADP3000-3[2] ADP3000-5[2] ADP3000-12[2]	V_{OUT}	 4.75 11.40	3.3 5.00 12.00	 5.25 12.60	V V V
COMPARATOR HYSTERESIS*	ADP3000			8	12.5	mV
OUTPUT HYSTERESIS*	ADP3000-3 ADP3000-5 ADP3000-12			20 32 75	33 50 120	mV mV mV
OSCILLATOR FREQUENCY*		f_{OSC}	350	400	450	kHz
DUTY CYCLE*	Full Load	DC	60	70	80	%
SWITCH ON TIME*	I_{LIM} Tied to V_{IN}	t_{ON}	3.0	3.5	4.0	µs
SW SATURATION VOLTAGE STEP-UP MODE STEP-DOWN MODE	 V_{IN} = 3.0 V, I_{SW} = 650 mA V_{IN} = 5.0 V, I_{SW} = 1 A V_{IN} = 12 V, I_{SW} = 650 mA	V_{SAT}		 0.5 0.8 1.1	 0.65 1.0 1.5	 V V V
FEEDBACK PIN BIAS CURRENT*	ADP3000 V_{FB} = 0 V	I_{FB}		160	220	nA
SET PIN BIAS CURRENT*	V_{SET} = V_{REF}	I_{SET}		140	300	nA
GAIN BLOCK OUTPUT LOW*	I_{SINK} = 300 µA V_{SET} = 1.00 V	V_{OL}		0.15	0.4	V
REFERENCE LINE REGULATION*	5 V ≤ V_{IN} ≤ 30 V 2 V ≤ V_{IN} ≤ 5 V			0.02 0.2	0.075 0.400	%/V %/V
GAIN BLOCK GAIN*	R_L = 100 kΩ[3]	A_V	1000	6000		V/V
CURRENT LIMIT	220 Ω from I_{LIM} to V_{IN}	I_{LIM}		400		mA
CURRENT LIMIT TEMPERATURE COEFFICIENT*				–0.3		%/°C
SWITCH OFF LEAKAGE CURRENT	Measured at SW1 Pin V_{SW1} = 12 V			1	10	µA
MAXIMUM EXCURSION BELOW GND	I_{SW1} ≤ 10 µA, Switch Off			–400	–350	mV

NOTES

*Denotes the specifications that apply over the full operating temperature range.

[1]This specification guarantees that both the high and low trip point of the comparator fall within the 1.20 V to 1.30 V range.

[2]The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.

[3]100 kΩ resistor connected between a 5 V source and the AO pin.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

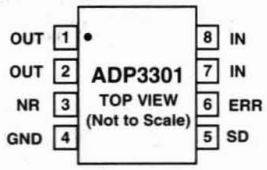
High Accuracy, Low Dropout Linear Regulator

ADP3301

FEATURES
- High Accuracy: 0.5%
- Low Ground Current
- Ultralow Dropout Voltage: 100 mV Typical @ 100 mA
- Requires Only C_O = 0.47 μF for Stability
- Current and Thermal Limiting
- Low Noise
- Dropout Detector
- Low Current Shutdown: 1 μA
- Several Fixed Voltage Options
- 3.0 V to 22 V Supply Range
- –40°C to +125°C Junction Temperature Range
- Thermally Enhanced SO-8 Package

APPLICATIONS
- Cellular Telephones
- Notebook, Palmtop Computers
- Battery Powered Systems
- Portable Instruments
- Post Regulator for Switching Supplies
- Bar Code Scanners

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Option*
ADP3301AR-2.7	–40°C to +125°C	SO-8
ADP3301AR-3.0	–40°C to +125°C	SO-8
ADP3301AR-3.2	–40°C to +125°C	SO-8
ADP3301AR-3.3	–40°C to +125°C	SO-8
ADP3301AR-5.0	–40°C to +125°C	SO-8

*SO = Small Outline Package. For outline information see Package Information section.
For custom voltage outputs, contact Analog Devices.

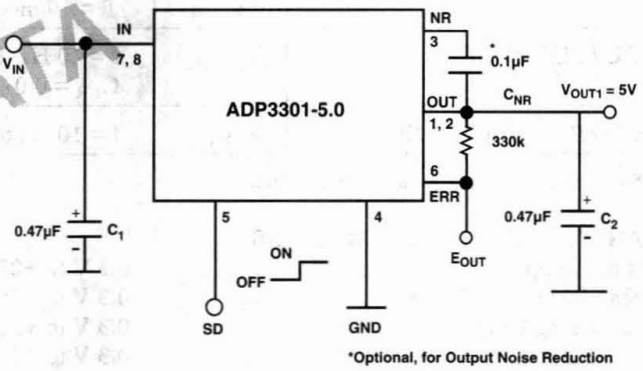
PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP3301 is a member of the ADP330x family of precision, micropower, low dropout regulators. It can supply a load current in excess of 100 mA. It features 1% overall output accuracy and very low 100 mV typical dropout voltage.

The ADP3301 has a wide input voltage range from 3 V to 22 V. It features an error flag that signals when the device is about to lose regulation. It also incorporates short circuit current protection as well as thermal shutdown.

The ADP3301 enhanced lead frame design allows for a maximum power dissipation of 630 mW @ 70°C ambient temperature and 1.15 W at room temperature without any external heat sink.



ADP3301 Application Circuit

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ADP3301–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@T_J = –40°C to +125°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
GROUND CURRENT	I_{GND}	I_L = 100 mA I_L = 0.1 mA		1 0.25	2 0.5	mA mA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} – 4.5 V I_L = 0.1 mA		0.6	0.8	mA
DROPOUT VOLTAGE	V_{DROP}	I_L = 100 mA I_L = 10 mA I_L = 1 mA		0.1 0.05 0.02	0.2 0.1 0.05	V V V
SHUTDOWN THRESHOLD	V_{THSD}	ON OFF	1.5	0.9 0.9	 0.3	V V
SHUTDOWN PIN INPUT CURRENT	I_{SDIN}	0 < V_{SD} < 5 V 5 ≤ V_{SD} ≤ 22 V		0	1 100	µA µA
GROUND CURRENT IN SHUTDOWN MODE	I_Q			0	1	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}				10	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT "LOW" VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.15	0.3	V
SHORT CIRCUIT OUTPUT CURRENT	I_{ISC}		120		400	mA
THERMAL REGULATION	$\frac{\Delta V0}{V0}$	V_{IN} = 22 V, I_L = 100 mA T = 10 ms		0.05	0.2	%/W
OUTPUT NOISE	V_{NOISE}	f = 10 Hz–100 kHz, C_{NR} = 0 C_{NR} = 0.01 µF		200 50		µV rms µV rms
OUTPUT IMPEDANCE	Z_{OUT}	f = 10 Hz to 1 MHz		0.1		Ω

PRELIMINARY TECHNICAL DATA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage . . . . . –0.3 V to +25 V
Shutdown Input Voltage . . . . . –0.3 V to +25 V
Error Flag Output Voltage . . . . . –0.3 V to +25 V
Noise Bypass Pin Voltage . . . . . –0.3 V to +25 V
Thermal Protection . . . . . +165°C
Output Short Circuit . . . . . Protected
Power Dissipation . . . . . Internally Limited
θ_{JA} . . . . . 87°C/W
θ_{JC} . . . . . 41°C/W
Operating Junction Temperature Range . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

θ_{JA} is specified for worst case conditions with devices soldered on a circuit board.

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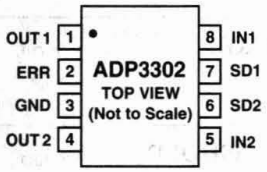
High Accuracy, Dual, Low Dropout Linear Regulator

ADP3302

FEATURES
- High Accuracy: 0.5%
- Low Ground Current
- Extreme Low Dropout Voltage: 100 mV Typical
- Requires Only C_O = 0.47 μF for Stability
- Current and Thermal Limiting
- Low Noise
- Dropout Detector
- 3.0 V to 22 V Supply Range
- –40°C to +125°C Junction Temperature Range
- Low Current Shutdown: 2 μA
- Several Fixed Voltage Options
- Thermally Enhanced SO-8 Package

APPLICATIONS
- Cellular Telephones
- Notebook and Palmtop Computers
- Battery Powered Systems
- Portable Instruments
- High Efficiency Linear Regulators

PIN CONFIGURATION



ORDERING INFORMATION

Model	Temperature Range	Package Option*
ADP3302AR-2.7	–40°C to +125°C	SO-8
ADP3302AR-5.0	–40°C to +125°C	SO-8
ADP3302AR-3.0	–40°C to +125°C	SO-8
ADP3302AR-5.0	–40°C to +125°C	SO-8
ADP3302AR-3.2	–40°C to +125°C	SO-8
ADP3302AR-3.2	–40°C to +125°C	SO-8
ADP3302AR-2.7	–40°C to +125°C	SO-8
ADP3302AR-3.3	–40°C to +125°C	SO-8
ADP3302AR-3.3	–40°C to +125°C	SO-8
ADP3302AR-5.0	–40°C to +125°C	SO-8

*SO = Small Outline Package. For outline information see Package Information section.
Customized options are also available with mixed output voltages.

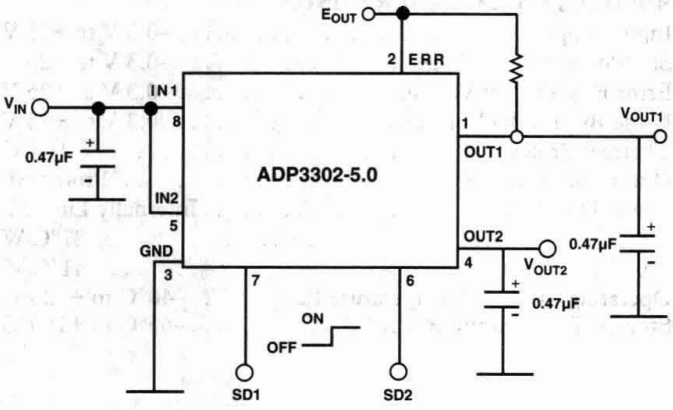
PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADP3302 is a member of the ADP330x family of precision micropower, low dropout regulators. The ADP3302 contains two fully independent 100 mA regulators with separate shutdown and merged error outputs. It features 1% overall output accuracy and very low 100 mV typical dropout voltage.

The ADP3302 has a wide input voltage range from 3 V to 22 V. It features an error flag that signals when either of the two regulators is about to lose regulation. It has short circuit current protection as well as thermal shutdown.

The ADP3302 enhanced lead frame design allows for a maximum power dissipation of 630 mW @ 70°C ambient temperature and 1.15 W at room temperature without any external heat sink.



ADP3302 Application Circuit

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ADP3302–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@T_J = –40°C to +125°C, V_{IN} = 7 V, C_{IN} = 0.47 µF, C_{OUT} = 0.47 µF, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
GROUND CURRENT	I_{GND}	$I_{L1} = I_{L2}$ = 100 mA $I_{L1} = I_{L2}$ = 0.1 mA		4 0.5	8 1.0	mA mA
GROUND CURRENT IN DROPOUT	I_{GND}	V_{IN} – 4.5 V I_L = 0.1 mA		0.4	0.8	mA
DROPOUT VOLTAGE	V_{DROP}	I_L = 100 mA I_L = 10 mA I_L = 1 mA		0.1 0.05 0.02	0.2 0.1 0.05	V V V
SHUTDOWN THRESHOLD	V_{THSD}	ON OFF	1.5	0.9 0.9	 0.3	V V
SHUTDOWN PIN INPUT CURRENT	I_{SDIN}	0 < V_{SD} < 5 V 5 ≤ V_{SD} ≤ 22 V		0	1 100	µA µA
GROUND CURRENT IN SHUTDOWN MODE	I_Q	$V_{SD1} = V_{SD2}$ = 0		0	2	µA
OUTPUT CURRENT IN SHUTDOWN MODE	I_{OSD}				10	µA
ERROR PIN OUTPUT LEAKAGE	I_{EL}	V_{EO} = 5 V			1	µA
ERROR PIN OUTPUT "LOW" VOLTAGE	V_{EOL}	I_{SINK} = 400 µA		0.15	0.3	V
SHORT CIRCUIT OUTPUT CURRENT	I_{OSC}		120		250	mA
THERMAL REGULATION	$\frac{\Delta V0}{V0}$	V_{IN} = 22 V, I_L = 100 mA T = 10 ms		0.05	0.2	%/W
OUTPUT NOISE	V_{NOISE}	f = 10 Hz–100 kHz, C_{NR} = 0 C_{NR} = 0.01 µF		200 50		µV rms V rms
OUTPUT IMPEDANCE	Z_{OUT}	f = 10 Hz to 1 MHz		0.1		Ω

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage . . . . . –0.3 V to +25 V
Shutdown Input Voltage . . . . . –0.3 V to +25 V
Error Flag Output Voltage . . . . . –0.3 V to +25 V
Noise Bypass Pin Voltage . . . . . –0.3 V to +25 V
Thermal Protection . . . . . 165°C
Output Short Circuit . . . . . Protected
Power Dissipation . . . . . Internally Limited
θ_{JA} . . . . . 87°C/W
θ_{JC} . . . . . 41°C/W
Operating Junction Temperature Range . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

θ_{JA} is specified for worst case conditions with devices soldered on a circuit board.

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+5 V Fixed, Adjustable Low-Dropout Linear Voltage Regulator

ADP3367*

FEATURES

Low Dropout: 150 mV @ 200 mA
300 mV @ 300 mA
Low Power CMOS: 17 μA Quiescent Current
Shutdown Mode: 0.2 μA Quiescent Current
300 mA Output Current Guaranteed
Pin Compatible with MAX667
Stable with 10 μF Load Capacitor
+2.5 V to +16.5 V Operating Range
Low Battery Detector
Fixed +5 V or Adjustable Output
High Accuracy: ±2%
Dropout Detector Output
Low Thermal Resistance Package*
ESD > 6000 V

APPLICATIONS

Handheld Instruments
Cellular Telephones
Battery Operated Devices
Portable Equipment
Solar Powered Instruments
High Efficiency Linear Power Supplies

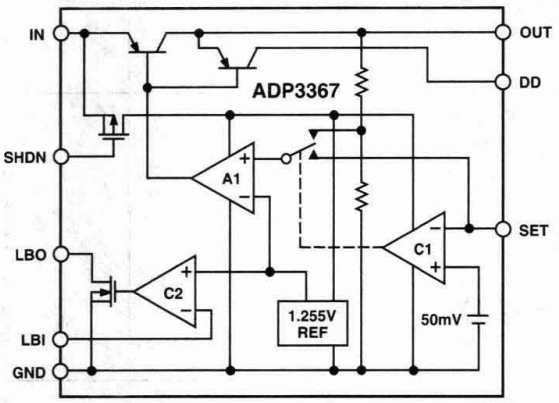
GENERAL DESCRIPTION

The ADP3367 is a low-dropout precision voltage regulator that can supply up to 300 mA output current. It can be used to give a fixed +5 V output with no additional external components or can be adjusted from +1.3 V to +16 V using two external resistors. Fixed or adjustable operation can be selected via the SET input. The low quiescent current (17 μA) in conjunction with the standby or shutdown mode (0.2 μA) makes this device especially suitable for battery powered systems. The dropout voltage when supplying 100 μA is only 15 mV allowing operation with minimal headroom thereby prolonging the useful battery life. At higher output current levels the dropout remains low increasing to just 150 mV when supplying 200 mA. A wide input voltage range from 2.5 V to 16.5 V is allowable. Additional features include a dropout detector and a low supply/battery monitoring comparator. The dropout detector can be used to signal loss of regulation while the low battery detector can be used to monitor the input supply voltage.

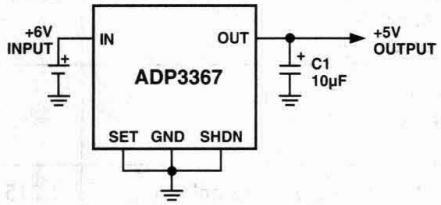
The ADP3367 is a much improved pin-compatible replacement for the MAX667. Improvements include lower supply current, tighter voltage accuracy and superior line and load regulation. Improved ESD protection (>6000 V) is achieved by advanced voltage clamping structures. The ADP3367 is specified over the industrial temperature range –40°C to +85°C and is available in narrow surface mount (SOIC) packages.

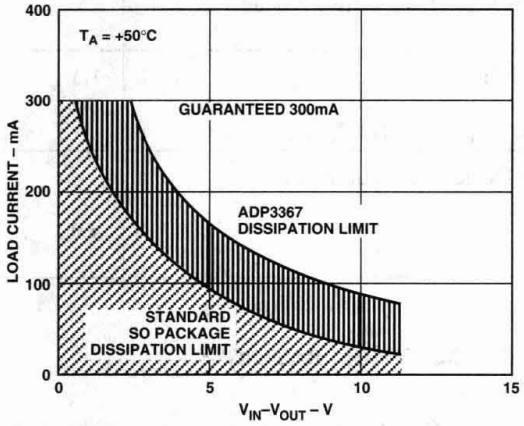
*Patent pending.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL OPERATING CIRCUIT





Load Current vs. Input-Output Differential Voltage

ADI's proprietary Thermal Coastline leadframe used in ADP3367AR packaging, has 30% lower thermal resistance than the standard leadframes. This improvement in heat flow rate results in lower die temperature hence improves reliability.

ADP3367–SPECIFICATIONS (V_{IN} = +9 V, GND = 0 V, V_{OUT} = +5 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V_{IN}	2.5		16.5	V	
Output Voltage, V_{OUT}	4.9	5.0	5.1	V	V_{SET} = 0 V, V_{IN} = 6 V, I_{OUT} = 10 mA
Maximum Output Current	200			mA	V_{IN} = +9 V, + 4.5 V < V_{OUT} < +5.5 V
Quiescent Current					
I_{GND}: Shutdown Mode		0.2	0.75	µA	V_{SHDN} = 2 V
I_{GND}: Normal Mode					V_{SHDN} = 0 V, V_{SET} = 0 V
		17	25	µA	I_{OUT} = 0 µA
		20	30	µA	I_{OUT} = 100 µA
		5	14	mA	I_{OUT} = 200 mA
Dropout Voltage					
V_{OUT} = 5 V		15	40	mV	I_{OUT} = 100 µA
		60	125	mV	I_{OUT} = 50 mA
		100	175	mV	I_{OUT} = 100 mA
		150	250	mV	I_{OUT} = 200 mA, T_A = +25°C
		175	300	mV	I_{OUT} = 200 mA
		300	500	mV	I_{OUT} = 300 mA
V_{OUT} = 3.3 V		94	140	mV	I_{OUT} = 50 mA
		210	312	mV	I_{OUT} = 100 mA
		430	625	mV	I_{OUT} = 200 mA, T_A = +25°C
Load Regulation		5	10	mV	I_{OUT} = 10 mA–100 mA, V_{IN} = 6 V
					I_{OUT} = 10 mA–200 mA, V_{IN} = 6 V
Line Regulation		0.1	5	mV	V_{IN} = 6 V to 10 V, I_{OUT} = 10 mA
Reference Voltage, V_{SET}	1.23	1.255	1.28	V	
SET Input Threshold		50		mV	
SET Input Current, I_{SET}		±0.01	±10	nA	V_{SET} = 1.5 V
Output Leakage Current, I_{OUT}		0.1	1	µA	V_{SHDN} = 2 V
Short Circuit Current, I_{OUT}		400		mA	T_A = +25°C
		450		mA	T_A = T_{MIN} to T_{MAX}
Low Battery Detector Input Threshold, V_{LBI}	1.215	1.255	1.295	V	
LBI Hysteresis		6		mV	
LBI Input Leakage Current, I_{LBI}		±0.01	±10	nA	V_{LBI} = 1.5 V
Low Battery Detector Output Voltage, V_{LBO}			0.25	V	V_{LBI} = 0 V, I_{LBO} = 10 mA, T_A = +25°C
			0.40	V	V_{LBI} = 0 V, I_{LBO} = 10 mA, T_A = T_{MIN} to T_{MAX}
Shutdown Input Voltage, V_{SHDN}	1.5			V	V_{IH}
			0.4	V	V_{IL}
Shutdown Input Current, I_{SHDN}		±0.01	±10	nA	V_{SHDN} = 0 V to V_{IN}
Dropout Detector Output Voltage			0.25	V	(V_{SET} = 0 V, V_{SHDN} = 0 V, R_{DD} = 100 kΩ,
					V_{IN} = 7 V, I_{OUT} = 10 mA)
	4.0				(V_{SET} = 0 V, V_{SHDN} = 0 V, R_{DD} = 100 kΩ,
					V_{IN} = 4.5 V, I_{OUT} = 10 mA)

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A= +25°C unless otherwise noted)

Input Voltage, V_{IN} . . . . . +18 V
Output Short Circuit to GND Duration . . . . . 1 sec
LBO Output Sink Current . . . . . 50 mA
LBO Output Voltage . . . . . GND to V_{OUT}
SHDN Input Voltage . . . . . –0.3 V to (V_{IN} + 0.3 V)
LBI, SET Input Voltage . . . . . –0.3 V to (V_{IN} + 0.3 V)
Power Dissipation, R-8 . . . . . 960 mW
(Derate 10 mW/°C above +50°C)
θ_{JA}, Thermal Impedance . . . . . 98°C/W
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
ESD Rating . . . . . > 6000 V

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADP3367AR	–40°C to +85°C	SO-8

*SO = Small Outline Package. For outline information see Package Information section.

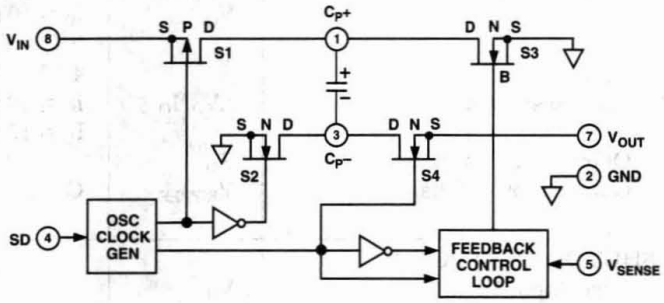
Switched Capacitor Voltage Converter with Regulated Output

ADP3603*

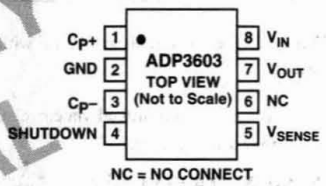
FEATURES
Input Voltage Range: 4.5 V to 6 V
50 mA Output Current
±2% Output Accuracy
High Switching Frequency: 120 kHz
Regulated Output
Small Outline 8-Pin SOIC Package
Shutdown Pin

APPLICATIONS
Voltage Inverters
Negative Voltage Regulators
Computer Peripherals and Add-On Cards
Portable Instruments
Battery Powered Devices
Pagers and Radio Control Receivers
Disk Drives
Mobile Phones

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The ADP3603 switched capacitor voltage converter provides a regulated output voltage with minimum voltage loss, minimum number of external components and does not require the use of an inductor.

The internal oscillator runs at 240 kHz nominal frequency which produces an output switching frequency of 120 kHz allowing the use of small charge pump and filter capacitors. For other output voltages from –1.2 V to –4.0 V, contact the factory.

*Patent pending.

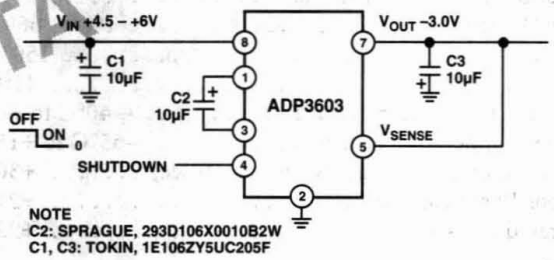


Figure 1. Typical Application Circuit

PRELIMINARY TECHNICAL DATA

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ADP3603–SPECIFICATIONS (V_{IN} = 5.0 V @ T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Condition[1]	Min	Typ	Max	Units
OPERATING SUPPLY RANGE	V_S		4.5	5	6	V
SUPPLY CURRENT	I_S			3	5	mA
Shutdown Mode					1	mA
OUTPUT						
Output Voltage	V_O	I_O = 25 mA	–2.85	–3.0	–3.15	V
	V_O	I_O = 10 mA to 50 mA, 0°C ≤ T_A ≤ +70°C, 4.5 V ≤ V_S ≤ 6.0 V	–2.7	–3.0	–3.3	V
Load Regulation	$\Delta V_O/I_O$	I_O = 10 mA–25 mA		0.7		mV/mA
		I_O = 10 mA–50 mA		1.2		mV/mA
Output Resistance[2]	R_O			12		Ω
Output Ripple Voltage[3]	V_{RIPPLE}	C1–C3 = 10 µF, I_{LOAD} = 10 mA		15		mV
		I_{LOAD} = 50 mA		25		mV
SHUTDOWN INPUT						
Logic Input High	V_{IH}		2.4			V
Input Current	I_{IH}			1		µA
Logic Input Low	V_{IL}				0.4	V
Input Current	I_{IL}			1		µA
Turn-On Time	t_{ON}	Figure 1, I_L = 50 mA		7		ms
Turn-Off Time	t_{OFF}	Figure 1, I_L = 50 mA		7		ms

NOTES
[1]Capacitors C1 and C2 used in the test circuit are 10 µF with 0.1 Ω ESR. Capacitors with higher ESR may reduce output voltage and efficiency.
[2]Open-loop output resistance.
[3]See Figure 1 conditions.
All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

Input Voltage (V+ to GND, GND to OUT) ..... +7.5 V
Output Short Circuit Protection ..... 1 sec
Power Dissipation ..... 660 mW
θ_{JA}[2] ..... 150°C/W
θ_{JC} ..... 41°C/W
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES
[1] This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]θ_{JA} is specified for worst case conditions with devices soldered on a circuit board.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADP3603AR	0°C to +70°C	SO-8

*SO = Small Outline Package. For outline information see Package Information section.

PIN DESCRIPTION

Pin	Function
1	C_P+, Pump Capacitor Positive Input.
2	Ground.
3	C_P–, Pump Capacitor Negative Input.
4	Shutdown, Logic Level Shutdown Pin. Application of a logic low to this pin will place the regulator in normal operation. The device will be put into shutdown mode with the shutdown pin pulled to V_{IN}. In shutdown mode the charge pump is turned off. Connect to ground for normal operation.
5	V_{SENSE}, Output Voltage Sense Line. This is used to improve load regulation performance by eliminating IR drop on the output traces. See application section for more detail. For normal operation, connect Pin 5 to V_{OUT} (Pin 7).
6	NC, No Internal Electrical Connection.
7	V_{OUT}, Output Pin. Regulated negative output voltage. Connect a low ESR capacitor between this pin and device GND.
8	V_{IN}, Positive Supply Input when 4.5 V ≤ V_{IN} ≤ 6 V. Connect a low-ESR bypass capacitor between this pin and the device ground pin.

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Switched Capacitor Voltage Converter with Regulated Output

ADP3604*

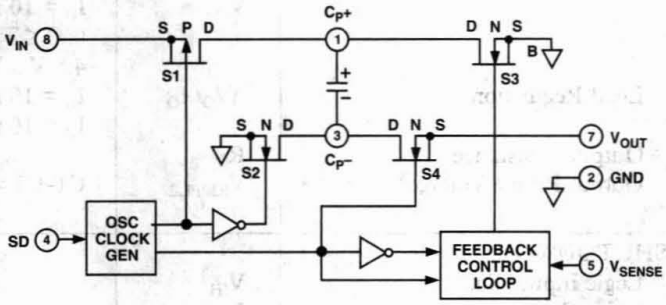
FEATURES

Input Voltage Range from 4.5 V to 6 V
120 mA Output Current
±2% Output Accuracy
High Switching Frequency: 120 kHz
Regulated Output
Small Outline 8-Pin SOIC Package
Shutdown Pin

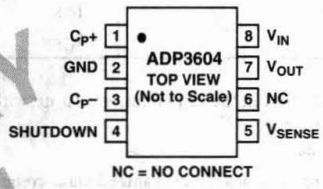
APPLICATIONS

Voltage Inverters
Voltage Regulators
Computer Peripherals and Add-On Cards
Portable Instruments
Battery Powered Devices
Pagers and Radio Control Receivers
Disk Drives
Mobile Phones

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



NC = NO CONNECT

20

GENERAL DESCRIPTION

The ADP3604 switched capacitor voltage converter provides a regulated output voltage with minimum voltage loss, minimum number of external components, and does not require the use of an inductor.

The internal oscillator runs at 240 kHz nominal frequency which produces an output switching frequency of 120 kHz, allowing the use of small charge pump and filter capacitors. For other output voltages from –1.2 V to –4.0 V, contact the factory.

*Patent pending.

PRELIMINARY TECHNICAL DATA

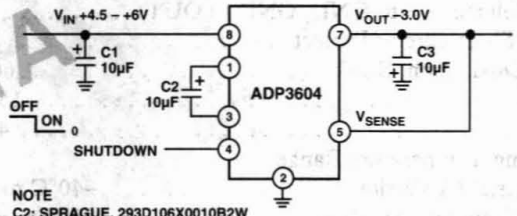


Figure 1. Typical Application Circuit

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ADP3604–SPECIFICATIONS (V_{IN} = 5.0 V @ T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
OPERATING SUPPLY RANGE	V_S		4.5	5	6	V
SUPPLY CURRENT	I_S			3	5	mA
Shutdown Mode					1	mA
OUTPUT						
Output Voltage	V_O	I_O = 60 mA	–2.94	–3.0	–3.06	V
	V_O	I_O = 10 mA to 120 mA, 0°C ≤ T_A ≤ +70°C, 4.5 V ≤ V_S ≤ 6.0 V	–2.7	–3.0	–3.3	V
Load Regulation	$\Delta V_O / I_O$	I_O = 10 mA–40 mA		0.9		mV/mA
		I_O = 10 mA–120 mA		1.5		mV/mA
Output Resistance[2]	R_O			8		Ω
Output Ripple Voltage[3]	V_{RIPPLE}	C1–C3 = 10 µF, I_{LOAD} = 80 mA		25		mV
		I_{LOAD} = 120 mA		55		mV
SHUTDOWN						
Logic Input High	V_{IH}		2.4			V
Input Current	I_{IH}			1		µA
Logic Input Low	V_{IL}				0.4	V
Input Current	I_{IL}			1		µA
Turn-On-Time	t_{ON}	Figure 1, I_L = 120 mA		5		ms
Turn-Off-Time	t_{OFF}	Figure 1, I_L = 120 mA		5		ms

NOTES

[1]Capacitors C1 and C2 used in the test circuit are 10 µF with 0.1 Ω ESR. Capacitors with higher ESR may reduce output voltage and efficiency.

[2]Open-loop output resistance.

[3]See Figure 1 conditions.

All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

Input Voltage (V+ to GND, GND to OUT) . . . . . +7.5 V
Output Short Circuit Protection . . . . . 1 sec
Power Dissipation, SO-8 . . . . . 660 mW
θ_{JA}[2] . . . . . 150°C/W
θ_{JC} . . . . . 41°C/W
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

NOTES

[1]This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]θ_{JA} is specified for worst case conditions with device soldered on a circuit board.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADP3604AR	0°C to +70°C	SO-8

*SO = Small Outline Package. For outline information see Package Information section.

PIN DESCRIPTION

Pin	Function
1	C_P+, Pump Capacitor Positive Input.
2	Ground.
3	C_P–, Pump Capacitor Negative Input.
4	Shutdown, Logic Level Shutdown Pin. Application of a logic low to this pin will place the regulator in normal operation. The device will be put into shutdown mode with the shutdown pin pulled to V_{IN}. In Shutdown mode the charge pump is turned off. Connect to ground for normal operation.
5	V_{SENSE}, Output Voltage Sense Line. This is used to improve load regulation performance by eliminating IR drop on the output traces. See application section for more detail. For normal operation, connect Pin 5 to V_{OUT} (Pin 7).
6	NC, No Internal Electrical Connection.
7	V_{OUT}, Output Pin. Regulated negative output voltage. Connect a low ESR capacitor between this pin and device GND.
8	V_{IN}, Positive Supply Input when 4.5 V ≤ V_{IN} ≤ 6 V. Connect a low-ESR bypass capacitor between this pin and the device ground pin.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Thermal Management Circuits
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Thermal Management Circuits–Selection Guides

4-to-20 mA Transmitters

Model	Power $+V_{CC}$ Volts	CMV Volts rms	CMR dB min	Accuracy ±% max	Input Range Volts	Int V_{REF}	Output Range mA	# Pins	Page No.	Comments	Fax-code
AD693†	+12–+36 @ 0.7 mA	V_{CC} – 4 V	80	0.05–0.07	@ 30 mV/60 mV	Y	0, 4–20	20	21–13	Calibrated 30/60 mV Input Spans	1235
AD694J/A	+4.5–+36 @ 2 mA		NA	0.015–0.3	or 0 to +2	Y	0, 4–20	16	21–15	Calibrated 2/10 V Input Spans	1236

Temperature Sensors

Model	Output 25°C	Output Scale Factor	Accuracy +25°C	Linearity °C	Operating Range °C	Digital Output	Supply Range Volts	I_Q µA	# Pins	Page No.	Comments	Fax-code
AD22100	1.375 V	22.5 mV/°C	±2	1% FS	–50 to +150		+4 to +6	650	3/8	21–19	V_{OUT} Proportional to V_{DD}	1091
AD22103	0.25 V	28 mV/°C	±2	0.5% FS	–50 to +150		+2.7 to +3.6	600	3/8	21–21	V_{OUT} Proportional to V_{DD}	1861
AD590	298.2 µA	1 µA/K	±0.5 µA–5 µA	1.5	–55 to +150		+4 to +30	$I_{OUT} = I_Q$	3	21–5		1186
AD592	298.2 µA	1 µA/K	±0.5 µA–1 µA	0.4–0.5	–55 to +150		+4 to +30	$I_{OUT} = I_Q$	3	21–7		1187
TMP35	250 mV	10 mV/°C	±2–3°C	0.5	–40 to +125		+2.7 to +5.5	50	3/5/8	21–35	I_{OUT} = 0.5 µA in Shutdown	1972
TMP36	750 mV	10 mV/°C	±2–3°C	0.5	–40 to +125		+2.7 to +5.5	50	3/5/8	21–35	I_{OUT} = 0.5 µA in Shutdown	1972
TMP37	500 mV	20 mV/°C	±2–3°C	0.5	–40 to +125		+2.7 to +5.5	50	3/5/8	21–35	I_{OUT} = 0.5 µA in Shutdown	1972

Temperature Switches

Model	Output 25°C	Output Scale Factor	Accuracy +25°C	Linearity °C	Operating Range °C	Digital Output	Supply Range Volts	I_Q µA	# Pins	Page No.	Comments	Fax-code
AD22105	NA	NA	±2	NA	–40 to +150	1 Open Col	+2.7 to +7		6/8	21–23	User Programmable	1974
TMP12	NA	NA	±3	0.5 typ	–40 to +125	2 Open Col	+4.5 to +12	600	8	21–31	Controller, with Window Comparator Heater Input, and Resistor Prgm Hysteresis	1970
TMP10	750 mV	10 mV/°C	±2	0.5 typ	–40 to +125	1 Open Col	+2.7 to +5.5	100	8	21–29	Single Setpoint Control	
TMP14	+2.5 V	5 mV/°C	±3	0.5 typ	–40 to +125	4 Open Col	+4.5 to +5.5	500	10	21–33	Quad Setpoint	

Temperature Switches with Temperature Output

Model	Output 25°C	Output Scale Factor	Accuracy +25°C	Linearity °C	Range °C	Operating Digital Output	Range Volts	I_Q µA	Supply # Pins	Page No.	Comments	Fax-code
TMP01	1.49 V	5 mV/K	±1.5 ± –3	0.5 typ	–55 to +150	2 Open Col	+4.5 to +13.2	800	8/14	21–25	Controller, with Window Comparator	1807

†Loop powered, no local supply needed.

Temperature Sensors with Digital Output

(Equations Apply to Both Models)

Model	Output 25°C	Output Scale Factor	Accuracy +25°C	Linearity °C	Operating Range °C	Digital Output	Supply Range Volts	I_Q µA	# Pins	Page No.	Comments	Fax-code
TMP03	35 Hz	°C = 235 – (400 * T1)/T2	±2	±1	–55 to +150	1 Open Col	+4.5 to +7	1000	3/8	21–27	Pulse Width Modulated Output	1850
TMP04	35 Hz	°F = 455 – (720 * T1)/T2	±2	±1	–55 to +150	TTL/CMOS	+4.5 to +7	1000	3/8	21–27	Pulse Width Modulated Output	1850

Thermocouple Signal Conditioners, J & K

Model	Output 25°C	Output Scale Factor	Accuracy +25°C	Linearity °C	Operating Range °C	Digital Output	Supply Range Volts	I_Q µA	# Pins	Page No.	Comments	Fax-code
AD594	0.25	10 mV/°C	1–3		+25–+100	1 Open Col	+5–±15	300	14	21–9	Set Point Mode Operation	1189
AD595	0.25	10 mV/°C	1–3		+25–+100	1 Open Col	+5–±15	300	14	21–9	Set Point Mode Operation	1189
AD596	0.282	10 mV/°C	4		+25–+100	1 Open Col	+5–±15	160	8/10	21–11	Set Point Controller	1190
AD597	0.282	10 mV/°C	4		+25–+100	1 Open Col	+5–±15	160	8/10	21–11	Set Point Controller	1190

5-Channel Bulb Monitor

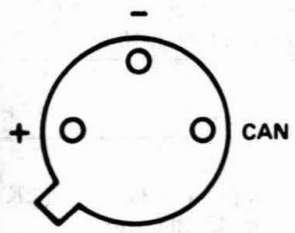
Model		# Pins	Page No.	Comments	Fax-code
AD22001	See Data Sheet for Specs	20	21–17		1021

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
Linear Current Output: 1 μA/K
Wide Range: –55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4 V to +30 V
Sensor Isolation from Case
Low Cost

PIN DESIGNATIONS



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4 V and +30 V the device acts as a high impedance, constant current regulator passing 1 μA/K. Laser trimming of the chip's thin-film resistors is used to calibrate the device to 298.2 μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4 V to +30 V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interface rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5 mWs @ 5 V @ +25°C.) These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10 MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5 V to 10 V results in only a 1 μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44 V and a reverse voltage of 20 V. Hence, supply irregularities or pin reversal will not damage the device.

***Protected by Patent No. 4,123,698.**

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AD590–SPECIFICATIONS (@ +25°C and V_S = +5 V unless otherwise noted)

Model	AD590J			AD590K			
	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ or E–)			+44			+44	Volts
Reverse Voltage (E+ to E–)			–20			–20	Volts
Breakdown Voltage (Case E+ or E–)			±200			±200	Volts
Rated Performance Temperature Range[1]	–55		+150	–55		+150	°C
Storage Temperature Range[1]	–65		+155	–65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		µA
Nominal Temperature Coefficient		1			1		µA/K
Calibration Error @ +25°C			**±5.0**			**±2.5**	°C
Absolute Error (Over Rated Performance Temperature Range)							
Without External Calibration Adjustment			**±10**			**±5.5**	°C
With +25°C Calibration Error Set to Zero			**±3.0**			**±2.0**	°C
Nonlinearity			**±1.5**			**±0.8**	°C
Repeatability[2]			±0.1			±0.1	°C
Long-Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/$\sqrt{\text{Hz}}$
Power Supply Rejection							
+4 V ≤ V_S ≤ +5 V		0.5			0.5		µA/V
+5 V ≤ V_S ≤ +15 V		0.2			0.2		µV/V
+15 V ≤ V_S ≤ +30 V		0.1			0.1		µA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		µs
Reverse Bias Leakage Current[4]							
(Reverse Voltage = 10 V)		10			10		pA
PACKAGE OPTIONS[5]							
TO-52 (H-03A)		AD590JH			AD590KH		
Flatpack (F-2A)		AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at –100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between +25°C readings after temperature cycling between –55°C and +150°C; guaranteed not tested.

[3]Conditions: constant +5 V, constant +125°C; guaranteed, not tested.

[4]Leakage current doubles every 10°C.

[5]For outline information see Package Information section.

Specifications subject to change without notice.

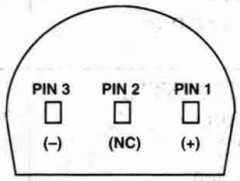
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES
High Precalibrated Accuracy: 0.5°C max @ +25°C
Excellent Linearity: 0.15°C max (0°C to +70°C)
Wide Operating Temperature Range: –25°C to +105°C
Single Supply Operation: +4 V to +30 V
Excellent Repeatability and Stability
High Level Output: 1 μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

CONNECTION DIAGRAM



★ PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1 μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

The AD592 can be employed in applications between –25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

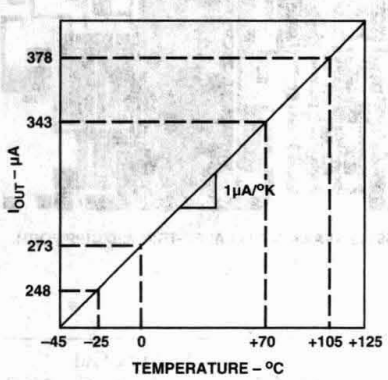
Typical application areas include: appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

The AD592 is available in three performance grades: the AD592AN, AD592BN and AD592CN. All devices are packaged in a plastic TO-92 case rated from –45°C to +125°C. Performance is specified from –25°C to +105°C. AD592 chips are also available, contact the factory for details.

***Protected by Patent No. 4,123,698.**

PRODUCT HIGHLIGHTS

1. With a single supply (4 V to 30 V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (–25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20 V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.



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AD592–SPECIFICATIONS (typical @ T_A = +25°C, V_S = +5 V, unless otherwise noted)

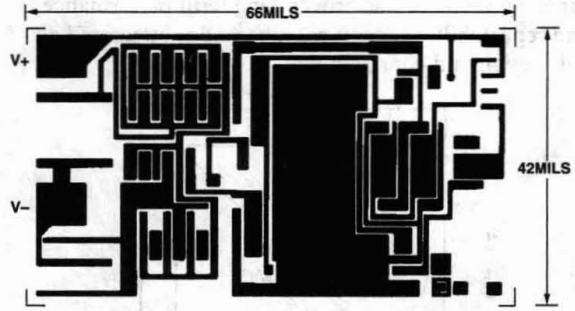
Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @ +25°C[1]		1.5	**2.5**		0.7	**1.0**		0.3	**0.5**	°C
T_A = 0°C to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = –25°C to +105°C										
Error over Temperature[3]		2.0	**3.5**		0.9	**2.0**		0.5	**1.0**	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @ +25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	–25		+105	–25		+105	–25		+105	°C
Package Temperature[6]	–45		+125	–45		+125	–45		+125	°C
Forward Voltage (+ to –)			**44**			**44**			**44**	V
Reverse Voltage (– to +)			**20**			**20**			**20**	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4 V < V_S < +5 V			**0.5**			**0.5**			**0.5**	°C/V
+5 V < V_S < +15 V			**0.2**			**0.2**			**0.2**	°C/V
+15 V < V_S < +30 V			**0.1**			**0.1**			**0.1**	°C/V

NOTES
[1]An external calibration trim can be used to zero the error @ +25°C.
[2]Defined as the maximum deviation from a mathematically best fit line.
[3]Parameter tested on all production units at +105°C only. C grade at –25°C also.
[4]Maximum deviation between +25°C readings after a temperature cycle between –45°C and +125°C. Errors of this type are noncumulative.
[5]Operation @ +125°C, error over time is noncumulative.
[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

Specifications subject to change without notice.

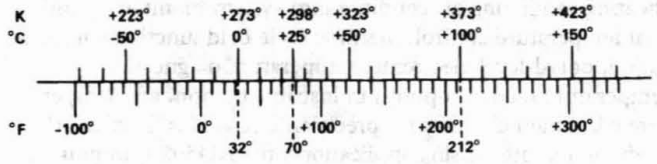
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION DIAGRAM



THE AD592 IS AVAILABLE IN LASER-TRIMMED CHIP FORM.

TEMPERATURE SCALE CONVERSION EQUATIONS



$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

ORDERING GUIDE

Model	Max Cal Error @ +25°C	Max Error –25°C to +105°C	Max Nonlinearity –25°C to +105°C	Package Option*
AD592CN	0.5°C	1.0°C	0.35°C	TO-92
AD592BN	1.0°C	2.0°C	0.4°C	TO-92
AD592AN	2.5°C	3.5°C	0.5°C	TO-92

*For outline information see Package Information section.

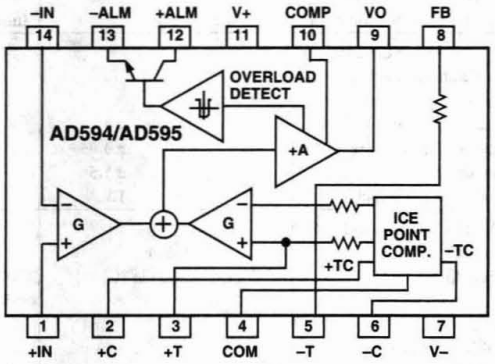
Monolithic Thermocouple Amplifiers with Cold Junction Compensation

AD594*/AD595*

FEATURES

- **Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples**
- **Can Be Used with Type T Thermocouple Inputs**
- **Low Impedance Voltage Output: 10 mV/°C**
- **Built-In Ice Point Compensation**
- **Wide Power Supply Range: +5 V to ±15 V**
- **Low Power: <1 mW typical**
- **Thermocouple Failure Alarm**
- **Laser Wafer Trimmed to 1°C Calibration Accuracy**
- **Setpoint Mode Operation**
- **Self-Contained Celsius Thermometer Operation**
- **High Impedance Differential Input**
- **Side-Brazed DIP or Low Cost Cerdip**

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10 mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output setpoint controller using either fixed or remote setpoint control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low impedance voltage output.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5 V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current 160 μA, but is also capable of delivering in excess of ±5 mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for the thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

***Protected by U.S. Patent No. 4,029,974.**

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0°C to +50°C, and are available in 14-pin, hermetically sealed, side-brazed ceramic DIPs as well as low cost cerdip packages.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pinout provides for operation as a setpoint controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range +5 V to dual supplies spanning 30 V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

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AD594/AD595—SPECIFICATIONS (@ +25°C and V_S = 5 V, Type J (AD594), Type K (AD595) Thermocouple, unless otherwise noted)

Model	AD594A			AD594C			AD595A			AD595C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATING													
$+V_S$ to $-V_S$			36			36			36			36	Volts
Common-Mode Input Voltage	$-V_S - 0.15$		$+V_S$	$-V_S - 0.15$		$+V_S$	$-V_S - 0.15$		$+V_S$	$-V_S - 0.15$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages													
+ALM	$-V_S$		$-V_S + 36$	$-V_S$		$-V_S + 36$	$-V_S$		$-V_S + 36$	$-V_S$		$-V_S + 36$	Volts
-ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	–55		+125	–55		+125	–55		+125	–55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT													
(Specified Temperature Range 0°C to +50°C)													
Calibration Error at +25°C[1]			**±3**			**±1**			**±3**			**±1**	°C
Stability vs. Temperature[2]			**±0.05**			**±0.025**			**±0.05**			**±0.025**	°C/°C
Gain Error			**±1.5**			**±0.75**			**±1.5**			**±0.75**	%
Nominal Transfer Function			10			10			10			10	mV/°C
AMPLIFIER CHARACTERISTICS													
Closed Loop Gain[3]		**193.4**				**193.4**			**247.3**			**247.3**	
Input Offset Voltage		(Temperature in °C) × 51.70 µV/°C			(Temperature in °C) × 51.70 µV/°C			(Temperature in °C) × 40.44 µV/°C			(Temperature in °C) × 40.44 µV/°C		µV
Input Bias Current		0.1			0.1			0.1			0.1		µA
Differential Input Range	–10		+50				–10		+50	–10		+50	mV
Common-Mode Range	**$-V_S - 0.15$**		**$-V_S - 4$**	**$-V_S - 0.15$**		**$-V_S - 4$**	**$-V_S - 0.15$**		**$-V_S - 4$**	**$-V_S - 0.15$**		**$-V_S - 4$**	Volts
Common-Mode Sensitivity – RTO			**10**			**10**			**10**			**10**	mV/V
Power Supply Sensitivity – RTO			**10**			**10**			**10**			**10**	mV/V
Output Voltage Range													
Dual Supply	**$-V_S + 2.5$**		**$+V_S - 2$**	**$-V_S + 2.5$**		**$+V_S - 2$**	**$-V_S + 2.5$**		**$+V_S - 2$**	**$-V_S + 2.5$**		**$+V_S - 2$**	Volts
Single Supply	0		$+V_S - 2$	0		$-V_S - 2$	0		$+V_S + 2$	0		$+V_S - 2$	Volts
Usable Output Current[4]		±5			±5			±5			±5		mA
3 dB Bandwidth		15			15			15			15		kHz
ALARM CHARACTERISTICS													
$V_{CE(SAT)}$ at 2 mA		0.3			0.3			0.3			0.3		Volts
Leakage Current			**±1**			**±1**			**±1**			**±1**	µA max
Operating Voltage at – ALM			**$+V_S - 4$**			**$+V_S - 4$**			**$+V_S - 4$**			**$+V_S - 4$**	Volts
Short Circuit Current		20			20			20			20		mA
POWER REQUIREMENTS													
Specified Performance	$+V_S = 5, -V_S = 0$			$+V_S = 5, -V_S = 0$			$+V_S = 5, -V_S = 0$			$+V_S = 5, -V_S = 0$			Volts
Operating[5]	$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			Volts
Quiescent Current (No Load)													
$+V_S$		160	300		160	300		160	300		160	300	µA
$-V_S$		100			100			100			100		µA
PACKAGE OPTION													
TO-116 (D-14)	AD594AD			AD594CD			AD595AD			AD595CD			
Cerdip (Q-14)	AD594AQ			AD594CQ			AD595AQ			AD595CQ			

NOTES

[1]Calibrated for minimum error at +25°C using a thermocouple sensitivity of 51.7 µV/°C. Since a J type thermocouple deviates from this straight line approximation, the AD594 will normally read 3.1 mV when the measuring junction is at 0°C. The AD595 will similarly read 2.7 mV at 0°C.

[2]Defined as the slope of the line connecting the AD594/AD595 errors measured at 0°C and 50°C ambient temperature.

[3]Pin 8 shorted to Pin 9.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50 kΩ resistor at output voltages below 2.5 V.

[5]$-V_S$ must not exceed –16.5 V.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

Thermocouple Conditioners and Setpoint Controllers

AD596*/AD597*

FEATURES
Low Cost
Operates with Type J (AD596) or Type K (AD597) Thermocouples
Built-In Ice Point Compensation
Temperature Proportional Operation – 10 mV/°C
Temperature Setpoint Operation – ON/OFF
Programmable Switching Hysteresis
High Impedance Differential Input

GENERAL DESCRIPTION

The AD596/AD597 is a monolithic temperature setpoint controller which has been optimized for use at elevated temperatures such as those found in oven control applications. The device cold junction compensates and amplifies a type J or K thermocouple input to derive an internal signal proportional to temperature. The internal signal is then compared with an externally applied setpoint voltage to yield a low impedance switched output voltage. Dead-Band or switching hysteresis can be programmed using a single external resistor. Alternately, the AD596/AD597 can be configured to provide a voltage output (10 mV/°C) directly from a type J or K thermocouple signal. It can also be used as a stand-alone voltage output temperature sensor.

The AD596/AD597 can be powered with a single supply from +5 V to +30 V, or dual supplies up to a total span of 36 V. Typical quiescent supply current is 160 μA which minimizes self-heating errors.

The AD596/AD597 H package option includes a thermocouple failure alarm that indicates an open thermocouple lead when operated in the temperature proportional measurement mode. The alarm output has a flexible format which can be used to drive relays, LEDs or TTL logic.

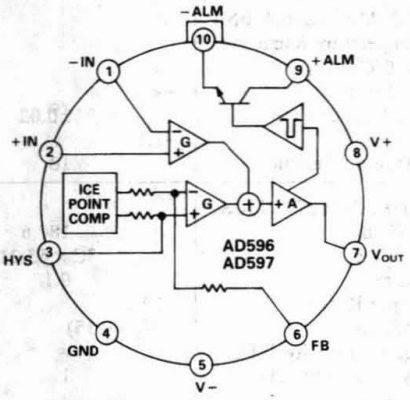
The device is packaged in a reliability qualified, cost effective 10-pin metal can, 8-pin plastic mini-DIP or SOIC and is trimmed to operate over an ambient temperature range from +25°C to +100°C. Operation over an extended ambient temperature range is possible with slightly reduced accuracy. The AD596 will amplify thermocouple signals covering the entire –200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate –200°C to +1250°C type K inputs.

The AD596/AD597 has a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C. If higher accuracy, or a lower ambient operating temperature is required, either the AD594 (J thermocouple) or AD595 (K thermocouple) should be considered.

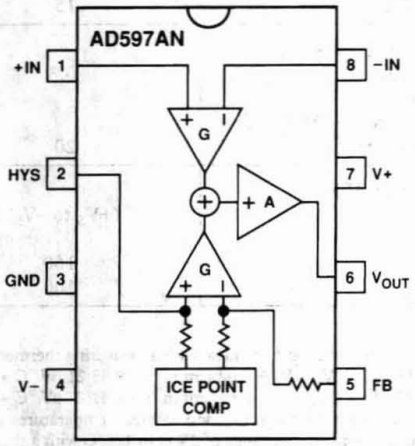
*Protected by U.S. Patent No. 4,029,974.

FUNCTIONAL BLOCK DIAGRAM

TO-100
(H) Package



8-Pin Plastic Mini-DIP (N) Package
or SOIC (R) Package



TOP VIEW

PRODUCT HIGHLIGHTS

1. The AD596/AD597 provides cold junction compensation and a high gain amplifier which can be used as a setpoint comparator.
2. The input stage of the AD596/AD597 is a high quality instrumentation amplifier that allows the thermocouple to float over most of the supply voltage range.
3. Linearization not required for thermocouple temperatures close to 175°C (+100°C to +540°C for AD596).
4. Cold junction compensation is optimized for ambient temperatures ranging from +25°C to +100°C.
5. In the stand-alone mode, the AD596/AD597 produces an output voltage that indicates its own temperature.

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AD596/AD597–SPECIFICATIONS (@ +60°C and V_S = 10 V, Type J (AD596), Type K (AD597) Thermocouple, unless otherwise noted)

Model	AD596AH			AD597AH			AD597AN/AR			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS										
$+V_S$ to $-V_S$			36			36			36	Volts
Common-Mode Input Voltage	$(-V_S - 0.15)$		$+V_S$	$(-V_S - 0.15)$		$+V_S$	$(-V_S - 0.15)$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages										
+ALM	$-V_S$		$(-V_S + 36)$	$-V_S$		$(-V_S + 36)$	$-V_S$		$(-V_S + 36)$	Volts
–ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Tcmperature Range	–55		+125	–55		+125	–40		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT										
(Specified Temperature Range +25°C to +100°C)										
Calibration Error[1]	**–4**		**+4**	**–4**		**+4**	**–4**		**+4**	°C
Stability vs. Temperature[2]		±0.02	±0.05		±0.02	±0.05		±0.02	±0.05	°C/°C
Gain Error	**–1.5**		**+1.5**	**–1.5**		**+1.5**	**–1.5**		**+1.5**	%
Nominal Transfer Function		10			10			10		mV/°C
AMPLIFIER CHARACTERISTICS										
Closed Loop Gain[3]		180.6			245.5			245.5		V/V
Input Offset Voltage		°C × 53.21 + 235			°C × 41.27 – 37			°C × 41.27 – 37		µV
Input Bias Current		0.1			0.1			0.1		µA
Differential Input Range	–10		+50	–10		+50	–10		+50	mV
Common Mode Range	$(-V_S - 0.15)$		$(+V_S - 4)$	$(+V_S - 0.15)$		$(+V_S - 4)$	$(-V_S - 0.15)$		$(+V_S - 4)$	Volts
Common Mode Sensitivity–RTO			**10**			**10**			**10**	mV/V
Power Supply Sensitivity–RTO		1	**10**		1	**10**		1	**10**	mV/V
Output Voltage Range										
Dual Supplies	**$(-V_S + 2.5)$**		**$(+V_S - 2)$**	**$(-V_S + 2.5)$**		**$(+V_S - 2)$**	**$(-V_S + 2.5)$**		**$(+V_S - 2)$**	Volts
Single Supply	**0**		**$(+V_S - 2)$**	**0**		**$(+V_S - 2)$**	**0**		**$(+V_S - 2)$**	Volts
Usable Output Current[4]	±5			±5			±5			mA
3 dB Bandwidth		15			15			15		kHz
ALARM CHARACTERISTICS[5]							Alarm Function Not Pinned Out			
$V_{CE(SAT)}$ at 2 mA		0.3			0.3					Volts
Leakage Current			**±1**			**±1**				µA
Operating Voltage at – ALM			**$(+V_S - 4)$**			**$(+V_S - 4)$**				Volts
Short Circuit Current		20			20					mA
POWER REQUIREMENTS										
Operating		$(+V_S$ to $-V_S) \leq 30$			$(+V_S$ to $-V_S) \leq 30$			$(+V_S$ to $-V_S) \leq 30$		Volts
Quiescent Current										
$+V_S$		160	**300**		160	**300**		160	**300**	µA
$-V_S$		100	**200**		100	**200**		100	**200**	µA

NOTES

[1]This is a measure of the deviation from ideal with a measuring thermocouple junction of 175°C and a chip temperature of 60°C. The ideal transfer function is given by:
AD596: $V_{OUT} = 180.57 \times (V_m - V_a + (\text{ambient in °C}) \times 53.21\ \mu V/°C + 235\ \mu V)$
AD597: $V_{OUT} = 245.46 \times (V_m - V_a + (\text{ambient in °C}) \times 41.27\ \mu V/°C - 37\ \mu V)$
where V_m, and V_a represent the measuring and ambient temperatures and are taken from the appropriate J or K thermocouple table. The ideal transfer function minimizes the error over the ambient temperature range of 25°C to 100°C with a thermocouple temperature of approximately 175°C.

[2]Defined as the slope of the line connecting the AD596/AD597 CJC errors measured at 25°C and 100°C ambient temperature.

[3]Pin 6 shorted to Pin 7.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50 kΩ resistor at output voltages below 2.5 V.

[5]Alarm function available on H package option only.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ORDERING GUIDE

Model	Package Description	Package Option[1]
AD596AH	TO-100	H-10A
AD597AH	TO-100	H-10A
AD597AN[2]	Plastic DIP	N-8
AD597AR[2]	SOIC	R-8

NOTES

[1]For outline information see Package Information section.

[2]Consult factory for availability.

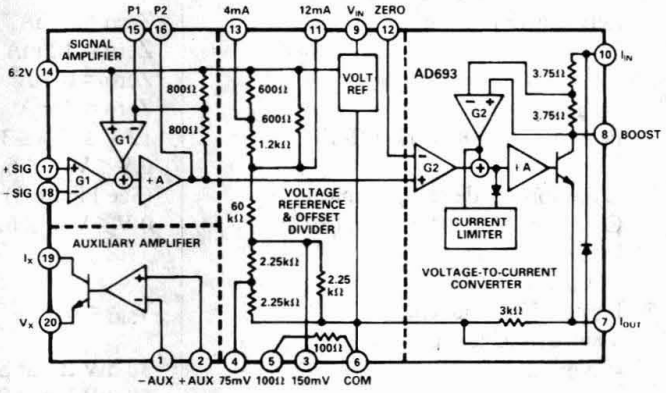
Loop-Powered 4–20 mA Sensor Transmitter

AD693

FEATURES

- **Instrumentation Amplifier Front End**
- **Loop-Powered Operation**
- **Precalibrated 30 mV or 60 mV Input Spans**
- **Independently Adjustable Output Span and Zero**
- **Precalibrated Output Spans: 4–20 mA Unipolar**
  0–20 mA Unipolar
  12 ± 8 mA Bipolar
- **Precalibrated 100 Ω RTD Interface**
- **6.2 V Reference with Up to 3.5 mA of Current Available**
- **Uncommitted Auxiliary Amp for Extra Flexibility**
- **Optional External Pass Transistor to Reduce Self-Heating Errors**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4–20 mA, two-wire current loop. An on-chip voltage reference and auxiliary amplifier are provided for transducer excitation; up to 3.5 mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for three-wire applications when 0–20 mA operation is desired.

Precalibrated 30 mV and 60 mV input spans may be set by simple pin strapping. Other spans from 1 mV to 100 mV may be realized with the addition of external resistors. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100 Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4–20mA, 12 ± 8 mA and 0–20 mA.

Active laser trimming of the AD693's thin-film resistors result in high levels of accuracy without the need for additional adjustments and calibration. Total unadjusted error is tested on every device to be less than 0.5% of full scale at +25°C, and less than 0.75% over the industrial temperature range. Residual nonlinearity is under 0.05%. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

For transmission of low-level signals from RTDs, bridges and pressure transducers, the AD693 offers a cost-effective signal conditioning solution. It is recommended as a replacement for discrete designs in a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in a 20-pin ceramic side-brazed DIP, 20-pin Cerdip, and 20-pin LCCC and is specified over the –40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD693 is a complete monolithic low-level voltage-to-current loop signal conditioner.
2. Precalibrated output zero and span options include 4–20 mA, 0–20 mA, and 12 ± 8 mA in two- and three-wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30 mV and 60 mV input spans.
4. The common-mode range of the signal amplifier input extends from ground to near the device's operating voltage.
5. Provision for transducer excitation includes a 6.2 V reference output and an auxiliary amplifier which may be configured for voltage or current output and signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. A monitored output is provided to drive an external pass transistor. This feature off-loads power dissipation to extend the temperature range of operation, enhance reliability, and minimize self-heating errors.
8. Laser-wafer trimming results in low unadjusted errors and affords precalibrated input and output spans.
9. Zero and span are independently adjustable and noninteractive to accommodate transducers or user defined ranges.
10. Six precalibrated temperature ranges are available with a 100 Ω RTD via pin strapping.

ORDERING GUIDE

Model	Package Description	Package Option*
AD693AD	Ceramic Side-Brazed DIP	D-20
AD693AQ	Cerdip	Q-20
AD693AE	Leadless Ceramic Chip Carrier (LCCC)	E-20A

*For outline information see Package Information section.

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AD693–SPECIFICATIONS

(@ +25°C and V_S = +24 V. Input Span = 30 mV or 60 mV. Output Span = 4–20 mA, R_L = 250 Ω, V_{CM} = 3.1 V, with external pass transistor unless otherwise noted.)

Model	Conditions	AD693AD/AQ/AE Min	Typ	Max	Units
LOOP-POWERED OPERATION					
TOTAL UNADJUSTED ERROR[1, 2]			±0.25	**±0.5**	% Full Scale
T_{MIN} to T_{MAX}			±0.4	**±0.75**	% Full Scale
100 Ω RTD CALIBRATION ERROR[3]	(See Figure 17)		±0.5	±2.0	°C
LOOP POWERED OPERATION[2]					
Zero Current Error[4]	Zero = 4 mA		±25	**±80**	µA
	Zero = 12 mA		±40	**±120**	µA
	Zero = 0 mA[5]	**+7**	+35	**+100**	µA
vs. Temp.	Zero = 4 mA		±0.5	±1.5	µA/°C
Power Supply Rejection (RTI)	12 V ≤ V_{OP} ≤ 36 V[6]		±3.0	**±5.6**	µV/V
	0 V ≤ V_{CM} ≤ 6.2 V				
Common-Mode Input Range	(See Figure 3)	0		+V_{OP} – 4 V[6]	V
Common-Mode Rejection (RTI)	0 V ≤ V_{CM} ≤ 6.2 V		±10	**±30**	µV/V
Input Bias Current[7]			**+5**	**+20**	nA
T_{MIN} to T_{MAX}			**+7**	**+25**	nA
Input Offset Current[7]	V_{SIG} = 0		±0.5	**±3.0**	nA
Transconductance					
Nominal	30 mV Input Span		0.5333		A/V
	60 mV Input Span		0.2666		A/V
Unadjusted Error			±0.05	**±0.2**	%
vs. Common-Mode	0 V ≤ V_{CM} ≤ 6.2 V				
	30 mV Input Span		±0.03	±0.04	%/V
	60 mV Input Span		±0.05	±0.06	%/V
Error vs. Temp.			±20	±50	ppm/°C
Nonlinearity[8]	30 mV Input Span		±0.01	**±0.05**	% of Span
	60 mV Input Span		±0.02	**±0.07**	% of Span
OPERATIONAL VOLTAGE RANGE					
Operational Voltage, V_{OP}[6]		**+12**		**+36**	V
Quiescent Current	Into Pin 9		+500	**+700**	µA
OUTPUT CURRENT LIMIT		**+21**	+25	**+32**	mA
COMPONENTS OF ERROR					
SIGNAL AMPLIFIER[9]					
Input Voltage Offset			±40	**±200**	µV
vs. Temp			±1.0	±2.5	µV/°C
Power Supply Rejection	12 V ≤ V_{OP} ≤ 36 V[6]		±3.0	**±5.6**	µV/V
	0 V ≤ V_{CM} ≤ 6.2 V				
V/I CONVERTER[9, 10]					
Zero Current Error	Output Span = 4–20 mA		±30	±80	µA
Power Supply Rejection	12 V ≤ V_{OP} ≤ 36 V[6]		±1.0	±3.0	µA/V
Transconductance					
Nominal			0.2666		A/V
Unadjusted Error			±0.05	±0.2	%
6.200 V REFERENCE[9, 12]					
Output Voltage Tolerance			±3	**±12**	mV
vs. Temp.			±20	±50	ppm/°C
Line Regulation	12 V ≤ V_{OP} ≤ 36 V[6]		±200	**±300**	µV/V
Load Regulation[11]	0 mA ≤ I_{REF} ≤ 3 mA		±0.3	**±0.75**	mV/mA
Output Current[13]	Loop Powered, (Figure 10)	**+3.0**	+3.5		mA
	3-Wire Mode, (Figure 15)		+5.0		mA
AUXILIARY AMPLIFIER					
Output Current Range	Pin I_X OUT	+0.01		+5	mA
Output Current Error	Pin V_X – Pin I_X		±0.005		%
TEMPERATURE RANGE					
Case Operating[14]	T_{MIN} to T_{MAX}	–40		+85	°C
Storage		–65		+150	°C

Specifications subject tochange without notice.

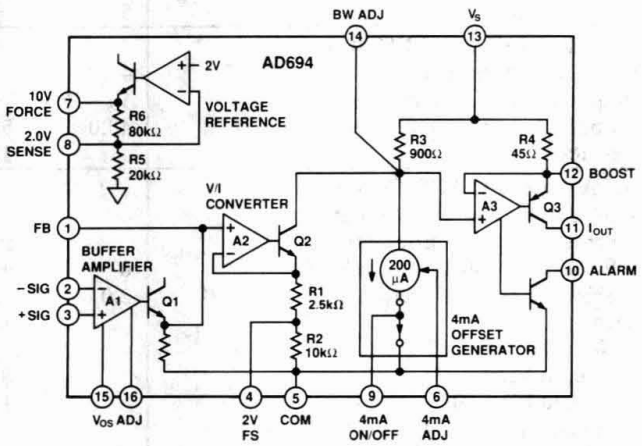
4–20 mA Transmitter

AD694*

FEATURES

4–20 mA, 0–20 mA Output Ranges
Precalibrated Input Ranges:
0 V to 2 V, 0 V to 10 V
Precision Voltage Reference
Programmable to 2.000 V or 10.000 V
Single or Dual Supply Operation
Wide Power Supply Range: +4.5 V to +36 V
Wide Output Compliance
Input Buffer Amplifier
Open-Loop Alarm
Optional External Pass Transistor to Reduce Self-Heating Errors
0.002% typ Nonlinearity

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD694 is a monolithic current transmitter that accepts high level signal inputs to drive a standard 4–20 mA current loop for the control of valves, actuators, and other devices commonly used in process control. The input signal is buffered by an input amplifier that can be used to scale the input signal or buffer the output from a current mode DAC. Precalibrated input spans of 0 V to 2 V and 0 V to 10 V are selected by simple pin strapping; other spans may be programmed with external resistor.

The output stage compliance extends to within 2 V of V_S and its special design allows the output voltage to extend below common in dual supply operation. An alarm warns of an open 4-to-20 mA loop or noncompliance of the output stage.

Active laser trimming of the AD694's thin film resistors results in high levels of accuracy without the need for additional adjustments and calibration. An external pass transistor may be used with the AD694 to off-load power dissipation, extending the temperature range of operation.

The AD694 is the ideal building block for systems requiring noise immune 4–20 mA signal transmission to operate valves, actuators, and other control devices, as well as for the transmission of process parameters such as pressure, temperature, or flow. It is recommended as a replacement for discrete designs in a variety of applications in industrial process control, factory automation, and system monitoring.

The AD694 is available in hermetically sealed, 16-pin cerdip and plastic SOIC, specified over the –40°C to +85°C industrial temperature range, and in a 16-pin plastic DIP, specified over the 0°C to +70°C temperature range.

***Protected by U.S. Patents: 30,586; 4,250,445; 4,857,862.**

PRODUCT HIGHLIGHTS

1. The AD694 is a complete voltage in to 4–20 mA out current transmitter.
2. Pin programmable input ranges are pre-calibrated at 0 V to 2 V and 0 V to 10 V.
3. The input amplifier may be configured to buffer and scale the input voltage, or to serve as an output amplifier for current output DACs.
4. The output voltage compliance extends to within 2 V of the positive supply and below common. When operated with a 5 V supply, the output voltage compliance extends 30 V below common.
5. The AD694 interfaces directly to 8-, 10-, and 12-bit single supply CMOS and bipolar DACs.
6. The 4 mA zero current may be switched on and off with a TTL control pin, allowing 0–20 mA operation.
7. An open collector alarm warns of loop failure due to open wires or noncompliance of the output stage.
8. A monitored output is provided to drive an external pass transistor. The feature off-loads power dissipation to extend the temperature range of operation and minimize self-heating error.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD694JN	0°C to +70°C	N-16
AD694AQ	–40°C to +85°C	Q-16
AD694AR	–40°C to +85°C	R-16
AD694BQ	–40°C to +85°C	Q-16
AD694BR	–40°C to +85°C	R-16

*N = Plastic DIP; Q = Cerdip, R = SOIC. For outline information see Package Information section.

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AD694—SPECIFICATIONS (@ +25°C, R_L = 250 Ω and V_S = +24 V, unless otherwise noted)

Model	AD694JN/AQ/AR			AD694BQ/BR			Units
	Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS							
Input Voltage Range	–0.2	V_S – 2.0 V	V_S – 2.5 V	–0.2	V_S – 2.0 V	**V_S – 2.5 V**	V
Input Bias Current							
Either Input, T_{MIN} to T_{MAX}		1.5	**5**		1.5	**5**	nA
Offset Current, T_{MIN} to T_{MAX}		±0.1	**±1**		±0.1	**±1**	nA
Offset Current Drift		±1.0	±5.0		±1.0	±5.0	pA/°C
Input Impedance	5			5			MΩ
OUTPUT CHARACTERISTICS							
Specified Performance	4		20	4		20	mA
Output Voltage Compliance	**V_S – 36 V**		**V_S – 2 V**	**V_S – 36 V**		**V_S – 2 V**	V
Output Impedance, 4–20 mA	40.0	50.0		40.0	50.0		MΩ
Slew Rate		1.3			1.3		mA/μs
SPAN AND ZERO ACCURACY[1]							
4 mA Offset Error @ 0 V Input[2]							
Error from 4.000 mA, 4 mA On		±10	**±20**		±5	**±10**	μA
Error from 0.000 mA, 4 mA Off	0	+10	**+20**	0	+5	**+10**	μA
Trim Range, 4 mA Zero	2.0		4.8	2.0		4.8	mA
Span							
Nominal Transfer Function							
Input FS = 2 V		8.0			8.0		mA/V
Input FS = 10 V		1.6			1.6		mA/V
Transfer Function Error from Nom,							
Input FS = 2 V, 10 V		±0.1	**±0.3**		±0.05	**±0.15**	% of Span
Nonlinearity[3]		±0.005	**±0.015**		±0.001	**±0.005**	% of Span
VOLTAGE REFERENCE							
Output Voltage: 10 V Reference	**9.960**	10.000	**10.040**	**9.980**	10.000	**10.020**	V
Output Voltage: 2 V Reference	**1.992**	2.000	**2.008**	**1.996**	2.000	**2.004**	V
ALARM CHARACTERISTICS							
$V_{CE(SAT)}$ @ 2.5 mA		0.35			0.35		V
Leakage Current			**±1**			**±1**	μA
Alarm Pin Current (Pin 10)		20			20		mA
POWER REQUIREMENTS							
Specified Performance		24			24		V
Operating Range							
2 V FS, V_{REF} = 2 V	**4.5**		**36**	**4.5**		**36**	V
2 V, 10 V FS, V_{REF} = 2 V, 10 V	**12.5**		**36**	**12.5**		**36**	V
Quiescent Current, 4 mA Off		1.5	**2.0**		1.5	**2.0**	mA
TEMPERATURE RANGE							
Specified Performance[4] AD694AQ/BQ/AR/BR	–40		+85	–40		+85	°C
AD694JN	0		+70	0		+70	°C
Operating AD694AQ/BQ/AR/BR	–55		+125	–55		+125	°C
AD694JN	–40		+85	–40		+85	°C
BUFFER AMPLIFIER[5]							
Input Offset Voltage							
Initial Offset		±150	**±500**		±50	**±500**	μV
Trim Range	**±2.5**	±4.0		**±2.5**	±4.0		mV
Frequency Response							
Unity Gain, Small Signal		300			300		kHz
Open-Loop Gain							
V_O = +10 V, $R_L \geq$ 10 kΩ		50			50		V/mV
Output Voltage @ Pin 1, FB[1]							
Minimum Output Voltage		1.0	10		1.0	10	mV
Maximum Output Voltage	V_S – 2.5 V	V_S – 2 V		V_S – 2.5 V	V_S – 2 V		V

NOTES

[1]The single supply op amps of the AD694, lacking pull down current, may not reach 0.000 V at their outputs. For this reason, span, offset, and nonlinearity are specified with the input amplifiers operating in their linear range. The input voltage used for the tests is 5 mV to 2 V and 5 mV to 10 V for the two precalibrated input ranges. Span and zero accuracy are tested with the buffer amplifier configured as a follower.

[2]Offset at 4 mA out and 0 mA out are extrapolated to 0.000 V input from measurements made at 5 mV and at full scale. See Note 1.

[3]Nonlinearity is specified as the maximum deviation of the output, as a % of span, from a straight line drawn through the endpoints of the transfer function.

[4]Devices tested at these temperatures with a pass transistor. Allowable temperature range of operation is dependent upon internal power dissipation. Absolute maximum junction and case temperature should not be exceeded. See section: "Power Dissipation Considerations."

[5]Buffer amplifier specs for reference. Buffer amplifier offset and drift already included in Span and Zero accuracy specs above.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

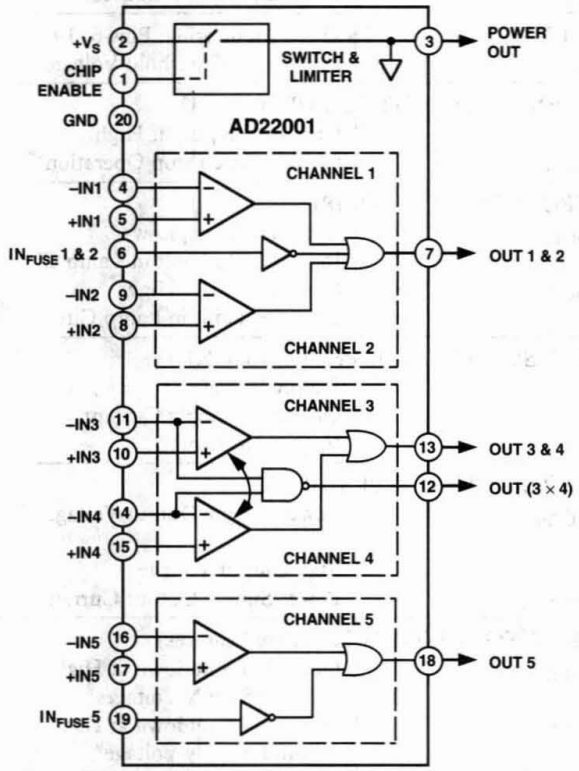
5-Channel Monolithic Comparator for Lamp Monitoring

AD22001*

FEATURES

- Continuous Status Checks of Five Bulbs
- Lamp Status Check in "ON" and "OFF" States
- Status Checks of Two In-Line Fuses
- Very Low Voltage Drop at Sensor Shunt Resistor (Comparator Threshold 1.75 mV at 22°C)
- Temperature and Supply Voltage Compensated
- Powered Directly from Car Battery: Protection Included for Transient, Reverse Supply, Load Dump
- Operating Temperature Range: –40°C to +125°C
- 15 V CMOS Compatible Digital Output Signals
- Voltage Limited Power Supply Output for 15 V CMOS Logic ICs

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD22001 is a monolithic, five-channel comparator circuit for monitoring the functionality of lamps in automotive applications.

The IC tests the series circuit leading to the lamp to determine if the circuit is intact and a functional lamp is in the socket. The AD22001 continuously checks the functionality of up to five bulbs in either their "on" or "off" state, and also tests for the presence of an in-line fuse in two of the series circuits.

Digital outputs indicate the status of each channel. Additionally, the AD22001 provides a voltage limited power supply output to supply 15 V CMOS circuits that may interface to the AD22001.

*Patents pending.

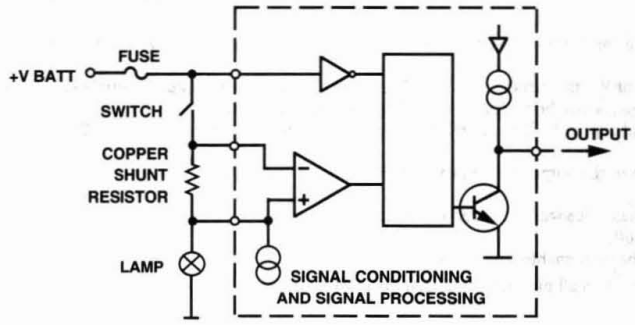
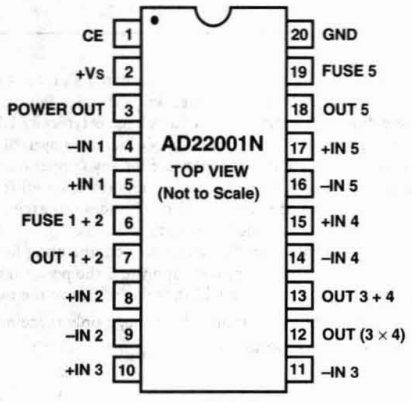


Figure 1. Typical Application Circuit for a Single Channel Lamp Monitor

CONNECTION DIAGRAM



ORDERING GUIDE

Model	Temperature Range	Package Option*
AD22001	–40°C to +125°C	N-20

*N = Plastic DIP Package. For outline information see Package Information section.

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AD22001–SPECIFICATIONS (T_A = +22°C, V_S = +13.5 V unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Units
DIFFERENTIAL INPUTS (Voltage Drop from Shunt Resistor: Pins 4 & 5, 8 & 9, 10 & 11, 14 & 15, 16 & 17)						
V_{INDIFF}	Comparator Threshold Voltage[1]		**1.5**	1.75	**2.0**	mV
V_{INCM}	Common-Mode Threshold Voltage[1]		**5**			V
	Power Supply Sensitivity of V_{INDIFF}[2]	9 V ≤ V_S ≤ 16 V		50		%
	Temperature Compensation of V_{INDIFF}[3]			3770		ppm/°C
I_{INB}	Input Bias Current			10		µA
I_{INC}	Constant Current Source[4]		30	60		µA
SINGLE-ENDED INPUTS (Fuse Monitoring: Pins 6, 19)						
V_{INF}	Fuse Input Threshold Voltage[5]				**4**	V
CHIP ENABLE CONTROL INPUT (Pin 1)						
V_{INCE}	Chip Enable, Input High		**9**			V
V_{INCD}	Chip Disable (Stop Operation)[6]				**6**	V
OUTPUTS (Pins 7, 12, 13, 18)						
V_{OUTL}	Output Voltage, Low Indicates No Fault in Lamp Circuit	Load = 500 µA			**0.6**	V
V_{OUTH}	Output Voltage, High Indicates Fault in Lamp Circuit	9 V ≤ V_S ≤ V_{SSDH} Load = 50 µA	**V_{OUTPS} – 2.5**		**V_{OUTPS}**	V
POWER SUPPLY (Pin 2: +V_S, Pin 20: GND)						
V_S	Supply Voltage		**9**		**30**	V
I_S	Quiescent Supply Current	Pin 1 High	**1**	3	**5**	mA
	V_{OUTH}: No Load	Pin 1 Low		100		µA
POWER SUPPLY OUTPUT (Pin 3)						
V_{OUTPS}	Power Supply Output Voltage	10 V < V_S < 14.5 V I_{OUTPS} ≤ 1 mA	**V_S – 0.5**	V_S – 0.3	**V_S**	V
	Max Output Voltage			16	**18**	V
I_{OUTPS}	Power Supply Output Current[7]		2			mA
OPERATING SHUTDOWN (Safety Features)						
V_{SSDH}	Operation Shutdown at High Power Supply Voltages[8]		**30**	33	**36**	V
V_{SSDL}	Operation Shutdown at Low Power Supply Voltage[9]		**7**		**9**	V
TEMPERATURE RANGE						
T_A	Operating Temperature Range		–40		+125	°C
PACKAGE						
	Plastic DIP (N-20)			AD22001N		

NOTES

[1]In the presence of a common-mode voltage greater than 5 V, if the shunt voltage applied to the comparator does not exceed the threshold (i.e., the bulb is switched on but does not draw current), then the device will indicate a failure.

[2]At V_S = 13.5 V, the differential input threshold voltage is typically 1.75 mV. With an increase of V_S, the threshold voltage, V_{INDIFF}, will change as well. Power supply sensitivity of 50% means that when the power supply voltage V_S increases by 10%, the threshold voltage V_{INDIFF} will be increased by half of this percentage value: 5%.

[3]This is the temperature coefficient to compensate for any temperature influence on the external copper PCB track shunt resistors. 3770 ppm/°C is equal to 6.6 µV/°C.

[4]This current source is used to test the lamp when it is switched off (cold lamp test).

[5]If the voltage at the input from the fuse (Pin 6 or 19) does not exceed the threshold voltage, then the output will indicate a failure.

[6]When the Chip Enable is open-circuited, the chip is disabled.

[7]Shorting V_{OUTPS} to ground will cause the device to stop operating for that period. However, the device will not suffer any damage.

[8]At this voltage, or above, the internal power supply and the power output V_{OUTPS} will be shut off.

[9]Below the minimum voltage, the circuit will shut down. Above the maximum, the circuit will be on if enabled.

All min and max specifications are guaranteed, although only those marked in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Forward Supply Voltage . . . . . +36 V
Reversed Supply Voltage . . . . . –34 V
Forward Transient (40 ms) . . . . . +60 V
Reverse Transient (40 ms) . . . . . –40 V
Voltage on Any Input Pin Relative to GND . . . –34 V to +36 V
Power Dissipation (V_S = 13.5 V) . . . . . 300 mW
Operating Temperature (Ambient) . . . . . –40°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Voltage Output Temperature Sensor with Signal Conditioning

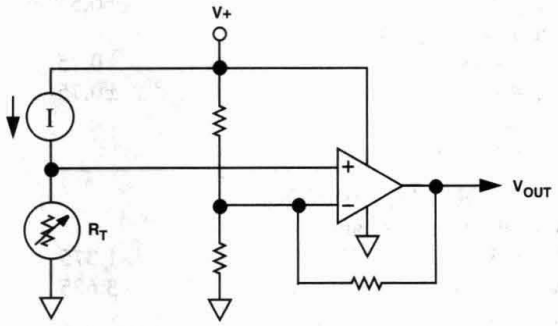
AD22100*

FEATURES
200°C Temperature Span
Accuracy Better than ±2% of Full Scale
Linearity Better than ±1% of Full Scale
Temperature Coefficient of 22.5 mV/°C
Output Proportional to Temperature × V+
Single Supply Operation
Reverse Voltage Protection
Minimal Self-Heating
High Level, Low Impedance Output

APPLICATIONS
HVAC Systems
System Temperature Compensation
Board Level Temperature Sensing
Electronic Thermostats

MARKETS
Industrial Process Control
Instrumentation
Automotive

SIMPLIFIED BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD22100 is a monolithic temperature sensor with on-chip signal conditioning. It can be operated over the temperature range –50°C to +150°C, making it ideal for use in numerous HVAC, instrumentation and automotive applications.

The signal conditioning eliminates the need for any trimming, buffering or linearization circuitry, greatly simplifying the system design and reducing the overall system cost.

The output voltage is proportional to the temperature times the supply voltage (ratiometric). The output swings from 0.25 V at –50°C to +4.75 V at +150°C using a single +5.0 V supply.

Due to its ratiometric nature, the AD22100 offers a cost effective solution when interfacing to an analog-to-digital converter. This is accomplished by using the ADC's +5 V power supply as a reference to both the ADC and the AD22100 (see Figure 1), eliminating the need for and cost of a precision reference.

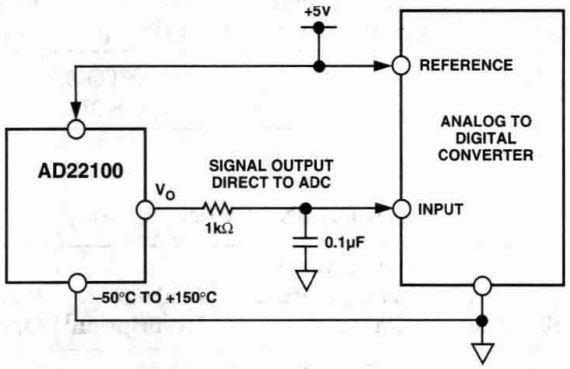


Figure 1. Application Circuit

*Protected by U.S. Patent Nos. 5030849 and 5243319.

AD22100–SPECIFICATIONS (T_A = +25°C and V+ = +4 V to +6 V unless otherwise noted)

Parameter	AD22100K Min	AD22100K Typ	AD22100K Max	AD22100A Min	AD22100A Typ	AD22100A Max	AD22100S Min	AD22100S Typ	AD22100S Max	Units
TRANSFER FUNCTION	V_{OUT} = (V+/5 V) × [1.375 V + (22.5 mV/°C) × T_A]									V
TEMPERATURE COEFFICIENT	(V+/5 V) × 22.5									mV/°C
TOTAL ERROR										
Initial Error										
T_A = +25°C		±0.5	±2.0		±1.0	±2.0		±1.0	±2.0	°C
Error over Temperature										
$T_A = T_{MIN}$		±0.75	±2.0		±2.0	±3.7		±3.0	±4.0	°C
$T_A = T_{MAX}$		±0.75	±2.0		±2.0	±3.0		±3.0	±4.0	°C
Nonlinearity										
$T_A = T_{MIN}$ to T_{MAX}			0.5			0.5			1.0	% FS[1]
OUTPUT CHARACTERISTICS										
Nominal Output Voltage										
V+ = 5.0 V, T_A = 0°C		1.375								V
V+ = 5.0 V, T_A = +100°C		3.625								V
V+ = 5.0 V, T_A = –40°C					0.475					V
V+ = 5.0 V, T_A = +85°C					3.288					V
V+ = 5.0 V, T_A = –50°C								0.250		V
V+ = 5.0 V, T_A = +150°C								4.750		V
POWER SUPPLY										
Operating Voltage	+4.0	+5.0	+6.0	+4.0	+5.0	+6.0	+4.0	+5.0	+6.0	V
Quiescent Current		500	650		500	650		500	650	µA
TEMPERATURE RANGE										
Guaranteed Temperature Range	0		+100	–40		+85	–50		+150	°C
Operating Temperature Range	–50		+150	–50		+150	–50		+150	°C
PACKAGE		TO-92 SOIC			TO-92 SOIC			TO-92 SOIC		

Specifications subject to change without notice.

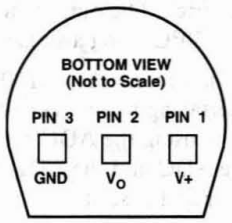
ORDERING GUIDE

Model/Grade	Guaranteed Temperature Range	Package Description[1]	Package Option[2]
AD22100KT	0°C to 100°C	TO-92	TO-92
AD22100KR	0°C to 100°C	SOIC	SO-8
AD22100AT	–40°C to +85°C	TO-92	TO-92
AD22100AR	–40°C to +85°C	SOIC	SO-8
AD22100ST	–50°C to +150°C	TO-92	TO-92
AD22100SR	–50°C to +150°C	SOIC	SO-8
AD22100KCHIPS	+25°C	N/A	N/A

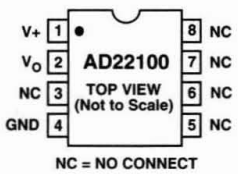
NOTES
[1]Minimum purchase quantities of 100 pieces for all chip orders.
[2]For outline information see Package Information section.

PIN CONFIGURATIONS

TO-92



SOIC



3.3 V Supply, Voltage Output Temperature Sensor with Signal Conditioning

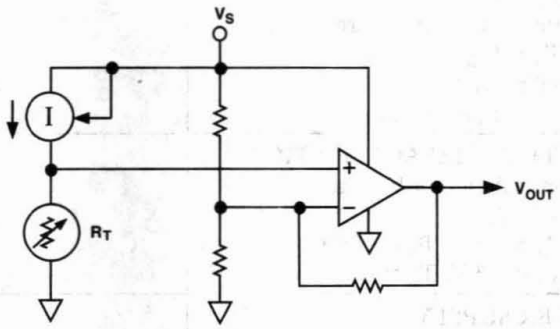
AD22103*

FEATURES
3.3 V, Single Supply Operation
Temperature Coefficient of 28 mV/°C
100°C Temperature Span (0°C to +100°C)
Accuracy Better Than 2.5% of Full Scale
Linearity Better Than 0.5% of Full Scale
Output Proportional to Temperature × V_S
Minimal Self-Heating
High Level, Low Impedance Output
Reverse Supply Protected

APPLICATIONS
Microprocessor Thermal Management
Battery and Low Powered Systems
Power Supply Temperature Monitoring
System Temperature Compensation
Board Level Temperature Sensing

MARKETS
Computers
Portable Electronic Equipment
Industrial Process Control
Instrumentation

SIMPLIFIED BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD22103 is a monolithic temperature sensor with on-chip signal conditioning. It can be operated over the temperature range 0°C to +100°C, making it ideal for use in numerous 3.3 V applications.

The signal conditioning eliminates the need for any trimming, buffering or linearization circuitry, greatly simplifying the system design and reducing the overall system cost.

The output voltage is proportional to the temperature times the supply voltage (ratiometric). The output swings from 0.25 V at 0°C to +3.05 V at +100°C using a single +3.3 V supply.

Due to its ratiometric nature, the AD22103 offers a cost effective solution when interfacing to an analog-to-digital converter. This is accomplished by using the ADC's power supply as a reference to both the ADC and the AD22103 (see Figure 1), eliminating the need for and cost of a precision reference.

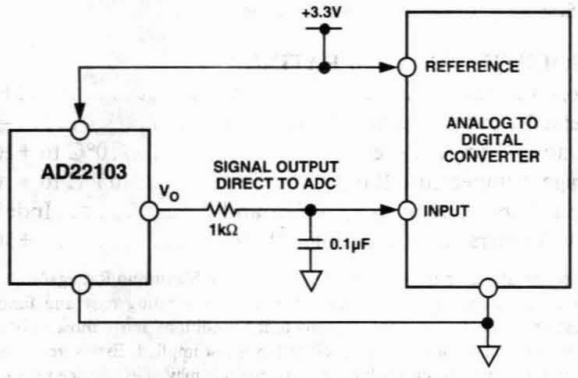


Figure 1. Application Circuit

*Protected by U.S. Patent Nos. 5030849 and 5243319.

AD22103–SPECIFICATIONS (T_A = +25°C and V_S = +2.7 V to +3.6 V unless otherwise noted)

Parameter	AD22103K Min	Typ	Max	Units
TRANSFER FUNCTION	$V_{OUT} = (V_S/3.3\ V) \times [0.25\ V + (28\ mV/°C) \times T_A]$			V
TEMPERATURE COEFFICIENT	$(V_S/3.3\ V) \times 28$			mV/°C
TOTAL ERROR				
Initial Error				
T_A = +25°C		±0.5	±2.0	°C
Error over Temperature				
$T_A = T_{MIN}$ to T_{MAX}		±0.75	±2.5	°C
Nonlinearity				
$T_A = T_{MIN}$ to T_{MAX}		0.1	0.5	% FS[1]
OUTPUT CHARACTERISTICS				
Nominal Output Voltage				
V_S = 3.3 V, T_A = 0°C		0.25		V
V_S = 3.3 V, T_A = +25°C		0.95		V
V_S = 3.3 V, T_A = +100°C		3.05		V
POWER SUPPLY				
Operating Voltage	+2.7	+3.3	+3.6	V
Quiescent Current	350	500	600	µA
TEMPERATURE RANGE				
Guaranteed Temperature Range	0		+100	°C
Operating Temperature Range	0		+100	°C
PACKAGE		TO-92 SOIC		

NOTES

[1]FS (Full Scale) is defined as that of the operating temperature range, 0°C to +100°C. The listed max specification limit applies to the guaranteed temperature range. For example, the AD22103K has a nonlinearity of (0.5%) × (100°C) = 0.5°C over the guaranteed temperature range of 0°C to +100°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . +10 V
Reversed Continuous Supply Voltage . . . . . –10 V
Operating Temperature . . . . . 0°C to +100°C
Storage Temperature Range . . . . . –65°C to +160°C
Output Short Circuit to V_S or Ground . . . . . Indefinite
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model /Grade	Guaranteed Temperature Range	Package Description	Package Option[1]
AD22103KT	0°C to +100°C	TO-92	TO-92
AD22103KR	0°C to +100°C	SOIC	SO-8
AD22103KCHIPS[2]	+25°C	N/A	N/A

NOTES

[1]For outline information see Package Information section.

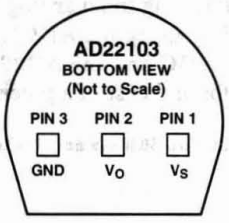
[2]Minimum purchase quantities of 100 pieces for all chip orders.

PIN DESCRIPTION

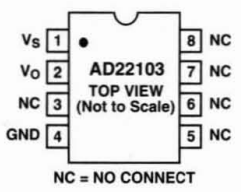
Mnemonic	Function
V_S	Power Supply Input
V_O	Device Output
GND	Ground Pin Must Be Connected to 0 V
NC	No Connect

PIN CONFIGURATIONS

TO-92



SOIC



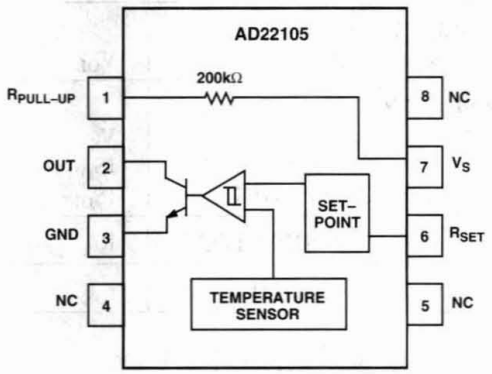
Low Voltage, Resistor Programmable Thermostatic Switch

AD22105

FEATURES
- User-Programmable Temperature Setpoint
- 2.0°C Setpoint Accuracy
- 4.0°C Preset Hysteresis
- Wide Supply Range (+2.7 V dc to +7.0 V dc)
- Wide Temperature Range (–40°C to +150°C)
- Low Power Dissipation (230 μW @ 3.3 V)

APPLICATIONS
- Industrial Process Control
- Thermal Control Systems
- CPU Monitoring (i.e., Pentium)
- Computer Thermal Management Circuits
- Fan Control
- Handheld/Portable Electronic Equipment

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD22105 is a solid state thermostatic switch. Requiring only one external programming resistor, the AD22105 can be set to switch accurately at any temperature in the wide operating range of –40°C to +150°C. Using a novel circuit architecture, the AD22105 asserts an open collector output when the ambient temperature exceeds the user-programmed setpoint temperature. The AD22105 has approximately 4°C of hysteresis which prevents rapid thermal on/off cycling.

The AD22105 is designed to operate on a single power supply voltage from +2.7 V to +7.0 V facilitating operation in battery powered applications as well as in industrial control systems. Because of low power dissipation (230 μW @ 3.3 V), self-heating errors are minimized and battery life is maximized.

An optional internal 200 kΩ pull-up resistor is included to facilitate driving light loads such as CMOS inputs.

Alternatively, a low power LED indicator may be driven directly.

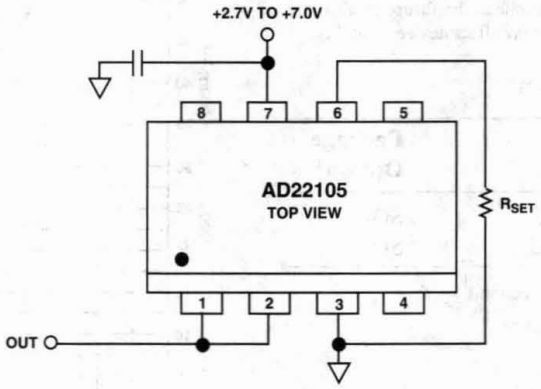

Figure 1. Typical Application Circuit

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AD22105–SPECIFICATIONS (V_S = 3.3 V, T_A = +25°C, R_{LOAD} = internal 200 kΩ, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TEMPERATURE ACCURACY						
Ambient Setpoint Accuracy	ACC			±0.5	±2.0	°C
Temperature Setpoint Accuracy	ACC_T	–40°C ≤ T_A ≤ +125°C			±3.0	°C
Power Supply Rejection	PSR	+2.7 V[1] < V_S < +7.0 V		±0.05	±0.15	°C/V
HYSTERESIS						
Hysteresis Value	HYS			4.1		°C
OPEN COLLECTOR OUTPUT						
Output Low Voltage	V_{OL}	I_{SINK} = 5 mA		250	400	mV
POWER SUPPLY						
Supply Range	V_S		+2.7		+7.0	V
Supply Current, Output "LOW"	IS_{ON}				120	µA
Supply Current, Output "HIGH"	IS_{OFF}				90	µA
INTERNAL PULL-UP RESISTOR	$R_{PULL-UP}$		140	200	260	kΩ
TURN-ON SETTLING TIME	t_{ON}			5		µs

NOTES
[1]The AD22105 will operate at voltages as low as +2.2 V.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Maximum Supply Voltage . . . . . +11 V
Maximum Output Voltage (Pin 2) . . . . . +11 V
Maximum Output Current (Pin 2) . . . . . 10 mA
Operating Temperature Range . . . . . –50°C to +150°C
Dice Junction Temperature . . . . . +160°C
Storage Temperature Range . . . . . –65°C to +160°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Package Description	Package Option*
AD22105AR	8-Lead SOIC	SO-8
AD22105AR-REEL7	8-Lead SOIC	SO-8

*For outline information see Package Information section.

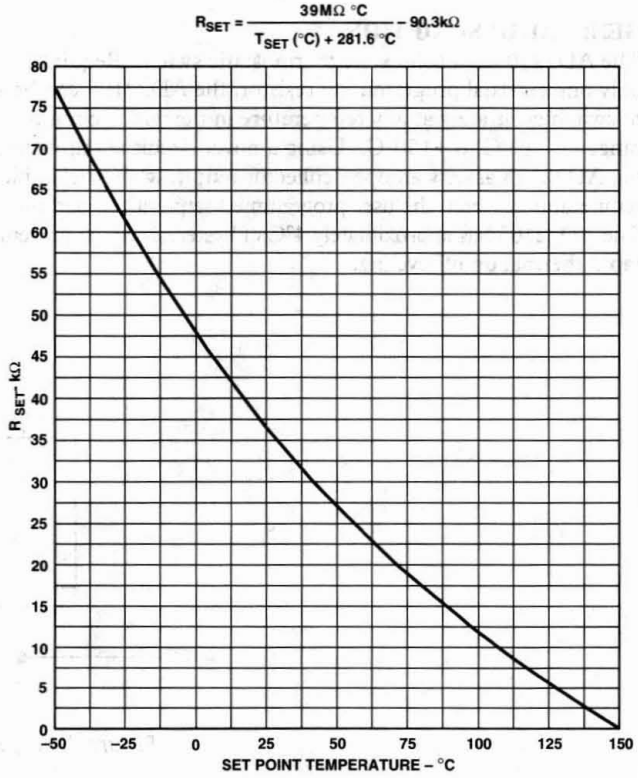


Figure 2. Setpoint Resistor Values

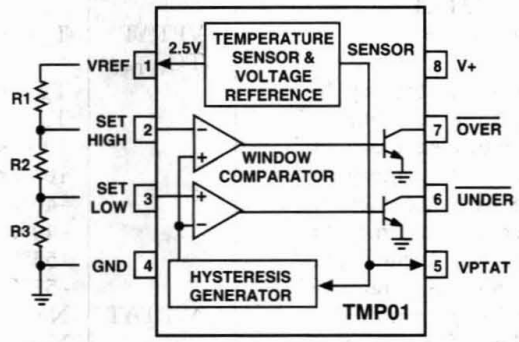
Low Power, Programmable Temperature Controller

TMP01*

FEATURES
–55°C to +125°C (–67°F to +257°F) Operation
±1.0°C Accuracy Over Temperature (typ)
Temperature-Proportional Voltage Output
User Programmable Temperature Trip Points
User Programmable Hysteresis
20 mA Open Collector Trip Point Outputs
TTL/CMOS Compatible
Single-Supply Operation (4.5 V to 13.2 V)
Low Cost 8-Pin DIP and SO Packages

APPLICATIONS
Over/Under Temperature Sensor and Alarm
Board Level Temperature Sensing
Temperature Controllers
Electronic Thermostats
Thermal Protection
HVAC Systems
Industrial Process Control
Remote Sensors

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The TMP01 is a temperature sensor which generates a voltage output proportional to absolute temperature and a control signal from one of two outputs when the device is either above or below a specific temperature range. Both the high/low temperature trip points and hysteresis (overshoot) band are determined by user-selected external resistors. For high volume production, these resistors are available on-board.

The TMP01 consists of a bandgap voltage reference combined with a pair of matched comparators. The reference provides both a constant 2.5 V output and a voltage proportional to absolute temperature (VPTAT) which has a precise temperature coefficient of 5 mV/K and is 1.49 V (nominal) at +25°C. The comparators compare VPTAT with the externally set temperature trip points and generate an open-collector output signal when one of their respective thresholds has been exceeded.

Hysteresis is also programmed by the external resistor chain and is determined by the total current drawn out of the 2.5 V reference. This current is mirrored and used to generate a hysteresis offset voltage of the appropriate polarity after a comparator has been tripped. The comparators are connected in parallel, which guarantees that there is no hysteresis overlap and eliminates erratic transitions between adjacent trip zones.

***Protected by U.S. Patent No. 5,195,827.**

The TMP01 utilizes proprietary thin-film resistors in conjunction with production laser trimming to maintain a temperature accuracy of ±1°C (typ) over the rated temperature range, with excellent linearity. The open-collector outputs are capable of sinking 20 mA, enabling the TMP01 to drive control relays directly. Operating from a +5 V supply, quiescent current is only 500 µA (max).

The TMP01 is available in the low cost 8-pin epoxy mini-DIP and SO (small outline) packages, and in die form.

ORDERING GUIDE

Model/Grade	Temperature Range[1]	Package Description	Package Option[2]
TMP01EP	XIND	Plastic DIP	N-8
TMP01FP	XIND	Plastic DIP	N-8
TMP01ES	XIND	SOIC	SO-8
TMP01FS	XIND	SOIC	SO-8
TMP01FJ[3]	XIND	TO-99 Can	H-08A
TMP01GBC	+25°C	Die	

NOTES
[1]XIND = –40°C to +85°C.
[2]For outline information see Package Information section.
[3]Consult factory for availability of MIL/883 version in TO-99 can.

TMP01EP/FP, TMP01ES/FS–SPECIFICATIONS Plastic DIP and Surface Mount Packages

(V+ = +5 V, GND = 0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUTS SET HIGH, SET LOW						
Offset Voltage	V_{OS}			0.25		mV
Offset Voltage Drift	TCV_{OS}			3		µV/°C
Input Bias Current, "E"	I_B			25	50	nA
Input Bias Current, "F"	I_B			25	100	nA
OUTPUT VPTAT[1]						
Output Voltage	VPTAT	T_A = +25°C, No Load		1.49		V
Scale Factor	TC_{VPTAT}			5		mV/K
Temperature Accuracy, "E"		T_A = +25°C, No Load	–1.5	±0.5	1.5	°C
Temperature Accuracy, "F"		T_A = +25°C, No Load	–3	±1.0	3	°C
Temperature Accuracy, "E"		10°C < T_A < 40°C, No Load		±0.75		°C
Temperature Accuracy, "F"		10°C < T_A < 40°C, No Load		±1.5		°C
Temperature Accuracy, "E"		–40°C < T_A < 85°C, No Load	–3.0	±1	3.0	°C
Temperature Accuracy, "F"		–40°C < T_A < 85°C, No Load	–5.0	±2	5.0	°C
Temperature Accuracy, "E"		–55°C < T_A < 125°C, No Load		±1.5		°C
Temperature Accuracy, "F"		–55°C < T_A < 125°C, No Load		±2.5		°C
Repeatability Error	ΔVPTAT	Note 4		0.25		Degree
Long Term Drift Error		Notes 2 and 6		0.25	0.5	Degree
Power Supply Rejection Ratio	PSRR	T_A = +25°C, 4.5 V ≤ V+ ≤ 13.2 V		±0.02	±0.1	%/V
OUTPUT VREF						
Output Voltage, "E"	VREF	T_A = +25°C, No Load	2.495	2.500	2.505	V
Output Voltage, "F"	VREF	T_A = +25°C, No Load	2.490	2.500	2.510	V
Output Voltage, "E"	VREF	–40°C < T_A < 85°C, No Load	2.490	2.500	2.510	V
Output Voltage, "F"	VREF	–40°C < T_A < 85°C, No Load	2.485	2.500	2.515	V
Output Voltage, "E"	VREF	–55°C < T_A < 125°C, No Load		2.5 ± 0.01		V
Output Voltage, "F"	VREF	–55°C < T_A < 125°C, No Load		2.5 ± 0.015		V
Drift	TC_{VREF}			–10		ppm/°C
Line Regulation		4.5 V ≤ V+ ≤ 13.2 V		±0.01	±0.05	%/V
Load Regulation		10 µA ≤ I_{VREF} ≤ 500 µA		±0.1	±0.25	%/mA
Output Current, Zero Hysteresis	I_{VREF}			7		µA
Hysteresis Current Scale Factor	SF_{HYS}	(Note 1)		5.0		µA/°C
Turn-On Settling Time		To Rated Accuracy		25		µs
OPEN-COLLECTOR OUTPUTS OVER, UNDER						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA		0.25	0.4	V
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA		0.6		V
Output Leakage Current	I_{OH}	V+ = 12 V		1	100	µA
Fall Time	t_{HL}	See Test Load		40		ns
POWER SUPPLY						
Supply Range	V+		4.5		13.2	V
Supply Current	I_{SY}	Unloaded, +V = 5 V		400	500	µA
Supply Current	I_{SY}	Unloaded, +V = 13.2 V		450	800	µA
Power Dissipation	P_{DISS}	+V = 5 V		2.0	2.5	mW

NOTES

[1]K = °C + 273.15.

[2]Guaranteed but not tested.

[3]Does not consider errors caused by heating due to dissipation of output load currents.

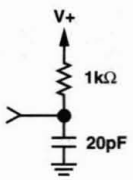
[4]Maximum deviation between +25°C readings after temperature cycling between –55°C and +125°C.

[5]Typical values indicate performance measured at T_A = +25°C.

[6]Observed in a group sample over an accelerated life test of 500 hours at 150°C.

Specifications subject to change without notice.

Test Load



ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage . . . . . –0.3 V to +15 V
Maximum Input Voltage
(SETHIGH, SETLOW) . . . . . –0.3 V to [(V+) + 0.3 V]
Maximum Output Current (VREF, VPTAT) . . . . . 2 mA
Maximum Output Current (Open Collector Outputs) . . 50 mA
Maximum Output Voltage (Open Collector Outputs) . . . . 15 V
Operating Temperature Range . . . . . –55°C to +150°C
Dice Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . – 65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

ANALOG DEVICES

Serial Digital Output Thermometers

TMP03/TMP04*

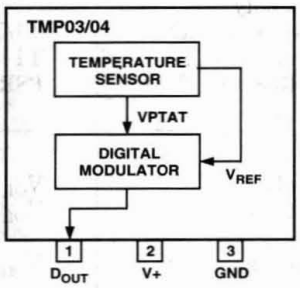
FEATURES

Low Cost 3-Pin Package
Modulated Serial Digital Output
Proportional to Temperature
±1.5°C Accuracy (typ) from –25°C to +100°C
Specified –40°C to +100°C, Operation to 150°C
Power Consumption 6.5 mW Max at 5 V
Flexible Open-Collector Output on TMP03
CMOS/TTL Compatible Output on TMP04
Low Voltage Operation (4.5 V to 7 V)

APPLICATIONS

Isolated Sensors
Environmental Control Systems
Computer Thermal Monitoring
Thermal Protection
Industrial Process Control
Power System Monitors

FUNCTIONAL BLOCK DIAGRAM



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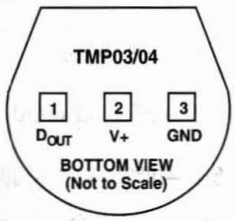
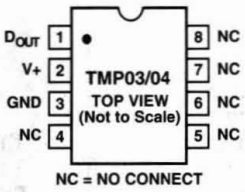
PACKAGE TYPES AVAILABLE

TO-92



SO-8 and RU-8 (TSSOP)



GENERAL DESCRIPTION

The TMP03/TMP04 is a monolithic temperature detector that generates a modulated serial digital output that varies in direct proportion to the temperature of the device. An onboard sensor generates a voltage precisely proportional to absolute temperature which is compared to an internal voltage reference and input to a precision digital modulator. The ratiometric encoding format of the serial digital output is independent of the clock drift errors common to most serial modulation techniques such as voltage-to-frequency converters. Overall accuracy is ±1.5°C (typical) from –25°C to +100°C, with excellent transducer linearity. The digital output of the TMP04 is CMOS/TTL compatible, and is easily interfaced to the serial inputs of most popular micro-processors. The open-collector output of the TMP03 is capable of sinking 5 mA. The TMP03 is best suited for systems requiring isolated circuits utilizing optocouplers or isolation transformers.

The TMP03 and TMP04 are specified for operation at supply voltages from 4.5 V to 7 V. Operating from +5 V, supply current (unloaded) is less than 1.3 mA.

The TMP03/TMP04 are rated for operation over the –40°C to +100°C temperature range in the low cost TO-92, SO-8, and TSSOP-8 surface mount packages. Operation extends to +150°C with reduced accuracy.

***Patent pending.**

ORDERING GUIDE

Model	Accuracy at +25°C	Temperature Range	Package Option*
TMP03FT9	±3.0	XIND	TO-92
TMP03FS	±3.0	XIND	SO-8
TMP03FRU	±3.0	XIND	TSSOP-8
TMP03GBC	±3.0	+25°C	Die
TMP04FT9	±3.0	XIND	TO-92
TMP04FS	±3.0	XIND	SO-8
TMP04FRU	±3.0	XIND	TSSOP-8
TMP04GBC	±3.0	+25°C	Die

*For outline information see Package Information section.

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TMP03/TMP04–SPECIFICATIONS

TMP03F (V+ = +5 V, –40°C ≤ T_A ≤ 100°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
Temperature Error		T_A = +25°C		1.0	3.0	°C
		–25°C < T_A < +100°C[1]		1.5	4.0	°C
		–40°C < T_A < –25°C[1]		2.0	5.0	°C
Temperature Linearity				0.5		°C
Long-Term Stability		1000 Hours at +125°C		0.5		°C
Nominal Mark-Space Ratio	T1/T2	T_A = 0°C		58.8		%
Nominal T1 Pulse Width	T1			10		ms
Power Supply Rejection Ratio	PSRR	Over Rated Supply T_A = +25°C		0.7	1.2	°C/V
OUTPUTS						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA			0.2	V
Output Low Voltage	V_{OL}	I_{SINK} = 5 mA 0°C < T_A < +100°C			2	V
Output Low Voltage	V_{OL}	I_{SINK} = 4 mA –40°C < T_A < 0°C			2	V
Digital Output Capacitance	C_{OUT}	(Note 2)		15		pF
Fall Time	t_{HL}	See Test Load		150		ns
Device Turn-On Time				20		ms
POWER SUPPLY						
Supply Range	V+		4.5		7	V
Supply Current	I_{SY}	Unloaded		0.9	1.3	mA

NOTES
[1]Maximum deviation from output transfer function over specified temperature range.
[2]Guaranteed but not tested.

Specifications subject to change without notice.

Test Load
10 kΩ to +5 V Supply, 100 pF to Ground

TMP04F (V+ = +5 V, –40°C ≤ T_A ≤ +100°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
Temperature Error		T_A = +25°C		1.0	3.0	°C
		–25°C < T_A < +100°C[1]		1.5	4.0	°C
		–40°C < T_A < –25°C[1]		2.0	5.0	°C
Temperature Linearity				0.5		°C
Long-Term Stability		1000 Hours at +125°C		0.5		°C
Nominal Mark-Space Ratio	T1/T2	T_A = 0°C		58.8		%
Nominal T1 Pulse Width	T1			10		ms
Power Supply Rejection Ratio	PSRR	Over Rated Supply T_A = +25°C		0.7	1.2	°C/V
OUTPUTS						
Output High Voltage	V_{OH}	I_{OH} = 800 µA	V+ –0.4			V
Output Low Voltage	V_{OL}	I_{OL} = 800 µA			0.4	V
Digital Output Capacitance	C_{OUT}	(Note 2)		15		pF
Fall Time	t_{HL}	See Test Load		200		ns
Rise Time	t_{LH}	See Test Load		160		ns
Device Turn-On Time				20		ms
POWER SUPPLY						
Supply Range	V+		4.5		7	V
Supply Current	I_{SY}	Unloaded		0.9	1.3	mA

NOTES
[1]Maximum deviation from output transfer function over specified temperature range.
[2]Guaranteed but not tested.

Specifications subject to change without notice.

Test Load
100 pF to Ground

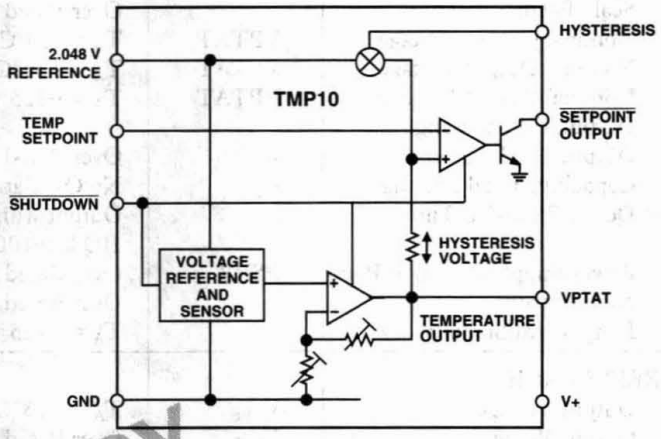
Single-Setpoint Temperature Controller

TMP10

FEATURES
Low Voltage Operation (2.7 V to 5.5 V)
Calibrated Directly in °C
10 mV/°C Scale Factor
±3°C Accuracy Over Temperature
±0.5°C Linearity (typ)
Onboard 2.048 V Precision Reference
Programmable Comparator Hysteresis
Either 1°C, 2°C, or 5°C
Specified –40°C to +125°C, Operation to +150°C
100 µA Max Quiescent Current
Shutdown Current: 1 µA max

APPLICATIONS
Environmental Control Systems
Thermal Protection
Battery Chargers
Fire Alarms
Power System Monitors
Power Supplies
CPU Thermal Management

FUNCTIONAL BLOCK DIAGRAM



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PRELIMINARY TECHNICAL DATA

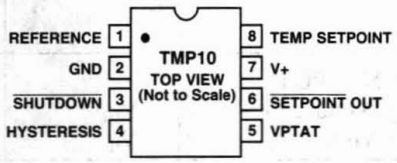
GENERAL DESCRIPTION

The TMP10 is a low voltage, precision, centigrade temperature sensor and controller. A voltage output that is linearly proportional to the Celsius (Centigrade) temperature, the VPTAT output, provides temperature measurement from –40°C to +125°C. The output scale factor is +10 mV/°C. The TMP10 does not require external calibration to provide typical accuracies of ±1°C at 25°C and ±2°C over the operating temperature range. An open-collector output comparator, and an onboard 2.048 V reference allow a single temperature setpoint to be established using two external resistors. One of three levels of thermal hysteresis, 1°C, 2°C, or 5°C, may be chosen for the temperature setpoint using the hysteresis pin. The hysteresis level is determined by connecting the hysteresis pin to: V_{REF}, GND, or leaving it floating. The TMP10 is designed for single supply operation from 2.7 V to 5.5 V. Supply current runs well below 100 µA providing very low self-heating, less than 0.1°C in still air. In addition, a shutdown function is provided to cut supply current to less than 1 µA for battery-powered applications. The TMP10 operates linearly up to +125°C from a single 2.7 V supply. Operation extends to +150°C with reduced accuracy when operating from a 5 V supply.

The TMP10 is available in 8-pin DIP, and SO-8 and TSSOP-8 surface-mount packages.

PIN CONFIGURATIONS

Plastic DIP, SO-8 and TSSOP-8 Packages



ORDERING GUIDE

Model	Accuracy at 25°C (°C max)	Linear Operating Temperature Range	Package Option*
TMP10FS	±2.0	–40°C to +125°C	SO-8
TMP10GS	±3.0	–40°C to +125°C	SO-8
TMP10GRU	±3.0	–40°C to +125°C	TSSOP-8
TMP10GP	±3.0	–40°C to +125°C	PDIP-8

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

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TMP10–SPECIFICATIONS (V_S = +2.7 V to +5.5 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VPTAT ACCURACY						
TMP10F		T_A = +25°C		±1	±2	°C
TMP10G		T_A = +25°C		±1	±3	°C
TMP10F		Over Rated Temperature		±2	±3	°C
TMP10G		Over Rated Temperature		±2	±4	°C
VPTAT OUTPUT						
Scale Factor		Over Rated Temperature		+10	+9.8/+10.2	mV/°C
Nominal Output Voltage	VPTAT	T_A = –40°C		100		mV
Nominal Output Voltage	VPTAT	T_A = +25°C		750		mV
Nominal Output Voltage	VPTAT	T_A = +125°C		1750		mV
Output Voltage Range			100		2000	mV
Output Load Current	I_L	Over Rated Temperature	0		200	µA
Capacitive Load Driving	C_L	No Oscillations (Note 1)	1000	10,000		pF
Device Turn-On Time		Output within ±1°C 100 kΩ//100 pF Load		0.5	1	ms
Power Supply Rejection Ratio	PSRR	Over Rated Supply		0.5		°C/V
Nonlinearity		Over Rated Temperature		0.5		°C
Long-Term Stability		T_A = +125°C for 1 kHrs		0.1		°C
REFERENCE						
Output Voltage	V_{REF}	T_A = +25°C	2.040	2.048	2.056	V
Output Voltage	V_{REF}	Over Rated Temperature	2.036	2.048	2.060	V
Temperature Coefficient	TC	Over Rated Temperature		15		ppm/°C
Output Current	I_{REF}	Over Rated Temperature			25	µA
COMPARATOR						
Offset Voltage	V_{OS}	T_A = +25°C		1		mV
Input Bias Current	I_B	T_A = +25°C		10	25	nA
Open-Collector Output	V_{OUT}	Over Rated Temperature I_{LOAD} = 400 µA			0.4	V
Open-Collector Output	I_{OUT}	Over Rated Temperature	0.5	1		mA
Hysteresis		Low		1		°C
		Medium		2		°C
		High		5		°C
SHUTDOWN INPUT						
Input High Voltage	V_{IH}	V_S = 2.7 V	1.8			V
Input Low Voltage	V_{IL}	V_S = 5.5 V			800	mV
POWER SUPPLY						
Supply Range	$+V_S$		2.7		5.5	V
Supply Current	I_{SY}	Unloaded at +5.5 V			100	µA
Shutdown Current	I_{SD}	Unloaded at +5.5 V		0.1	1	µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

Airflow and Temperature Sensor

TMP12*

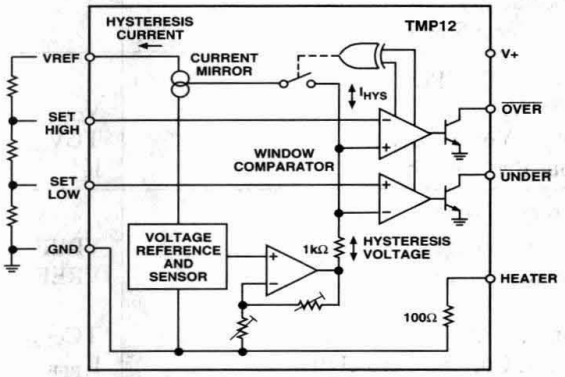
FEATURES

Temperature Sensor Includes 100 Ω Heater
Heater Provides Power IC Emulation
Accuracy ±3°C typ. from −40°C to +100°C
Operation to +150°C
5 mV/°C Internal Scale-Factor
Resistor Programmable Temperature Setpoints
20 mA Open-Collector Setpoint Outputs
Programmable Thermal Hysteresis
Internal 2.5 V Reference
Single 5 V Operation
400 μA Quiescent Current (Heater OFF)
Minimal External Components

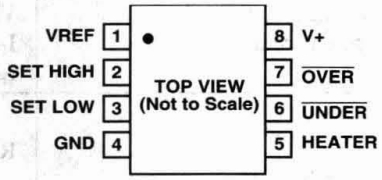
APPLICATIONS

System Airflow Sensor
Equipment Over-Temperature Sensor
Over-Temperature Protection
Power Supply Thermal Sensor
Low-Cost Fan Controller

FUNCTIONAL BLOCK DIAGRAM



PINOUTS
DIP and SO



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GENERAL DESCRIPTION

The TMP12 is a silicon-based airflow and temperature sensor designed to be placed in the same airstream as heat generating components that require cooling. Fan cooling may be required continuously, or during peak power demands, e.g. for a power supply, and if the cooling systems fails, system reliability and/or safety may be impaired. By monitoring temperature while emulating a power IC, the TMP12 can provide a warning of cooling system failure.

The TMP12 generates an internal voltage that is linearly proportional to Celsius (Centigrade) temperature, nominally +5 mV/°C. The linearized output is compared with voltages from an external resistive divider connected to the TMP12's 2.5 V precision reference. The divider sets up one or two reference voltages, as required by the user, providing one or two temperature setpoints. Comparator outputs are open-collector transistors able to sink over 20 mA. There is an on-board hysteresis generator provided to speed up the temperature-setpoint output transitions, this also reduces erratic output transitions in noisy environments. Hysteresis is programmed by the external resistor chain and is determined by the total current drawn from the 2.5 V reference. The TMP12 airflow sensor also incorporates a precision, low temperature coefficient 100 Ω heater resistor that may be connected directly to an external 5 V supply. When the heater is activated it raises the die temperature in the DIP package approximately 20°C above ambient (in still air). The purpose of the heater in the TMP12 is to emulate a power IC, such as a regulator or Pentium CPU which has a high internal dissipation.

When subjected to a fast airflow, the package and die temperatures of the power device and the TMP12 (if located in the same airstream) will be reduced by an amount proportional to the rate of airflow. The internal temperature rise of the TMP12 may be reduced by placing a resistor in series with the heater, or reducing the heater voltage.

The TMP12 is intended for single 5 V supply operation, but will operate on a 12 V supply. The heater is designed to operate from 5 V only. Specified temperature range is from −40°C to +125°C, operation extends to +150°C at 5 V with reduced accuracy.

The TMP12 is available in 8-pin plastic DIP and SO packages.

***Protected by U.S. Patent No. 5,195,827.**

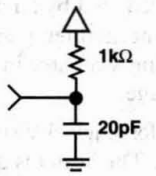
TMP12–SPECIFICATIONS (V_S = +5 V, −40°C ≤ T_A ≤ +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
Accuracy (High, Low Setpoints)		T_A = +25°C		±2	±3	°C
Accuracy (High, Low Setpoints)		T_A = −40°C to +100°C		±3	±5	°C
Internal Scale Factor		T_A = −40°C to +100°C	+4.9	+5	+5.1	mV/°C
Power Supply Rejection Ratio	PSRR	4.5 V ≤ +V_S ≤ 5.5 V		0.1	0.5	°C/V
Linearity		T_A = −40°C to +125°C		0.5		°C
Repeatability		T_A = −40°C to +125°C		0.3		°C
Long Term Stability		T_A = +125°C for 1 k Hrs		0.3		°C
SETPOINT INPUTS						
Offset Voltage	V_{OS}			0.25		mV
Output Voltage Drift	TCV_{OS}			3		µV/°C
Input Bias Current	I_B			25	100	nA
VREF OUTPUT						
Output Voltage	VREF	T_A = +25°C, No Load	2.49	2.50	2.51	V
Output Voltage	VREF	T_A = −40°C to +100°C, No Load		2.5 ± 0.015		V
Output Drift	TC_{VREF}			−10		ppm/°C
Output Current, Zero Hysteresis	I_{VREF}			7		µA
Hysteresis Current Scale Factor	SF_{HYS}			5		µA/°C
OPEN-COLLECTOR OUTPUTS						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA		0.25	0.4	V
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA		0.6		V
Output Leakage Current	I_{OH}	V_S = 12 V		1	100	µA
Fall Time	t_{HL}	See Test Load		40		ns
HEATER						
Resistance	R_H	T_A = +25°C	97	100	103	Ω
Temperature Coefficient		T_A = −40°C to +125°C		100		ppm/°C
Maximum Continuous Current	I_H	See Note 1			60	mA
POWER SUPPLY						
Supply Range	+V_S		4.5		5.5	V
Supply Current	I_{SY}	Unloaded at +5 V		400	600	µA
	I_{SY}	Unloaded at +12 V[2]		450		µA

NOTES
[1]Guaranteed but not tested.
[2]TMP12 is specified for operation from a 5 V supply. However, operation is allowed up to a 12 V supply, but not tested at 12 V. Maximum heater supply is 6 V.

Specifications subject to change without notice.

TEST LOAD



ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . −0.3 V to +15 V
Heater Voltage . . . . . +6 V
Setpoint Input Voltage . . . . . −0.3 V to [(V+) +0.3 V]
Reference Output Current . . . . . 2 mA
Open-Collector Output Current . . . . . 50 mA
Open-Collector Output Voltage . . . . . +15 V
Operating Temperature Range . . . . . −55°C to +150°C
Dice Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . −65°C to +160°C
Lead Temperature(Soldering, 60 sec) . . . . . +300°C

ORDERING GUIDE

Model/Grade	Temperature Range[1]	Package Description	Package Option[2]
TMP12FP	XIND	Plastic DIP	N-8
TMP12FS	XIND	SOIC	SO-8
TMP12GBC	+25°C	Die	

NOTES
[1]XIND = –40°C to +125°C
[2]For outline information see Package Information section.

Quad-Setpoint, Programmable Temperature Monitor and Controller

TMP14

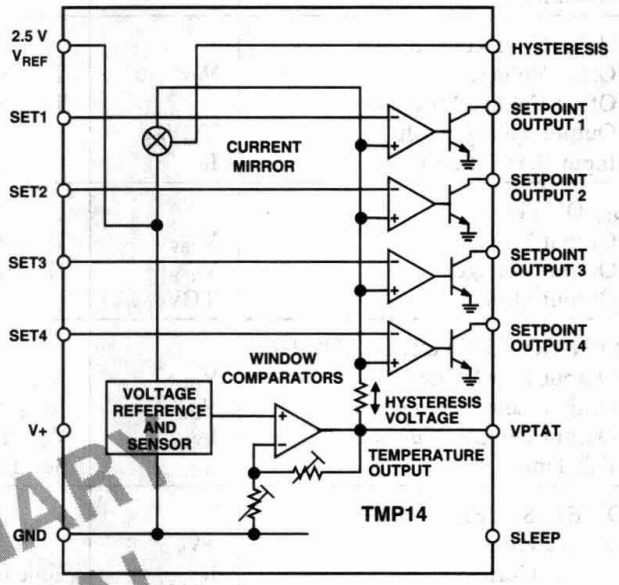
FEATURES

Four Programmable Temperature Setpoints
Programmable Thermal Hysteresis
Accuracy ±3°C typ from –40°C to +125°C
Temperature Output Scale-Factor 5 mV/°C
Resistor Programmable Temperature Setpoints
5 mA Open-Collector Setpoint Outputs
Internal 2.5 V Reference
500 µA Max Quiescent Current at +5 V

APPLICATIONS

Power Supply Monitor & Control System
Multiple-Fan Controller System
Workstation Thermal Management System

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The TMP14 is a temperature sensor and controller that generates an output voltage proportional to temperature and provides four temperature trip points. The four trip points, or temperature setpoints, and their hysteresis are determined by voltage levels set by the user. An on-chip voltage reference provides an easy method for setting the temperature trip points and hysteresis. For applications that are sensitive to power consumption, a sleep mode is provided which cuts power consumption to 1/50th of nominal.

The TMP14 consists of a bandgap voltage reference combined with four matched comparators. The reference provides both a temperature-stable 2.5 V output, and a voltage proportional to absolute temperature (VPTAT) which has precise temperature coefficient of 5 mV/°C. The VPTAT output is nominally 1.49 V at +25°C. The comparators determine whether the VPTAT output is above the voltages set up by external resistive dividers (temperature trip points) and generate an open-collector output signal when one of their respective thresholds has been exceeded.

Hysteresis is programmed by a user-selected voltage at the hysteresis pin. This voltage adjusts the hysteresis current which is used to generate a hysteresis offset voltage. The comparator's noninverting inputs are connected in parallel, which guarantees that there is no hysteresis overlap and eliminates erratic transitions between adjacent trip zones.

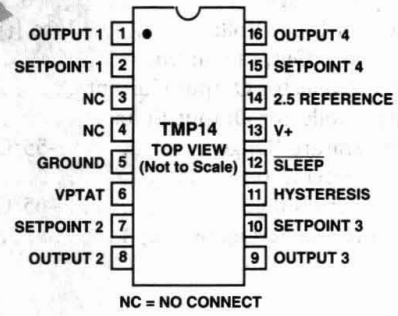
Utilizing a proprietary thin-film resistor process in conjunction with production laser trimming, a temperature accuracy of ±3°C at 25°C is guaranteed. The open-collector outputs are capable of sinking 5 mA, and provide TTL/CMOS logic compatibility with an external pull-up resistor. Operating from a single 5 V supply, the quiescent current is 500 µA max, and only 10 µA max in sleep mode.

The TMP14 is available in the 16-pin epoxy mini-DIP and SO (small outline) packages.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATIONS

Plastic DIP and SOIC



HYSTERESIS AND SLEEP FUNCTIONS

Hysteresis	Connect Pin 11 to
0.6°C	+2.5 V Reference
1.5°C	Leave Open
5°C	Ground

Power Control	Connect Pin 12 to
Active	Logic "1"
Sleep	Logic "0"

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To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

TMP14–SPECIFICATIONS (V_S = +5 V, –40°C ≤ T_A ≤ +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
Accuracy (Setpoints 1, 2, 3, & 4)		T_A = +25°C		±2	±3	°C
Accuracy (Setpoints 1, 2, 3, & 4)		T_A = –40°C to +125°C		±3	±5	°C
VPTAT Output Scale Factor			+4.9	+5	+5.1	mV/°C
Setpoint Hysteresis Levels		T_A = +25°C		0.6, 1.5, 5		°C
Power Supply Rejection Ratio	PSRR	4.5 V ≤ +V_S ≤ 5.5 V		0.1	0.5	°C/V
Linearity				0.5		°C
SETPOINT INPUTS						
Offset Voltage	V_{OS}	T_A = +25°C		0.25	1	mV
Offset Voltage Mismatch		T_A = +25°C		0.1	0.5	mV
Output Voltage Drift	TCV_{OS}			3		µV/°C
Input Bias Current	I_B			25	100	nA
V_{REF} OUTPUT						
Output Voltage	V_{REF}	T_A = +25°C, No Load	2.49	2.50	2.51	V
Output Voltage	V_{REF}	No Load		2.5 ± 0.015		V
Output Drift	TCV_{REF}			–10		ppm/°C
OPEN-COLLECTOR OUTPUTS						
Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA		0.25	0.4	V
Output Low Voltage	V_{OL}	I_{SINK} = 5 mA		0.6		V
Output Leakage Current	I_{OH}	V_S = 12 V		1	100	µA
Fall Time	t_{HL}	See Test Load		40		ns
POWER SUPPLY						
Supply Range	+V_S		4.5		5.5	V
Supply Current	I_{SY}	Unloaded at +5 V		400	500	µA
	I_{SY}	Unloaded at +12 V		450		µA

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage . . . . . –0.3 V to +15 V
Maximum Setpoint Input Voltage . . . –0.3 V to [(V+) +0.3 V]
Maximum Reference Output Current . . . . . 2 mA
Maximum Open-Collector Output Current . . . . . 20 mA
Maximum Open-Collector Output Voltage . . . . . +15 V
Operating Temperature Range . . . . . –55°C to +150°C
Dice Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . –65°C to +160°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
TMP14GP	–40°C to +125°C	Plastic DIP	N-16
TMP14GS	–40°C to +125°C	SOIC	SO-16

*For outline information see Package Information section.

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ANALOG DEVICES

Low Voltage Temperature Sensors

TMP35/TMP36/TMP37*

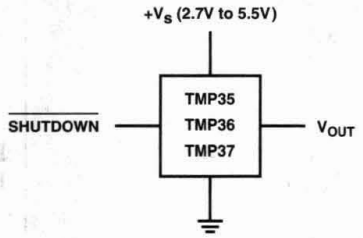
FEATURES

Low Voltage Operation (2.7 V to 5.5 V)
Calibrated Directly in °C
10 mV/°C Scale Factor (20 mV/°C on TMP37)
±2°C Accuracy Over Temperature (typ)
±0.5°C Linearity (typ)
Stable with Large Capacitive Loads
Specified −40°C to +125°C, Operation to +150°C
Less than 50 μA Quiescent Current
Shutdown Current 0.5 μA max
Low Self-Heating

APPLICATIONS

Environmental Control Systems
Thermal Protection
Industrial Process Control
Fire Alarms
Power System Monitors
CPU Thermal Management

FUNCTIONAL DIAGRAM



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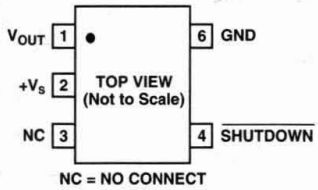
PRODUCT DESCRIPTION

The TMP35, TMP36, and TMP37 are low voltage, precision centigrade temperature sensors. They provide a voltage output that is linearly proportional to the Celsius (Centigrade) temperature. The TMP35/TMP36/TMP37 do not require any external calibration to provide typical accuracies of ±1°C at +25°C and ±2°C over the –40°C to +125°C temperature range. The low output impedance of the TMP35/TMP36/TMP37, linear output, and precise calibration simplify interfacing to temperature control circuitry and A/D converters. All three devices are intended for single supply operation from 2.7 V to 5.5 V maximum. Supply current runs well below 50 μA providing very low self-heating, less than 0.1°C in still air. In addition, a shutdown function is provided to cut supply current to less than 0.5 μA. The TMP35 is functionally-compatible with the LM35/LM45 and provides a 250 mV output at +25°C. The TMP35 reads temperatures from +10°C to +125°C. The TMP36 is specified from –40°C to +125°C, provides a 750 mV output at 25°C and operates to +125°C from a single 2.7 V supply. Both the TMP35 and TMP36 have an output scale factor of +10 mV/°C. The TMP37 is intended for applications over the range +5°C to +100°C, and provides an output scale factor of 20 mV/°C. The TMP37 provides a 500 mV output at +25°C. Operation extends to +150°C with reduced accuracy for all devices when operating from a 5 V supply.

The TMP35/TMP36/TMP37 are all available in low cost 3-pin TO-92, and SO-8 and 5-pin SOT-25 surface mount packages.

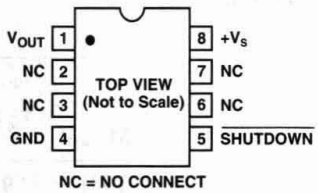
PACKAGE TYPES AVAILABLE

SOT-25 (SOT23-5)



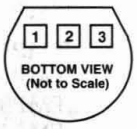
NC = NO CONNECT

SO-8



NC = NO CONNECT

TO-92



PIN 1 - $+V_S$, PIN 2 - V_{OUT}, PIN 3 - GND

*Patent pending.

TMP35/TMP36/TMP37F/G–SPECIFICATIONS (V_S = +2.7 V to 5.5 V, −40°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ACCURACY						
TMP35/TMP36/TMP37F		T_A = +25°C		±1	±2	°C
TMP35/TMP36/TMP37G		T_A = +25°C		±1	±3	°C
TMP35/TMP36/TMP37F		Over Rated Temperature		±2	±3	°C
TMP35/TMP36/TMP37G		Over Rated Temperature		±2	±4	°C
Scale Factor, TMP35		+10°C ≤ T_A ≤ +125°C		+10	+9.8/+10.2	mV/°C
Scale Factor, TMP36		−40°C ≤ T_A ≤ +125°C		+10	+9.8/+10.2	mV/°C
Scale Factor, TMP37		+5°C ≤ T_A ≤ +85°C		+20	+19.6/+20.4	mV/°C
Scale Factor, TMP37		+5°C ≤ T_A ≤ +100°C 3.0 V ≤ +V_S ≤ 5.5 V		+20	+19.6/+20.4	mV/°C
Load Regulation		0 µA ≤ I_L ≤ 50 µA		1	20	m°C/µA
Power Supply Rejection Ratio	PSRR	T_A = +25°C		30	100	m°C/V
Power Supply Rejection Ratio	PSRR	3.0 V ≤ +V_S ≤ 5.5 V		50		m°C/V
Linearity				0.5		°C
Long-Term Stability		T_A = +150°C for 1 kHrs		0.4		°C
SHUTDOWN						
Logic High Input Voltage	V_{IH}	V_S = 2.7 V	1.8			V
Logic Low Input Voltage	V_{IL}	V_S = 5.5 V			400	mV
OUTPUT						
TMP35 Output Voltage		T_A = +25°C		250		mV
TMP36 Output Voltage		T_A = +25°C		750		mV
TMP37 Output Voltage		T_A = +25°C		500		mV
Output Voltage Range			100		2,000	mV
Output Load Current	I_L		0		50	µA
Short-Circuit Current	I_{SC}	Note 1			250	µA
Capacitive Load Driving	C_L	No Oscillations[1]	1,000	10,000		pF
Device Turn-On Time		Output within ±1°C 100 kΩ‖100 pF Load[1]		0.5	1	ms
POWER SUPPLY						
Supply Range	+V_S		2.7		5.5	V
Supply Current	$I_{SY\ (ON)}$	Unloaded			50	µA
Supply Current (Shutdown)	$I_{SY\ (OFF)}$	Unloaded		0.01	0.5	µA

NOTES
[1]Guaranteed but not tested.
[2]Does not consider errors caused by self-heating

Specifications subject to change without notice.

ORDERING GUIDE

Model	Accuracy at 25°C (°C max)	Linear Operating Temp. Range	Package[1]
TMP35FT9	±2.0	+10°C to +125°C	TO-92
TMP35GT9	±3.0	+10°C to +125°C	TO-92
TMP35FS	±2.0	+10°C to +125°C	SO-8
TMP35GS	±3.0	+10°C to +125°C	SO-8
TMP35GRT[2]	±3.0	+10°C to +125°C	SOT-25
TMP36FT9	±2.0	–40°C to +125°C	TO-92
TMP36GT9	±3.0	–40°C to +125°C	TO-92
TMP36FS	±2.0	–40°C to +125°C	SO-8
TMP36GS	±3.0	–40°C to +125°C	SO-8
TMP36GRT[2]	±3.0	–40°C to +125°C	SOT-25
TMP37FT9	±2.0	+5°C to +100°C	TO-92
TMP37GT9	±3.0	+5°C to +100°C	TO-92
TMP37FS	±2.0	+5°C to +100°C	SO-8
TMP37GS	±3.0	+5°C to +100°C	SO-8
TMP37GRT[2]	±3.0	+5°C to +100°C	SOT-25

NOTES
[1]For outline information see Package Information section.
[2]Consult factory for availability.

Time Domain & Laser Diode Drivers
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Time Domain & Laser Diode Drivers–Selection Guides

Pulse Width Modulator

Model	# Bits	Power V_S Volts	Power I_S mA	Trigger Rate for Specs MHz	Trigger Rate Max MHz	Prop Delay ns	Rise & Fall Time ns	Full Scale	# Pins	Page No.	Comments	Fax-code
AD9560A	8	+5	87	20	40	44	3	90% Clock	28	*	With Autocalibration, Programmable Edge Placement	1894
AD9561	8	+5	170	20	50	TBD	3	100%	28	22–5	Programmable Edge Placement	

Laser Diode Drivers

Model	# Bits	Power V_S Volts	Power I_S mA	Trigger Rate for Specs MHz	Trigger Rate Max MHz	Prop Delay ns	Rise & Fall Time ns	Full Scale	# Pins	Page No.	Comments	Fax-code
AD9660	N/A	+5	150	200	200	1.6	1.7/2.8	180 mA	28	22–7	Dual Feedback Loops for Bias/Write	1906
AD9661A	N/A	+5	+95	100	200	2.9–5	2/2	120	28	22–9	With Light Power Control	1971

8-Bit, Programmable Delay Generators

Model	Power $+V_S$ V	Power $-V_S$ V	Power $+I_S$ mA	Power $-I_S$ mA	Prop Delay ns	Max Trigger Rate MHz	Rise & Fall Time ns	INL Bits	DNL Bits	Min Pulse Width ns	Max Pulse Width ms	# Pins	Page No.	Comments	Fax-code
AD9500	+5	–5	24	37	7.4	60	2	±1/2	±1	2.5	10	24/28	*	With Separate Trigger & Reset Inputs	1460
AD9501	+5	–	83	–	30	22	3.5	±1/2	±1	7.5	10	20	22–3	18 ps Resolution	1461

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

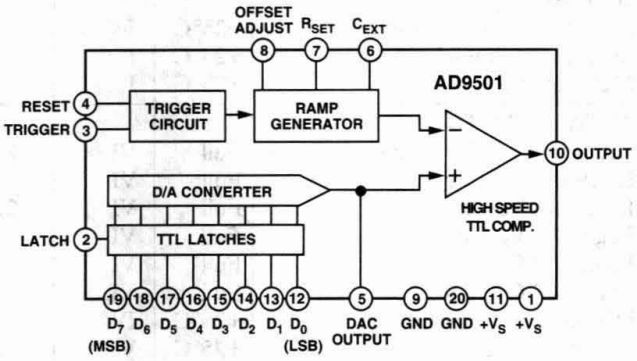
Digitally Programmable Delay Generator

AD9501

FEATURES
Single +5 V Supply
TTL and CMOS Compatible
10 ps Delay Resolution
2.5 ns to 10 μs Full-Scale Range
Maximum Trigger Rate 50 MHz
MIL-STD-883 Compliant Version Available

APPLICATIONS
Disk Drive Deskewing
Data Communications
Test Equipment
Radar I & Q Matching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9501 is a digitally programmable delay generator which provides programmed time delays of an input pulse. Operating from a single +5 V supply, the AD9501 is TTL- or CMOS-compatible, and is capable of providing accurate timing adjustments with resolutions as low as 10 ps. Its accuracy and programmability make it ideal for use in data deskewing and pulse delay applications, as well as clock timing adjustments.

Full-scale delay range is set by the combination of an external resistor and capacitor, and can range from 2.5 ns to 10 μs for a single AD9501. An eight-bit digital word selects a time delay within the full-scale range. When triggered by the rising edge of an input pulse, the output of the AD9501 will be delayed by an amount equal to the selected time delay (t_D) plus an inherent propagation delay (t_{PD}).

The AD9501 is available for a commercial temperature range of 0°C to +70°C in a 20-pin plastic DIP, 20-pin ceramic DIP, and a 20-lead plastic leaded chip carrier (PLCC). Devices fully compliant to MIL-STD-883 are available in ceramic DIPs. Refer to the Analog Devices Military Products Databook or current AD9501/883B data sheet for detailed specifications.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage	+7 V
Digital Input Voltage Range	–0.5 V to $+V_S$
Trigger/Reset Input Volt. Range	–0.5 V to $+V_S$
Minimum R_{SET}	30 Ω
Digital Output Current (Sourcing)	10 mA
Digital Output Current (Sinking)	50 mA
Operating Temperature Range	
AD9501JN/JP/JQ	0°C to +70°C
AD9501SQ/883B	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature[2]	+175°C
Lead Soldering Temperature (10 sec)	+300°C

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: 20-lead plastic leaded chip carrier θ_{JA}= 73°C/W; θ_{JC}= 29°C/W. 20-pin ceramic DIP θ_{JA}= 65°C/W; θ_{JC}= 20°C/W. 20-pin plastic DIP θ_{JA}= 65°C/W; θ_{JC}= 26°C/W.

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ORDERING GUIDE

Device	Temperature Range	Package Description	Package Option*
AD9501JN	0°C to +70°C	20-Pin Plastic DIP	N-20
AD9501JP	0°C to +70°C	20-Lead PLCC	P-20A
AD9501JQ	0°C to +70°C	20-Pin Ceramic DIP	Q-20
AD9501SQ/883B	–55°C to +125°C	20-Pin Ceramic DIP	Q-20

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

AD9501–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

[$+V_S$ = +5 V; C_{EXT} = Open; R_{SET} = 3090 Ω (Full-scale range =100 ns); Pin 8 grounded; and device output connected to Pin 4 RESET input unless otherwise noted]

Parameter	Temp	Test Level	COMMERCIAL 0°C to +70°C AD9501JN/JP/JQ Min	Typ	Max	MILITARY −55°C to +125°C AD9501SQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY									
Differential Nonlinearity	+25°C	I			0.5			0.5	LSB
Integral Nonlinearity	+25°C	I			1			1	LSB
Monotonicity	+25°C	I		Guaranteed			Guaranteed		
DIGITAL INPUTS									
Latch Input "1" Voltage	Full	VI	2.0			2.3			V
Latch Input "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			60			60	μA
Logic "0" Current	Full	VI			3			3	μA
Digital Input Capacitance	+25°C	IV			5.5			5.5	pF
Data Setup Time (t_S)[1]	+25°C	V		2.5			2.5		ns
Data Hold Time (t_H)[2]	+25°C	V		2.5			2.5		ns
Latch Pulse Width (t_L)	+25°C	V		3.5			3.5		ns
Reset/Trigger Pulse Width (t_R, t_T)	+25°C	V		2			2		ns
DYNAMIC PERFORMANCE									
Maximum Trigger Rate[3]	+25°C	IV	18	22		18	22		MHz
Minimum Propagation Delay (t_{PD})[4]	+25°C	I		25	30		25	30	ns
Propagation Delay Tempco[5]	Full	V		25			25		ps/°C
Full-Scale Range Tempco	Full	V		36			36		ps/°C
Delay Uncertainty	+25°C	V		53			53		ps
Reset Propagation Delay (t_{RD})[6]	+25°C	I		14.5	17.5		14.5	17.5	ns
Reset-to-Trigger Holdoff (t_{THO})[7]	+25°C	V		4.5			4.5		ns
Trigger-to-Reset Holdoff (t_{RHO})[8]	+25°C	V		19			19		ns
Minimum Output Pulse Width[9]	+25°C	V		7.5			7.5		ns
Output Rise Time[10]	+25°C	I		2.3	3.5		2.3	3.5	ns
Output Fall Time[10]	+25°C	I		1.0	2.0		1.0	2.0	ns
DAC Settling Time (t_{LD})[11]	+25°C	V		30			30		ns
Linear Ramp Settling Time (t_{LRS})[12]	+25°C	V		20			20		ns
DIGITAL OUTPUT									
Logic "1" Voltage (Source 1 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (Sink 4 mA)	Full	VI		0.24	0.4		0.24	0.5	V
POWER SUPPLY[13]									
Positive Supply Current (+5.0 V)	Full	VI		69.5	83		69.5	83	mA
Power Dissipation	Full	VI			415			415	mW
Power Supply Rejection Ratio[14]									
Full-Scale Range Sensitivity	+25°C	I		0.7	2.0		0.7	2.0	ns/V
Minimum Prop Delay Sensitivity	+25°C	I		0.45	1.7		0.45	1.7	ns/V

NOTES

[1]Digital data inputs must remain stable for the specified time prior to the positive transition of the LATCH signal.

[2]Digital data inputs must remain stable for the specified time after the positive transition of the LATCH signal.

[3]Programmed delay (t_D) = 0 ns. Maximum self-resetting trigger rate is limited to 6.9 MHz with 100 ns programmed delay. If t_D= 0 ns and external RESET signal is used, maximum trigger rate is 23 MHz.

[4]Programmed delay (t_D) = 0 ns. In operation, any programmed delays are in addition to the minimum propagation delay (t_{PD}).

[5]Programmed delay (t_D) = 0 ns. [Minimum propagation delay (t_{PD})].

[6]Measured from 50% transition point of the RESET signal input to the 50% transition point of the falling edge of the output.

[7]Minimum time from the falling edge of RESET to the triggering input to insure valid output pulse, using external RESET pulse.

[8]Minimum time from triggering event to rising edge of RESET to insure valid output event, using external RESET pulse. Extends to 125 ns when programmed delay is 100 ns.

[9]When self-resetting with a full-scale programmed delay.

[10]Measured from +0.4 V to +2.4 V; source = 1 mA; sink = 4 mA.

[11]Measured from the data input to the time when the AD9501 becomes 8-bit accurate, after a full-scale change in the program delay data word.

[12]Measured from the RESET input to the time when the AD9501 becomes 8-bit accurate, after a full-scale programmed delay.

[13]Supply voltage should remain stable within ±5% for normal operation.

[14]Measured at $+V_S$ = +5.0 V ± 5%; specification shown is for worst case.

Specifications subject to change without notice.

ANALOG DEVICES

Pulse Width Modulator

AD9561

FEATURES
50 MHz Pulse Rate
8-Bit Resolution
Center, Left, or Right Justify
Low Power: 700 mW typical
Minimum Pulse Width: <5 ns
Maximum PW: 100% Full Scale

APPLICATIONS
Laser Printers
Digital Copiers
Color Copiers

GENERAL DESCRIPTION

The AD9561 is a second generation, high speed, digitally programmable pulse width modulator (PWM). Output pulse width is proportional to an 8-bit DATA input value. Two additional CONTROL inputs determine if the pulse is placed at the beginning, middle, or end of the clock period. Pulse width and placement can be changed every clock cycle up to 50 MHz.

Pulse width modulation is a well proven method for controlling gray scale and resolution enhancement in scanning laser print engines. Modulating pulse width enables exceptional continuous tone reproduction as well as resolution enhancement.

The AD9561 utilizes precision analog circuits to control dot size so that near-photographic quality images are practical without high frequency or high bandwidth required by all-digital approaches.

The AD9561 has improved performance and features versus its predecessor, the highly successful AD9560. An improved ramp topology enables control of pulse width through 100% of the dot clock period as opposed to 95% for the AD9560. This enables smooth transition across dot boundaries for line screen applications.

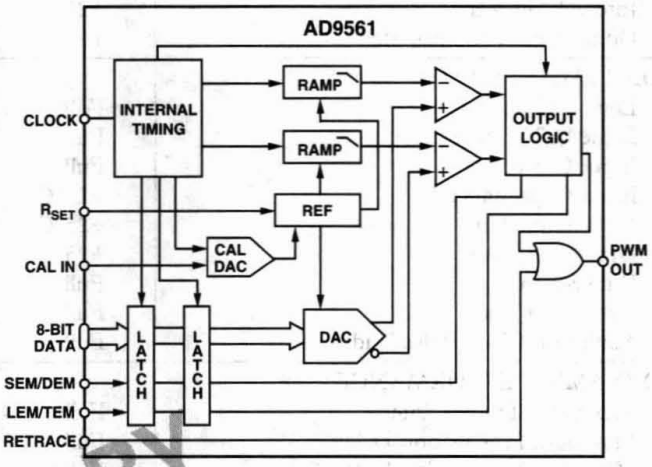
Additionally, input data setup and hold time is symmetrical at 2 ns each, making interface to image processing circuits simpler. Finally, chip design and pinout are optimized to decrease sensitivity of analog circuits to digital coupling. (See layout section for detailed recommendations for optimum results.)

Inputs are TTL or CMOS compatible, and outputs are CMOS compatible. The AD9561JR is packaged in a 28-lead plastic SOIC. It is rated over the commercial temperature range, 0°C to +70°C.

HIGHLIGHTS

1. Single +5 V power supply.
2. On-chip autocalibration.
3. Pulse placement flexibility.
4. High resolution: 256 pulse widths.

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

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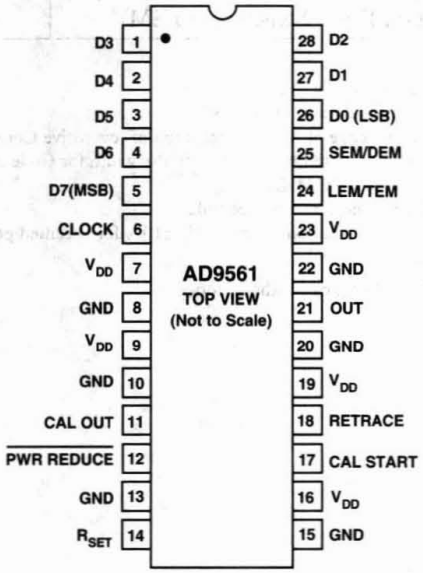
ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD9561JR	0°C to +70°C	28-Lead SOIC
AD9561JR-REEL[2]	0°C to +70°C	28-Lead SOIC

NOTES
[1]For outline information see Package Information section.
[2]Tape and Reel ordered in multiples of 1000 ICs.

PIN CONFIGURATION



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AD9561–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V, R_{SET} = 750 Ω, CLOCK = 20 MHz unless otherwise noted)

Parameter	Temp	Test Level	AD9561KR Min	AD9561KR Typ	AD9561KR Max	Units
RESOLUTION			8			Bits
ACCURACY (@ 20 MHz)						
Differential Nonlinearity	+25°C	I		0.4		LSB
Integral Linearity[1]	+25°C	I		1.5		LSB
Odd/Even Pulse Mismatch[2]	+25°C	V		1.5		LSB
DIGITAL INPUTS						
Logic "1" Voltage	Full	I	2.0			V
Logic "0" Voltage	Full	I			0.8	V
Input Current	Full	I			±1	μA
Input Capacitance	+25°C	V		5		pF
Data Setup Time	+25°C	IV		2	3	ns
Data Hold Time	+25°C	IV		2	3	ns
Data Setup Time	Full	IV			4	ns
Data Hold Time	Full	IV			4	ns
Minimum Clock Pulse Width	Full	V		6		ns
DYNAMIC PERFORMANCE						
Maximum Trigger Rate	Full	IV	50			MHz
Minimum Propagation Delay (t_{PD})[3]	Full	I	TBD	TBD	TBD	ns
Minimum Propagation Delay TC	Full	V		TBD		ps/°C
Output Pulse Width @ Code 25[4]	Full	V		4		ns
Output Pulse Width @ Code 254	Full	V		100		% Clock
Output Rise Time (into 10 pF)[5]	Full	I		1.5	3	ns
Output Fall Time (into 10 pF)[5]	Full	I		1.5	3	ns
PWM OUTPUT						
Logic "1" Voltage (2 mA Load)	Full	I	4.6			V
Logic "0" Voltage (2 mA Load)	Full	I			0.4	V
POWER SUPPLY[6]						
Positive Supply Current (+5.0 V)	Full	I		140	170	mA
Power Dissipation	Full	I		700	850	mW
Power Down Current	Full	I		70	85	mA
Power Down Dissipation	Full	I		350	425	mW
Power Supply Rejection Ratio Propagation Delay Sensitivity (TEM)[7]	+25°C	V		TBD		ns/V

PRELIMINARY TECHNICAL DATA

NOTES
[1]Best Fit between Codes 25 and 235.
[2]Due to mismatch in dual ramp linearities
[3]Measured from rising edge of clock to transition of overdrive Codes 0 and 255.
[4]Minimum pulse width limited by rise time. Pulse width for Code 25 will be greater when CLOCK < 20 MHz.
[6]Output load = 10 pF and 2 mA source/sink.
[6]Power supply should be maintained at +5 V, ±10% for specified performance.
[7]Tested from +4.5 V to +5.5 V.

Specification subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage	+7 V
Digital Input Voltage Range	–0.5 V to +5 V
Minimum R_{SET}	TBD Ω
Digital Output Current (Sourcing)[2]	10 mA
Digital Output Current (Sinking)[2]	10 mA
Operating Temperature Range[3]	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
Lead Soldering Temperature (10 sec)[4]	+300°C

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability may be impaired. Functional operation under any of these conditions is not necessarily implied.
[2]CAL OUT should drive a single high impedance input.
[3]Typical Thermal Impedance: 28-lead SOIC (plastic); q_{JA} = °C/W; q_{JC} = °C/W.
[4]When soldering surface mount packages in vapor phase equipment, temperature should not exceed 220°C for more than one minute.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

200 MHz Laser Diode Driver with Light Power Control

AD9660

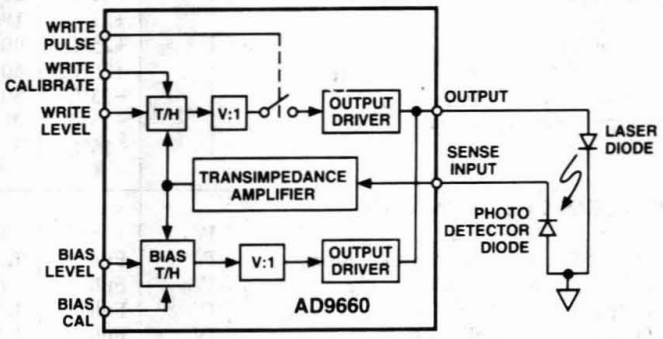
FEATURES

1.5 ns Rise/2.0 ns Fall Times
Output Current: 180 mA @ 3 V, 200 mA @ 2.5 V
Bias Current: 90 mA @ 3 V
Modulation Current: 60 mA @ 3 V
Offset Current: 30 mA @ 3 V
Single +5 V Power Supply
Switching Rate: 200 MHz
Onboard Light Power Control Loops

APPLICATIONS

Laser Printers and Copiers
Optical Disk Drives
FO Datacomm

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9660 is a highly integrated driver for laser diode applications such as optical disk drives, printers, and copiers. The AD9660 gets feedback from an external photo detector and includes two analog feedback loops to allow users to set "bias" and "write" (for optical disk drives) power levels of the laser, and switch between the two power levels at up to 200 MHz. Output rise and fall times are typically 1.5 ns and 2.0 ns to complement printer applications that use image enhancing techniques such as pulse width modulation to achieve gray scale, and allow disk drive applications to improve density and take advantage of pulsed write formats. Control signals are TTL/CMOS compatible.

The driver output provides up to 180 mA of current @ 3 V, 90 mA of BIAS current, 60 mA of modulation current, and 30 mA of offset current. The onboard disable circuit turns off the output drivers and returns the light power control loops to a safe state.

The AD9660 can also be used in closed loop applications in which the output power level follows an analog WRITE LEVEL voltage input. By optimizing the external hold capacitor, and the photo detector, the write loop can achieve bandwidths as high as 25 MHz.

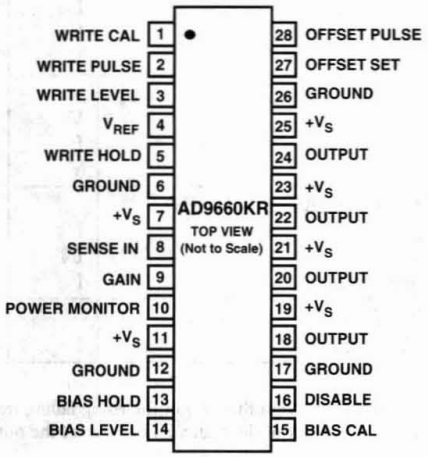
The AD9660 is offered in a 28-pin plastic SOIC for operation over the commercial temperature range (0°C to +70°C).

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9660KR	0°C to +70°C	R-28
AD9660KR-REEL	0°C to +70°C	R-28 (1000/reel)

*For outline information see Package Information section.

PIN ASSIGNMENTS



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AD9660–SPECIFICATIONS

($+V_S$ = +5 V, Temperature = +25°C unless otherwise noted. Sourced currents defined as positive.)

Parameter	Test Level	Temp	AD9660KR Min	Typ	Max	Units	Conditions
ANALOG INPUTS (WRITE LEVEL, BIAS LEVEL)							
Input Voltage Range	IV	Full	V_{REF}		V_{REF} + 1.6	V	
Input Bias Current	I	+25°C	–50		+50	µA	
Analog Bandwidth	V	Full		25		MHz	External Hold Cap = 20 pF
OUTPUTS							
Maximum Output Current, I_{OUT}	I	+25°C	200			mA	V_{OUT} = 2.5 V
I_{OUT}	I	+25°C	180			mA	V_{OUT} = 3.0 V
Bias Current, I_{BIAS}	I	+25°C	90			mA	V_{OUT} = 3.0 V
Modulation Current, $I_{MODULATION}$	I	+25°C	60			mA	V_{OUT} = 3.0 V
Offset Current, I_{OFFSET}	I	+25°C	30			mA	V_{OUT} = 3.0 V
Output Compliance Range	I	+25°C	0		3.0	V	
Idle Current	I	+25°C	3		13	mA	WRITE PULSE = LOW, DISABLE = HIGH
SWITCHING PERFORMANCE							
Maximum Pulse Rate	IV	+25°C	200	250		MHz	3 dB Reduction in I_{OUT}
Output Propagation Delay (t_{PD}), Rising[1]	IV	Full	1.6		3.0	ns	
Output Propagation Delay (t_{PD}), Falling[1]	IV	Full	1.6		2.5	ns	
Output Current Rise Time[2]	IV	Full	1.1	1.5	1.7	ns	
Output Current Fall Time[3]	IV	Full	1.4	2.0	2.8	ns	
WRITE CAL Aperture Delay[4]	V	+25°C		13		ns	
Disable Time[5]	V	+25°C		5		ns	
HOLD NODES (WRITE HOLD, BIAS HOLD)							
Input Bias Current	I	+25°C	–200		200	nA	V_{HOLD} = 2.5 V
Input Voltage Range	IV	Full	V_{REF}		V_{REF} + 1.6	V	Open Loop Application Only
Minimum External Hold Cap	V	Full		20		pF	
TTL INPUTS[6]							
Logic "1" Voltage	I	+25°C	2.0			V	DISABLE = LOW
Logic "1" Voltage	IV	Full	2.0			V	While Other
Logic "0" Voltage	I	+25°C			0.8	V	TTL Inputs Are
Logic "0" Voltage	IV	Full			0.8	V	Tested
Logic "1" Current	I	+25°C	–10	20	10	µA	
Logic "0" Current	I	+25°C	–1.5			mA	
BANDGAP REFERENCE							
Output Voltage V_{REF}	I	+25°C	1.55	1.75	1.90	V	
Temperature Coefficient	V			–0.2		mV/°C	
Output Current	V	+25°C	–0.5		1.0	mA	
SENSE IN							
Current Gain	V	+25°C		1.85		mA/mA	
Voltage	I	+25°C	3.7	4.0	4.3	V	$I_{MONITOR}$ = 2 mA
Input Resistance	V	+25°C		<150		Ω	
POWER SUPPLY (DISABLE = HIGH)							
$+V_S$ Voltage	I	+25°C	4.75	5.00	5.25	V	DISABLE = HIGH
$+V_S$ Current	I	+25°C	75	110	150	mA	
Power Dissipation	I	+25°C		550		mW	
OFFSET CURRENT							
OFFSET SET Voltage	I	+25°C	1.1	1.4	1.7	V	$I_{MONITOR}$ = 4.0 mA

NOTES

[1]Propagation delay measured from the 50% of the rising/falling transition of WRITE PULSE to 50% point of the rising/falling edge of the output modulation current.

[2]Rise time measured between the 10% and 90% points of the rising transition of the modulation current.

[3]Fall time measured between the 10% and 90% points of the falling transition of the modulation current.

[4]Aperture Delay is measured from the 50% point of the rising edge of WRITE PULSE to the time when the output modulation begins to recalibrate, WRITE CAL is held during this test.

[5]Disable Time is measured from the 50% point of the rising edge of DISABLE to the 50% point of the falling transition of the output current. Fall time during disable is similar to fall time during normal operation.

[6]WRITE PULSE, WRITE CAL, BIAS CAL, OFFSET PULSE are TTL compatible inputs.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
V_{REF} Current	2 mA
WRITE LEVEL, BIAS LEVEL	–0.5 V to $+V_S$
TTL INPUTS	–0.5 V to $+V_S$
Output Current	300 mA
Operating Temperature	
AD9660KR	0°C to +70°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature[2]	+150°C
Lead Soldering Temp (10 sec)	+300°C

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]Typical thermal impedance is θ_{JA} = 45°C/W, θ_{JC} = 41°C/W.

Laser Diode Driver with Light Power Control

AD9661A

FEATURES
< 2 ns Rise/Fall Times
Output Current: 120 mA
Single +5 V Power Supply
Switching Rate: 200 MHz typ
Onboard Light Power Control Loop

APPLICATIONS
Laser Printers and Copiers

GENERAL DESCRIPTION

The AD9661A is a highly integrated driver for laser diode applications such as printers and copiers. The AD9661A gets feedback from an external photo detector and includes an analog feedback loop to allow users to set the power level of the laser, and switch the laser on and off at up to 100 MHz. Output rise and fall times are 2 ns to complement printer applications that use image enhancing techniques such as pulse width modulation to achieve gray scale and resolution enhancement. Control signals are TTL/CMOS compatible.

The driver output provides up to 120 mA of current into an infrared N type laser, and the onboard disable circuit turns off the output driver and returns the light power control loop to a safe state.

The AD9661A can also be used in closed-loop applications in which the output power level follows an analog POWER LEVEL voltage input. By optimizing the external hold capacitor and the photo detector, the loop can achieve bandwidths as high as 25 MHz.

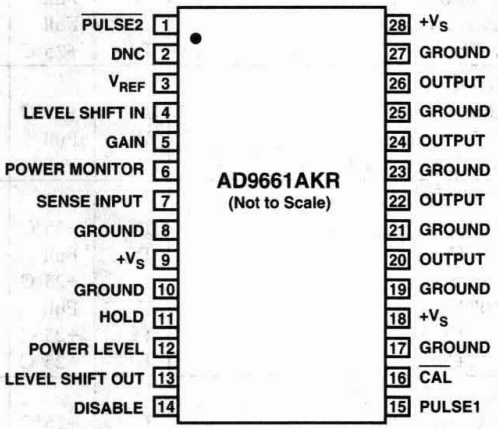
The AD9661A is offered in a 28-pin plastic SOIC for operation over the commercial temperature range (0°C to +70°C).

ORDERING GUIDE

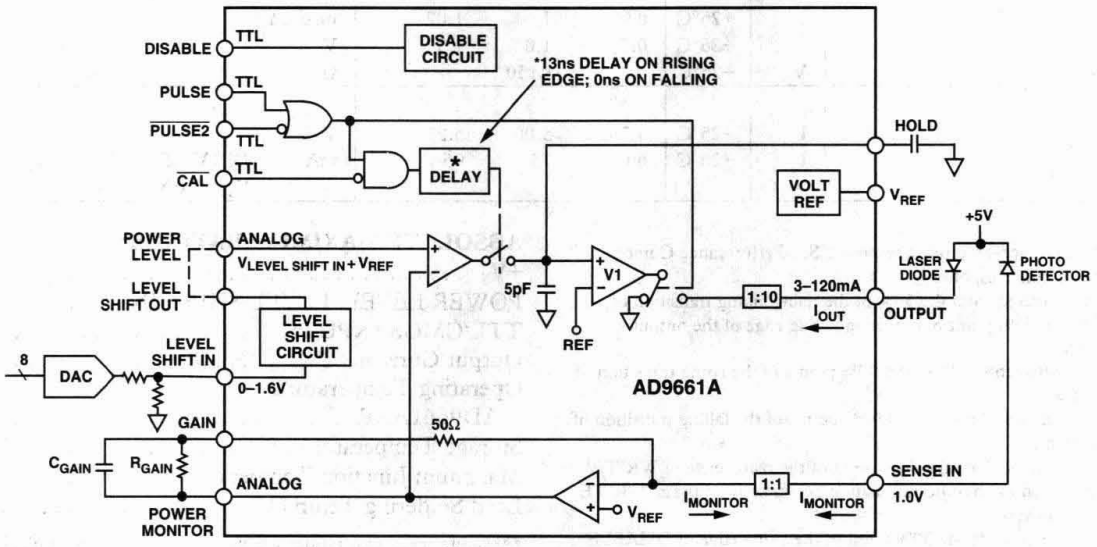
Model	Temperature Range	Package Option*
AD9661AKR	0°C to +70°C	R-28
AD9661AKR-REEL	0°C to +70°C	R-28 (1000/Reel)

*For outline information see Package Information section.

PIN ASSIGNMENTS



FUNCTIONAL BLOCK DIAGRAM



AD9661A–SPECIFICATIONS ($+V_S$ = +5 V, Temperature = +25°C unless otherwise noted)

Parameter	Test Level	Temp	AD9661AKR Min	Typ	Max	Units	Conditions
ANALOG INPUT							
Input Voltage Range, POWER LEVEL	IV	Full	V_{REF}		V_{REF} + 1.6	V	
Input Bias Current, POWER LEVEL	I	+25°C	–50		+50	µA	
Analog Bandwidth, Control Loop[1]	V	+25°C		25		MHz	C_{HOLD} = 33 pF, R_F = 1 kΩ, C_F = 2 pF
Input Voltage Range, LEVEL SHIFT IN	IV	Full	0.1		1.6	V	
Input Bias Current, LEVEL SHIFT IN	I	+25°C	–10		0	µA	
Analog Bandwidth, Level Shift[2]	V	Full		130		MHz	
Level Shift Offset	I	+25°C	–32		+32	mV	
Level Shift Gain	I	+25°C	0.95	1.0	1.05	V/V	
OUTPUTS							
Output Current, I_{OUT}	I	+25°C	120			mA	V_{OUT} = 2.5 V
Output Compliance Range	IV	+25°C	2.50		5.25	V	
Idle Current	I	+25°C		2	5.0	mA	PULSE = LOW, DISABLE = LOW
Disable Current	IV	+25°C			1.0	µA	PULSE = LOW, DISABLE = HIGH
SWITCHING PERFORMANCE							
Maximum Pulse Rate	V	+25°C		200		MHz	Output Current –3 dB
Output Propagation Delay (t_{PD}), Rising[3]	IV	Full	2.9	3.9	5.0	ns	
Output Propagation Delay (t_{PD}), Falling[3]	IV	Full	3.2	3.7	4.3	ns	
Output Current Rise Time[4]	IV	Full		1.5	2.0	ns	
Output Current Fall Time[5]	IV	Full		1.5	2.0	ns	
$\overline{CAL}$ Aperture Delay[6]	IV	Full		13		ns	
Disable Time[7]	IV	+25°C		3	5	ns	
HOLD NODE							
Input Bias Current	I	+25°C	–200		200	nA	V_{HOLD} = 2.5 V
Input Voltage Range	IV	Full	V_{REF}		V_{REF} + 1.6	V	Open-Loop Application Only
Minimum External Hold Cap	V	Full		25		pF	
TTL/CMOS INPUTS[8]							
Logic "1" Voltage	I	+25°C	2.0			V	
Logic "1" Voltage	IV	Full	2.0			V	
Logic "0" Voltage	I	+25°C			0.8	V	
Logic "0" Voltage	IV	Full			0.8	V	
Logic "1" Current	I	+25°C	–10		10	µA	V_{HIGH} = 5.0 V
Logic "0" Current	I	+25°C	–1.5			mA	V_{LOW} = 0.8 V
BANDGAP REFERENCE							
Output Voltage (V_{REF})	I	+25°C	1.6	1.8	1.9	V	
Temperature Coefficient	V	+25°C		–0.1		mV/°C	
Output Current	V	+25°C	–0.5		1.0	mA	
SENSE IN							
Current Gain	I	+25°C	0.95	1	1.02	mA/mA	
Voltage	I	+25°C	0.7	1.0	1.3	V	
Input Resistance	V	+25°C		<150		Ω	
POWER SUPPLY							
$+V_S$ Voltage	I	+25°C	4.75	5.00	5.25	V	
$+V_S$ Current	I	+25°C	60	75	95	mA	DISABLE = HIGH, V_{HOLD} = V_{REF}, V_S = 5.0 V

NOTES

[1]Based on rise time of closed-loop pulse response. See Performance Curves.

[2]Based on rise time of pulse response.

[3]Propagation delay measured from the 50% of the rising/falling transition of WRITE PULSE to the 50% point of the rising/falling edge of the output modulation current.

[4]Rise time measured between the 10% and 90% points of the rising transition of the modulation current.

[5]Fall time measured between the 10% and 90% points of the falling transition of the modulation current.

[6]Aperture Delay is measured from the 50% point of the rising edge of WRITE PULSE to the time when the output modulation begins to recalibrate, WRITE CAL is held during this test.

[7]Disable Time is measured from the 50% point of the rising edge of DISABLE to the 50% point of the falling transition of the output current. Fall time during disable is similar to fall time during normal operation.

[8]PULSE, $\overline{PULSE2}$, DISABLE, and $\overline{CAL}$ are TTL/CMOS compatible inputs.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$	+6 V
POWER LEVEL, LEVEL SHIFT IN	0 V to $+V_S$
TTL/CMOS INPUTS	–0.5 V to $+V_S$
Output Current	200 mA
Operating Temperature	
AD9661AKR	0°C to +70°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	+150°C
Lead Soldering Temp (10 sec)	+300°C

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

µP Supervisory Circuits & Reset Generators
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μP Supervisory Circuits & Reset Generators–Selection Guides

With On-Chip V_{BATT} Switch

Model	V_{CC} Range Min	V_{BATT} Range Min	Battery Switch Mode V_{CC} Mode V_{OUT} I_{OUT} = 1 mA Min	Battery Switch Mode V_{CC} Mode V_{OUT} I_{OUT} = 100 mA Min	V_{BB} Indicator	Reset Generator Threshold min Volts	Reset Timeout Delay ms Min	Reset Timeout Delay ms Max	# Pins	Page No.	Comments	Fax-code
ADM696	+3	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	Yes	+1.25	35	70	16	23–7	With Low-Line Input	1568
ADM690	+4.75	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	No	+4.5	35	70	8	23–5		1562
ADM691	+4.75	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	No	+4.25	35	70	16	23–5	Full Feature Set	1562
ADM692	+4.5	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	No	+4.25	35	70	8	23–5		1562
ADM693	+4.5	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	Yes	+4.5	35	70	16	23–5	Full Feature Set	1562
ADM694	+4.75	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	No	+4.5	140	280	8	23–5		1562
ADM695	+4.75	+2	V_{CC} – 50 mV	V_{CC} – 500 mV	Yes	+4.5	140	280	16	23–5	Full Feature Set	1562

Without On-Chip V_{BATT} Switch

Model	V_{CC} Range Min	V_{BATT} Range Min	Battery Switch Mode V_{CC} Mode V_{OUT} I_{OUT} = 1 mA Min	Battery Switch Mode V_{CC} Mode V_{OUT} I_{OUT} = 100 mA Min	V_{BB} Indicator	Reset Generator Threshold Min Volts	Reset Timeout Delay ms Min	Reset Timeout Delay ms Max	# Pins	Page No.	Comments	Fax-code
ADM697	+3	NA	NA	NA	NA	+1.25	35	70	16	23–7	5 ns/$\overline{CE}$ Output	1568
ADM698	+3	NA	NA	NA	NA	+4.5	140	280	8	23–9		1570
ADM699	+3	NA	NA	NA	NA	+4.5	140	280	8	23–9	With Watchdog Input	1570

Reset Generators with Debounced Manual Input

Model	Reset Threshold Voltage Min	Power Fail Indicator	Power Fail Threshold min/max Volts	Reset Timeout Delay ms Min	Reset Timeout Delay ms Max	Watchdog Timeout (Long) Int. Oscillator min/max sec	WD Timer Input Width ns	# Pins	Page No.	Comments	Fax-code
ADM706P†	+2.55	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +2.7 V to +5.5 V	1866
ADM706R	+2.55	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +2.7 V to +5.5 V	1866
ADM708R	+2.55	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +2.7 V to +5.5 V	1866
ADM706S	+2.85	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +3.0 V to +5.5 V	1866
ADM708S	+2.85	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +3.0 V to +5.5 V	1866
ADM706T	+3	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +3.5 V to +5.5 V	1866
ADM708T	+3	Yes	1.2/1.3	160	280	1/2.25	100	8	23–13	V_{CC} = +3.5 V to +5.5 V	1866
ADM706	+4.25	Yes	1.2/1.3	160	280	1/2.25	50	8	23–11	V_{CC} = +4.5 V to +5.5 V	1865
ADM708	+4.25	Yes	1.2/1.3	160	280	1/2.25		8	23–11	V_{CC} = +4.5 V to +5.5 V	1865
ADM705	+4.5	Yes	1.2/1.3	160	280	1/2.25	50	8	23–11	V_{CC} = +4.5 V to +5.5 V	1865
ADM707	+4.5	Yes	1.2/1.3	160	280	1/2.25		8	23–11	V_{CC} = +4.5 V to +5.5 V	1865
ADM709L	+4.5	No		140	380			8	23–15	V_{CC} = +4.5 V to +5.5 V	1893
ADM709M	+4.25	No		140	380			8	23–15	V_{CC} = +4.5 V to +5.5 V	1893
ADM709T	+3	No		140	380			8	23–15	V_{CC} = +3.15 V to +5.5 V	1893
ADM709S	+2.85	No		140	380			8	23–15	V_{CC} = +3 V to +5.5 V	1893
ADM709R	+2.55	No		140	380			8	23–15	V_{CC} = +2.7 V to +5.5 V	1893

†Active high reset output.

ANALOG DEVICES

Microprocessor Supervisory Circuits

ADM690–ADM695

FEATURES

Superior Upgrade for MAX690–MAX695
Specified Over Temperature
Low Power Consumption (5 mW)
Precision Voltage Monitor
Reset Assertion Down to 1 V V_{CC}
Low Switch On-Resistance 1.5 Ω Normal, 20 Ω in Backup
High Current Drive (100 mA)
Watchdog Timer—100 ms, 1.6 s, or Adjustable
600 nA Standby Current
Automatic Battery Backup Power Switching
Extremely Fast Gating of Chip Enable Signals (5 ns)
Voltage Monitor for Power Fail

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems

GENERAL DESCRIPTION

The ADM690–ADM695 family of supervisory circuits offers complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include µP reset, backup battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning. The complete family provides a variety of configurations to satisfy most microprocessor system requirements.

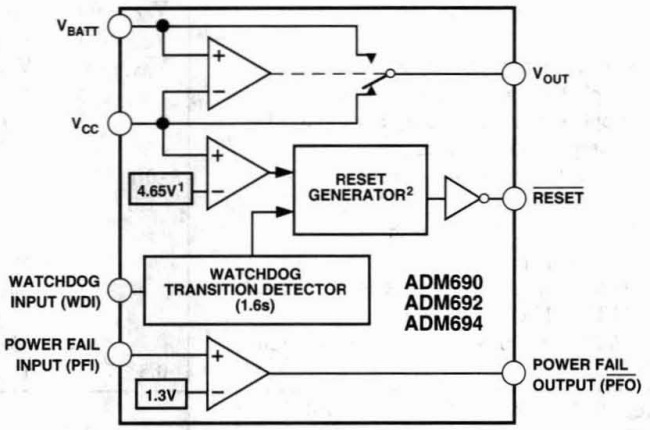
The ADM690, ADM692 and ADM694 are available in 8-pin DIP packages and provide:

1. Power-on reset output during power-up, power-down and brownout conditions. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.3 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5 V.

The ADM691, ADM693 and ADM695 are available in 16-pin DIP and small outline packages and provide three additional functions.

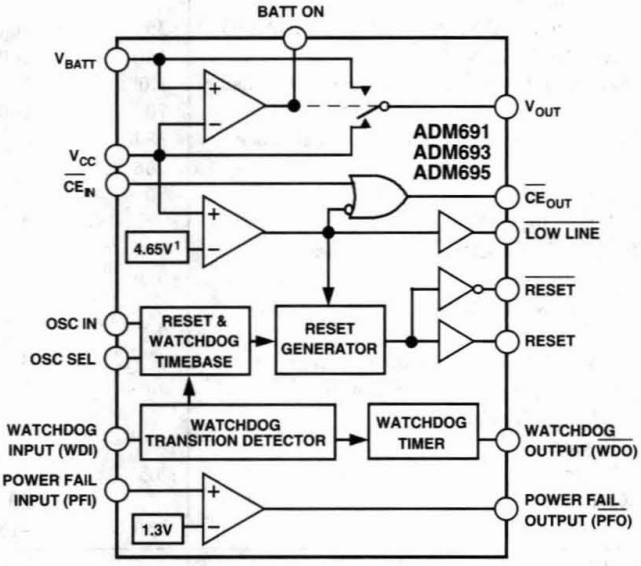
1. Write protection of CMOS RAM or EEPROM.
2. Adjustable reset and watchdog timeout periods.
3. Separate watchdog timeout, backup battery switchover, and low V_{CC} status outputs.

FUNCTIONAL BLOCK DIAGRAMS



[1]VOLTAGE DETECTOR = 4.65V (ADM690, ADM694)
4.40V (ADM692)

[2]RESET PULSE WIDTH = 50ms (ADM690, ADM692)
200ms (ADM694)



[1]VOLTAGE DETECTOR = 4.65V (ADM691, ADM695)
4.40V (ADM693)

The ADM690–ADM695 family is fabricated using an advanced epitaxial CMOS process combining low power consumption (5 mW), extremely fast Chip Enable gating (5 ns) and high reliability. $\overline{\text{RESET}}$ assertion is guaranteed with V_{CC} as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop thereby permitting increased output current drive of up to 100 mA without the need for an external pass transistor.

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ADM690–ADM695–SPECIFICATIONS (V_{CC} = Full Operating Range, V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	4.75		5.5	V	
ADM692, ADM693	4.5		5.5	V	
V_{BATT} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	2.0		4.25	V	
ADM692, ADM693	2.0		4.0	V	
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.025		V	I_{OUT} = 1 mA
	V_{CC} – 0.5	V_{CC} – 0.25		V	$I_{OUT} \leq$ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.02		V	I_{OUT} = 250 µA, $V_{CC} < V_{BATT}$ – 0.2 V
Supply Current (Excludes I_{OUT})		1	1.95	mA	I_{OUT} = 100 mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	T_A = +25°C
	–1.0		+0.02	µA	
Battery Switchover Threshold		70		mV	Power Up
V_{CC} – V_{BATT}		50		mV	Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.3	V	I_{SINK} = 3.2 mA
BATT ON Output Short Circuit Current		35		mA	BATT ON = V_{OUT} = 4.5 V Sink Current
	0.5	1	25	µA	BATT ON = 0 V Source Current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold					
ADM690, ADM691, ADM694, ADM695	4.5	4.65	4.73	V	
ADM692, ADM693	4.25	4.4	4.48	V	
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
ADM690, ADM691, ADM692, ADM693	35	50	70	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
ADM694, ADM695	140	200	280	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period, V_{CC} = 5 V, T_A = +25°C
	70	100	140	ms	Short Period, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, External Clock	3840		4097	Cycles	Long Period
	768		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
$\overline{\text{RESET}}$ Output Voltage @ V_{CC} = +1 V		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
$\overline{\text{RESET}}$, $\overline{\text{LOW LINE}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{\text{RESET}}$, $\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 4.25 V
Output Short Circuit Source Current	1	3	25	µA	
Output Short Circuit Sink Current		25		mA	
WDI Input Threshold					V_{CC} = 5 V[1]
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{OUT}, T_A = +25°C
	–50	–15		µA	WDI = 0 V, T_A = +25°C
POWER FAIL DETECTOR					
PFI Input Threshold	1.25	1.3	1.35	V	V_{CC} = +5 V
PFI Input Current	–25	±0.01	+25	nA	
$\overline{\text{PFO}}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	3.5			V	I_{SOURCE} = 1 µA
$\overline{\text{PFO}}$ Short Circuit Source Current	1	3	25	µA	PFI = Low, $\overline{\text{PFO}}$ = 0 V
$\overline{\text{PFO}}$ Short Circuit Sink Current		25		mA	PFI = High, $\overline{\text{PFO}}$ = V_{OUT}
CHIP ENABLE GATING					
$\overline{\text{CE}}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}
$\overline{\text{CE}}_{IN}$ Pull-Up Current		3		µA	
$\overline{\text{CE}}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	V_{OUT} – 1.5			V	I_{SOURCE} = 3.0 mA
	V_{OUT} – 0.05			V	I_{SOURCE} = 1 µA, V_{CC} = 0 V
$\overline{\text{CE}}$ Propagation Delay		5	9	ns	

Specifications subject to change without notice.

ANALOG DEVICES

Microprocessor Supervisory Circuits

ADM696/ADM697

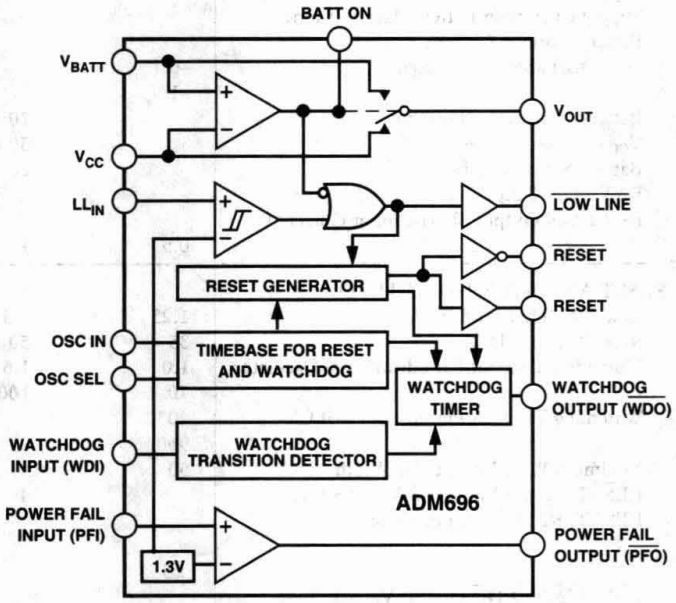
FEATURES

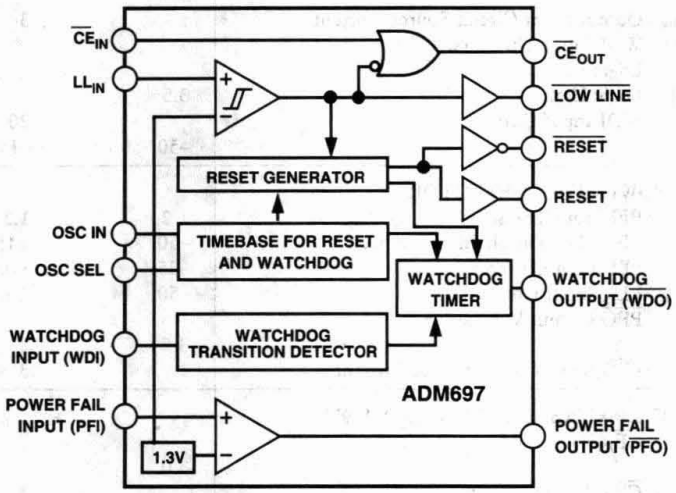
Superior Upgrade for MAX696/MAX697
Specified Over Temperature
Adjustable Low Line Voltage Monitor
Power OK/Reset Time Delay
Reset Assertion Down to 1 V V_{CC}
Watchdog Timer—100 ms, 1.6 s, or Adjustable
Low Switch On Resistance
1.5 Ω Normal, 20 Ω in Backup
600 nA Standby Current
Automatic Battery Backup Switching (ADM696)
Fast On-Board Gating of Chip Enable Signals (ADM697)
Voltage Monitor for Power Fail or Low Battery Warning

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The ADM696/ADM697 supervisory circuits offer complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include µP reset, backup-battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning.

The ADM696/ADM697 are available in 16-pin DIP and small outline packages and provide the following functions:

1. Power-On Reset output during power-up, power-down and brownout conditions. The RESET voltage threshold is adjustable using an external voltage divider. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.
2. A Reset pulse if the optional watchdog timer has not been toggled within specified time.
3. Separate watchdog time-out and low line status outputs.
4. Adjustable reset and watchdog timeout periods.
5. A 1.3 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than V_{CC}.
6. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic (ADM696).
7. Write protection of CMOS RAM or EEPROM (ADM697).

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM696AN	–40°C to +85°C	N-16
ADM696AR	–40°C to +85°C	R-16
ADM696AQ	–40°C to +85°C	Q-16
ADM696SQ	–55°C to +125°C	Q-16
ADM697AN	–40°C to +85°C	N-16
ADM697AR	–40°C to +85°C	R-16
ADM697AQ	–40°C to +85°C	Q-16
ADM697SQ	–55°C to +125°C	Q-16

*For outline information see Package Information section.

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ADM696/ADM697–SPECIFICATIONS (V_{CC} = Full Operating Range, V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	3.0		5.5	V	
V_{BATT} Operating Voltage Range	2.0		V_{CC} – 0 3	V	
BATTERY BACKUP SWITCHING (ADM696)					
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.025		V	I_{OUT} = 1 mA
	V_{CC} – 0.5	V_{CC} – 0.25		V	I_{OUT} ≤ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.02		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} – 0.2 V
Supply Current (Excludes I_{OUT})		1	1.95	mA	I_{OUT} = 100 mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	T_A = +25°C
	–1		+0.02	µA	
Battery Switchover Threshold		70		mV	Power-Up
V_{CC} – V_{BATT}		50		mV	Power-Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.4	V	I_{SINK} = 1.6 mA
BATT ON Output Short Circuit Current		7		mA	BATT ON = V_{OUT} = 2.4 V Sink Current
	0.5	1	25	µA	BATT ON = V_{OUT}, V_{CC} = 0 V, Source Current
RESET AND WATCHDOG TIMER					
Low Line Threshold (LL_{IN})	1.25	1.3	1.35	V	V_{CC} = +5 V, +3 V
Reset Timeout Delay	35	50	70	ms	OSC SEL = HIGH, V_{CC}= 5 V, T_A = +25°C
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period, V_{CC} = 5 V, T_A = +25°C
	70	100	140	ms	Short Period, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, External Clock	4032		4097	Cycles	Long Period
	960		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V, V_{CC} = 5 V
$\overline{RESET}$ Output Voltage @ V_{CC} = +1 V		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
RESET, $\overline{RESET}$ Output Voltage			0.4	V	I_{SINK} = 400 µA, V_{CC} = 2 V, V_{BATT} = 0 V
			0.4	V	I_{SINK} = 1.6 mA, 3 V < V_{CC} < 5.5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{LOW\ LINE}$, $\overline{WDO}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA,
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
Output Short Circuit Source Current	1	3	25	µA	
WDI Input Threshold					V_{CC} = 5 V[1]
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WD1 = V_{OUT}, (V_{CC}) T_A = +25°C
	–50	–15		µA	WD1 = 0 V, T_A = +25°C
POWER FAIL DETECTOR					
PFI Input Threshold	1.2	1.3	1.4	V	V_{CC} = +3 V, +5 V
PFI–LL_{IN} Threshold Difference	–50	±15	+50	mV	V_{CC} = +3 V, +5 V
PFI Input Current	–25	±0.01	+25	nA	
LL_{IN} Input Current	–50	±0.01	+50	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{PFO}$ Short Circuit Source Current	1	3	25	µA	PFI = Low, $\overline{PFO}$ = 0 V
CHIP ENABLE GATING (ADM697)					
$\overline{CE}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}, V_{CC} = 5 V
$\overline{CE}_{IN}$ Pullup Current		3		µA	
$\overline{CE}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA
	V_{CC} – 0.5			V	I_{SOURCE} = 800 µA
$\overline{CE}$ Propagation Delay		5	25	ns	
OSCILLATOR					
OSC IN Input Current		±2		µA	
OSC SEL Input Pullup Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0 V
OSC IN Frequency with Ext. Capacitor		4		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

NOTE

[1]WDI is a three-level input which is internally biased to 38% of V_{CC} and has an input impedance of approximately 125 kΩ.

Specifications subject to change without notice.

ANALOG DEVICES

Microprocessor Supervisory Circuits

ADM698/ADM699

FEATURES

Superior Upgrade for MAX698/MAX699
Guaranteed $\overline{\text{RESET}}$ Assertion with V_{CC} = 1 V
Low 0.6 mA Supply Current
Precision 4.65 V Voltage Monitor
Power OK/Reset Time Delay
Watchdog Timer
Minimum Component Count
Performance Specified over Temperature

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

GENERAL DESCRIPTION

The ADM698/ADM699 supervisory circuits provide power supply monitoring and watchdog timing for microprocessor systems.

The ADM698 monitors the 5 V V_{CC} power supply and generates a $\overline{\text{RESET}}$ pulse during power up, power down and during low voltage "Brown Out" conditions. The $\overline{\text{RESET}}$ output is guaranteed to be functional (logic low) with V_{CC} as low as 1 V.

The ADM699 features an identical monitoring circuit as in the ADM698 plus an additional watchdog timer input to monitor microprocessor activity. The $\overline{\text{RESET}}$ output is forced low if the watchdog input is not toggled within the 1 second watchdog timeout period.

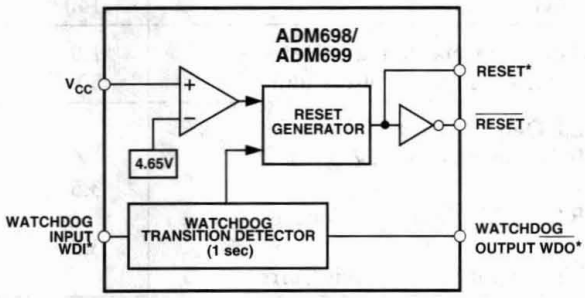
Both parts are available in 8-pin plastic DIP and 16-lead SOIC packages. The 16-lead SOIC contains additional outputs $\overline{\text{RESET}}$ (without inversion) and Watchdog Output $\overline{\text{WDO}}$ (ADM699 only).

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM698AN	–40°C to +85°C	N-8
ADM698AR	–40°C to +85°C	R-16
ADM698AQ	–40°C to +85°C	Q-8
ADM698SQ	–55°C to +125°C	Q-8
ADM699AN	–40°C to +85°C	N-8
ADM699AR	–40°C to +85°C	R-16
ADM699AQ	–40°C to +85°C	Q-8
ADM699SQ	–55°C to +125°C	Q-8

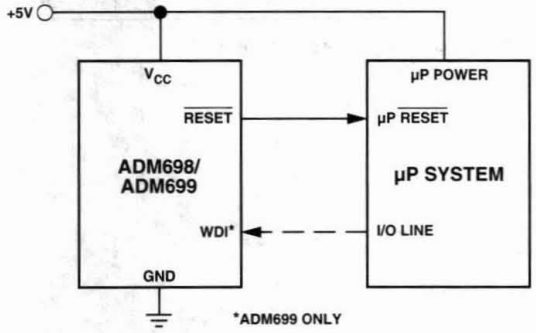
For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



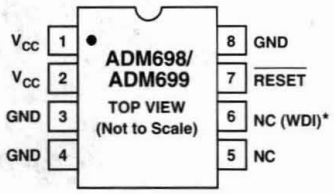
*WDI (ADM699 ONLY)
$\overline{\text{RESET}}$ (SOIC ONLY)
$\overline{\text{WDO}}$ (ADM699 SOIC ONLY)

TYPICAL APPLICATION CIRCUIT



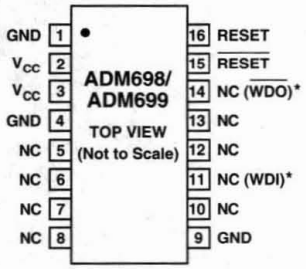
*ADM699 ONLY

PIN CONFIGURATION (DIP)



*( ) ADM699 ONLY
NC = NO CONNECT

PIN CONFIGURATION (SOIC)



*( ) ADM699 ONLY
NC = NO CONNECT

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ADM698/ADM699–SPECIFICATIONS (V_{CC} = +5 V ± 10%, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	3.0		5.5	V	
Supply Current		0.6	1.95	mA	
Power-Down Reset Assertion	4.5	4.65	4.73	V	
Power-Up Reset Deassertion			4.73	V	
Reset Threshold Hysteresis		40		mV	
Reset Active Time	140	200	280	ms	T_A = +25°C, V_{CC} = +5 V
Watchdog Timeout Period (ADM699)	1.0	1.6	2.25	s	T_A = +25°C, V_{CC} = +5 V
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
$\overline{\text{RESET}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.4 V
$\overline{\text{RESET}}$ Output Voltage (V_{CC} = 1 V)		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1.0 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
RESET and $\overline{\text{WDO}}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 4.4 V
$\overline{\text{RESET}}$ Output Short Circuit Current		25		mA	Output Sink Current
WDI Input Threshold (ADM699)					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{CC}, T_A = +25°C
	–50	–20		µA	WDI = 0 V, T_A = +25°C

Specifications subject to change without notice.

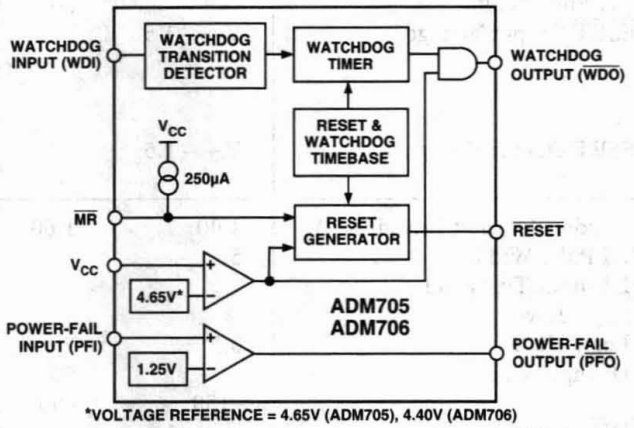
Low Cost µP Supervisory Circuits

ADM705–ADM708

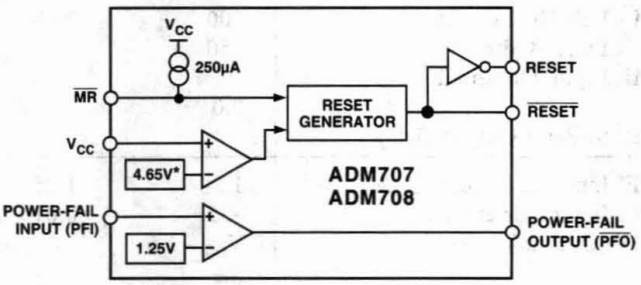
FEATURES
- Guaranteed $\overline{\text{RESET}}$ Valid with V_{CC} = 1 V
- 190 µA Quiescent Current
- Precision Supply-Voltage Monitor
  - +4.65 V (ADM705/ADM707)
  - +4.40 V (ADM706/ADM708)
- 200 ms Reset Pulse Width
- Debounced TTL/CMOS Manual Reset Input ($\overline{\text{MR}}$)
- Independent Watchdog Timer—1.6 sec Timeout (ADM705/ADM706)
- Active High Reset Output (ADM707/ADM708)
- Voltage Monitor for Power-Fail or Low Battery Warning
- Superior Upgrade for MAX705–MAX708

APPLICATIONS
- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Critical µP Monitoring
- Automotive Systems
- Critical µP Power Monitoring

FUNCTIONAL BLOCK DIAGRAMS



*VOLTAGE REFERENCE = 4.65V (ADM705), 4.40V (ADM706)



*VOLTAGE REFERENCE = 4.65V (ADM707), 4.40V (ADM708)

GENERAL DESCRIPTION

The ADM705–ADM708 are low cost µP supervisory circuits. They are suitable for monitoring the +5 V power supply/battery and can also monitor microprocessor activity.

The ADM705/ADM706 provide the following functions:

1. Power-On Reset output during power-up, power-down and brownout conditions. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.
2. Independent watchdog timeout, $\overline{\text{WDO}}$, that goes low if the watchdog input has not been toggled within 1.6 seconds.
3. A 1.25 V threshold detector for power-fail warning, low battery detection, or to monitor a power supply other than 5 V.
4. An active low debounced manual reset input ($\overline{\text{MR}}$).

The ADM707/ADM708 differ in that:

1. A watchdog timer function is not available.
2. An active high reset output in addition to the active low output is available.

Two supply-voltage monitor levels are available. The ADM705/ADM707 generate a reset when the supply voltage falls below 4.65 V, while the ADM706/ADM708 requires that the supply falls below 4.40 V before a reset is issued.

All parts are available in 8-pin DIP and SOIC packages.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ADM705–ADM708–SPECIFICATIONS (V_{CC} = +4.75 V to +5.5 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		190	250	µA	
Reset Threshold	4.5	4.65	4.75	V	ADM705, ADM707
	4.25	4.40	4.50	V	ADM706, ADM708
Reset Threshold Hysteresis		40		mV	
Reset Pulse Width	160	200	280	ms	
$\overline{\text{RESET}}$ Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA
			0.3	V	V_{CC} = 1 V, I_{SINK} = 50 µA
			0.3	V	V_{CC} = 1.2 V, I_{SINK} = 100 µA
RESET Output Voltage	V_{CC} – 1.5			V	ADM707, ADM708, I_{SOURCE} = 800 µA
			0.4	V	ADM707, ADM708, I_{SINK} = 1.2 mA
Watchdog Timeout Period (t_{WD})	1.00	1.60	2.25	sec	
WDI Pulse Width (t_{WP})	50			ns	V_{IL} = 0.4 V, V_{IH} = V_{CC} × 0.8
WDI Input Threshold					
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		50	150	µA	WDI = V_{CC}
	–150	–50		µA	WDI = 0 V
$\overline{\text{WDO}}$ Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 1.2 mA
$\overline{\text{MR}}$ Pull-Up Current	100	250	600	µA	$\overline{\text{MR}}$ = 0 V
$\overline{\text{MR}}$ Pulse Width	150			ns	
$\overline{\text{MR}}$ Input Threshold			0.8	V	
	2.0			V	
$\overline{\text{MR}}$ to Reset Output Delay			250	ns	
PFI Input Threshold	1.2	1.25	1.3	V	
PFI Input Current	–25	0.01	25	nA	
PFO Output Voltage	V_{CC} – 1.5			V	I_{SOURCE} = 800 µA
			0.4	V	I_{SINK} = 3.2 mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} ..... –0.3 V to +6 V
All Other Inputs ..... –0.3 V to V_{CC} + 0.3 V
Input Current
  V_{CC} ..... 20 mA
  GND ..... 20 mA
Digital Output Current ..... 20 mA
Power Dissipation, N-8 DIP ..... 727 mW
  θ_{JA} Thermal Impedance ..... 135°C/W
Power Dissipation, SO-8 SOIC ..... 470 mW
  θ_{JA} Thermal Impedance ..... 110°C/W
Operating Temperature Range
  Industrial (A Version) ..... –40°C to +85°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
  Vapor Phase (60 secs) ..... +215°C
  Infrared (15 secs) ..... +220°C
Storage Temperature Range ..... –65°C to +150°C
ESD Rating ..... >5 kV

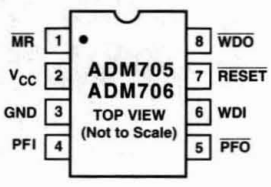
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

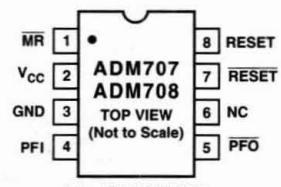
ORDERING GUIDE

Model	Temperature Range	Package Option*
ADM705AN	–40°C to +85°C	N-8
ADM705AR	–40°C to +85°C	SO-8
ADM706AN	–40°C to +85°C	N-8
ADM706AR	–40°C to +85°C	SO-8
ADM707AN	–40°C to +85°C	N-8
ADM707AR	–40°C to +85°C	SO-8
ADM708AN	–40°C to +85°C	N-8
ADM708AR	–40°C to +85°C	SO-8

*For outline information see Package Information section.

PIN CONFIGURATIONS





NC = NO CONNECT

+3 V, Voltage Monitoring µP Supervisory Circuits

ADM706P/R/S/T, ADM708R/S/T

FEATURES

Precision Supply-Voltage Monitor
- **+2.63 V (ADM706P/R, ADM708R)**
- **+2.93 V (ADM706S, ADM708S)**
- **+3.08 V (ADM706T, ADM708T)**

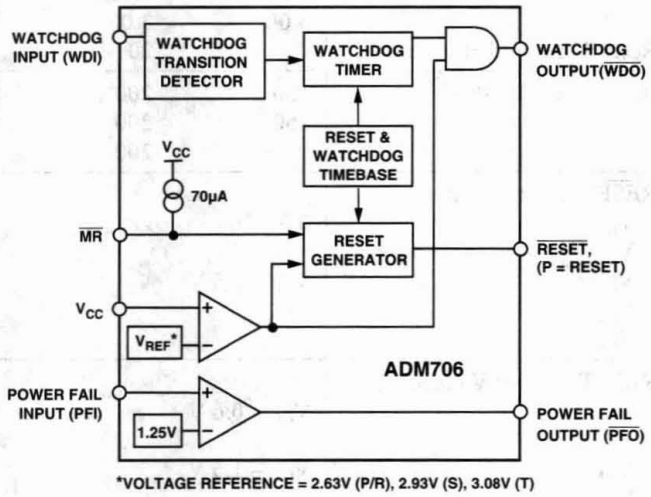
100 µA Quiescent Current
200 ms Reset Pulse Width
Debounced Manual Reset Input ($\overline{MR}$)
Independent Watchdog Timer—1.6 sec Timeout (ADM706x)
Reset Output
- **Active High (ADM706P)**
- **Active Low (ADM706R/S/T)**
- **Both Active High and Active Low (ADM708R/S/T)**

Voltage Monitor for Power-Fail or Low Battery Warning
Guaranteed $\overline{RESET}$ Valid with V_{CC} = 1 V
Superior Upgrade for MAX706P/R/S/T, MAX708R/S/T

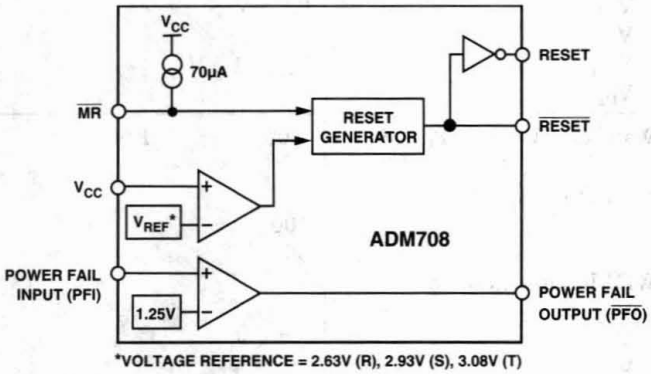
APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Critical µP Monitoring
Automotive Systems
Battery Operated Systems
Portable Instruments

FUNCTIONAL BLOCK DIAGRAMS



*VOLTAGE REFERENCE = 2.63V (P/R), 2.93V (S), 3.08V (T)



*VOLTAGE REFERENCE = 2.63V (R), 2.93V (S), 3.08V (T)

GENERAL DESCRIPTION

The ADM706P/R/S/T and the ADM708R/S/T microprocessor supervisory circuits are suitable for monitoring either 3 V or 3.3 V power supplies.

The ADM706P/R/S/T provide the following functions

1. Power-supply monitoring circuitry which generates a Reset output during power-up, power-down and brownout conditions. The reset output remains operational with V_{CC} as low as 1 V.
2. Independent watchdog monitoring circuitry which is activated if the watchdog input has not been toggled within 1.6 seconds.
3. A 1.25 V threshold detector for power fail warning, low battery detection, or to monitor an additional power supply .
4. An active low debounced manual reset input ($\overline{MR}$).

The ADM706R, ADM706S, ADM706T are identical except for the reset threshold monitor levels which are 2.63 V, 2.93 V, and 3.08 V respectively. The ADM706P is identical to the ADM706R in that the reset threshold is 2.63 V. It differs only in that it has an active high reset output.

The ADM708R/S/T provide the same functionality as the ADM706R/S/T and only differ in that:

1. A watchdog timer function is not available.
2. An active high reset output (RESET) in addition to the active low ($\overline{RESET}$) output is available.

All parts are available in 8-pin DIP and narrow SOIC packages.

ADM706P/R/S/T, ADM708R/S/T–SPECIFICATIONS (V_{CC} = 2.70 V to 5.5 V (ADM70_P/R), V_{CC} = 3.00 V to 5.5 V (ADM70_S), V_{CC} = 3.15 V to 5.5 V (ADM70_T), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		100	200	µA	V_{CC} < 3.6 V
		150	350	µA	V_{CC} < 5.5 V
Reset Threshold (V_{RST})	2.55	2.63	2.70	V	ADM70_P/R
	2.85	2.93	3.00	V	ADM70_S
	3.00	3.08	3.15	V	ADM70_T
Reset Threshold Hysteresis		20		mV	
Reset Pulse Width	160	200	280	ms	ADM70_P/R, V_{CC} = 3 V
	160	200	280	ms	ADM70_S/T, V_{CC} = 3.3 V
		200		ms	V_{CC} = 5.0 V
$\overline{\text{RESET}}$ Output Voltage					ADM70_R/S/T
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC} – 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA
V_{OL}			0.3	V	V_{CC} = 1 V, I_{SINK} = 100 µA
RESET Output Voltage					ADM706P
V_{OH}	V_{CC} – 0.6 V			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 215 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC} – 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA
RESET Output Voltage					ADM708_
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 500 µA
V_{OH}	V_{CC} – 1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA
Watchdog Timeout Period	1.00	1.60	2.25	sec	ADM70_P/R; V_{CC} = 3 V. ADM70_S/T, V_{CC} = 3.3V
WDI Pulse Width					V_{IL} = 0.4 V, V_{IH} = (V_{CC}) × (0.8)
	100			ns	V_{RST} (max) < V_{CC} < 3.6 V
	50			ns	4.5 V < V_{CC} < 5.5 V
WDI Input Threshold					ADM706_
V_{IL}			0.6	V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IH}	0.7 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IL}			0.8	V	V_{CC} = 5.0 V
V_{IH}	3.5			V	V_{CC} = 5.0 V
WDI Input Current	–1.0	0.02	1.0	µA	WDI = 0 V or V_{CC}
$\overline{\text{WDO}}$ Output Voltage					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 500 µA
V_{OH}	V_{CC} – 1.5V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA
$\overline{\text{MR}}$ Pull Up Current					$\overline{\text{MR}}$ = 0 V
	25	70	250	µA	V_{RST} (max) < V_{CC} < 3.6 V
	100	250	600	µA	4.5 V < V_{CC} < 5.5 V
$\overline{\text{MR}}$ PulseWidth					
	500			ns	V_{RST} (max) < V_{CC} < 3.6 V
	150			ns	4.5 V < V_{CC} < 5.5 V
$\overline{\text{MR}}$ Input Threshold					
V_{IL}			0.6	V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IH}	0.7 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IL}			0.8	V	4.5 V < V_{CC} < 5.5 V
V_{IH}	2.0			V	4.5 V < V_{CC} < 5.5 V

Specifications subject to change without notice.

Power Supply Monitor with Reset

ADM709

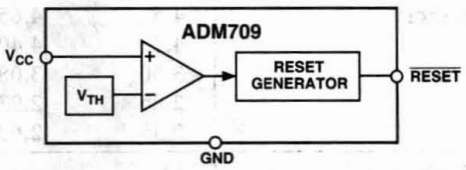
FEATURES

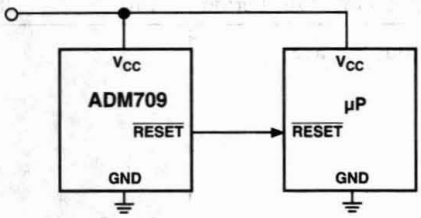
Precision Supply Voltage Monitor
+5 V, +3.3 V, +3 V Power Supply Monitor
35 µA Quiescent Current
140 ms (min) Power-On Reset Pulse
Low Cost
8-Pin DIP/SO Packages
Upgrade for MAX709

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Critical µP Monitoring
Automotive Systems
Critical µP Power Monitoring

FUNCTIONAL BLOCK DIAGRAM





Typical Operating Circuit

GENERAL DESCRIPTION

The ADM709 contains a power supply monitor which generates a system reset during power-up, power-down and brownout conditions. When V_{CC} falls below the reset threshold, $\overline{\text{RESET}}$ goes low and holds the µP in reset. On power-up the $\overline{\text{RESET}}$ output is held low for 140 ms after V_{CC} rises above the threshold. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.

Three supply-voltage threshold levels are available suitable for +5 V, +3.3 V and for +3 V supply monitoring. The actual reset voltage threshold is given below.

The ADM709 is available in 8-pin DIP and SOIC packages.

Table I. Reset Threshold

Suffix	Voltage (V)
L	4.65
M	4.40
T	3.08
S	2.93
R	2.63

ORDERING GUIDE

Model	Reset Threshold	Temperature Range	Package Option*
ADM709LAN	4.65 V	–40°C to +85°C	N-8
ADM709LAR	4.65 V	–40°C to +85°C	SO-8
ADM709MAN	4.40 V	–40°C to +85°C	N-8
ADM709MAR	4.40 V	–40°C to +85°C	SO-8
ADM709TAN	3.08 V	–40°C to +85°C	N-8
ADM709TAR	3.08 V	–40°C to +85°C	SO-8
ADM709SAN	2.93 V	–40°C to +85°C	N-8
ADM709SAR	2.93 V	–40°C to +85°C	SO-8
ADM709RAN	2.63 V	–40°C to +85°C	N-8
ADM709RAR	2.63 V	–40°C to +85°C	SO-8

*N = Plastic DIP; SO = SOIC. For outline information see Package Information section.

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ADM709–SPECIFICATIONS (V_{CC} = Full Operating Range, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0		5.5	V	T_A = 0°C to +70°C
	1.2		5.5	V	T_A = –40°C to +85°C
Supply Current		35	85	µA	V_{CC} < 3.6 V, T_A = 0°C to +70°C
		35	110	µA	V_{CC} < 3.6 V, T_A = –40°C to +85°C
		65	150	µA	V_{CC} < 5.5 V, T_A = 0°C to +70°C
		65	200	µA	V_{CC} < 5.5 V, T_A = –40°C to +85°C
Reset Threshold	4.5	4.65	4.75	V	ADM709L
	4.25	4.40	4.50	V	ADM709M
	3.00	3.08	3.15	V	ADM709T
	2.85	2.93	3.00	V	ADM709S
	2.55	2.63	2.70	V	ADM709R
V_{CC} to $\overline{RESET}$ Delay		20		µs	V_{CC} = Reset Threshold max–min
$\overline{RESET}$ Active Time-Out Period	140	280	380	ms	V_{CC} = Reset Threshold max, V_{CC} Rising
$\overline{RESET}$ Output Voltage			0.3	V	ADM709R/S/T, I_{SINK} = 1.2 mA. V_{CC} = Reset Threshold min
			0.4	V	ADM709L/M, I_{SINK} = 3.2 mA. V_{CC} = Reset Threshold min
			0.3	V	I_{SINK} = 50 µA. $V_{CC} \geq$ 1.0 V
			0.4	V	I_{SINK} = 100 µA. $V_{CC} \geq$ 1.2 V
	$0.8 \times V_{CC}$			V	ADM709R/S/T, I_{SOURCE} = 500 µA, $V_{CC} \geq$ Reset Threshold max
	V_{CC} – 1.5 V			V	ADM709L/M, I_{SOURCE} = 800 µA, $V_{CC} \geq$ Reset Threshold max

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

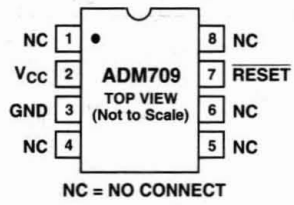
V_{CC} ..... –0.3 V to +6 V
$\overline{RESET}$ Output ..... –0.3 V to V_{CC} + 0.3 V
V_{CC} Input Current ..... 20 mA
$\overline{RESET}$ Output Current ..... 20 mA
Power Dissipation, N-8 DIP ..... 727 mW
  θ_{JA} Thermal Impedance ..... 135°C/W
Power Dissipation, SO-8 SOIC ..... 470 mW
  θ_{JA} Thermal Impedance ..... 110°C/W
Operating Temperature Range
  Industrial (A Version) ..... –40°C to +85°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Vapor Phase (60 secs) ..... +215°C
Infrared (15 secs) ..... +220°C
Storage Temperature Range ..... –65°C to +150°C
ESD Rating ..... >5 kV

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

PIN FUNCTION DESCRIPTION

Mnemonic	Pin No.	Function
NC	1, 4, 5, 6, 8	No Connect Pins.
V_{CC}	2	+5 V, +3.3 V, +3 V Power Supply Input.
$\overline{RESET}$	7	Logic Output. It remains low while V_{CC} is below the reset threshold voltage and for 280 ms (typ) after V_{CC} rises above the threshold.
GND	3	Ground, 0 V.

PIN CONFIGURATION



NC = NO CONNECT

Video Graphics/Digital Video Converters
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Video Graphics/Digital Video Converters–Selection Guides

Video Graphics

Model	# Bits	Power Supply Requirements Volts	mA	I_{OUT} mA	Update Rate, MHz	# Pins	Page No.	Comments	Fax-code
Triple Video DIAs, RS-343IRS-170									
ADV101	8	+5	125	22	30, 50, 80	44	24–7	30 pV/sec Glitch	1586
ADV7120	8	+5	125	22	30, 50, 80	40/44	24–13	ADV7120, in BT101 Pinout	1595
ADV7121	10	+5	125	22	30, 50, 80	40	24–15	With Blank and Sync Pin	1596
ADV7122	10	+5	125	22	30, 50, 80	44	24–15	ADV7121, With Blank and Sync Pin	1597
Triple Pseudo Color RAM DIAs, RS-343IRS-170									
ADV476	6	+5	220	21	33/50/66	28/44	24–11	With Blank on all 3 CHs, Pins with INMOS 171, 176	1592
ADV471	6	+5	220	21	35/50/66/80	44	*	With 15 × 24 Overlay Register, Sync on All 3 CHs	1589
ADV453	8	+5	220	21	40, 66	40/44	*	With 3 × 24 Overlay Register	1587
ADV458	8	+5	370	21	110–165	84	*	With Read and Blank Masks, 4:1, 5:1 Pixel Ports	1588
ADV478	8	+5	220	21	35/50/66/80	44	*	With 15 × 24 Overlay Register, Sync on All 3 CHs	1594
ADV7151	10	+5	450	21	85/110–220	100	*	With Clock Control, 3 Palette RAMS, 1:1, 2:, 4:1 Pixel Port	1603
Triple True Color RAM DIAs, RS-343IRS-170									
ADV473	8	+5	400	21	66–135	68	24–9	With 15 × 28 Overlay Register, Sync on All 3 CHs, V_{REF}	1590
ADV7129	10	+5	500	40	360	304	24–17	10 Bit, 360 MHz, 192-Bit Pixel Port 8:1 Mux, True Color with 64 × 64 Cursor, 2000 × 2000 × 24	1854
ADV7150	10	5	400	20	110–220	160	24–19	Mux Pixel Ports 1:1, 2:1, 4:1	1602
ADV7152	10	5	400	20	110–220	100	24–21	Mux Pixel Ports 1:1, 2:1	1604
ADV7160	10	5	450	20	110–220	160	24–23	Windows 64 × 64 Hardware Cursor, 96-Bit Pixel Port 2:1, 4:1, 8:1, (1600 × 1280 × 24 & 85 Hz), PLL	1851
ADV7162	10	5	450	20	110–220	160	24–23	Windows 64 × 64 Hardware Cursor, 96-Bit Pixel Port 2:1, 4:1, 8:1, (1600 × 1280 × 24 & 85 Hz), PLL	1852
Digital CCIR-601 to PALINSTC Video Encoders									
ADV7175	10	5	200	34.7	27	44	24–25	Digital RGB to Analog NTSC/PAL, Can Do S-VHS, Y/C, RGB, 8-/16-Bit Video & I^2C, 4 10-Bit D/As, with Macrovision Anti-Taping Device, Must Be a Licensee to Purchase	1948
ADV7176	10	5	200	34.7	27	44	24–25	Digital RGB to Analog NTSC/PAL, Can Do S-VHS, Y/C, RGB, 8-/16-Bit Video & I^2C, 4 10-Bit D/As	1948

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

RGB to NTSC/PAL Converters†

Model	Power V_{SS} V	Power I_{SS} mA	BW MHz	LUMA Gain Error %	LUMA Linearity %	Composite Output Gain Error %	Composite Output Diff Phase °	Composite Output Diff Gain %	# Pins	Page No.	Comments	Fax-code
AD720	±5	±35	5	5	0.1	5	0.1	0.1	28	*	With Int Delay Generator & Filters	1255
AD721	±5	±35	5	5	0.1	5	0.1	0.1	28	*	With Triple Input Buffer (Drive RGB Monitor)	1255
AD722	+5	40	5	5	0.6	5	0.1	0.1	16	24–5	With Subcarrier Clock Generator, +5 V	1909

*This product is not in the catalog section of this databook; for a complete data sheet call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.
†For Digital YUV to Analog NTSC/PAL Converters, see D/A Section: Video.

RGB to NTSC/PAL Encoder

AD722

FEATURES
Low Cost, Integrated Solution
+5 V Operation
Accepts FSC Clock or Crystal, or 4FSC Clock
Composite Video and Separate Y/C (S-Video) Outputs
Minimal External Components:
No External Filters or Delay Lines Required
Onboard DC Restoration
Accepts Either HSYNC & VSYNC or CSYNC
Phase Lock to External Subcarrier
Drives 75 Ω Reverse-Terminated Loads
Logic Selectable NTSC or PAL Encoding Modes
Compact 16-Pin SOIC

APPLICATIONS
RGB to NTSC or PAL Encoding

PRODUCT DESCRIPTION

The AD722 is a low cost RGB to NTSC/PAL Encoder that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide composite video output. All three outputs can simultaneously drive 75 Ω, reverse-terminated cables. All logical inputs are CMOS compatible. The chip operates from a single +5 V supply. No external delay lines or filters are required. The AD722 may be powered down when not in use.

The AD722 accepts either FSC or 4FSC clock. When a clock is not available, a low cost parallel-resonant crystal (3.58 MHz (NTSC) or 4.43 MHz (PAL)) and the AD722's on-chip oscillator generate the necessary subcarrier clock. The AD722 also accepts the subcarrier clock from an external video source.

The interface to VGA Controllers and MPEG Video Decoders is simple: an on-chip logic "XNOR" accepts the available vertical (VSYNC) and horizontal sync (HSYNC) signals and creates the composite sync (CSYNC) signal on-chip. If available, the AD722 will also accept a standard CSYNC signal by connecting VSYNC to +5 V and applying CSYNC to HSYNC pin. The AD722 contains decoding logic to identify valid HSYNC pulses for correct burst insertion.

Delays in the U and V chroma filters are matched by an on-chip sampled-data delay line in the Y signal path. To prevent aliasing, a prefilter at 5 MHz is included ahead of the delay line and a post-filter at 5 MHz is added after the delay line to suppress harmonics in the output. These low-pass filters are optimized for minimum pulse overshoot. The overall luma delay, relative to chroma, has been designed to be 170 ns, which precompensates for delays in the filters used in the IF section of a television receiver. This precompensation delay is already present in TV broadcasts. The AD722 comes in a space-saving SOIC and is specified for the 0°C to +70°C commercial temperature range.

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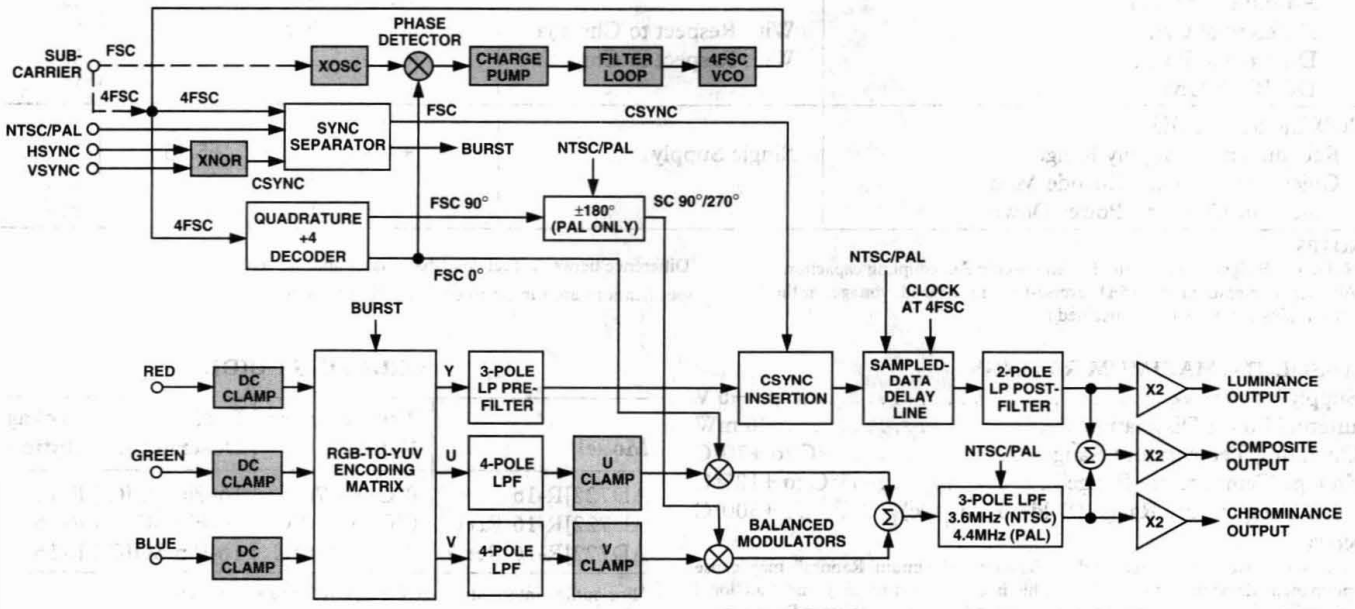
FUNCTIONAL BLOCK DIAGRAM



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AD722–SPECIFICATIONS (Unless otherwise noted, V_S = +5, T_A = +25°C, using FSC synchronous clock. All loads are 150 Ω ± 5% at the IC pins. Outputs are measured at the 75 Ω reverse terminated load.)

Parameter	Conditions	Min	Typ	Max	Units
SIGNAL INPUTS (RDIN, GRIN, BLIN)					
Input Amplitude	NTSC			714	mV p-p
	PAL			700	mV p-p
Black Level		0		3	V
Input Resistance[1]	Red, Green, Blue	1			MΩ
Input Capacitance			5		pF
LOGIC INPUTS (SYNC, FSC, ENCD, NTSC)	CMOS Logic Levels				
Logic LO Input Voltage				1	V
Logic HI Input Voltage		4			V
Logic LO Input Current (DC)			<1		µA
Logic HI Input Current (DC)			<1		µA
VIDEO OUTPUTS[2]					
Luminance (LUMA)					
Roll-off @ 5 MHz	NTSC		–10		dB
	PAL		–7		dB
Gain Error		–15	–5	+15	%
Linearity			±0.6		%
Sync Level	NTSC	243	286	329	mV
	PAL		300		mV
DC Black Level			1.3		V
Chrominance (CRMA)					
Bandwidth	NTSC		3.6		MHz
	PAL		4.4		MHz
Color Burst Amplitude	NTSC	170	240	330	mV p-p
	PAL		252		mV
Color Signal to Burst Ratio Error		–15	±3	15	%
Color Burst Width	NTSC		2.51		µs
	PAL		2.28		µs
Phase Error[3]			±3		Degrees
DC Black Level			2.1		V
Chroma Feedthrough	R, G, B = 0		10	40	mV p-p
Chroma/Luma Time Alignment			–140		ns
Composite (COMP)					
Absolute Gain Error		–5	±1	5	%
Differential Gain	With Respect to Chroma		0.5		%
Differential Phase	With Respect to Chroma		2.0		%
DC Black Level			1.6		V
POWER SUPPLIES					
Recommended Supply Range	Single Supply	+4.75		+5.25	V
Quiescent Current—Encode Mode			30	40	mA
Quiescent Current—Power Down			1		mA

NOTES
[1]R, G, and B signals are inputted to an on-chip AC coupling capacitor.
[2]All outputs measured at a 75 Ω reverse-terminated load; voltages at the IC output pins are twice those specified here.
[3]Difference between ideal color-bar phases and the actual values.
Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage V_S ..... +6 V
Internal Power Dissipation ..... 600 mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +125°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C

NOTE
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics: 16-Pin SOIC Package: θ_{JA} = 100°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD722JR-16	0°C to +70°C	16-Pin SOIC	R-16
AD722JR-16-Reel	0°C to +70°C	16-Pin SOIC	R-16
AD722JR-16-Reel7	0°C to +70°C	16-Pin SOIC	R-16

*For outline information see Package Information section.

ANALOG DEVICES

CMOS 80 MHz, Triple 8-Bit Video DAC

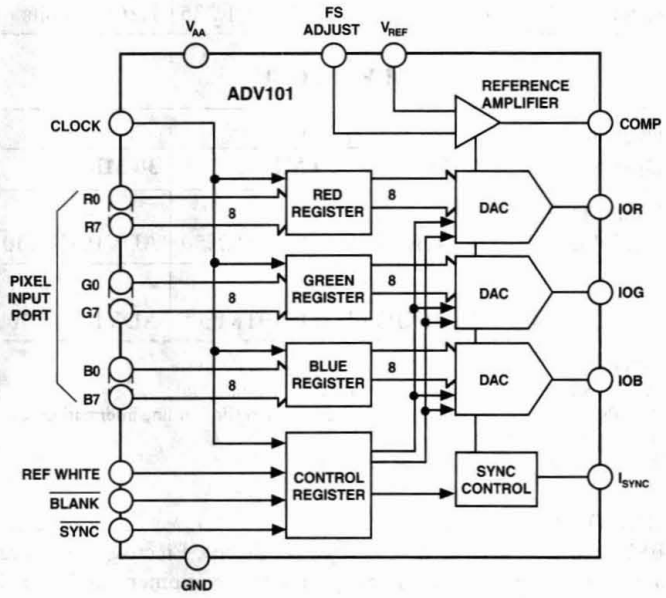
ADV101*

FEATURES
80 MHz Pipelined Operation
Triple 8-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP or 44-Pin PLCC Package
Plug-In Replacement for BT101
Power Dissipation: 400 mW

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Desktop Publishing

SPEED GRADES
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV101 is a digital-to-analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV101 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV101 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV101 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC.

ADV is a registered trademark of Analog Devices Inc.

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential nonlinearity of ±0.5 LSB. Integral nonlinearity is guaranteed to be a maximum of ±1 LSB.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

ORDERING GUIDE[1]

Package Option[2]	Speed		
	80 MHz	50 MHz	30 MHz
Plastic DIP (N-40A)	ADV101KN80	ADV101KN50	ADV101KN30
PLCC[3] (P-44A)	ADV101KP80	ADV101KP50	ADV101KP30

NOTES
[1]All devices are specified for 0°C to +70°C operation.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.
[3]PLCC: Plastic Leaded Chip Carrier (J-lead).

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND ..... +7 V
Voltage on Any Digital Pin .... GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Soldering Temperature (10 secs) ..... 300°C
Vapor Phase Soldering (1 minute) ..... 220°C
IOR, IOB, IOG, I_{SYNC} to GND[2] ..... 0 V to V_{AA}

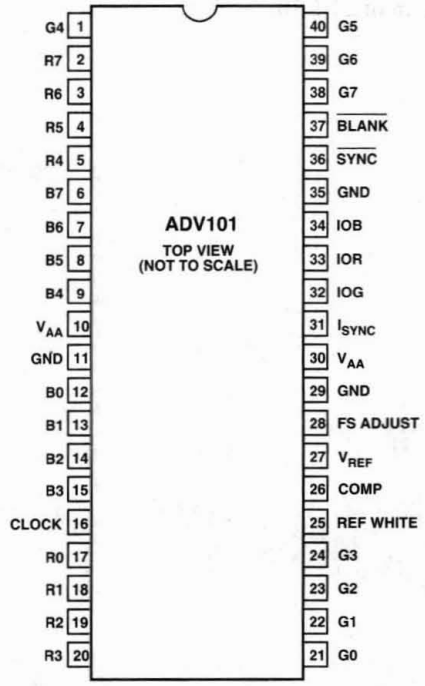
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

CAUTION

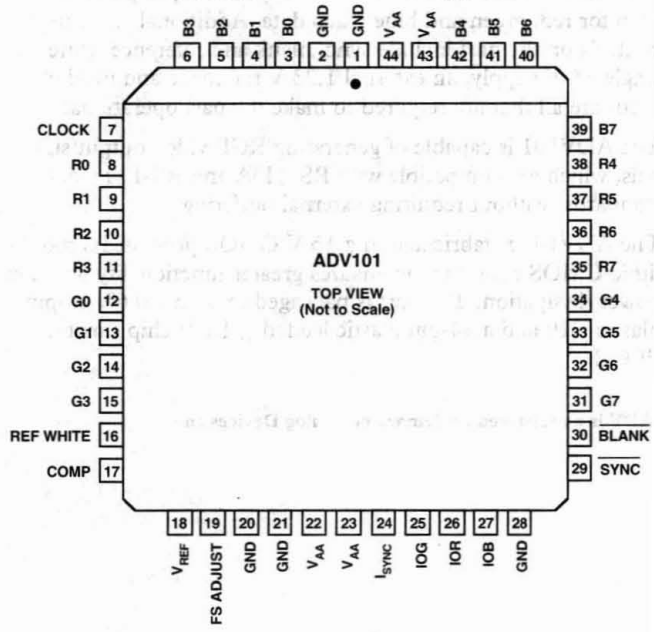
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV101 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP



PLCC



CMOS 135 MHz True-Color Graphics Triple 8-Bit Video RAM-DAC

ADV473

FEATURES
ADV478/ADV471 (ADV®) Register Level Compatible
IBM PS/2,* VGA*/XGA* Compatible
135 MHz Pipelined Operation
Triple 8-Bit D/A Converters
Triple 256 × 8 (256 × 24) Color Palette RAM
Three 15 × 8 Overlay Registers
On-Board Voltage Reference
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs and Outputs
Sync on All Three Channels
Programmable Pedestal (0 or 7.5 IRE)
Standard MPU I/O Interface
+5 V CMOS Monolithic Construction
68-Pin PLCC Package

APPLICATIONS
High Resolution Color Graphics
True-Color Visualization
CAE/CAD/CAM
Image Processing
Desktop Publishing

MODES
24-Bit True Color
8-Bit Pseudo Color
15-Bit True Color
8-Bit True Color

SPEED GRADES
135 MHz, 110 MHz
80 MHz, 66 MHz

GENERAL DESCRIPTION

The ADV473 is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for true-color computer graphics systems.

The ADV473 integrates a number of graphic functions onto one device allowing 24-bit direct true-color operation at the maximum screen update rate of 135 MHz. It can also be used in other modes, including 15-bit true color and 8-bit pseudo or indexed color. The ADV473 is fully PS/2 and VGA register level compatible. It is also capable of implementing IBM's XGA standard.

The device consists of three, high speed, 8-bit, video D/A converters (RGB), a 256 × 24 RAM which can be configured as a look-up table or a linearization RAM, a 24-bit wide parallel pixel input port and three 15 × 8 overlay registers. The part is controlled through the MPU port by the various on-board control/command registers.

(Continued on next page)

ADV is a registered trademark of Analog Devices Inc.
***Personal System/2 and VGA are trademarks of International Business Machines Corp.**

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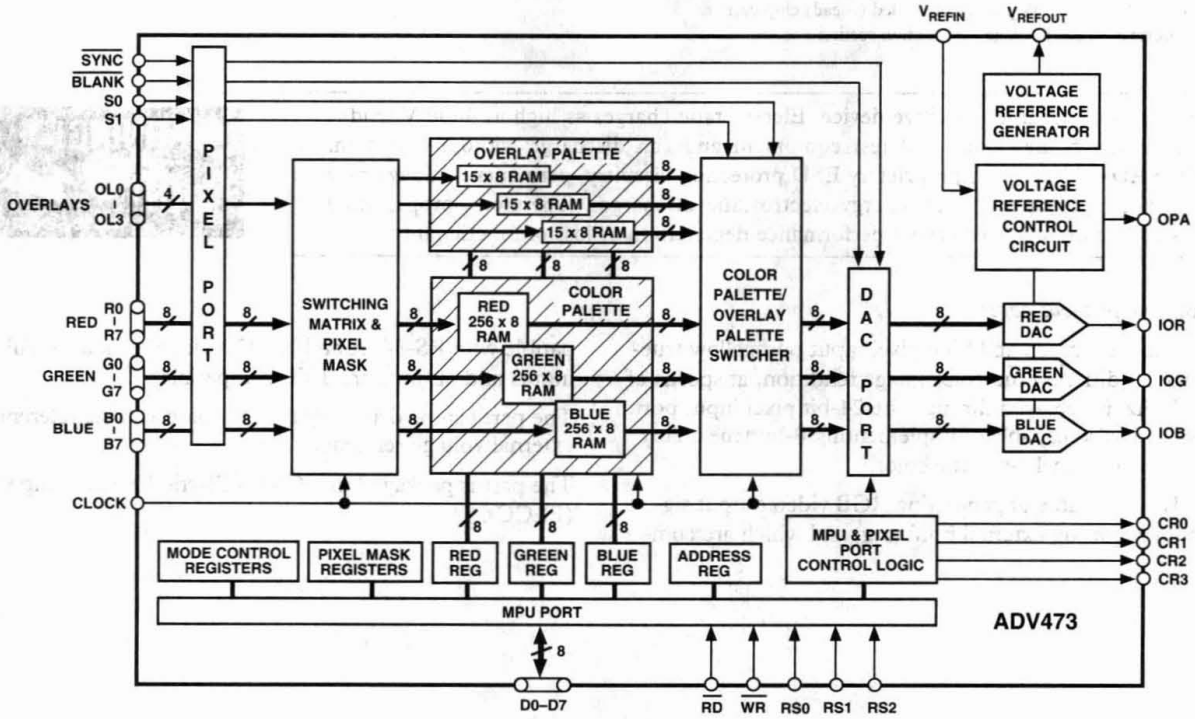
FUNCTIONAL BLOCK DIAGRAM



ADV473–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{AA}	4.75	5.00	5.25	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Voltage	V_{REF}	1.14	1.235	1.26	Volts

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND ..... 7 V
Voltage on Any Digital Pin .... GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) ..... –55°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Vapor Phase Soldering (2 minutes) ..... +220°C
IOR, IOG, IOB to GND[2] ..... GND–0.5 V to V_{AA}

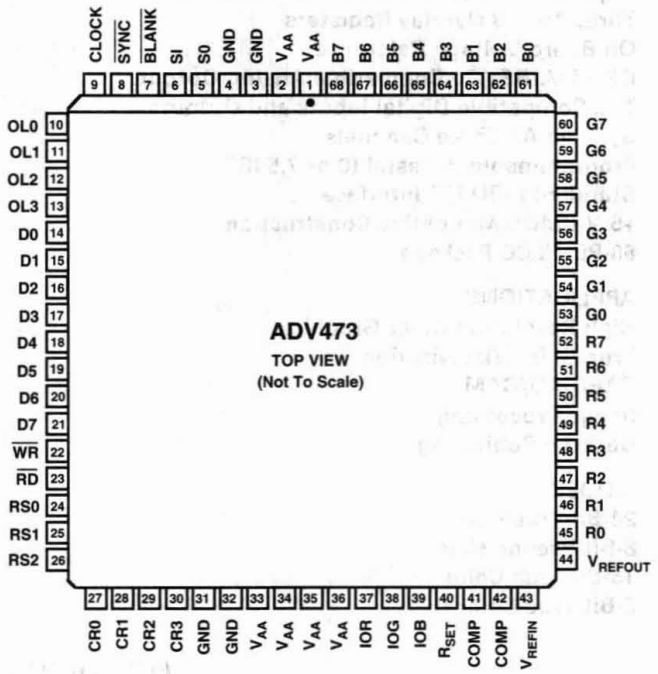
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE

Model	Speed	Temperature Range	No. of Pins	Package Option*
ADV473KP135	135 MHz	0°C to +70°C	68	P-68A
ADV473KP110	110 MHz	0°C to +70°C	68	P-68A
ADV473KP80	80 MHz	0°C to +70°C	68	P-68A
ADV473KP66	66 MHz	0°C to +70°C	68	P-68A

NOTE
*All devices are packaged in a 68-pin plastic leaded (J-lead) chip carrier.
For outline information see Package Information section

PIN CONFIGURATION
68-Pin PLCC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV473 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

(Continued from previous page)

The individual red, green and blue pixel input ports allow true-color, image rendition. True-color image rendition, at speeds of up to 135 MHz, is achieved through the 24-bit pixel input port. The ADV473 is also capable of implementing 8-bit true color, 8-bit pseudo color and 15-bit true color.

The ADV473 is capable of generating RGB video output signals, without requiring external buffering, and which are compatible with RS-343A and RS-170 video standards. All digital inputs and outputs are TTL compatible.

The part can be driven by the on-board voltage reference or an external voltage reference.

The part is packaged in a 68-pin Plastic Leaded Chip Carrier (PLCC).

CMOS Monolithic 256×18 Color Palette RAM-DAC

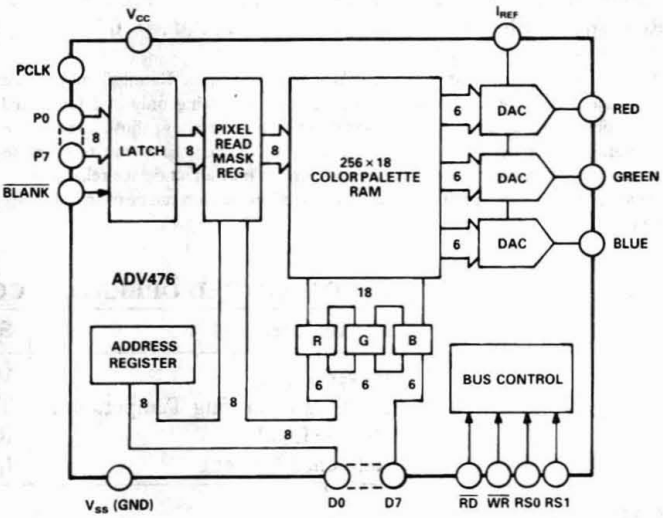
ADV476

FEATURES
Personal System/2* and VGA* Compatible
Plug-in Replacement for INMOS 171/176
66 MHz Pipelined Operation
Three 6-Bit D/A Converters
256×18 Color Palette RAM
RS-343A/RS-170 Compatible Outputs
Blank on All Three Channels
Standard MPU Interface
Asynchronous Access to All Internal Registers
+5 V CMOS Monolithic Construction
Low Power Dissipation
Standard 28-Pin, 0.6" DIP and 44-Pin PLCC

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Desktop Publishing

AVAILABLE CLOCK RATES
66 MHz
50 MHz
35 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV476 (ADV®) is a pin compatible and software compatible RAM-DAC designed specifically for VGA and Personal System/2 color graphics.

The ADV476 is a complete analog output RAM-DAC on a single monolithic chip. The part contains a 256×18 color lookup table, a pixel mask register as well as a triple 6-bit video D/A converter. The ADV476 is capable of simultaneously displaying up to 256 colors, from a total color palette of 262,144 addressable colors.

The on-chip asynchronous MPU bus allows access to the color lookup table without affecting the input video data via the pixel port. The pixel read mask register provides a convenient way of filtering the displayed colors without updating the color lookup table. The ADV476 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV476 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation and small board area. The part is packaged in a 0.6", 28-pin DIP and a 44-pin PLCC.

PRODUCT HIGHLIGHTS

1. Standard video refresh rates, 35 MHz, 50 MHz and 66 MHz.
2. Fully compatible with VGA and Personal System/2 color graphics.
3. Guaranteed monotonic. Integral and differential linearity guaranteed to be a maximum of ±1 LSB.
4. Low glitch energy, 75 pV secs.

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ADV is a registered trademark of Analog Devices, Inc.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to GND ..... +7 V
Voltage on any Digital Pin ..... GND – 0.5 V to V_{CC} + 0.5 V
Ambient Operating Temperature (T_A) ..... –55°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Vapor Phase Soldering (1 minute) ..... +220°C
Red, Green, Blue to GND[2] ..... 0 V to V_{CC}

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog output short circuit to any power supply or common can be of an indefinite duration.

ORDERING GUIDE[1, 2]

Model	Speed	Package Type	Package Option[3]
ADV476KN35	35 MHz	28-Pin DIP	N-28
ADV476KN50	50 MHz	28-Pin DIP	N-28
ADV476KN66	66 MHz	28-Pin DIP	N-28
ADV476KP35	35 MHz	44-Pin PLCC	P-44A
ADV476KP50	50 MHz	44-Pin PLCC	P-44A
ADV476KP66	66 MHz	44-Pin PLCC	P-44A

NOTES
[1]All devices are specified for 0°C to +70°C operation. (Industrial Temp Range –40°C to +85°C available on special request, please contact your local Analog Devices representative).
[2]Devices are packaged in 0.6" 28-pin plastic DIPs (N-28), and 44-pin J-leaded PLCC (P-44A).
[3]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

RECOMMENDED OPERATING CONDITIONS

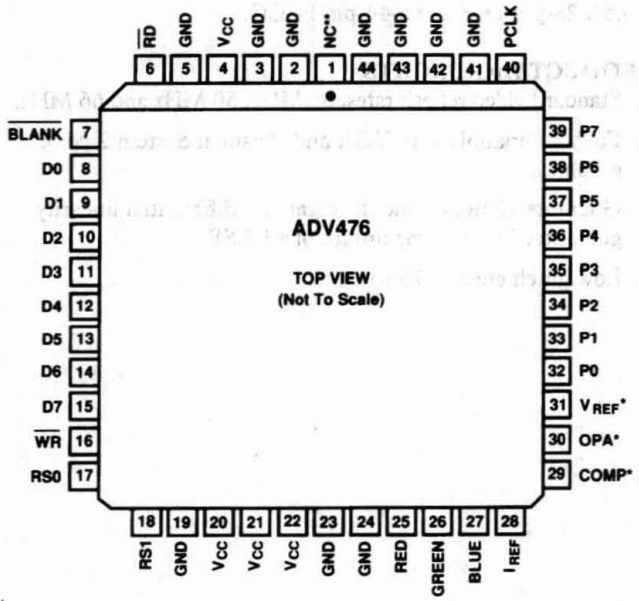
Parameter	Symbol	Min	Typ	Max	Units
Power Supply	V_{CC}	4.5	5.00	5.5	Volts
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	R_L		37.5		Ω
Reference Current	I_{REF}	–3		–10	mA

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV476 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

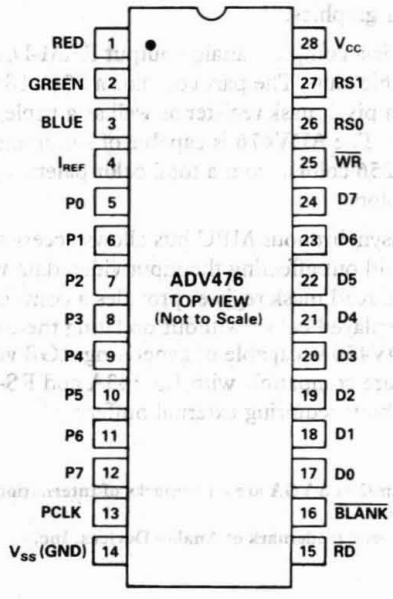
PIN CONFIGURATIONS

PLCC



*V_{REF} MUST BE TERMINATED THROUGH A 0.1μF CERAMIC CAPACITOR TO V_{CC} OPA IS LEFT UNCONNECTED; COMP IS CONNECTED TO I_{REF} (SEE FIGURE 8).
**NC = NO CONNECT

DIP



The above pins allow the ADV476KP (44-Pin PLCC) to be alternatively driven by a voltage reference. If it is desired to use a voltage reference configuration instead of the current reference configuration described in this data sheet, the above listed pins must be connected as described in Figure 6 of the ADV478/ADV471 data sheet of this reference manual.

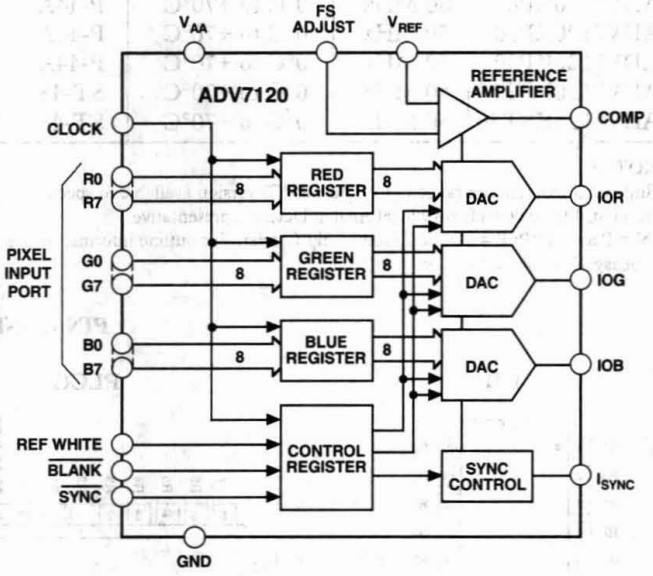
CMOS
80 MHz, Triple 8-Bit Video DAC
ADV7120

FEATURES
80 MHz Pipelined Operation
Triple 8-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP, 44-Pin PLCC and 48 Lead TQFP

APPLICATIONS
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Desktop Publishing
Direct Digital Synthesis (DDS) and I/Q Modulation

SPEED GRADES*
80 MHz
50 MHz
30 MHz

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7120 (ADV®) is a digital to analog video converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems. It is also ideal for any high speed communications type applications requiring low cost, high speed DACs. It consists of three, high speed, 8-bit, video D/A converters (RGB); a standard TTL input interface and high impedance, analog output, current sources.

The ADV7120 has three separate, 8-bit, pixel input ports, one each for red, green and blue video data. Additional video input controls on the part include composite sync, blank and reference white. A single +5 V supply, an external 1.23 V reference and pixel clock input are all that are required to make the part operational.

The ADV7120 is capable of generating RGB video output signals, which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

The ADV7120 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The part is packaged in both a 0.6", 40-pin plastic DIP and a 44-pin plastic leaded (J-lead) chip carrier, PLCC. The ADV7120 is also available in a very small 48-lead Thin Quad Flatpack (TQFP).

ADV is a registered trademark of Analog Devices, Inc.

*** Speed grades up to 140 MHz are also available upon special request. Please contact Analog Devices or its representatives for further details.**

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Compatible with a wide variety of high resolution color graphics video systems.
3. Guaranteed monotonic with a maximum differential nonlinearity of ±0.5 LSB. Integral nonlinearity is guaranteed to be a maximum of ±1 LSB.

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ORDERING GUIDE

Model	Speed	Temperature Range[1]	Package Option[2]
ADV7120KN80	80 MHz	0°C to +70°C	N-40A
ADV7120KN50	50 MHz	0°C to +70°C	N-40A
ADV7120KN30	30 MHz	0°C to +70°C	N-40A
ADV7120KP80	80 MHz	0°C to +70°C	P-44A
ADV7120KP50	50 MHz	0°C to +70°C	P-44A
ADV7120KP30	30 MHz	0°C to +70°C	P-44A
ADV7120KST50	50 MHz	0°C to +70°C	ST-48
ADV7120KST30	30 MHz	0°C to +70°C	ST-48

NOTES
[1]Industrial temperature range (–40°C to +85°C) version available to special request. Please consult your local Analog Device representative.
[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier. For outline information see Package Information section.

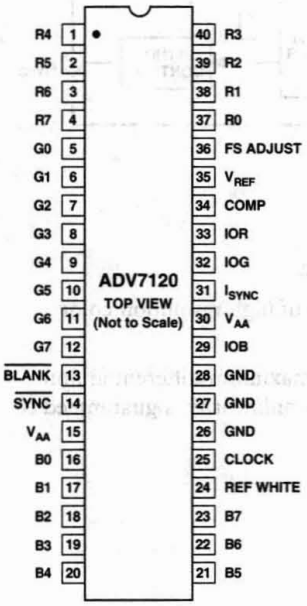
ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND ..... +7 V
Voltage on Any Digital Pin ..... GND –0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Soldering Temperature (10 secs) ..... 300°C
Vapor Phase Soldering (1 minute) ..... 220°C
IOR, IOB, IOG, I_{SYNC} to GND[2] ..... 0 V to V_{AA}

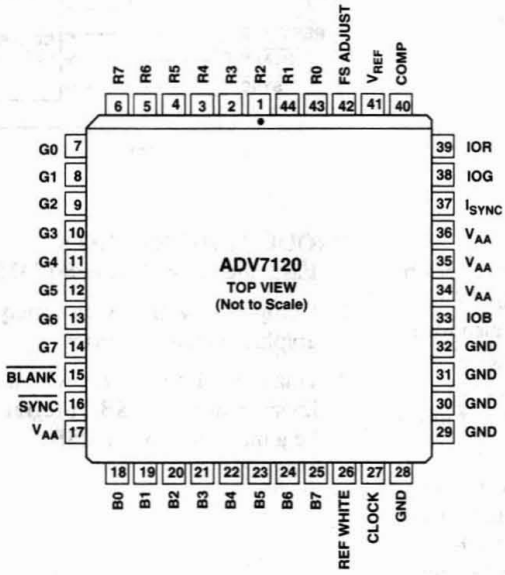
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATIONS

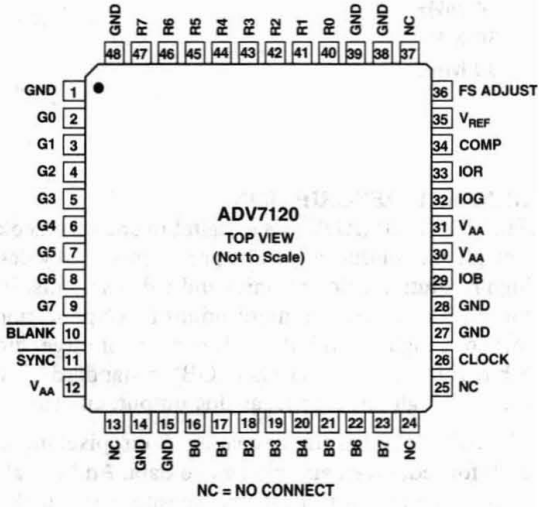
DIP



PLCC



TQFP



NOTE
For the ADV7120 in TQFP package: The REF WHITE pin is not available. The ISYNC pin is not available and is internally connected to the IOG pin.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7120 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

CMOS
80 MHz, Triple 10-Bit Video DACs

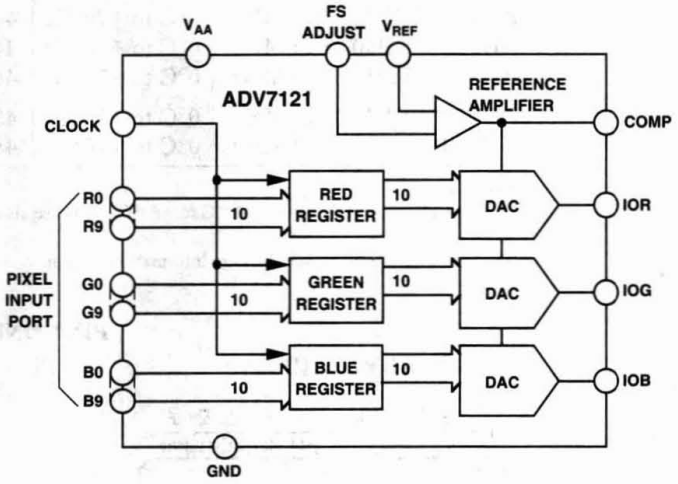
ADV7121/ADV7122

FEATURES
80 MHz Pipelined Operation
Triple 10-Bit D/A Converters
RS-343A/RS-170 Compatible Outputs
TTL Compatible Inputs
+5 V CMOS Monolithic Construction
40-Pin DIP Package (ADV7121)
44-Pin PLCC Package (ADV7122)
48-Lead TQFP (ADV7122)

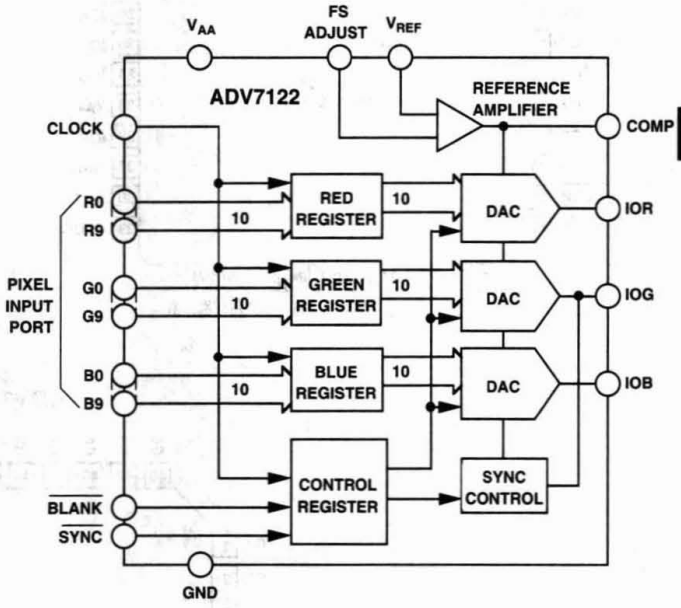
APPLICATIONS
High Definition Television (HDTV)
High Resolution Color Graphics
CAE/CAD/CAM Applications
Image Processing
Instrumentation
Video Signal Reconstruction
Direct Digital Synthesis (DDS)
I/Q Modulation

SPEED GRADES
80 MHz
50 MHz
30 MHz

ADV7121 FUNCTIONAL BLOCK DIAGRAM



ADV7122 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7121/ADV7122 (ADV®) is a video speed, digital-to-analog converter on a single monolithic chip. The part is specifically designed for high resolution color graphics and video systems including high definition television (HDTV). It is also ideal for any application requiring a low cost, high speed DAC function especially in communications. It consists of three, high speed, 10-bit, video D/A converters (RGB), a standard TTL input interface and high impedance, analog output, current sources.

The ADV7121/ADV7122 has three separate, 10-bit, pixel input ports, one each for red, green and blue video data. A single +5 V power supply, an external 1.23 V reference and pixel clock input is all that is required to make the part operational. The ADV7122 has additional video control signals, composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$.

The ADV7121/ADV7122 is capable of generating RGB video output signals which are compatible with RS-343A, RS-170 and most proposed production system HDTV video standards, including SMPTE 240M.

The ADV7121/ADV7122 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation. The ADV7121 is packaged in a 0.6", 40-pin plastic DIP package. The ADV7122 is packaged in a 44-pin plastic leaded (J-lead) chip carrier, PLCC, and 48-lead thin quad flatpack (TQFP).

PRODUCT HIGHLIGHTS

1. Fast video refresh rate, 80 MHz.
2. Guaranteed monotonic to 10 bits. Ten bits of resolution allows for implementation of linearization functions such as gamma correction and contrast enhancement.
3. Compatible with a wide variety of high resolution color graphics systems including RS-343A/RS-170 and the proposed SMPTE 240M standard for HDTV.

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*Speed grades up to 140 MHz are also available on special request. Please contact Analog Devices or its representatives for details.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

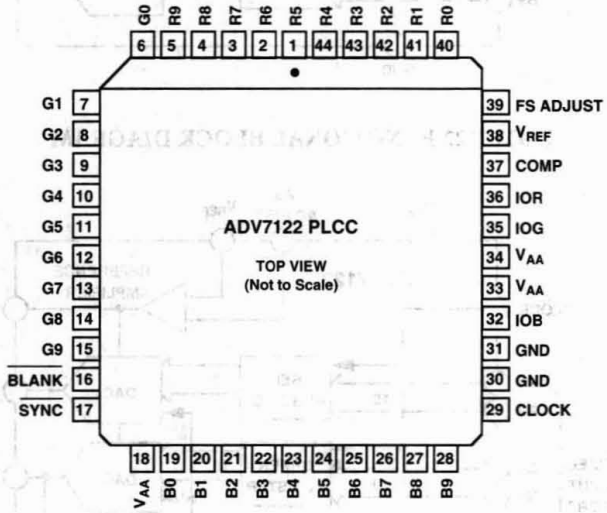
ORDERING GUIDE

Model	Speed	Temperature Range[1]	Package Description	Package Option[2]
ADV7121KN80	80 MHz	0°C to +70°C	40-Pin Plastic DIP	N-40A
ADV7121KN50	50 MHz	0°C to +70°C	40-Pin Plastic DIP	N-40A
ADV7121KN30	30 MHz	0°C to +70°C	40-Pin Plastic DIP	N-40A
ADV7122KP80	80 MHz	0°C to +70°C	44-Lead Plastic Leaded Chip Carrier (PLCC)	P-44A
ADV7122KP50	50 MHz	0°C to +70°C	44-Lead Plastic Leaded Chip Carrier (PLCC)	P-44A
ADV7122KP30	30 MHz	0°C to +70°C	44-Lead Plastic Leaded Chip Carrier (PLCC)	P-44A
ADV7122KST50	50 MHz	0°C to +70°C	48-Lead Thin Quad Flatpack (TQFP)	ST-48
ADV7122KST30	30 MHz	0°C to +70°C	48-Lead Thin Quad Flatpack (TQFP)	ST-48

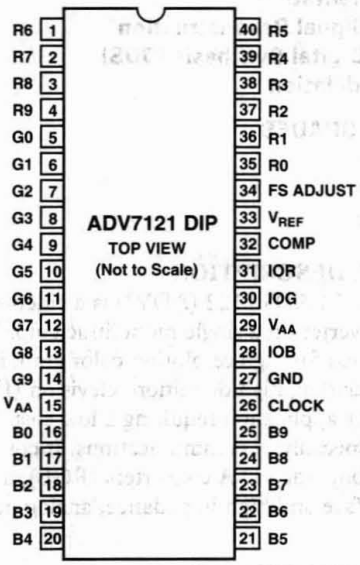
NOTES
[1]Industrial Temperature range (–40°C to +85°C) parts are also available to special ranges. Please contact your local Analog Devices representative.
[2]For outline information see Package Information section.

PIN CONFIGURATIONS

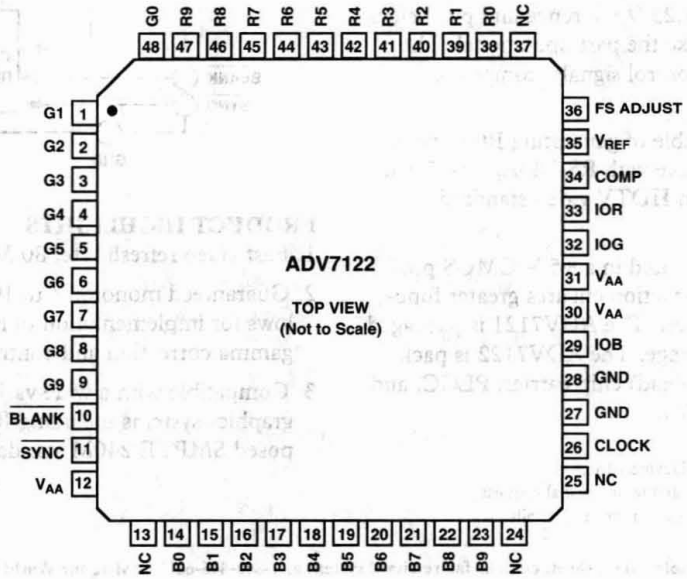
ADV7122 (PLCC)



ADV7121 (DIP)



ADV7122 (TQFP)



192-Bit, 360 MHz True-Color CMOS Video DAC with Onboard PLL

ADV7129

FEATURES

192-Bit Pixel Port Allows 2000 × 2000 × 24 Screen Resolution
360 MHz, 24-Bit True-Color Operation
Triple 8-Bit D/A Converters
8:1 Multiplexing
64 × 64 × 2 Programmable Cursor
Onboard PLL
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Internal Voltage Reference
Standard 8-Bit MPU I/O Interface Programmable Pixel Port
+5 V CMOS Monolithic Construction
304-Pin PQFP Package

APPLICATIONS

Ultrahigh Resolution Color Graphics
Image Processing
Drives 24-Bit Color 2K × 2K Monitors

GENERAL DESCRIPTION

The ADV7129 is a complete analog output, video DAC on a single CMOS (ADV®) monolithic chip. The part is specifically designed for use in the highest resolution graphics and imaging systems. The ultimate level of integration, comprised of 360 MHz triple 8-bit DACs, a programmable pixel port, an internal voltage reference and an onboard PLL, makes the ADV7129 the only choice for the very highest level of performance and functionality.

The device consists of three high speed, 8-bit, video D/A converters (RGB), a programmable 64 × 64 × 2 cursor with its own color palette. An onboard phase locked loop clock generator is provided to provide high speed operation without requiring high speed external crystal or clock circuitry.

The part is fully controlled through the MPU port by the onboard command registers. This MPU port can be may be updated at any time without corrupting the contents of the cursor or causing sparkle effects on the screen.

The ADV7129 supports 24-bit true-color formats where screen resolution is the primary design goal. The individual Red, Green and Blue pixel input ports allow true-color image rendition at resolutions of 2000 × 2000 × 24-bit.

The ADV7129 is capable of generating RGB video output signals that are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

An internal voltage reference is also provided to simplify system design.

The ADV7129 is fabricated in a +5 V CMOS process.

The ADV7129 is packaged in a 304-pin PQFP package.

ADV is a registered trademark of Analog Devices, Inc.

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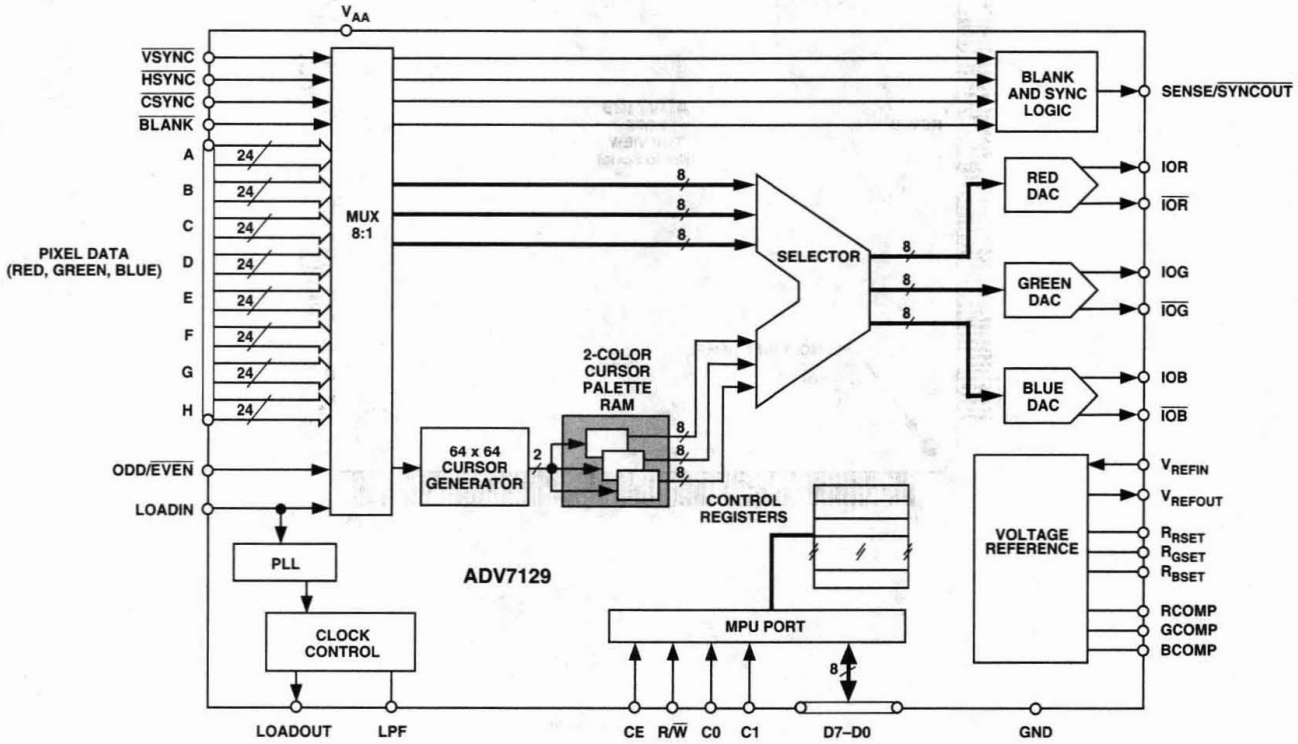
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND ..... 7 V
Voltage on Any Digital Pin .... GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) ..... 0°C to +70°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +260°C
Vapor Phase Soldering (1 minute) ..... +220°C
Analog Outputs to GND[2] ..... GND – 0.5 V to V_{AA}
Current on Any DAC Output ..... 40 mA

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

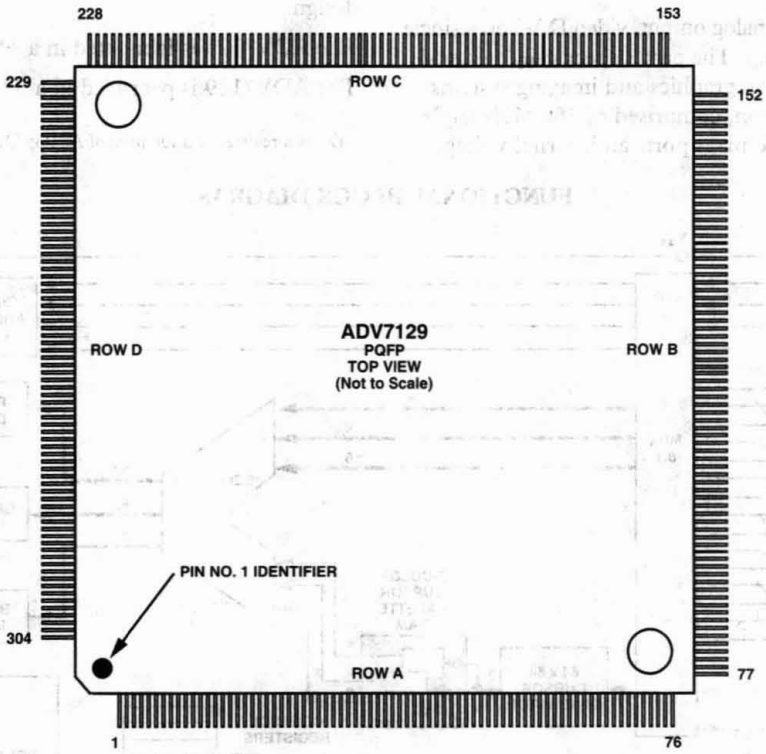
Model	Temperature Range	Package Option*
ADV7129KS	0°C to +70°C	S-304

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7129 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

304-LEAD PQFP PIN CONFIGURATION



CMOS 220 MHz True-Color Graphics Triple 10-Bit Video RAM-DAC

ADV7150

FEATURES

220 MHz, 24-Bit (30-Bit Gamma Corrected) True Color
Triple 10-Bit "Gamma Correcting" D/A Converters
Triple 256 × 10 (256 × 30) Color Palette RAM
On-Chip Clock Control Circuit
Palette Priority Select Registers
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Standard MPU I/O Interface
- **10-Bit Parallel Structure**
- **8+2 Byte Structure**

Programmable Pixel Port: 24-Bit, 15-Bit and 8-Bit (Pseudo)
Pixel Data Serializer
- **Multiplexed Pixel Input Ports; 1:1, 2:1, 4:1**

+5 V CMOS Monolithic Construction
160-Lead Plastic Quad Flatpack (QFP)
Thermally Enhanced to Achieve θ_{JC} < 1.0°C/W

MODES OF OPERATION

24-Bit True Color (30-Bit Gamma Corrected)
- **@ 220 MHz**
- **@ 170 MHz**
- **@ 135 MHz**
- **@ 110 MHz**
- **@ 85 MHz**

8-Bit Pseudo Color
15-Bit True Color

APPLICATIONS

High Resolution, True Color Graphics
Professional Color Prepress Imaging

GENERAL DESCRIPTION

The ADV7150 (ADV®) is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in high performance, color graphics workstations. The ADV7150 integrates a number of graphic functions onto one device allowing 24-bit direct True-Color operation at the maximum screen update rate of 220 MHz. The ADV7150 implements 30-bit True Color in 24-bit frame buffer designs. The part also supports other modes, including 15-bit True Color and 8-bit Pseudo or Indexed Color. Either the Red, Green or Blue input pixel ports can be used for Pseudo Color.

The device consists of three, high speed, 10-bit, video D/A converters (RGB), three 256 × 10 (one 256 × 30) color look-up tables, palette priority selects, a pixel input data multiplexer/serializer and a clock generator/divider circuit. The ADV7150 is capable of 1:1, 2:1 and 4:1 multiplexing. The on-board palette priority select inputs enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled and programmed through the microprocessor (MPU) port. The part also contains a number of on-board test registers, associated with self diagnostic testing of the device. The individual Red, Green and Blue pixel input ports allow True-Color, image rendition. True-Color image rendition, at speeds of up to 220 MHz, is achieved through the use of the on-board data multiplexer/serializer. The pixel input ports flexibility allows for direct interface to most standard frame buffer memory configurations.

(Continued on next page)

ADV is a registered trademark of Analog Devices, Inc.

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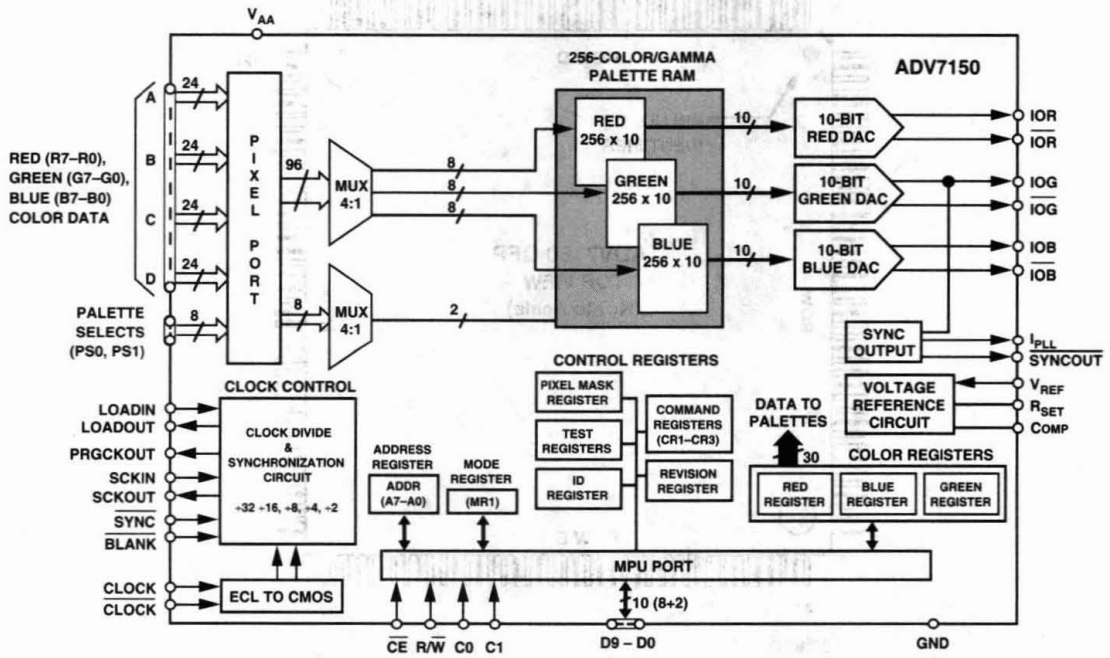
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND ..... 7 V
Voltage on Any Digital Pin ..... GND – 0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) ..... –55°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +260°C
Vapor Phase Soldering (1 minute) ..... +220°C
Analog Outputs to GND[1] ..... GND – 0.5 to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE[1, 2, 3]

Speed			
220 MHz	ADV7150LS220	110 MHz	ADV7150LS110
170 MHz	ADV7150LS170	85 MHz	ADV7150LS85
135 MHz	ADV7150LS135		

NOTES

[1]ADV7150 is packaged in a 160-pin plastic quad flatpack, QFP.
[2]All devices are specified for 0°C to +70°C operation.
[3]Contact Sales Office for latest information on package design.

(Continued from previous page)

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 24-bit True-Color resolution, while also allowing for the on-board implementation of linearization algorithms, such as Gamma-Correction. This allows effective 30-bit True-Color operation.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. An external ECL oscillator source with differential outputs is all that is required to drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the ADV7150. The part can also be driven by an external clock generator chip circuit, such as the AD730.

The ADV7150 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the users system level debugging.

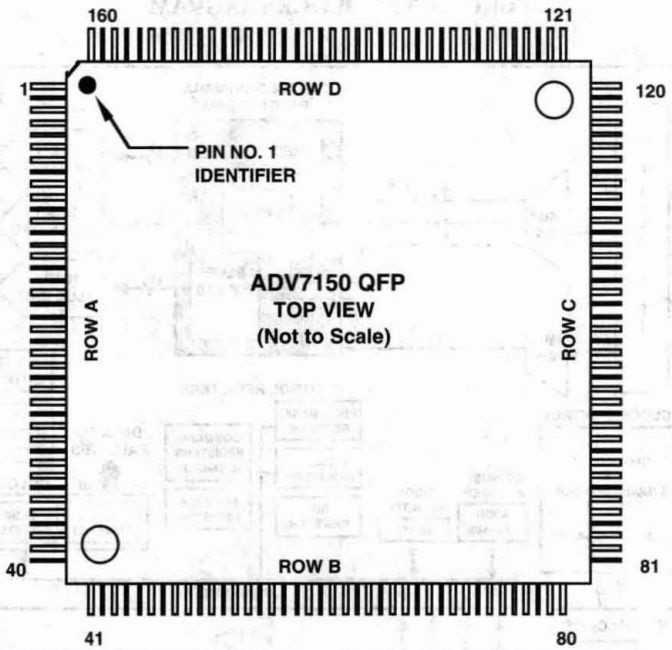
The ADV7150 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7150 is packaged in a plastic 160-pin power quad flatpack (QFP). Superior thermal dissipation is achieved by inclusion of a copper heatslug, within the standard package outline to which the die is attached.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7150 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

160-LEAD QFP CONFIGURATION



CMOS 220 MHz True-Color Graphics Triple 10-Bit Video RAM-DAC

ADV7152

FEATURES

220 MHz, 24-Bit (30-Bit Gamma Corrected) True Color
Triple 10-Bit "Gamma Correcting" D/A Converters
Triple 256 × 10 (256 × 30) Color Palette RAM
On-Chip Clock Control Circuit
Palette Priority Select Registers
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Standard MPU I/O Interface
- **10-Bit Parallel Structure**
- **8+2 Byte Structure**

Programmable Pixel Port: 24-Bit and 8-Bit (Pseudo)
Pixel Data Serializer
Multiplexed Pixel Input Ports; 1:1, 2:1
+5 V CMOS Monolithic Construction
100-Lead Plastic Quad Flatpack (QFP)
Thermally Enhanced to Achieve θ_{JC} < 1.0°C/W

MODES OF OPERATION

24-Bit True Color (30-Bit Gamma Corrected)
- **@ 220 MHz**
- **@ 170 MHz**
- **@ 135 MHz**
- **@ 110 MHz**
- **@ 85 MHz**

8-Bit Pseudo Color
15-Bit True Color

APPLICATIONS

High Resolution, True Color Graphics
Professional Color Prepress Imaging

GENERAL DESCRIPTION

The ADV7152 (ADV®) is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in high performance, color graphics workstations. The ADV7152 integrates a number of graphic functions onto one device allowing 24-bit direct True-Color operation at the maximum screen update rate of 220 MHz. The ADV7152 implements 30-bit True Color in 24-bit frame buffer designs. The part also supports other modes, including 15-bit True Color and 8-bit Pseudo or Indexed Color. Either the Red, Green or Blue input pixel ports can be used for Pseudo Color.

The device consists of three, high speed, 10-bit, video D/A converters (RGB), three 256 × 10 (one 256 × 30) color look-up tables, palette priority selects, a pixel input data multiplexer/serializer and a clock generator/divider circuit. The ADV7152 implements 1:1 and 2:1 pixel data multiplexing. The on-board palette priority select inputs enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled and programmed through the microprocessor (MPU) port. The part also contains a number of on-board test registers, associated with self diagnostic testing of the device.

The individual Red, Green and Blue pixel input ports allow True-Color, image rendition. True-Color image rendition, at speeds of up to 220 MHz, is achieved through the use of the on-board data multiplexer/serializer. The pixel input ports flexibility allows for direct interface to most standard frame buffer memory configurations.

(Continued on next page)

ADV is a registered trademark of Analog Devices, Inc.

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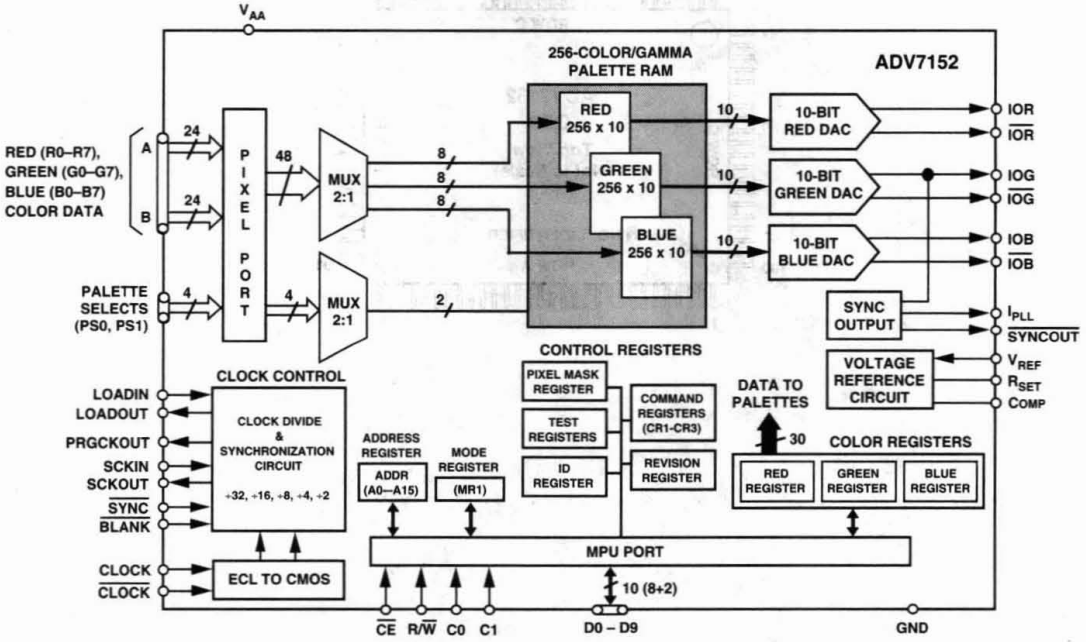
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

V_{AA} to GND ..... 7 V
Voltage on Any Digital Pin ..... GND – 0.5 V to V_{AA} +0.5 V
Ambient Operating Temperature (T_A) ..... –55°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
Lead Temperature (Soldering, 10 secs) ..... +260°C
Vapor Phase Soldering (1 minute) ..... +220°C
Analog Outputs to GND[1] ..... GND – 0.5 to V_{AA}

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE[1, 2, 3]

Speed			
220 MHz	ADV7152LS220	110 MHz	ADV7152LS110
170 MHz	ADV7152LS170	85 MHz	ADV7152LS85
135 MHz	ADV7152LS135		

NOTES

[1]ADV7152 is packaged in a 100-pin plastic quad flatpack, QFP.
[2]All devices are specified for 0°C to +70°C operation.
[3]Contact Sales Office for latest information on package design.

(Continued from previous page)

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 24-bit True-Color resolution, while also allowing for the on-board implementation of linearization algorithms, such as Gamma-Correction. This allows effective 30-bit True-Color operation.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. An external ECL oscillator source with differential outputs is all that is required to drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the ADV7152. The part can also be driven by an external clock generator chip circuit, such as the AD730.

The ADV7152 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the users system level debugging.

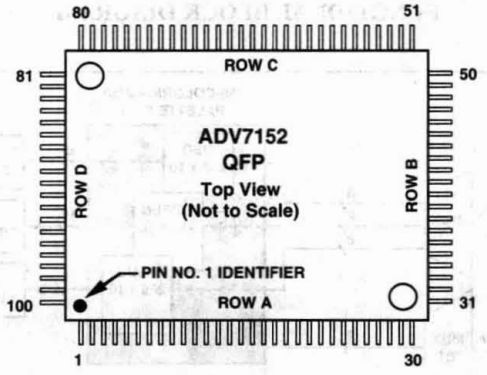
The ADV7152 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7152 is packaged in a plastic 100-pin power quad flatpack (QFP). Superior thermal dissipation is achieved by inclusion of a copper heatslug, within the standard package outline to which the die is attached.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7152 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

100-LEAD QFP CONFIGURATION



96-Bit, 220 MHz True-Color Video RAM-DACs

ADV7160/ADV7162

FEATURES

96-Bit Pixel Port for 1600 × 1280 × 24 Screen Resolution
220 MHz, 24-Bit (30-Bit Gamma Corrected) True-Color
Triple 10-Bit "Gamma Correcting" D/A Converters
2% (max) DAC to DAC Color Matching
Triple 256 × 10 (256 × 30) Color Palette RAM
On-Board User Definable Cursor (64 × 64 × 2)
Three Color Overlay
Cursor Palette RAM
Fully Programmable On-Board PLL
RS-343A/RS-170 Compatible RGB Analog Outputs
Tri-Level SYNC Functionality
TTL Compatible Digital Inputs
Standard MPU I/O Interface
Programmable Pixel Port: 24-Bit, 16-Bit, 15-Bit & 8-Bit (Pseudo)
Pixel Data Serializer:
Multiplexed Pixel Input Ports; 2:1, 4:1, 8:1
+5 V CMOS Monolithic Construction
160-Lead Plastic Quad Flatpack (QFP): ADV7162
160-Lead "Thermally Enhanced" QFP (PQUAD): ADV7160

MODES OF OPERATION

1600 × 1200 × 30/24-Bit Resolution @ 85 Hz Screen Refresh
1600 × 1200 × 16/15-Bit Resolution @ 85 Hz Screen Refresh
1600 × 1200 × 8-Bit Resolution @ 85 Hz Screen Refresh

APPLICATIONS

Windows Accelerators
High Resolution, True Color Graphics
Professional Color Prepress Imaging
Digital TV (HDTV, Digital Video)

SPEED GRADES

@ 220 MHz
@ 170 MHz
@ 140 MHz

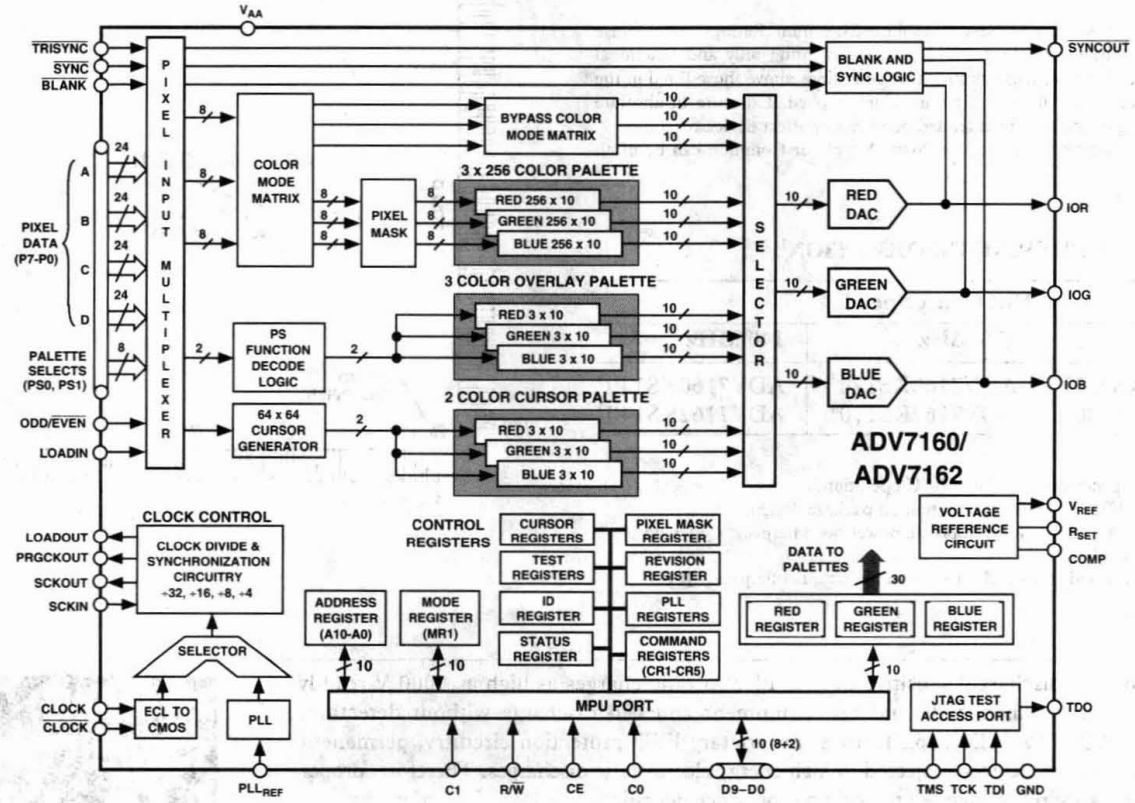
GENERAL DESCRIPTION

The ADV7160/ADV7162® is a 96-bit pixel port Video RAM-DAC with color enhanced triple 10-bit DACs. The device also includes a PLL and 64 × 64 hardware cursor. The ADV7160/ADV7162 is specifically designed for use in the graphics subsystem of high performance, color graphics workstations and windows accelerators.

(Continued on next page)

ADV is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

(Continued from previous page)

The ADV7160/ADV7162 integrates a number of graphic functions onto one device allowing 24-bit direct True-Color (30-bit Corrected-Color) operation at the maximum screen resolution of 1600 × 1280 at a refresh rate of 85 Hz. The ADV7160/ADV7162 integrates a 256 × 30 Color Palette RAM with three high speed, 10-bit, digital-to analog converters (RGB DACs). It also contains a user-definable, X-Windows compatible, 64 × 64 × 2 cursor generator and associated RAM. An on-board Overlay Palette RAM is also included. The device's 96-bit Programmable Pixel Port enables various data formats to be input to the part. An on-board clock and synchronization circuit controls all clocking functions for both the part and graphics subsystem.

There are two video data paths through the ADV7160/ADV7162. One routes the data from the pixel port through the RAM to the DACs, the other bypasses the RAM and routes data direct from the pixel port to the DACs. Either path can be selected on a pixel by pixel basis. This allows for the overlay of an active video window on a graphics background.

The on-board palette priority select inputs enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled and programmed through the microprocessor (MPU) port.

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 24-bit True-Color resolution, while also allowing for the on-board implementation of linearization algorithms, such as Gamma-Correction and Monitor Callibration. This allows effective 30-bit True-Color operation.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. The high accuracy, low jitter on board PLL eliminates the need for an external high speed clock generator. The PLL can be programmed to produce a pixel clock that is a multiple of the PLL reference clock.

The ADV7162 is packaged in a standard plastic 160-pin quad flatpack (QFP).

The ADV7160 is packaged in a plastic 160-pin power quad flatpack (PQUAD). Superior thermal distribution is achieved by the inclusion of a copper heatslug, within the standard package outline, to which the die is attached. This part is ideally suited for high performance applications where external environmental conditions are unpredictable and uncontrollable.

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND	7 V
Voltage on Any Digital Pin	GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A)	0°C to +70°C
Storage Temperature (T_S)	–65°C to +150°C
Junction Temperature (T_J)	+150°C
Lead Temperature (Soldering, 10 secs)	+260°C
Vapor Phase Soldering (1 minute)	+220°C
Analog Outputs to GND[2]	GND – 0.5 V to V_{AA}

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING INFORMATION[1, 2, 3]

Dot Clock Speed		
220 MHz	**170 MHz**	**140 MHz**
ADV7160KS220[3]	ADV7160KS170[3]	ADV7160KS140[3]
ADV7162KS220[4]	ADV7162KS170[4]	ADV7162KS140[4]

NOTES

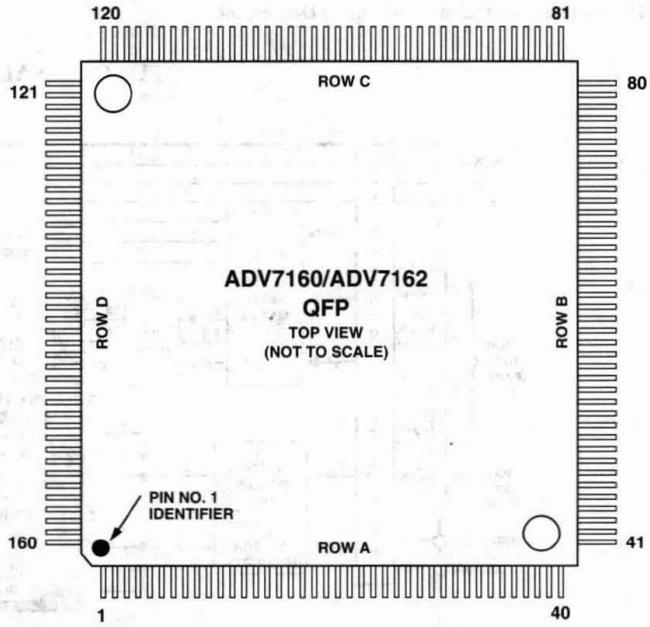
[1]All devices are specified for 0°C to +70°C operation.

[2]Contact Sales Office for latest information on package design.

[3]ADV7160 is packaged in a 160-pin plastic power quad flatpack, QFP with heatsink embedded.

[4]ADV7162 is packaged in a standard 160-pin plastic quad flatpack, QFP.

160-Lead QFP Configuration



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7160/ADV7162 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Integrated Digital CCIR-601 YCrCb to PAL/NTSC Video Encoders

ADV7175/ADV7176

FEATURES

- CCIR-601 YCrCb to PAL/NTSC Video Encoder
- Single 27 MHz Clock Required (×2 Oversampling)
- Pixel Port Supports:
  - CCIR-656 4:2:2 8-Bit Parallel Input Format
  - 4:2:2 16-Bit Parallel Input Format
- SMPTE 170M NTSC Compatible Composite Video Output
- CCIR624/CCIR601 PAL Compatible Composite Video Output
- SCART/PeriTV Support
- YUV Output Mode
- Simultaneous Composite and S-VHS Y/C or RGB YUV Video Outputs
- Programmable Luma Filters (Low-Pass/Notch)
- Square Pixel Support (Slave Mode)
- Allows Subcarrier Phase Locking with External Video Source
- 10-Bit DAC Resolution for Encoded Video Channels
- 8-Bit DAC Resolution for RGB Output
- YUV Interpolation for Accurate Subcarrier Construction
- Programmable Subcarrier Frequency and Phase
- Programmable LUMA Delay
- Color Signal Control/Burst Signal Control
- Interlaced/Noninterlaced Operation
- Complete On-Chip Video Timing Generator
- Master/Slave Operation Supported
- Master Mode Timing Programmability
- Macrovision Antitaping Facility Rev 6.1/7.x (ADV7175 Only)*
- Close Captioning Support
- Teletext Support (Passthrough Mode)
- On-Board Color Bar Generation
- On-Board Voltage Reference
- 2-Wire Serial MPU Interface (I^2C Compatible)
- +5 V CMOS Monolithic Construction
- 44-Pin PQFP Thermally Enhanced Package

APPLICATIONS

- MPEG-1 and MPEG-2 Video
- DVD
- Digital Satellite/Cable Systems (Set Top Boxes/IRDs)
- Video Games
- CD Video/Karaoke
- Professional Studio Quality
- PC Video/Multimedia

GENERAL DESCRIPTION

The ADV7175/ADV7176 is an integrated digital video encoder that converts Digital CCIR-601 4:2:2 component video data into a standard analog baseband television signal compatible with world wide standards NTSC, PAL B/D/G/H/I, PAL M or PAL N. In addition to the composite output signal, there is the facility to output S-VHS Y/C video, YUV or RGB video. The Y/C, YUV or RGB format is simultaneously available at the analog outputs with the composite video signal. Each analog output generates a standard video-level signal into a doubly terminated 75 Ω load.

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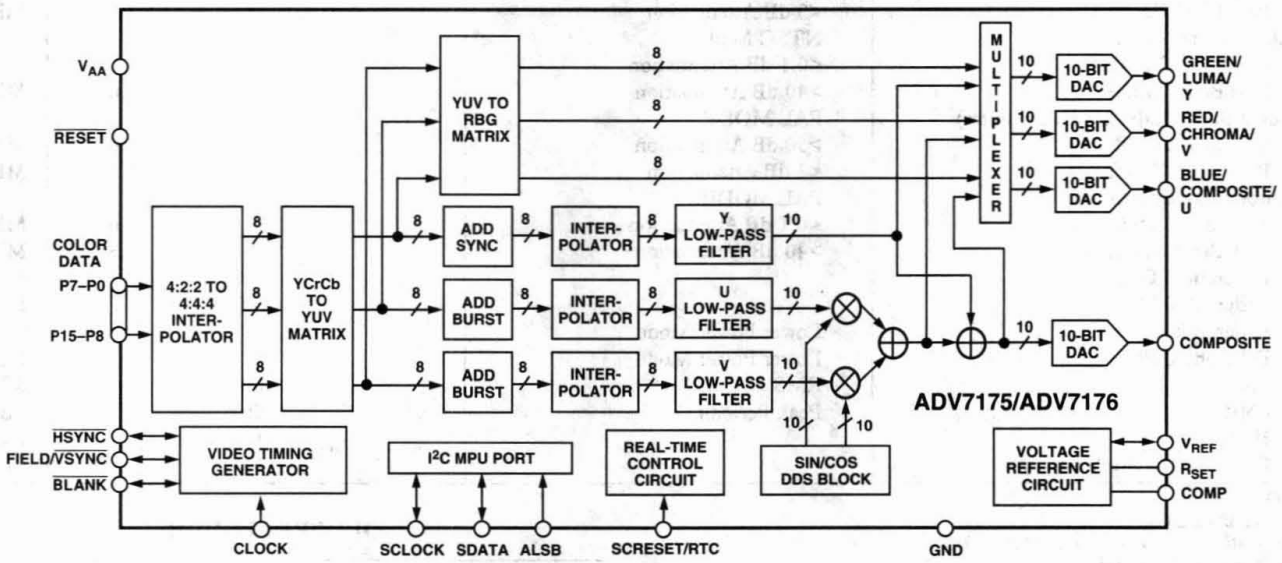
FUNCTIONAL BLOCK DIAGRAM



*This device is protected by U.S. Patent Numbers 4631603, 4577216, 4819098 and other intellectual property rights. The Macrovision anticopy process is licensed for noncommercial home use only, which is its sole intended use in the device. Please contact sales office for latest Macrovision version available.

ADV7175/ADV7176–SPECIFICATIONS (V_{AA} = +5 V[1], V_{REF} = 1.235 V R_{SET} = 150 Ω. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Model / Parameter	Conditions[1]	ADV7175/ADV7176 Min	Typ	Max	Units
STATIC PERFORMANCE					
Resolution (Each DAC)				10	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2			V
Input Low Voltage, V_{INL}				0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±1	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 3.2 mA			0.4	V
Floating-State Leakage Current				10	μA
Floating-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Output Current[3]		33	34.7	37	mA
Output Current[4]			8		mA
Full-Scale DAC Output			182.5		IRE
LSB Size			33.9		μA
DAC-to-DAC Matching			2	5	%
Output Compliance, V_{OC}		0		+1.4	V
Output Impedance, R_{OUT}			15		kΩ
Output Capacitance, C_{OUT}	I_{OUT} = 0 mA			30	pF
VOLTAGE REFERENCE					
Voltage Reference Range, V_{REF}	$I_{VREFOUT}$ = 20 μA	1.112	1.235	1.359	V
POWER REQUIREMENTS[5]					
V_{AA}			5		V
I_{DAC}[6]			140	155	mA
I_{CCT}[7]			110	150	mA
Power Supply Rejection Ratio	COMP = 0.1 μF		0.02	0.5	%/%
DYNAMIC PERFORMANCE[8]					
Luma Bandwidth[9] (Low-Pass Filter)	NTSC Mode				
Stopband Cutoff	>50 dB Attenuation			7.5	MHz
Pass Band Cutoff	<3 dB Attenuation			2.5	MHz
Chroma Bandwidth	NTSC Mode				
Stopband Cutoff	<0.1 dB Attenuation			3.6	MHz
Pass Band Cutoff	>40 dB Attenuation			1.0	MHz
Luma Bandwidth[9] (Low-Pass Filter)	PAL MODE				
Stopband Cutoff	>50 dB Attenuation			8.0	MHz
Pass Band Cutoff	<3 dB Attenuation			3.4	MHz
Chroma Bandwidth	PAL MODE				
Stopband Cutoff	<0.1 dB Attenuation			4.0	MHz
Pass Band Cutoff	>40 dB Attenuation			1.3	MHz
Differential Gain			0.8		%
Differential Phase			0.8		Degree
Differential Gain	Lower Power Mode		7		%
Differential Phase	Lower Power Mode		2		Degree
SNR	RMS		60		dB rms
SNR	Peak Periodic		56		dB p-p
Hue Accuracy			1.0		Degree
Color Saturation Accuracy			1.0		%

NOTES
[1]±5% for all versions.
[2]Temperature range T_{MIN} to T_{MAX}: 0°C to 70°C.
[3]Full drive into 37.5 Ω load.
[4]Minimum drive with buffered/scaled output load.
[5]Power measurements are taken with Clock Frequency = 27 MHz. Max T_J = 100°C.
[6]I_{DAC} is the total current to drive all four DACs. Turning off one DAC reduces I_{DAC} correspondingly
[7]I_{CCT} (Circuit Currrent) is the continuous currrent required to drive the device.
[8]Guaranteed by characterization.
[9]These specifications are for the low-pass filter only. For the other internal filters please see Figure 3.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADV7175KS	0°C to 70°C	S-44
ADV7176KS	0°C to 70°C	S-44

*For outline information see Package Information section.

DSP, Fixed-Point Processors
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ADSP-2181 – DSP Microcomputer	25–9

DSP, Fixed-Point Processors—Selection Guide

Model	Instruction Cycle Time ns	Internal Program Memory RAM/ROM	Internal Data Memory RAM/ROM	Internal Program Cache Word	Program Memory Boot	Serial Ports	Programmable Timer	External Interrupts	Low Power Modes	Pin Count	Page No.	Faxcode
ADSP-2100A	80	—	—	16 × 24	—	—	—	4	—	100	25–5	1576
ADSP-2101	50	2K × 24	1K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2103 (3 V)	77	2K × 24	1K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2105	100	1K × 24	0.5K × 26	—	√	1	√	3	5	68	25–5	1579
ADSP-2111 (HIP)*	50	2K × 24	1K × 16	—	√	2	√	3	5	100	25–5	1579
ADSP-2115	50	1K × 24	0.5K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2161	40, 52, 60	0/8K × 2	0/0.5K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2162 (3 V)	40, 52, 60	0/8K × 24	0/0.5K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2163	40, 52, 60	0/4K × 24	0/0.5K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2164 (3 V)	40, 52, 60	0/4K × 24	0/0.5K × 16	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2165	50	1K/12 × 24	1K × 16/0	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2166 (3 V)	50	1K/12 × 24	1K × 16/0	—	√	2	√	3	5	68/80	25–5	1579
ADSP-2171 (HIP)*	30	2K × 24	2K × 16	—	√	2	√	4	6	128	25–7	1869
ADSP-2181**	30	16K × 24	16K × 16		√	2	√	7	6	128	25–9	1927
ADSP-21csp01**	20	4K × 24	4K × 16	64 × 24	√	2	√	5	6	160	25–3	1975

NOTES
*HIP = Host Interface Port.
**Internal DMA.

ANALOG DEVICES

Concurrent Signal Processor

ADSP-21csp01

FEATURES

Performance

- 20 ns Instruction Cycle Time from 25 MHz Crystal @ 5.0 V
- 50 MIPS Sustained Performance
- 24-Bit Address Bus with a Unified 16M Address Space
- 32 Flexible Data Registers Provide Local Variable Storage
- 64 Data Addressing Registers Support 16 Data Structures
- Background Registers Provide Single-Cycle Context Switch
- Multifunction Instructions Combine Memory Read or Write with Arithmetic Operation
- Single-Cycle Linked-List Update
- 64-Word, Selective Instruction Cache Provides Three Bus Performance
- Single-Cycle Arithmetic Execution
- Two 40-Bit Accumulators
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with Fast Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode
- Low Three-Cycle Interrupt Latency

Integration

- 20K Bytes of On-Chip RAM, Configured as:
  - 4K Words of On-Chip Program or Data RAM (24 Bits)
  - 4K Words of On-Chip Data RAM (16 Bits)
- Five Channel DMA Controller
- Dual Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator, & Barrel Shifter Computational Units
- Two Independent Data Address Generators Provide:
  - Pre-Modify and Post-Modify Addressing
  - Modification with a Constant
  - Circular/Modulo Addressing
- Powerful Program Sequencer Provides:
  - Zero Overhead Looping
  - Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler

System Interface

- 16-Bit Internal DMA Port for High Speed Access to On-Chip Memory
- Four Memory Strobes & Separate I/O Memory Space Permits "Glueless" System Design
- Programmable Wait State Generation
- Acknowledge Pin Supports Asynchronous Memory Interface
- Two Synchronous Serial Ports with Companding Hardware, Four 8-Word FIFOs, Separate Receive and Transmit Clocks, DMA, and TDM Multichannel Support
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory (e.g., EPROM) or through Internal DMA Port
- 12 Programmable Flag Pins (6 Input and 6 Output) Provide Flexible System Signaling
- Four External Interrupts (Plus 12 Internal and Software Interrupts for a Total of 16)
- IEEE JTAG Standard 1149.1 Test Access Port
- 160-Lead PQFP

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The ADSP-21csp01 is a single chip DSP optimized for concurrent signal processing (CSP) and other high speed numeric processing applications. The ADSP-21csp01 combines high performance, high bandwidth, 16M address space, DMA ports, and fast task switching support to provide efficient multisignal or multichannel processing. The ADSP-21csp01 processor is based on the architecture used for the ADSP-2100 Family. Although this architecture has been modified to improve the processor's performance and add new features, the ADSP-2100 Family code can be ported easily to the ADSP-21csp01.

The ADSP-21csp01's flexible architecture and comprehensive instruction set supports a high degree of parallelism. In one cycle the ADSP-21csp01 can perform all of the following operations:

- perform a computation
- perform one or two data moves
- update one or two data address pointers
- generate a program address
- fetch an instruction
- decode an instruction

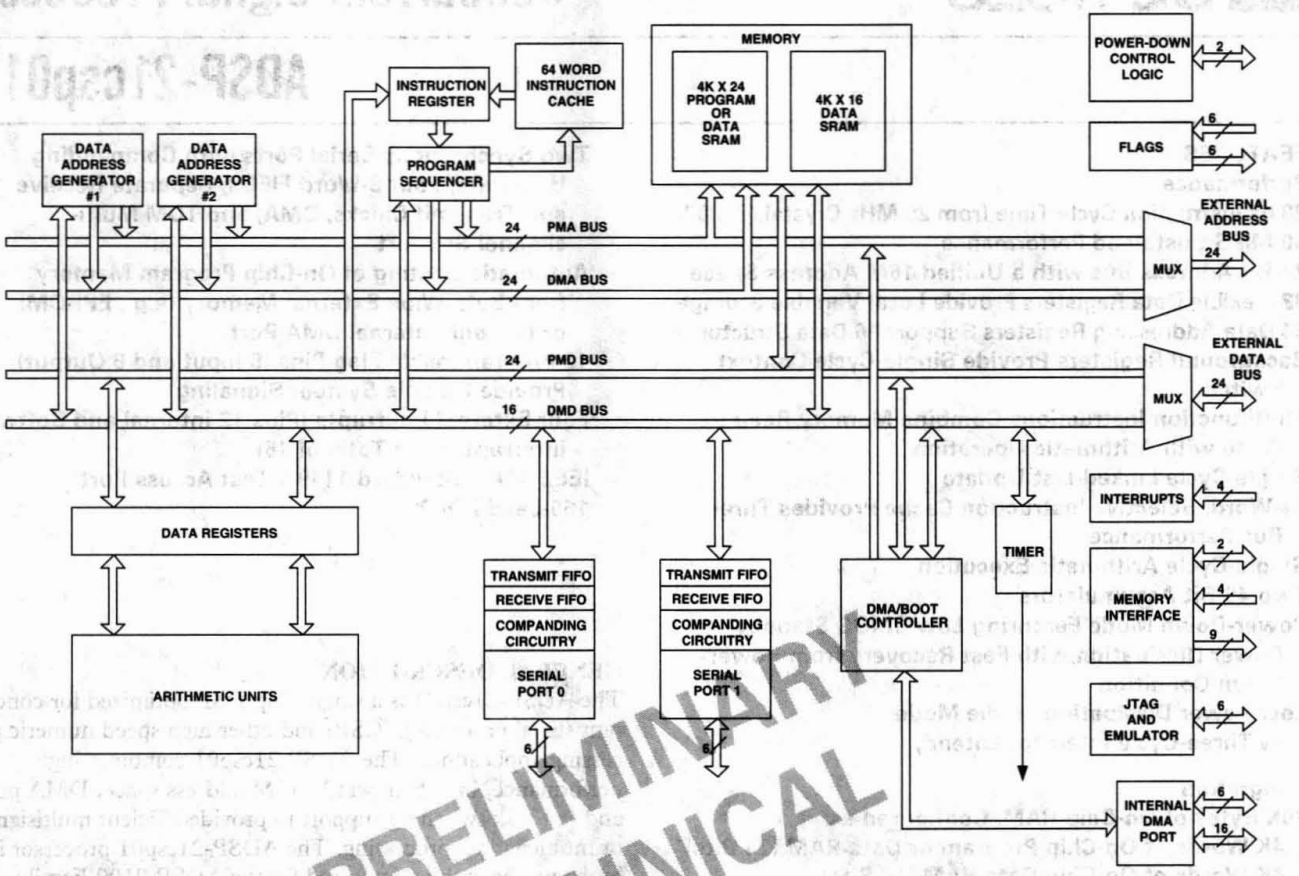
These operations take place while the processor continues to complete the following tasks:

- receive and transmit data through one or two serial ports
- receive or transmit data through the IDMA port
- decrement the timer

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

ADSP-2100 Family DSP Microcomputers

ADSP-21xx

SUMMARY

16-Bit Fixed-Point DSP Microprocessors with On-Chip Memory
Enhanced Harvard Architecture for Three-Bus Performance: Instruction Bus & Dual Data Buses
Independent Computation Units: ALU, Multiplier/ Accumulator, and Shifter
Single-Cycle Instruction Execution & Multifunction Instructions
On-Chip Program Memory RAM or ROM & Data Memory RAM
Integrated I/O Peripherals: Serial Ports, Timer, Host Interface Port (ADSP-2111 Only)

FEATURES

25 MIPS, 40 ns Maximum Instruction Rate
Separate On-Chip Buses for Program and Data Memory
Program Memory Stores Both Instructions and Data (Three-Bus Performance)
Dual Data Address Generators with Modulo and Bit-Reverse Addressing
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory (e.g., EPROM)
Double-Buffered Serial Ports with Companding Hardware, Automatic Data Buffering, and Multichannel Operation
ADSP-2111 Host Interface Port Provides Easy Interface to 68000, 80C51, ADSP-21xx, etc.
Automatic Booting of ADSP-2111 Program Memory Through Host Interface Port
Three Edge- or Level-Sensitive Interrupts
Low Power IDLE Instruction
PGA, PLCC, PQFP, and TQFP Packages
MIL-STD-883B Versions Available

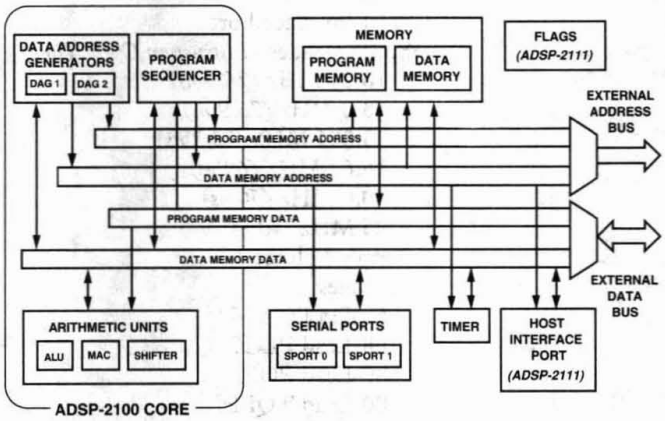
GENERAL DESCRIPTION

The ADSP-2100 Family processors are single-chip microcomputers optimized for digital signal processing (DSP) and other high speed numeric processing applications. The ADSP-21xx processors are all built upon a common core. Each processor combines the core DSP architecture—computation units, data address generators, and program sequencer—with differentiating features such as on-chip program and data memory RAM, a programmable timer, one or two serial ports, and, on the ADSP-2111, a host interface port.

The ADSP-216x series are memory-variant versions of the ADSP-2101 and ADSP-2103 that contain factory-programmed on-chip ROM program memory. These devices offer different amounts of on-chip memory for program and data storage. Table II shows the features available in the ADSP-216x series of custom ROM-coded processors.

The ADSP-216x products eliminate the need for an external boot EPROM in your system, and can also eliminate the need for any external program memory by fitting the entire application program in on-chip ROM. These devices thus provide an excellent option for volume applications where board space and system cost constraints are of critical concern.

FUNCTIONAL BLOCK DIAGRAM



Development Tools

The ADSP-21xx processors are supported by a complete set of tools for system development. The ADSP-2100 Family Development Software includes C and assembly language tools that allow programmers to write code for any of the ADSP-21xx processors. The ANSI C compiler generates ADSP-21xx assembly source code, while the runtime C library provides ANSI-standard and custom DSP library routines. The ADSP-21xx assembler produces object code modules which the linker combines into an executable file. The processor simulators provide an interactive instruction-level simulation with a reconfigurable, windowed user interface. A PROM splitter utility generates PROM programmer compatible files.

EZ-ICE® in-circuit emulators allow debugging of ADSP-21xx systems by providing a full range of emulation functions such as modification of memory and register values and execution breakpoints. EZ-LAB® demonstration boards are complete DSP systems that execute EPROM-based programs.

The EZ-Kit Lite is a very low cost evaluation/development platform that contains both the hardware and software needed to evaluate the ADSP-21xx architecture.

Additional details and ordering information is available in the *ADSP-2100 Family Software & Hardware Development Tools* data sheet (ADDS-21xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

Additional Information

This data sheet provides a general overview of ADSP-21xx processor functionality. For detailed design information on the architecture and instruction set, refer to the *ADSP-2100 Family User's Manual*, available from Analog Devices.

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Table I. ADSP-21xx Processor Features

Feature	2101	2103	2105	2115	2111
Data Memory (RAM)	1K	1K	½K	½K	1K
Program Memory (RAM)	2K	2K	1K	1K	2K
Timer	●	●	●	●	●
Serial Port 0 (Multichannel)	●	●	–	●	●
Serial Port 1	●	●	●	●	●
Host Interface Port	–	–	–	–	●
Speed Grades *(Instruction Cycle Time)*					
10.24 MHz *(76.9 ns)*	–	●	–	–	–
13.0 MHz *(76.9 ns)*	–	–	–	–	●
13.824 MHz *(72.3 ns)*	–	–	●	–	–
16.67 MHz *(60 ns)*	●	–	–	●	●
20.0 MHz *(50 ns)*	●	–	●	●	●
25 MHz *(40 ns)*	●	–	–	●	–
Supply Voltage	5 V	3.3 V	5 V	5 V	5 V
Packages					
68-Pin PGA	●	–	–	–	–
68-Lead PLCC	●	●	●	●	–
80-Lead PQFP	●	●	–	●	–
80-Lead TQFP	–	–	–	●	–
100-Pin PGA	–	–	–	–	●
100-Lead PQFP	–	–	–	–	●
Temperature Grades					
K *Commercial* 0°C to +70°C	●	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●	●
T *Extended* –55°C to +125°C	●	–	–	–	●

Table II. ADSP-216x ROM-Programmed Processor Features

Feature	2161	2162	2163	2164
Data Memory (RAM)	½K	½K	½K	½K
Program Memory (ROM)	8K	8K	4K	4K
Program Memory (RAM)	–	–	–	–
Timer	●	●	●	●
Serial Port 0 (Multichannel)	●	●	●	●
Serial Port 1	●	●	●	●
Supply Voltage	5 V	3.3 V	5 V	3.3 V
Speed Grades *(Instruction Cycle Time)*				
10.24 MHz *(97.6 ns)*	–	●	–	●
16.67 MHz *(60 ns)*	●	–	●	–
25 MHz *(40 ns)*	–	–	●	–
Packages				
68-Lead PLCC	●	●	●	●
80-Lead PQFP	●	●	●	●
Temperature Grades				
K *Commercial* 0°C to +70°C	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●

ADSP-2171/ADSP-2172/ADSP-2173

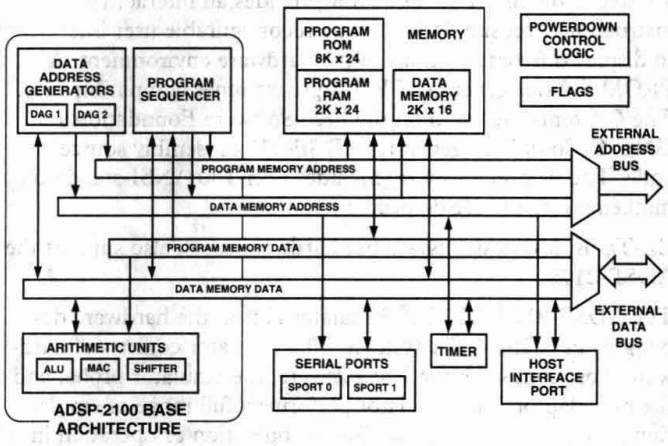
FEATURES

30 ns Instruction Cycle Time (33 MIPS) from 16.67 MHz Crystal at 5.0 V
50 ns Instruction Cycle Time (20 MIPS) from 10 MHz Crystal at 3.3 V
ADSP-2100 Family Code & Function Compatible with New Instruction Set Enhancements for Bit Manipulation Instructions, Multiplication Instructions, Biased Rounding, and Global Interrupt Masking
Bus Grant Hang Logic
2K Words of On-Chip Program Memory RAM
2K Words of On-Chip Data Memory RAM
8K Words of On-Chip Program Memory ROM (ADSP-2172)
8- or 16-Bit Parallel Host Interface Port
300 mW Typical Power Dissipation at 5.0 V at 30 ns
70 mW Typical Power Dissipation at 3.3 V at 50 ns
Powerdown Mode Featuring Less than 0.55 mW (ADSP-2171/ADSP-2172) or 0.36 mW (ADSP-2173) CMOS Standby Power Dissipation with 100 Cycle Recovery from Powerdown
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides
Zero Overhead Looping
Conditional Instruction Execution
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Host Interface Port
Stand-Alone ROM Execution (Optional)
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
128-Lead TQFP and 128-Lead PQFP

GENERAL DESCRIPTION

The ADSP-2171, ADSP-2172, and ADSP-2173 are single-chip microcomputers optimized for digital signal processing (DSP) and other high-speed numeric processing applications. The ADSP-2171 and ADSP-2172 are designed for 5.0 V applications. The ADSP-2173 is designed for 3.3 V applications. The ADSP-2172 also has 8K words (24-bit) of program ROM.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-217x combines the ADSP-2100 base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a host interface port, a programmable timer, extensive interrupt capabilities, and on-chip program and data memory.

In addition, the ADSP-217x supports new instructions, which include bit manipulations–bit set, bit clear, bit toggle, bit test–new ALU constants, new multiplication instruction (x squared), biased rounding, and global interrupt masking, for increased flexibility. The ADSP-217x also has a Bus Grant Hang Logic ($\overline{\text{BGH}}$) feature.

The ADSP-217x provides 2K words (24-bit) of program RAM and 2K words (16-bit) of data memory. The ADSP-2172 provides an additional 8K words (24-bit) of program ROM. Powerdown circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-217x is available in 128-pin TQFP and 128-pin PQFP packages.

Fabricated in a high-speed, double metal, low power, CMOS process, the ADSP-217X operates with a 30 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-217x's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-217x can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- receive and transmit data through the two serial ports
- receive and/or transmit data through the host interface port
- decrement timer

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Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-217x. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-217x assembly source code. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

EZ-Tools, low cost, easy-to-use hardware tools, also support the ADSP-217x.

The ADSP-217x EZ-ICE® Emulator aids in the hardware debugging of ADSP-217x systems. The emulator consists of hardware, host computer resident software, the emulator probe, and the pin adaptor. The emulator performs a full range of emulation functions including stand-alone operation or operation in the target, setting up to 20 breakpoints, single-step or full-speed operation in the target, examining and altering registers and memory values, and PC upload/download functions. If you plan to use the emulator, you should consider the emulator's restrictions (differences between emulator and processor operation).

The EZ-LAB® Evaluation Board is a PC plug-in card, but it can operate in stand-alone mode. The evaluation board/system development board executes EPROM-based or downloaded programs. Modular Analog Front End daughter cards with different codecs will be made available.

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Additional Information

This data sheet provides a general overview of ADSP-217x functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual.* For more information about the Development System and ADSP-217x programmer's reference information, refer to the *ADSP-2100 Family Assembler Tools & Simulator Manual.*

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-217x. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-217x executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

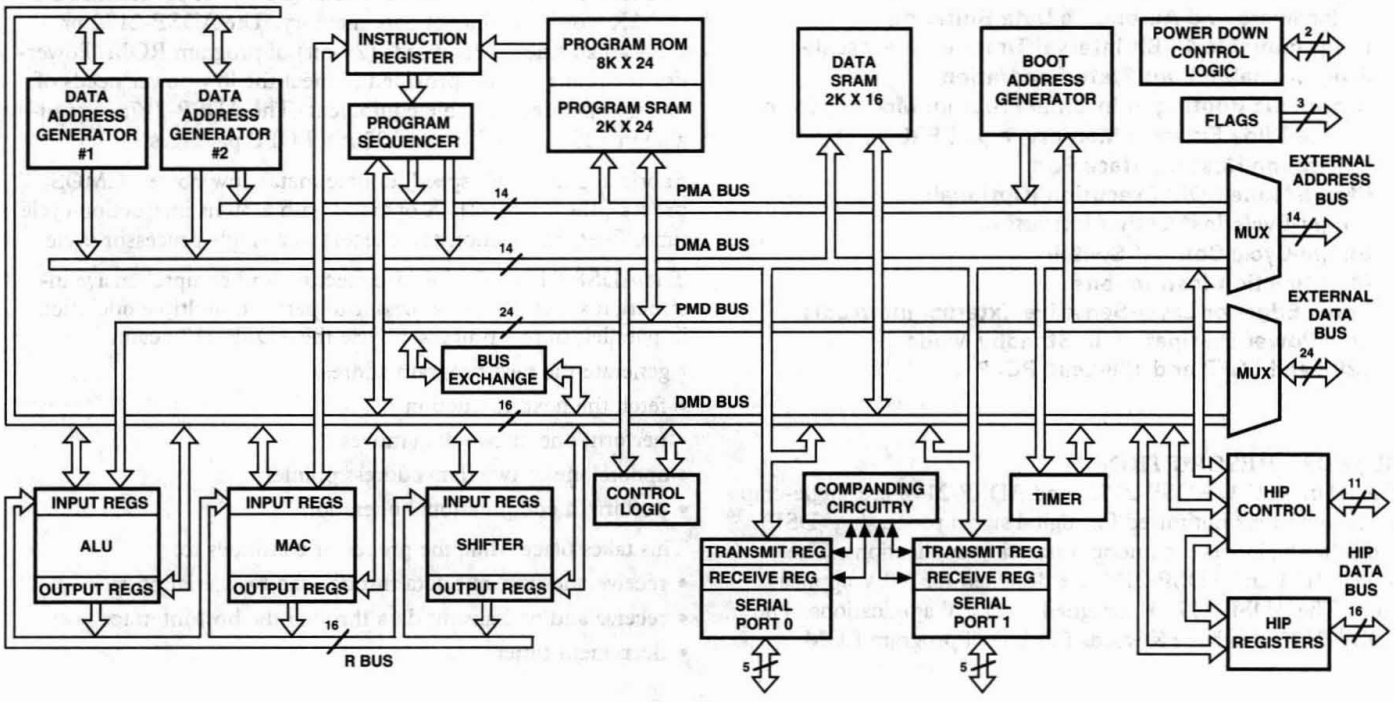


Figure 1. ADSP-217x Block Diagram

ANALOG DEVICES

DSP Microcomputer

ADSP-2181

FEATURES

PERFORMANCE

- 30 ns Instruction Cycle Time from 16.67 MHz Crystal @ 5.0 Volts
- 33 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 100 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

INTEGRATION

- ADSP-2100 Family Code Compatible, with Instruction Set Extensions
- 80K Bytes of On-Chip RAM, Configured as
  - 16K Words On-Chip Program Memory RAM
  - 16K Words On-Chip Data Memory RAM
- Dual Purpose Program Memory for Both Instruction and Data Storage
- Independent ALU, Multiplier/Accumulator, & Barrel Shifter Computational Units
- Two Independent Data Address Generators
- Powerful Program Sequencer Provides
  - Zero Overhead Looping
  - Conditional Instruction Execution
- Programmable 16-Bit Interval Timer with Prescaler
- 128-Lead TQFP/128-Lead PQFP

SYSTEM INTERFACE

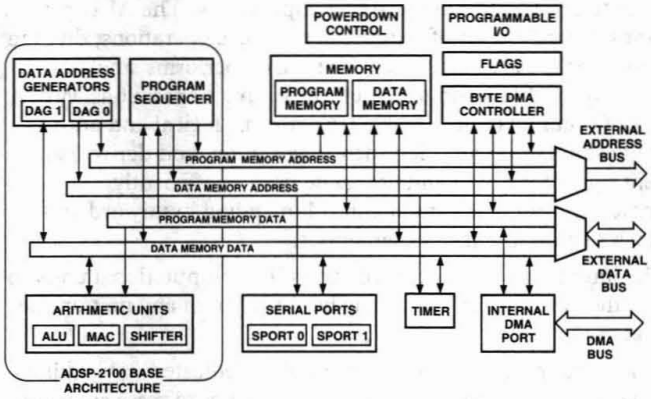
- 16-Bit Internal DMA Port for High Speed Access to On-Chip Memory
- 4 MByte Memory Interface for Storage of Data Tables & Program Overlays
- 8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers
- I/O Memory Interface with 2048 Locations Supports Parallel Peripherals
- Programmable Memory Strobe & Separate I/O Memory Space Permits "Glueless" System Design
- Programmable Wait State Generation
- Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
- Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port
- Six External Interrupts
- 13 Programmable Flag Pins Provide Flexible System Signaling
- ICE-Port™ Emulator Interface Supports Debugging in Final Systems

ICE-Port is a trademark of Analog Devices, Inc.

GENERAL DESCRIPTION

The ADSP-2181 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-2181 combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2181 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM, and 16K words (16-bit) of data RAM. Power down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2181 is available in 128-pin TQFP and 128-pin PQFP packages.

In addition, the ADSP-2181 supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers, and global interrupt masking, for increased flexibility.

Fabricated in a high speed, double metal, low power, 0.5 µm CMOS process, the ADSP-2181 operates with a 30 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2181's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2181 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- receive and transmit data through the two serial ports
- receive and/or transmit data through the internal DMA port
- receive and/or transmit data through the byte DMA port
- decrement timer .

ARCHITECTURE OVERVIEW

The ADSP-2181 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single

processor cycle. The ADSP-2181 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSP-2181. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2181 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2181 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2181 can fetch an operand from program memory and the next instruction in the same cycle.

In addition to the address and data bus for external memory connection, the ADSP-2181 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2181 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2181 can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2181 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs, and three flags that are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2181 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2181 SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

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DSP, Floating-Point Processors
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DSP, Floating-Point Processors—Selection Guide

Model	Instruction Cycle Time ns	Internal Program Memory	Internal Data Memory	Internal Program Cache Word	Serial Ports	Program-mable Timer	External Interrupts	Low Power Modes	Pin Count	Page No.	Fax-code
ADSP-21020	30	None	None	32 × 48	None	√	4	1	223	26–3	1578
ADSP-21062	25	(2 Megabit Total)		32 × 48	2	√	3	1	240	26–5	1882
ADSP-21060	25	(4 Megabit Total)		32 × 48	2	√	3	1	240	26–5	1870

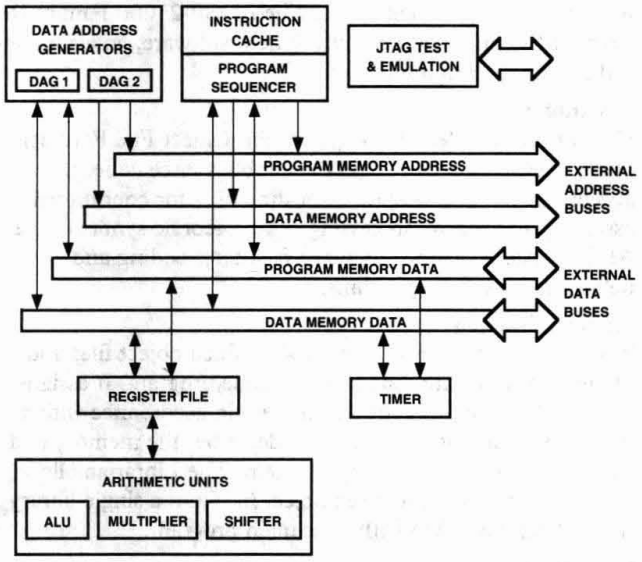
30-/40-Bit IEEE Floating-Point DSP Microprocessor

ADSP-21020

FEATURES

Superscalar IEEE Floating-Point Processor
Off-Chip Harvard Architecture Maximizes Signal Processing Performance
30 ns, 33.3 MIPS Instruction Rate, Single-Cycle Execution
100 MFLOPS Peak, 66 MFLOPS Sustained Performance
1024-Point Complex FFT Benchmark: 0.58 ms
Divide (y/x): 180 ns
Inverse Square Root ($1/\sqrt{x}$): 270 ns
32-Bit Single-Precision and 40-Bit Extended-Precision IEEE Floating-Point Data Formats
32-Bit Fixed-Point Formats, Integer and Fractional, with 80-Bit Accumulators
IEEE Exception Handling with Interrupt on Exception
Three Independent Computation Units: Multiplier, ALU, and Barrel Shifter
Dual Data Address Generators with Indirect, Immediate, Modulo, and Bit Reverse Addressing Modes
Two Off-Chip Memory Transfers in Parallel with Instruction Fetch and Single-Cycle Multiply & ALU Operations
Multiply with Add & Subtract for FFT Butterfly Computation
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
Single-Cycle Register File Context Switch
15 (or 25) ns External RAM Access Time for Zero-Wait-State, 30 (or 40) ns Instruction Execution
IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation Circuitry
223-Pin PGA Package (Ceramic)

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-21020 is the first member of Analog Devices' family of single-chip IEEE floating-point processors optimized for digital signal processing applications. Its architecture is similar to that of Analog Devices' ADSP-2100 family of fixed-point DSP processors.

Fabricated in a high-speed, low-power CMOS process, the ADSP-21020 has a 30 ns instruction cycle time. With a high-performance on-chip instruction cache, the ADSP-21020 can execute every instruction in a single cycle.

The ADSP-21020 features:

- **Independent Parallel Computation Units**
  The arithmetic/logic unit (ALU), multiplier and shifter perform single-cycle instructions. The units are architecturally arranged in parallel, maximizing computational throughput. A single multifunction instruction executes parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.
- **Data Register File**
  A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port (16-register) register file, combined with the ADSP-21020's Harvard architecture, allows unconstrained data flow between computation units and off-chip memory.
- **Single-Cycle Fetch of Instruction and Two Operands**
  The ADSP-21020 uses a modified Harvard architecture in which data memory stores data and program memory stores both instructions and data. Because of its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch an operand from data memory, an operand from program memory, and an instruction from the cache, all in a single cycle.
- **Memory Interface**
  Addressing of external memory devices by the ADSP-21020 is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM.

  The ADSP-21020 provides programmable memory wait states, and external memory acknowledge controls allow interfacing to peripheral devices with variable access times.
- **Instruction Cache**
  The ADSP-21020 includes a high performance instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with program memory data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.
- **Hardware Circular Buffers**
  The ADSP-21020 provides hardware to implement circular buffers in memory, which are common in digital filters and Fourier transform implementations. It handles address pointer wraparound, reducing overhead (thereby increasing performance) and simplifying implementation. Circular buffers can start and end at any location.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

- **Flexible Instruction Set**
  The ADSP-21020's 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21020 can conditionally execute a multiply, an add, a subtract and a branch in a single instruction.

DEVELOPMENT SYSTEM

The ADSP-21020 is supported with a complete set of software and hardware development tools. The ADSP-21000 Family Development System includes development software, an evaluation board and an in-circuit emulator.

- **Assembler**
  Creates relocatable, COFF (Common Object File Format) object files from ADSP-21xxx assembly source code. It accepts standard C preprocessor directives for conditional assembly and macro processing. The algebraic syntax of the ADSP-21xxx assembly language facilitates coding and debugging of DSP algorithms.
- **Linker/Librarian**
  The Linker processes separately assembled object files and library files to create a single executable program. It assigns memory locations to code and to data in accordance with a user-defined architecture file that describes the memory and I/O configuration of the target system. The Librarian allows you to group frequently used object files into a single library file that can be linked with your main program.
- **Simulator**
  The Simulator performs interactive, instruction-level simulation of ADSP-21xxx code within the hardware configuration described by a system architecture file. It flags illegal operations and supports full symbolic disassembly. It provides an easy-to-use, window oriented, graphical user interface that is identical to the one used by the ADSP-21020 EZ-ICE Emulator. Commands are accessed from pull-down menus with a mouse.
- **PROM Splitter**
  Formats an executable file into files that can be used with an industry-standard PROM programmer.
- **C Compiler and Runtime Library**
  The C Compiler complies with ANSI specifications. It takes advantage of the ADSP-21020's high-level language architectural features and incorporates optimizing algorithms to speed up the execution of code. It includes an extensive runtime library with over 100 standard and DSP-specific functions.
- **C Source Level Debugger**
  A full-featured C source level debugger that works with the simulator or EZ-ICE emulator to allow debugging of assembler source, C source, or mixed assembler and C.
- **Numerical C Compiler**
  Supports ANSI Standard (X3J11.1) Numerical C as defined by the Numeric C Extensions Group. The compiler accepts C source input containing Numerical C extensions for array selection, vector math operations, complex data types, circular pointers, and variably dimensioned arrays, and outputs ADSP-21xxx assembly language source code.
- **ADSP-21020 EZ-LAB® Evaluation Board**
  The EZ-LAB Evaluation Board is a general-purpose, stand-alone ADSP-21020 system that includes 32K words of program memory and 32K words of data memory as well as analog I/O. A PC RS-232 download path enables the user to download and run programs directly on the EZ-LAB. In addition, it may be used in conjunction with the EZ-ICE Emulator to provide a powerful software debug environment.
- **ADSP-21020 EZ-ICE® Emulator**
  This in-circuit emulator provides the system designer with a PC-based development environment that allows nonintrusive access to the ADSP-21020's internal registers through the processor's 5-pin JTAG Test Access Port. This use of on-chip emulation circuitry enables reliable, full-speed performance in any target. The emulator uses the same graphical user interface as the ADSP-21020 Simulator, allowing an easy transition from software to hardware debug. (See "Target System Requirements for Use of EZ-ICE Emulator" on page 27.)

ADDITIONAL INFORMATION

This data sheet provides a general overview of ADSP-21020 functionality. For additional information on the architecture and instruction set of the processor, refer to the ADSP-21020 User's Manual. For development system and programming reference information, refer to the ADSP-21000 Family Development Software Manuals and the ADSP-21020 Programmer's Quick Reference. Applications code listings and benchmarks for key DSP algorithms are available on the DSP Applications BBS; call (617) 461-4258, 8 data bits, no parity, 1 stop bit, 300/1200/2400/9600 baud.

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ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Cycle Time (ns)	Package[2]
ADSP-21020KG-80	0°C to +70°C	20	50	223-Lead Ceramic Pin Grid Array
ADSP-21020KG-100	0°C to +70°C	25	40	223-Lead Ceramic Pin Grid Array
ADSP-21020KG-133	0°C to +70°C	33.3	30	223-Lead Ceramic Pin Grid Array
ADSP-21020BG-80	–40°C to +85°C	20	50	223-Lead Ceramic Pin Grid Array
ADSP-21020BG-100	–40°C to +85°C	25	40	223-Lead Ceramic Pin Grid Array
ADSP-21020BG-120	–40°C to +85°C	30	33.3	223-Lead Ceramic Pin Grid Array
ADSP-21020TG-80	–55°C to +125°C	20	50	223-Lead Ceramic Pin Grid Array
ADSP-21020TG-100	–55°C to +125°C	25	40	223-Lead Ceramic Pin Grid Array
ADSP-21020TG-120	–55°C to +125°C	30	33.3	223-Lead Ceramic Pin Grid Array
ADSP-21020TG-80/883B	–55°C to +125°C	20	50	223-Lead Ceramic Pin Grid Array
ADSP-21020TG-100/883B	–55°C to +125°C	25	40	223-Lead Ceramic Pin Grid Array
ADSP-21020TG-120/883B	–55°C to +125°C	30	33.3	223-Lead Ceramic Pin Grid Array

NOTES
[1]G = Ceramic Pin Grid Array.
[2]For outline information see Package Information section.

ADSP-2106x SHARC DSP Microcomputer Family

ADSP-21062/ADSP-21060

SUMMARY

High Performance Signal Processor for Communications, Graphics, and Imaging Applications

Super Harvard ARchitecture Computer (SHARC™)—Four Independent Buses for Dual Data Fetch, Instruction Fetch, and Nonintrusive I/O

32-Bit IEEE Floating-Point Computation Units—Multiplier, ALU, and Shifter

Dual-Ported On-Chip SRAM and Integrated I/O Peripherals—A Complete System-On-A-Chip

Integrated Multiprocessing Features

KEY FEATURES

40 MIPS, 25 ns Instruction Rate, Single-Cycle Instruction Execution

120 MFLOPS Peak, 80 MFLOPS Sustained Performance

Dual Data Address Generators with Modulo and Bit-Reverse Addressing

Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup

IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation

240-Lead Thermally Enhanced PQFP Package

32-Bit Single-Precision & 40-Bit Extended-Precision IEEE Floating-Point Data Formats or 32-Bit Fixed-Point Data Format

Parallel Computations

Single-Cycle Multiply & ALU Operations in Parallel with Dual Memory Read/Writes & Instruction Fetch

Multiply with Add & Subtract for Accelerated FFT Butterfly Computation

4 Mbit/2 Mbit On-Chip SRAM (ADSP-21060/ADSP-21062)

Dual-Ported for Independent Access by Core Processor and DMA

Off-Chip Memory Interfacing

4 Gigawords Addressable

Programmable Wait State Generation, Page-Mode DRAM Support

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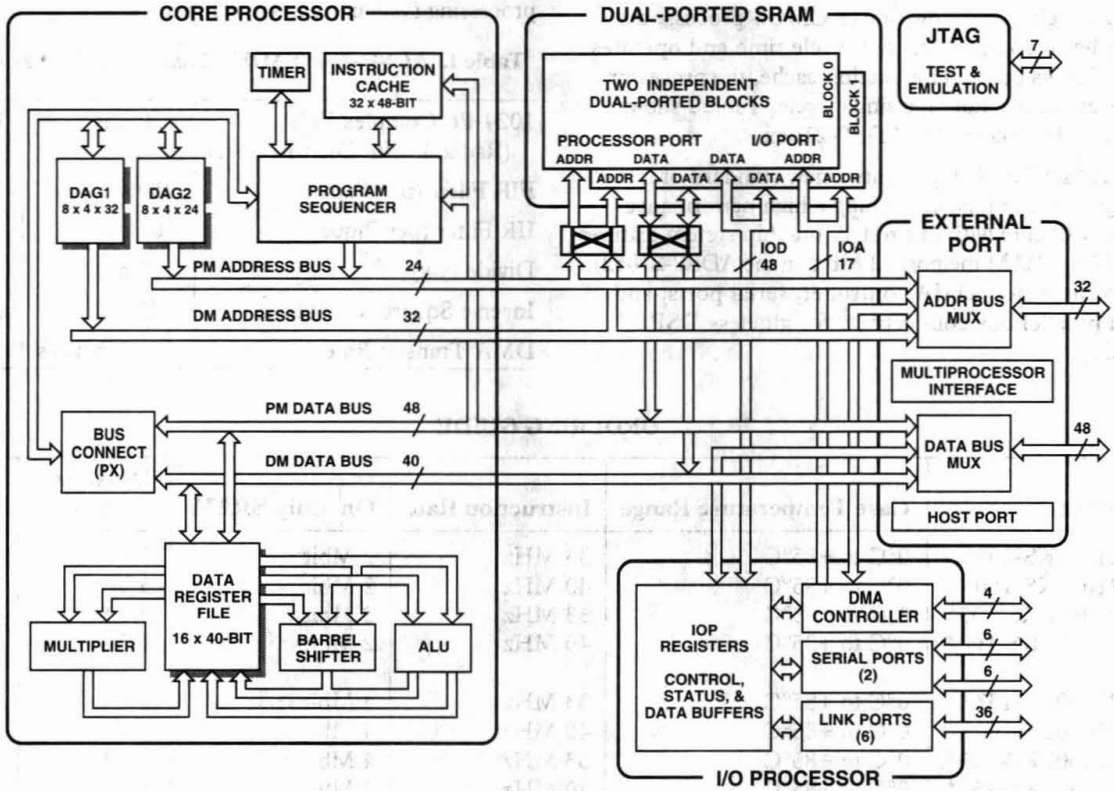

Figure 1. ADSP-21060/ADSP-21062 Block Diagram

MA Controller

10 DMA Channels for Transfers Between ADSP-2106x Internal Memory and External Memory, External Peripherals, Host Processor, Serial Ports, or Link Ports

Background DMA Transfers at 40 MHz, in Parallel with Full-Speed Processor Execution

Host Processor Interface to 16- & 32-Bit Microprocessors

Host Can Directly Read/Write ADSP-2106x Internal Memory

Multiprocessing

Glueless Connection for Scalable DSP Multiprocessing Architecture

Distributed On-Chip Bus Arbitration for Parallel Bus Connect of Up to Six ADSP-2106xs Plus Host

Six Link Ports for Point-to-Point Connectivity and Array Multiprocessing

240 Mbytes/s Transfer Rate Over Parallel Bus

240 Mbytes/s Transfer Rate Over Link Ports

Serial Ports

Two 40 Mbit/s Synchronous Serial Ports with Companding Hardware

Independent Transmit & Receive Functions

GENERAL NOTE

This data sheet represents production released specifications for the ADSP-21062 (5 V) processor, Revision 1.x. This data sheet also represents preliminary specifications for the ADSP-21062L (3.3 V), ADSP-21060 (5 V), and the ADSP-21060L (3.3 V) parts.

GENERAL DESCRIPTION

The ADSP-21062 and ADSP-21060 SHARC—Super Harvard ARchitecture Computers—are signal processing microcomputers that offer new capabilities and levels of performance. The ADSP-2106x SHARCs are 32-bit processors optimized for high performance DSP applications. The ADSP-2106x builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-2106x has a 25 ns instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I shows performance benchmarks for the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including a 4 Mbit SRAM memory (2 Mbit on the ADSP-21062), host processor interface, DMA controller, serial ports, and link port and parallel bus connectivity for glueless DSP multiprocessing.

Figure 1 shows a block diagram of the ADSP-2106x, illustrating the following architectural features:

Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
Data Address Generators (DAG1, DAG2)
Program Sequencer with Instruction Cache
Interval Timer
On-Chip SRAM
External Port for Interfacing to Off-Chip Memory & Peripherals
Host Port & Multiprocessor Interface
DMA Controller
Serial Ports & Link Ports
JTAG Test Access Port

Figure 2 shows a typical single-processor system. A multiprocessing system is shown in Figure 3.

Table I. ADSP-21060/ADSP-21062 Benchmarks (@ 40 MHz)

1024-Pt. Complex FFT (Radix 4, with Digit Reverse)	0.46 ms	18,221 cycles
FIR Filter (per Tap)	25 ns	1 cycle
IIR Filter (per Biquad)	100 ns	4 cycles
Divide (y/x)	150 ns	6 cycles
Inverse Square Root ($1/\sqrt{x}$)	225 ns	9 cycles
DMA Transfer Rate	240 Mbytes/s	

ORDERING GUIDE

Part Number*	Case Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Option[2]
ADSP-21062KS-133	0°C to +85°C	33 MHz	2 Mbit	5 V	PQFP
ADSP-21062KS-160	0°C to +85°C	40 MHz	2 Mbit	5 V	PQFP
ADSP-21062LKS-133*	0°C to +85°C	33 MHz	2 Mbit	3.3 V	PQFP
ADSP-21062LKS-160*	0°C to +85°C	40 MHz	2 Mbit	3.3 V	PQFP
ADSP-21060KS-133*	0°C to +85°C	33 MHz	4 Mbit	5 V	PQFP
ADSP-21060KS-160*	0°C to +85°C	40 MHz	4 Mbit	5 V	PQFP
ADSP-21060LKS-133*	0°C to +85°C	33 MHz	4 Mbit	3.3 V	PQFP
ADSP-21060LKS-160*	0°C to +85°C	40 MHz	4 Mbit	3.3 V	PQFP

NOTES

[1]Part numbers marked with an * are shipping as x-grade (preproduction) material at the time of this printing.

[2]These parts are packaged in a 240-lead, thermally enhanced Plastic Quad Flatpack (PQFP).
For outline information see Package Information section.

[3]Parts for the industrial and military temperature ranges will be available later in 1996.

DSP, Development Tools
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ADDS-210xx-TOOLS – ADSP-21000 Family Development Tools	27–5

DSP, Development Tools—Selection Guides

Software

Model	Product Description
ADDS-21xx-SW-PC	IBM-PC† version of Development Software for the ADSP-2100 Family. Development Software includes Assembler, Linker, Simulator, Prom Splitter, and Librarian plus the C Tools. C Tools include the C Compiler, Runtime Library and C Source-Level Debugger.
ADDS-21xx-SW-SUN	SUN4 version of Development Software and C Tools.
ADDS-210xx-SW-PC	IBM-PC† version of Development Software for the ADSP-21000 Family. Development Software includes Assembler, Linker, Simulator, Prom Splitter, and Librarian plus the C Tools. C Tools include the C Compiler, Runtime Library and C Source-Level Debugger.
ADDS-210xx-SW-SUN	SUN4 version of Development Software plus the C Tools.

Hardware

ADDS-2101-EZ-KIT	ADSP-2101/ADSP-2105 low cost development package. Includes IBM PC Development Software and evaluation board.
ADDS-2111-EZ-KIT	ADSP-2111 low cost development package. Includes IBM PC Development Software and evaluation board.
ADDS-2101-EZ-LAB	ADSP-2101 (EZ-LAB®) evaluation board.
ADDS-2111-EZ-LAB	ADSP-2111 evaluation board.
ADDS-2171-EZ-LAB	ADSP-2171 evaluation board.
ADDS-21020-EZ-LAB	ADSP-21020 evaluation board.
ADDS-2106x-EZ-LAB	ADSP-21060/ADSP-21062 evaluation board.
ADDS-2101-EZ-ICE	ADSP-2101 low cost compact (EZ-ICE®) in-circuit emulator.
ADDS-2111-EZ-ICE	ADSP-2111 low cost compact in-circuit emulator.
ADDS-2171-EZ-ICE	ADSP-2171 in-circuit emulator.
ADDS-2181-EZ-ICE	ADSP-2181 in-circuit emulator.
ADDS-21020-EZ-ICE	ADSP-21020 low cost compact in-circuit emulator.
ADDS-2106x-EZ-ICE	ADSP-21060/ADSP-21062 in-circuit emulator.
ADDS-21xx-EZLITE	ADSP-2181 low cost demo/evaluation board.
ADDS-21020-EZ-KIT-PL	ADSP-21020/ADSP-21010 low cost development package. Includes IBM PC Development Software, C Compiler Tools, and evaluation board.

Training Courses

ADDS-21xx-WKSHP	ADSP-2100 Family 3-Day Workshop. Offered in Norwood, Massachusetts; California; Georgia and Europe.
ADDS-210xx-WKSHP	ADSP-21000 Family 3-Day Workshop. Offered in Norwood, Massachusetts; California; Georgia and Europe.

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†IBM PC is a trademark of International Business Machines Corporation.

ADSP-2100 Family Development Tools

ADDS-21xx-TOOLS

FEATURES

DEVELOPMENT SOFTWARE TOOLS

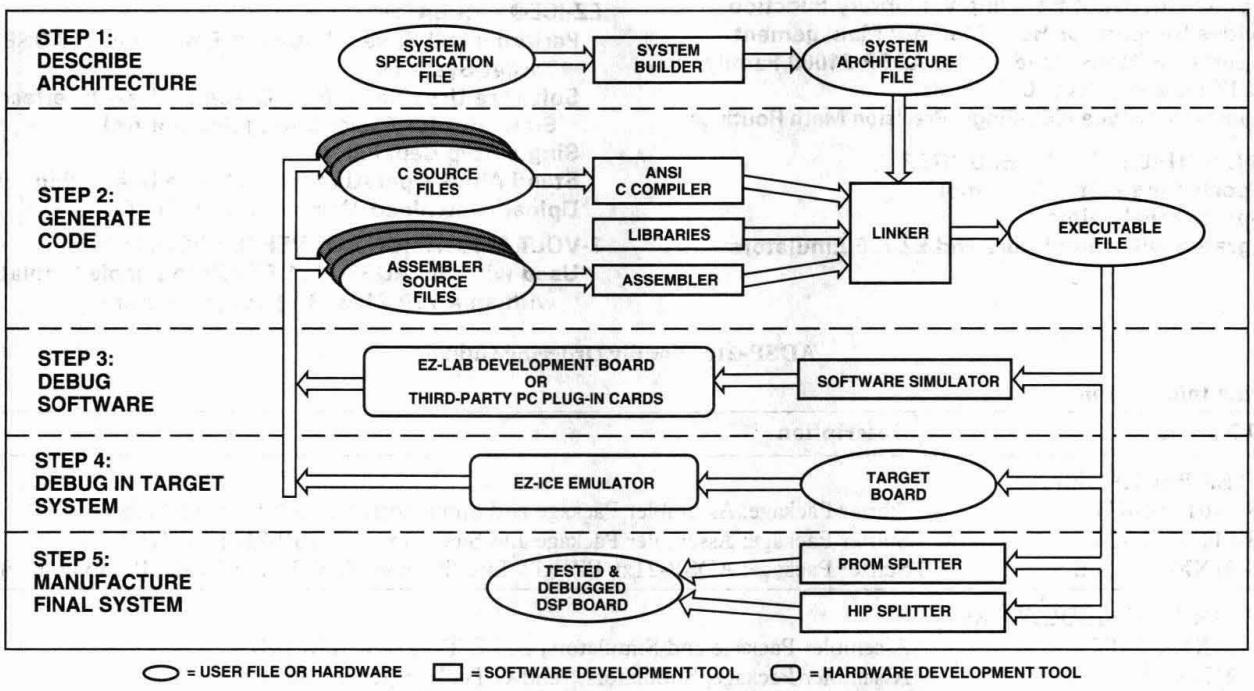
SYSTEM BUILDER
- Defines Architecture of ADSP-21xx System
- Specifies Amount of RAM/ROM Memory

ASSEMBLER
- Easy-to-Program, Algebraic Instruction Syntax
- Supports C Language Constructs
- Provides Flexible Macro Processing
- Encourages Modular Code Development

LINKER
- Maps Assembler Output to Target System Memory
- Supports User-Defined Library Routines
- Creates Memory Map Listing

PROM SPLITTER & HOST PROCESSOR PORT (HIP) SPLITTER
- Generates PROM Programmer Compatible Files in a Variety of Industry-Standard Formats
- Formats Executable File for Programming PROMs or for Host Processor Booting

SYSTEM DEVELOPMENT PROCESS OVERVIEW



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ADDS-21xx-TOOLS

SIMULATOR
- Features Reconfigurable GUI (Graphical User Interface)
- Supports Full Symbolic Disassembly and On-Line Assembly
- Provides Breakpoint and Single-Step Execution
- Includes CBUG™ C Source-Level Debugger as Integrated Tool
- Supports Multiple Break Conditions
- Provides Full View of All Processor Registers and Memory for Direct Modification of Contents
- Profiles Code Execution History
- Uses Data Files to Simulate Parallel I/O Ports, Serial Ports, HIPs, and Analog I/O Interface
- Plots Data Memory Graphically

G21 OPTIMIZING C COMPILER & C RUNTIME LIBRARY
- Compliant with ANSI C Standards
- Includes C-Callable Library of ANSI-Standard and DSP Functions
- Supports In-Line Assembly Code Using asm () Construct
- Incorporates Optimizing Algorithms
- Generates Reliable and ROM-able Code
- Simplifies Interrupt Handling via Library Functions
- Provides Support for Heap Memory Management
- Supports Switches Used by the ADSP-21000 Family G21K Floating Point C Compiler
- Supports Float Type IEEE-Single Precision Math Routines

CBUG C SOURCE-LEVEL DEBUGGER
- Supports Single Step Execution
- Supports Breakpoints
- Integrated with Simulators and EZ-ICE Emulators

DEVELOPMENT HARDWARE TOOLS

EZ-LAB® EVALUATION BOARD
- Complete Hardware Platform with Memory and I/O
- Preprogrammed with DSP Demo Programs
- Contains Audio/Voice I/O Port with Microphone Input and Powered Output for Speaker
- Memory Expansion and I/O from Bus Expansion Connector
- Serial Port Interface via SPORT Connector

EZ-KIT STARTER PACKAGES
- Complete Hardware and Software Development Kit
- Includes an EZ-LAB Evaluation Board and ADSP-2100 Family Assembler/Linker and Simulator Software for IBM PC

EZ-KIT LITE
- Low Cost Development System
- Including Hardware and Software
  - MS Windows 3.1 Based Monitor
  - Includes a Variety of Demonstration Programs with Source Code
  - Development Platform for all ADSP-21xx Processors
  - Audio Input/Output and Expansion Connectors

EZ-ICE® EMULATOR
- Performs Full-Speed, In-Circuit Emulation of ADSP-21xx Target Systems
- Software Uses Same GUI (Graphical User Interface) as Simulator for Easier Debugging Control
- Single-Step Capability
- Stand Alone Operation for Software Debugging
- Upload/Download Memory with IBM PC

3-VOLT EMULATION CONVERTER BOARD
- Used with the ADSP-2101 EZ-ICE to Enable Emulation with an ADSP-2103 (3 V) Target System

ADSP-2100 Family Ordering Guide

Ordering Information

Model Number	Description
STARTER PACKAGES	
ADDS-2101-EZ-KIT	Starter Package: Assembler Package and Simulators,* ADSP-2101 EZ-LAB
ADDS-2111-EZ-KIT	Starter Package: Assembler Package and Simulators,* ADSP-2111 EZ-LAB
ADDS-21XX-EZLITE	Starter Package: ADSP-21xx EZ-KIT Lite (includes ADSP-2181 EZ-LAB, monitor software)
SOFTWARE AND HARDWARE	
ADDS-21XX-SW-PC	Assembler Package and Simulators, and C Tools (for IBM PC)
ADDS-21XX-SW-SUN	Assembler Package, Simulators,* and C Tools** (for the Sun4)
ADDS-2101-EZ-ICE	ADSP-2101 EZ-ICE Emulator
ADDS-2101-EZ-LAB	ADSP-2101 EZ-LAB Evaluation Board
ADDS-2101-3V	ADSP-2101 3-Volt Emulation Converter Board
ADDS-2111-EZ-ICE	ADSP-2111 EZ-ICE Emulator
ADDS-2111-EZ-LAB	ADSP-2111 Evaluation Board
ADDS-2171-EZ-ICE	ADSP-2171 EZ-ICE Emulator (for TQFP)
ADDS-2171-EZ-ICE-P	ADSP-2171 EZ-ICE Emulator (with PQFP Clip-On Adaptor)
ADDS-2171-EZ-LAB	ADSP-2171 EZ-LAB Evaluation Board
ADDS-2181-EZ-ICE	ADSP-2181 EZ-ICE Emulator
AVAILABLE FROM OTHER VENDORS	A comprehensive listing of additional hardware and software tools is available in the Analog Devices' *DSP Third Party Developer Directory.*

NOTES
*Assembler, Assembly Library/Librarian, Linker, PROM Splitter, HIP Splitter, and ADSP-21xx Simulators.
**G21 C Compiler, C Runtime Library, and CBUG C Source-Level Debugger.

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EZ-ICE and EZ-LAB are registered trademarks of Analog Devices, Inc.

ANALOG DEVICES

ADSP-21000 Family Development Tools

ADDS-210xx-TOOLS

FEATURES

DEVELOPMENT SOFTWARE TOOLS

ASSEMBLER
- Easy-to-Use Algebraic Syntax

LINKER
- Combines Object and Library Files

ASSEMBLY LIBRARY/LIBRARIAN
- Includes Set of Arithmetic and DSP Functions

SIMULATOR
- Reconfigurable, MS Windows GUI Interface
- Full Symbolic Disassembly and On-Line Assembly
- Simulates Memory and Port Configurations
- Plots Memory Graphically

PROM SPLITTER

OPTIMIZING G21K ANSI C COMPILER
- Includes C-Callable Library of ANSI Standard and DSP Functions
- Supports In-Line Assembly Code

CBUG™ C SOURCE LEVEL DEBUGGER
- Integrated with Simulator and Emulator; Uses Same GUI Interface

C RUNTIME LIBRARY
- Includes Over 150 DSP and Mathematical Functions

DEVELOPMENT HARDWARE TOOLS

EZ-LAB® DEVELOPMENT BOARD
- Enables Evaluation, Prototyping, and Development of ADSP-21000 Family-Based Systems
- 16-Bit IBM-AT Compatible Plug-In Board

EZ-KIT
- Includes the EZ-LAB Development Board, Development Software Tools, and C Compiler and Runtime Library

EZ-ICE® EMULATOR
- Full Speed, In-Circuit Emulation
- 8-Bit IBM-PC/AT Compatible Plug-In Board with Small 11-Pin JTAG In-Circuit Probe

ICEPAC™ EMBEDDABLE IN-CIRCUIT EMULATOR
- Incorporates Embedded Emulation Functionality in a Plug-In Target Board (ADSP-2106x Only)

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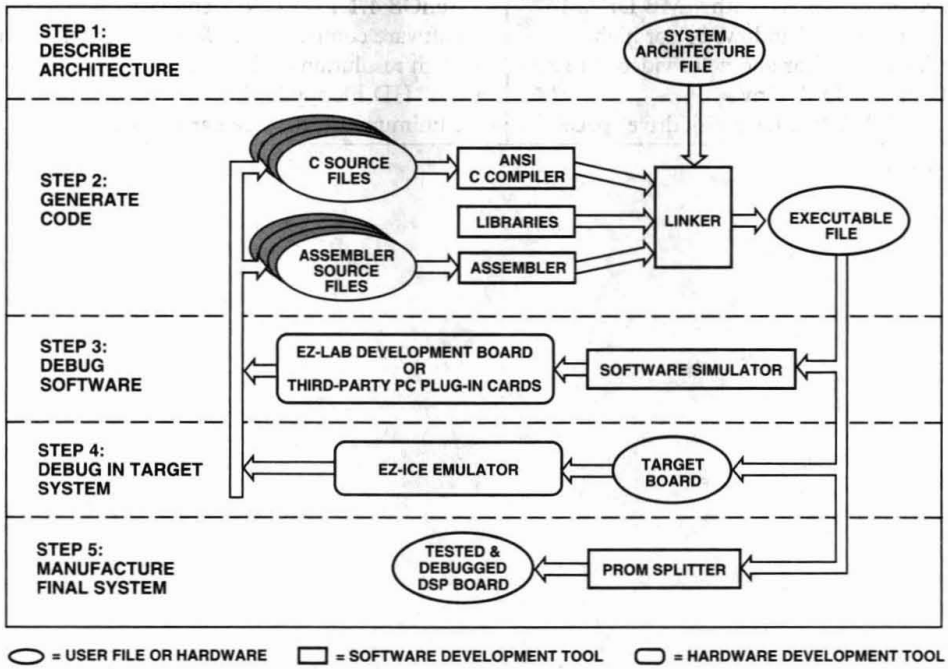
EZ-LAB and EZ-ICE are registered trademarks of Analog Devices, Inc.

SYSTEM DEVELOPMENT DIAGRAM



ADDS-210xx-TOOLS

INTRODUCTION TO DEVELOPMENT TOOLS

The ADSP-21000 Family Development Tools let you design applications for the ADSP-21000 family of Floating-Point DSP processors, including the ADSP-2106x SHARC. These tools enable you to develop hardware architectures together with creating and debugging code for your applications throughout the research, design, development, and test stages. The System Development Diagram illustrates how the tools work together. These tools are compatible with IBM-AT or Sun4 host platforms.

Components of the ADSP-21000 Family Development Tools fall into one of two broad categories: Software Tools and Hardware Tools.

Development Software Tools

- Assembler
- Linker
- Simulator
- PROM Splitter
- Assembly Library/Librarian
- Optimizing G21K ANSI C Compiler with Numeric C Extensions
- CBUG C Source-Level Debugger
- C Runtime Library

The Assembler translates ADSP-21000 Family assembly language source files into object code. The G21K C Compiler compiles C source files into object files or, optionally, into assembly language source files. The Linker then links the multiple object files together with various library files to form an executable program.

The ADSP-21000 Family Simulator runs the program on a software model of the DSP, reproducing the execution of the program by the processor in hardware. The simulator displays different portions of the virtual hardware environment through a reconfigurable windows interface identical to the emulator software interface.

Development Hardware Tools

- EZ-LAB Development Board
- EZ-ICE In-Circuit Emulator
- ICEPAC Embeddable In-Circuit Emulator (SHARC only)
- EZ-KIT and EZ-KIT Plus

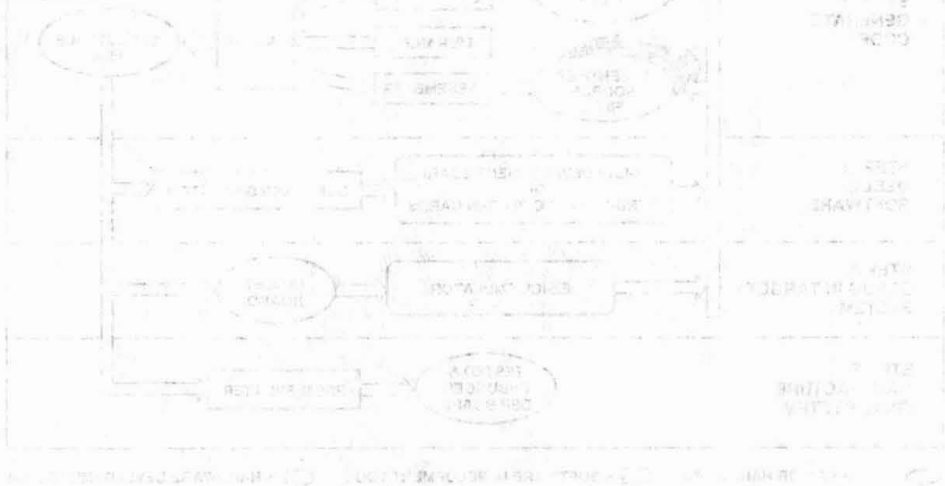
The ADSP-2106x and ADSP-21020 EZ-LAB Development Boards are ready-to-run target system and evaluation platforms. They let you download and execute your ADSP-21000 family programs in real time. EZ-ICE, an in-circuit emulator, provides a controlled environment for observing, debugging, and testing by directly connecting to the target processor through its (IEEE 1149.1) JTAG interface. The ICEPAC, a small daughter card, incorporates embedded emulation functionality that effectively adds all of the capabilities of the EZ-ICE to your PC plug-in target board.

The EZ-KIT for the ADSP-2106x SHARC and the EZ-KIT Plus for the ADSP-21020 include the EZ-LAB Development Board, the ADSP-21000 Family Development Software, the C Compiler, C Runtime Library, and the CBUG Source Level Debugger.

Minimum Host Platform Requirements*

IBM-AT	Sun4
• 386-based or greater AT with 4 MB DRAM • DOS 3.1 or higher; Windows 3.1 or higher • EGA or VGA Monitor and color video card • 3.5" HD Floppy Disk Drive • Minimum 11 MB free hard disk drive space	• SunOS 4.1.1 for UNIX software; Windows version software compatible in Windows emulation mode • High resolution color monitor • 3.5" HD Floppy Disk Drive • Minimum 19 MB free hard disk drive space

*Some tools may vary.



Power Supplies
Modular AC/DC Converters

GENERAL DESCRIPTION
Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 100 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES
- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±15 V), and Triple (±15 V/+5 V) Output Supplies
- Current Outputs:
  100 mA to 500 mA for Dual and Triple Output Supplies
  1000 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS
Power Requirements
- Input Voltage Range: 105 V ac to 125 V ac
- Frequency: 50 Hz to 250 Hz

Electrical Specifications
- Temperature Coefficient: 0.02%/°C
- Output Voltage Accuracy: ±2%, max
  See Specifications Table
- Breakdown Voltage: 500 V rms, min
- Isolation Resistance: 50 MΩ
- Short Circuit Protection: All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements
- Operating Temperature Range: –25°C to +71°C
- Storage Temperature Range: –25°C to +85°C

SPECIFICATIONS–Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	902-2	±15	±100	0.02	0.02	+300 mV –0 mV	0.5	3.5 × 2.5 × 0.875
		920	±15	±200	0.02	0.02	+300 mV –0 mV	0.5	3.5 × 2.5 × 1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5 × 2.5 × 1.62
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5 × 2.5 × 1.25
			+5	500	0.02	0.05	±1%	0.5	
Chassis Mounted	Dual Output	970	±15	±200	0.05	0.05	±2%	1	4.4 × 2.7 × 1.45
		975	±15	±500	0.05	0.05	±2%	1	4.4 × 2.7 × 2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4 × 2.7 × 1.45
		977	5	5000	0.05	0.10	±2%	100 (p-p typ)	4.75 × 2.7 × 1.45

*Consult Analog Devices Power Supplies Catalog for additional information.
Specifications subject to change without notice.

Power Supplies
Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Nine models are offered in four power levels of 1 watt, 1.8 watts, 4.5 watts and 6 watts. Input voltage versions include 5 volt, 12 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±40 mA to 1000 mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free-Air Convection Cooling
  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation—Full Range: ±0.3% (±1% max, 949) Load Regulation—No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p, with 15 µF tantalum capacitor across each output (2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: –25°C to +71°C
Storage Temperature Range: –40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W AND 6 W MODELS

Line Regulation—Full Range: ±0.07% max (±0.02% max, 960 Series) (±0.1% max, 943)
Load Regulation—No Load to Full Load: ±0.07% max (±0.02% max, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: –25°C to +71°C
Storage Temperature Range: –40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS - Typical @ +25°C at nominal input voltage unless otherwise noted[1]

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[2] Voltage Rate Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52 A	±1%	±0.02%	62%	2.0 × 2.0 × 0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25 × 0.8 × 0.4
941	±12	±150	5	4.75/5.25	1.17 A	±1%	±0.01%	58%	2.0 × 2.0 × 0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25 × 0.8 × 0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25 × 0.8 × 0.4
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0 × 2.0 × 0.38
949	±15	±60[3]	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0 × 1.0 × 0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0 × 2.0 × 0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0 × 2.0 × 0.38

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
[2]Consult Analog Devices Power Supplies Catalog for additional information.
[3]Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.

Specifications subject to change without notice.

Package Information
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D-20		20-Lead	D8-3	29–5
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*Special order only.

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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N-16	P	16-Lead		29–10
N-18	P	18-Lead		29–10
N-20	P	20-Lead		29–10
N-22	P	22-Lead		29–10
N-24	P	24-Lead		29–10
N-24A	P	24-Lead (Double Width)		29–10
N-24B		24-Lead		29–10
N-28	P	28-Lead		29–10
N-28A	P	28-Lead		29–10
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N-48	P	48-Lead		29–10
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ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
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ADI Letter Designator	PMI Letter Designator	Package Description	MIL-M38510 Applicable Configuration	Page
Leaded Chip Carrier (Ceramic)				
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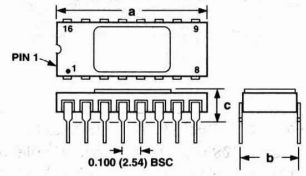
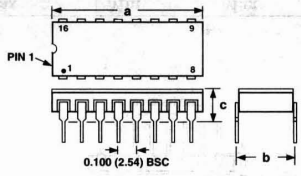
Z-16C		16-Lead		29–18
Z-28		28-Lead		29–18
Z-40		40-Lead		29–18
Z-68		68-Lead		29–18



Side Brazed DIP (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
D-8		8-Lead	0.512 (13.005)	0.528 (14.14)	0.280 (7.11)	0.320 (8.13)		0.210 (5.33)
D-14	YB**	14-Lead		0.785 (19.94)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-16	QB**	16-Lead		0.840 (21.34)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-18	XB**	18-Lead		0.960 (23.38)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-20		20-Lead		1.060 (26.92)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-22	RB**	22-Lead		1.111 (28.22)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-24	VB**	24-Lead		1.290 (32.77)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
D-24A		24-Lead (Single Width)		1.280 (32.51)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-28	TB**	28-Lead		1.490 (37.85)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
D-28A		28-Lead (Single Width)		1.480 (37.59)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
D-40		40-Lead		2.096 (53.24)	0.520 (13.21)	0.630 (16.00)		0.225 (5.72)
D-48		48-Lead	2.376 (60.35)	2.424 (63.57)	0.520 (13.21)	0.630 (16.00)		0.225 (5.72)

*For complete package dimensions see data sheet.
**Special order only

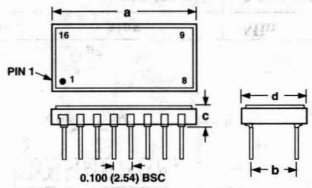


Side Brazed DIP for Hybrids (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
DH-24A		24-Lead		1.212 (30.79)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
DH-28		28-Lead		1.414 (35.92)	0.590 (14.99)	0.610 (15.49)		0.225 (5.72)

*For complete package dimensions see data sheet.

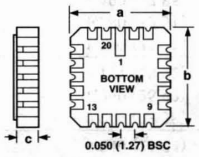
Package Information–Outline Dimensions



Bottom Brazed DIP (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*		d*	
			Min	Max	Min	Max	Min	Max	Min	Max
DH-40A		40-Lead	2.074 (52.68)	2.116 (53.75)	0.89 (22.61)	0.91 (23.11)		0.225 (5.72)	1.08 (27.41)	1.10 (27.97)
DH-48A		48-Lead	2.450 (62.23)	2.500 (63.50)	0.990 (25.15)	1.010 (25.65)	0.177 (4.50)	0.233 (5.92)	1.287 (32.69)	1.313 (33.35)

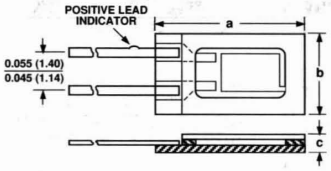
*For complete package dimensions see data sheet.



Leadless Chip Carrier (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
E-20A	RC	20-Terminal	0.342 (8.69)	0.358 (9.09)	0.342 (8.69)	0.358 (9.09)	0.064 (1.63)	0.100 (2.54)
E-28A	TC	28-Terminal	0.442 (11.23)	0.458 (11.63)	0.442 (11.23)	0.458 (11.63)	0.064 (1.63)	0.100 (2.54)
E-44A		44-Terminal	0.640 (16.26)	0.662 (16.82)	0.640 (16.26)	0.662 (16.82)	0.064 (1.63)	0.100 (2.54)
E-68A		68-Terminal	0.940 (23.88)	0.965 (24.51)	0.940 (23.88)	0.965 (24.51)	0.065 (1.65)	0.103 (2.62)

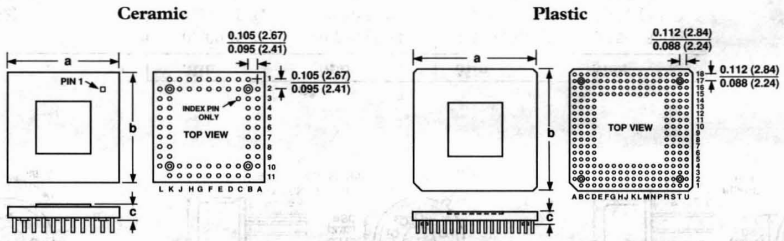
*For complete package dimensions see data sheet.



Flatpack (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
F-2A		2-Lead		0.250 (6.35)	0.081 (2.06)	0.093 (2.36)	0.044 (1.12)	0.066 (1.68)

*For complete package dimensions see data sheet.



Pin Grid Array (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
G-68A		68-Lead	1.080 (27.43)	1.110 (28.19)	1.080 (27.43)	1.110 (28.19)	0.123 (3.12)	0.164 (4.17)
G-100A		100-Lead	1.308 (33.22)	1.332 (33.83)	1.308 (33.22)	1.332 (33.83)		0.169 (4.29)
G-144A		144-Lead	1.559 (39.60)	1.591 (40.41)	1.559 (39.60)	1.591 (40.41)		0.914 (23.22)
G-223A		223-Lead	1.844 (46.84)	1.876 (47.65)	1.844 (46.84)	1.876 (47.65)	0.138 (3.51)	0.164 (4.17)

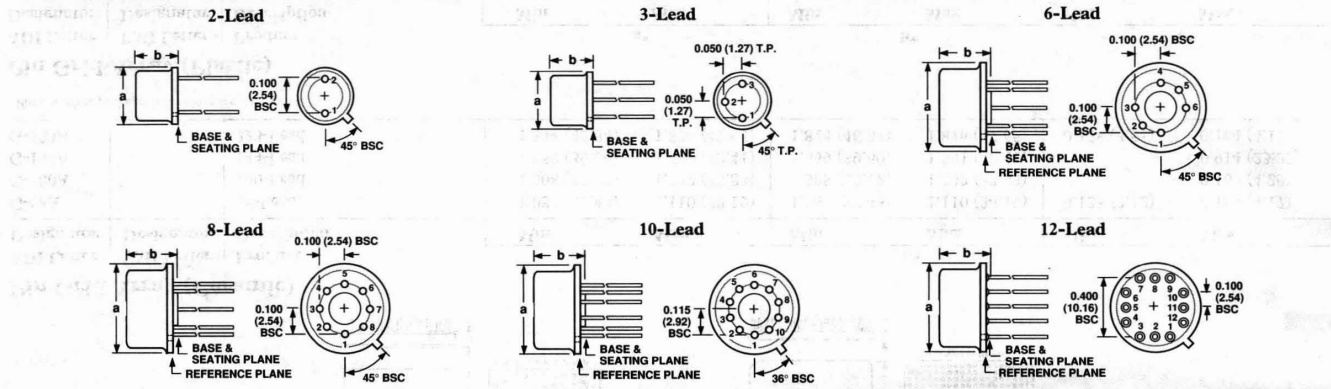
*For complete package dimensions see data sheet.

Pin Grid Array (Plastic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
223-PPGA		223-Lead	1.856 (47.14)	1.864 (47.35)	1.856 (47.14)	1.864 (47.35)	0.130 (3.30)	0.166 (4.22)

*For complete package dimensions see data sheet.

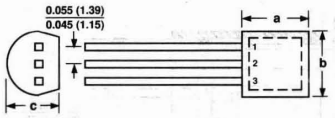
Package Information–Outline Dimensions



Metal Can

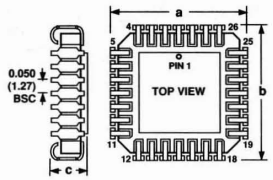
ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*	
			Min	Max	Min	Max
H-02A		2-Lead	0.209 (5.31)	0.230 (5.84)	1.125 (3.17)	0.150 (3.81)
H-03A		3-Lead (TO-52)	0.209 (5.31)	0.230 (5.84)	0.115 (2.92)	0.150 (3.81)
H-03B		3-Lead (TO-5 Style)	0.335 (8.51)	0.370 (9.40)	0.165 (4.19)	0.185 (4.70)
	H	6-Lead (TO-78)	0.335 (8.51)	0.370 (9.40)	0.175 (4.45)	0.230 (5.84)
H-08A	J	8-Lead (TO-99)	0.335 (8.51)	0.370 (9.40)	0.175 (4.45)	0.230 (5.84)
H-10A	K	10-Lead (TO-100)	0.335 (8.51)	0.370 (9.40)	0.175 (4.45)	0.230 (5.84)
H-12A		12-Lead (TO-8 Style)	0.592 (15.04)	0.615 (15.62)	0.148 (3.76)	0.226 (5.74)

*For complete package dimensions see data sheet.



Plastic TO-92

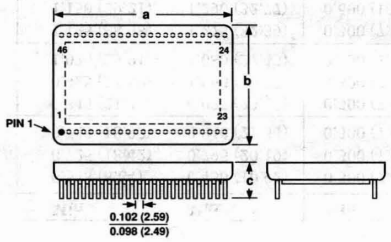
ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
TO-92		3-Lead	0.170 (4.32)	0.210 (5.33)	0.175 (4.45)	0.205 (5.21)	0.125 (3.18)	0.165 (4.19)



J-Leaded Chip Carrier

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
J-28		28-Lead	0.498 (12.65)	0.491 (12.47)	0.498 (12.65)	0.491 (12.47)		0.125 (3.18)
J-44		44-Lead	0.680 (17.27)	0.700 (17.78)	0.680 (17.27)	0.700 (17.78)	0.100 (2.54)	0.135 (3.43)
J-68		68-Lead	0.980 (24.89)	1.000 (25.4)	0.980 (24.89)	1.000 (25.4)	0.100 (2.54)	0.135 (3.43)

*For complete package dimensions see data sheet.

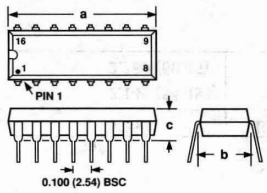


Metal Platform DIP

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
M-40		40-Lead		2.145 (54.483)		1.145 (29.083)		0.19 (4.83)
M-46		46-Lead		2.380 (60.45)		1.580 (40.13)		0.231 (5.87)

*For complete package dimensions see data sheet.

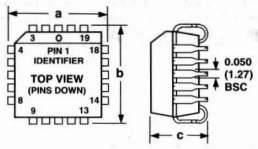
Package Information–Outline Dimensions



Plastic DIP

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
N-8	P	8-Lead	0.348 (8.84)	0.430 (10.92)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-14	P	14-Lead	0.725 (18.42)	0.795 (20.19)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-16	P	16-Lead	0.745 (18.92)	0.840 (21.34)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-18	P	18-Lead	0.845 (21.46)	0.925 (23.49)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-20	P	20-Lead	0.925 (23.50)	1.060 (26.90)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-22	P	22-Lead	1.020 (25.91)	1.080 (27.43)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-24	P	24-Lead	1.125 (28.58)	1.275 (32.39)	0.300 (7.62)	0.325 (8.26)		0.210 (5.33)
N-24A	P	24-Lead (Double Width)	1.150 (29.21)	1.290 (32.77)	0.600 (15.24)	0.625 (15.88)		0.250 (6.35)
N-24B		24-Lead	1.185 (30.10)	1.205 (30.60)	0.330 (8.40)	0.346 (8.80)		0.162 (4.10)
N-28	P	28-Lead	1.380 (35.10)	1.565 (39.75)	0.600 (15.24)	0.625 (15.88)		0.250 (6.35)
N-28A	P	28-Lead	1.440 (36.58)	1.450 (36.83)	0.594 (15.09)	0.606 (15.39)		0.200 (5.08)
N-40A	P	40-Lead		2.080 (52.83)	0.580 (14.73)	0.620 (15.75)		0.200 (5.08)
N-48	P	48-Lead	2.385 (60.58)	2.480 (62.99)	0.590 (14.99)	0.630 (16.00)		0.250 (6.35)

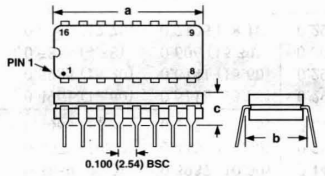
*For complete package dimensions see data sheet.



Plastic Leaded Chip Carrier (PLCC)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
P-20A	PC	20-Lead	0.385 (9.78)	0.395 (10.03)	0.385 (9.78)	0.395 (10.03)	0.165 (4.19)	0.180 (4.57)
P-28A	PC	28-Lead	0.485 (12.32)	0.495 (12.57)	0.485 (12.32)	0.495 (12.57)	0.165 (4.19)	0.180 (4.57)
P-44A		44-Lead	0.685 (17.40)	0.695 (17.65)	0.685 (17.40)	0.695 (17.65)	0.165 (4.19)	0.180 (4.57)
P-68A		68-Lead	0.885 (22.48)	0.995 (25.27)	0.885 (22.48)	0.995 (25.27)	0.169 (4.29)	0.175 (4.45)

*For complete package dimensions see data sheet.

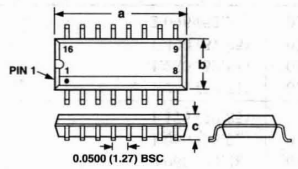


Cerdip

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
Q-8	Z	8-Lead		0.405 (10.29)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-14	Y	14-Lead		0.785 (19.94)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-16	Q	16-Lead		0.840 (21.34)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-18	X	18-Lead		0.960 (24.38)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-20	R	20-Lead		1.060 (26.92)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-22		22-Lead		1.175 (29.85)	0.390 (9.09)	0.420 (10.67)		0.200 (5.08)
Q-24	W	24-Lead		1.280 (32.51)	0.290 (7.37)	0.320 (8.13)		0.200 (5.08)
Q-24A		24-Lead (Wide Body)		1.280 (32.51)	0.590 (14.99)	0.620 (15.75)		0.200 (5.08)
Q-28	T	28-Lead		1.490 (37.85)	0.590 (14.99)	0.620 (15.75)		0.225 (5.72)
Q-40		40-Lead		2.096 (52.23)	0.590 (14.99)	0.63 (16.00)		0.225 (5.72)

*For complete package dimensions see data sheet.

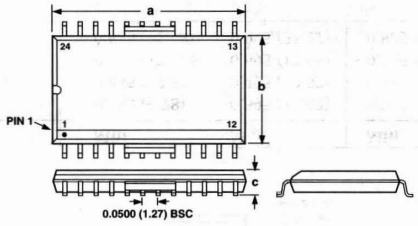
Package Information–Outline Dimensions



Small Outline (SO)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
R-8		8-Lead	0.1890 (4.80)	0.1968 (5.00)	0.1497 (3.80)	0.1574 (4.00)	0.094 (2.39)	0.102 (2.59)
SO-8	SO-8	8-Lead	0.1890 (4.80)	0.1968 (5.00)	0.1497 (3.80)	0.1574 (4.00)	0.0532 (1.35)	0.0688 (1.75)
R-14	SO-14	14-Lead	0.3367 (8.55)	0.3444 (8.75)	0.1497 (3.80)	0.1574 (4.00)	0.0532 (1.35)	0.0688 (1.75)
R-16A	SO-16	16-Lead	0.3859 (9.80)	0.3937 (10.00)	0.1497 (3.80)	0.1574 (4.00)	0.0532 (1.35)	0.0688 (1.75)
R-16	SOL-16	16-Lead (Wide Body)	0.3977 (10.10)	0.4133 (10.50)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-18	SOL-18	18-Lead	0.4469 (11.35)	0.4625 (11.75)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-20	SOL-20	20-Lead	0.4961 (12.60)	0.5118 (13.00)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-24	SOL-24	24-Lead	0.5985 (15.20)	0.6141 (15.60)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)
R-24A		24-Lead	0.586 (14.88)	0.606 (15.39)	0.205 (5.21)	0.221 (5.61)	0.067 (1.70)	0.089 (2.25)
R-28	SOL-28	28-Lead	0.6969 (17.70)	0.7125 (18.10)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)

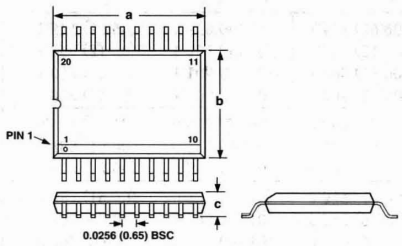
*For complete package dimensions see data sheet.



Thermally Enhanced SOIC

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
RB-24		24-Lead	0.5985 (15.20)	0.6141 (15.60)	0.2914 (7.40)	0.2992 (7.60)	0.0926 (2.35)	0.1043 (2.65)

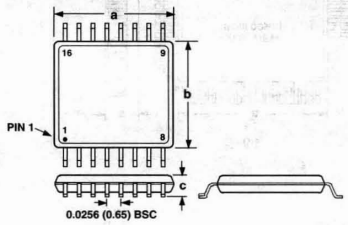
*For complete package dimensions see data sheet.



Shrink Small Outline Package (SSOP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
RS-20		20-Lead	0.271 (6.90)	0.295 (7.50)	0.205 (5.21)	0.212 (5.38)	0.068 (1.73)	0.078 (1.98)
RS-24		24-Lead	0.318 (8.08)	0.328 (8.33)	0.205 (5.21)	0.212 (5.38)	0.068 (1.73)	0.078 (1.98)
RS-28		28-Lead	0.397 (10.08)	0.407 (10.34)	0.205 (5.21)	0.212 (5.38)	0.068 (1.73)	0.078 (1.98)

*For complete package dimensions see data sheet.



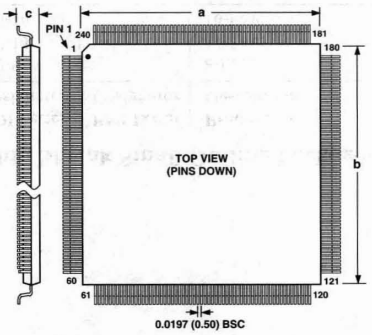
Thin Shrink Small Outline Package (TSSOP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
RU-8		8-Lead	0.114 (2.90)	0.122 (3.10)	0.169 (4.30)	0.177 (4.50)		0.0433 (1.10)
RU-14		14-Lead	0.193 (4.90)	0.201 (5.10)	0.169 (4.30)	0.177 (4.50)		0.0433 (1.10)
RU-16		16-Lead	0.193 (4.90)	0.201 (5.10)	0.169 (4.30)	0.177 (4.50)		0.0433 (1.10)
RU-20		20-Lead	0.252 (6.40)	0.260 (6.60)	0.169 (4.30)	0.177 (4.50)		0.0433 (1.10)
RU-24		24-Lead	0.303 (7.70)	0.311 (7.90)	0.169 (4.30)	0.177 (4.50)		0.0433 (1.10)
RU-28		28-Lead	0.378 (9.60)	0.386 (9.80)	0.169 (4.30)	0.177 (4.50)		0.0433 (1.10)

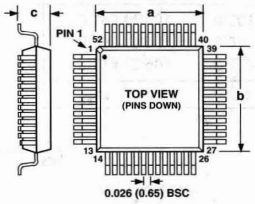
*For complete package dimensions see data sheet.

Package Information–Outline Dimensions

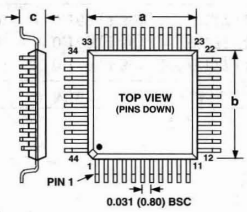
S-240, S-304



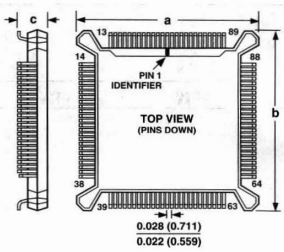
S-52, S-80, S-100, S-160



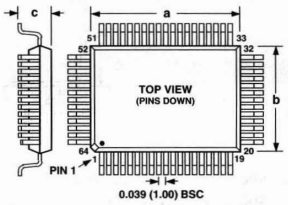
S-44, S-128



S-100A (Bumpered)



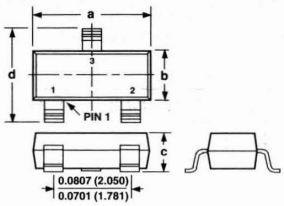
S-64



Plastic Quad Flatpack Package (PQFP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
S-44		44-Terminal	0.390 (9.90)	0.398 (10.10)	0.390 (9.90)	0.398 (10.10)		0.096 (2.45)
S-52		52-Terminal	0.390 (9.90)	0.398 (10.10)	0.390 (9.90)	0.398 (10.10)		0.096 (2.45)
S-64		64-Terminal	0.783 (19.90)	0.791 (20.10)	0.547 (13.90)	0.555 (14.10)		0.122 (3.40)
S-80		80-Terminal	0.547 (13.90)	0.555 (14.10)	0.547 (13.90)	0.555 (14.10)		0.096 (2.45)
S-100		100-Terminal	0.783 (19.90)	0.791 (20.10)	0.547 (13.90)	0.555 (14.10)		0.096 (2.45)
S-100A		100-Terminal (Bumpered)	0.897 (22.78)	0.903 (22.94)	0.897 (22.78)	0.903 (22.94)		0.180 (4.57)
S-128		128-Terminal	1.098 (27.90)	1.106 (28.10)	1.098 (27.90)	1.106 (28.10)		0.154 (3.92)
S-160		160-Terminal	1.098 (27.90)	1.106 (28.10)	1.098 (27.90)	1.106 (28.10)		0.154 (3.92)
S-240		240-Terminal**	1.256 (31.90)	1.264 (32.10)	1.256 (31.90)	1.264 (32.10)		0.161 (4.10)
S-304		304-Terminal	1.571 (39.90)	1.579 (40.10)	1.571 (39.90)	1.579 (40.10)		0.167 (4.50)

*For complete package dimensions see data sheet.
**Thermally Enhanced

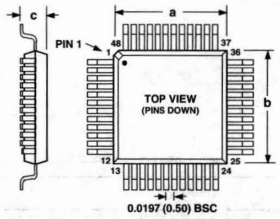


Surface Mount SOT-23

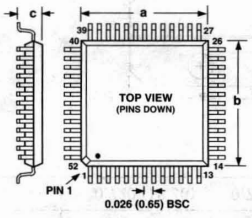
ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*		d*	
			Min	Max	Min	Max	Min	Max	Min	Max
SOT-23		3-Lead	0.1102 (2.799)	0.1200 (3.048)	0.0470 (1.194)	0.0550 (1.397)	0.0320 (3.30)	0.0440 (1.118)	0.0827 (2.101)	0.1040 (2.642)

*For complete package dimensions see data sheet.

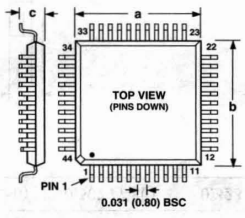
ST-48, ST-100, ST-128, ST-160



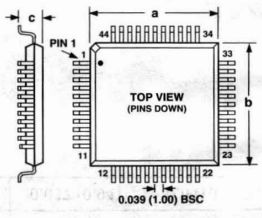
ST-52, ST-80



ST-44, ST-64



ST-44A

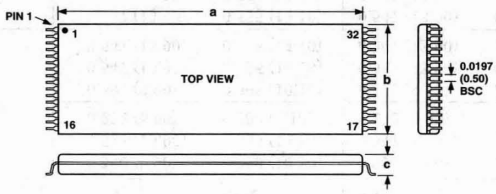


Thin Quad Flatpack Package (TQFP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
ST-44		44-Terminal	0.390 (9.90)	0.398 (10.10)	0.390 (9.90)	0.398 (10.10)		0.063 (1.60)
ST-44A		44-Terminal	0.547 (13.90)	0.555 (14.10)	0.547 (13.90)	0.555 (14.10)		0.063 (1.60)
ST-48		48-Terminal	0.272 (6.90)	0.280 (7.10)	0.272 (6.90)	0.280 (7.10)		0.063 (1.60)
ST-52		52-Terminal	0.390 (9.90)	0.398 (10.10)	0.390 (9.90)	0.398 (10.10)		0.063 (1.60)
ST-64		64-Terminal	0.547 (13.90)	0.555 (14.10)	0.547 (13.90)	0.555 (14.10)		0.063 (1.60)
ST-80		80-Terminal	0.547 (13.90)	0.555 (14.10)	0.547 (13.90)	0.555 (14.10)		0.063 (1.60)
ST-100		100-Terminal	0.547 (13.90)	0.555 (14.10)	0.547 (13.90)	0.555 (14.10)		0.063 (1.60)
ST-128		128-Terminal	0.547 (13.90)	0.555 (14.10)	0.547 (13.90)	0.555 (14.10)		0.063 (1.60)
ST-160		160-Terminal	0.941 (23.90)	0.947 (24.10)	0.941 (23.90)	0.947 (24.10)		0.063 (1.60)

*For complete package dimensions see data sheet.

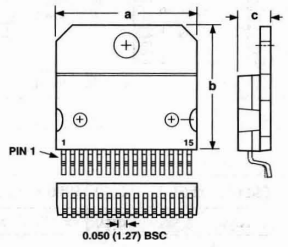
Package Information–Outline Dimensions



Thin Small Outline Package (TSOP)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
U-32		32-Lead	0.720 (18.30)	0.728 (18.50)	0.307 (7.80)	0.323 (8.20)	0.037 (0.94)	0.0410 (1.04)

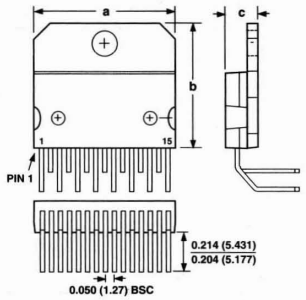
*For complete package dimensions see data sheet.



Surface-Mount Package (DDPAK)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
VR-15		15-Lead	0.778 (19.76)	0.798 (20.27)	0.684 (17.37)	0.694 (17.63)	0.172 (4.37)	0.182 (4.62)

*For complete package dimensions see data sheet.



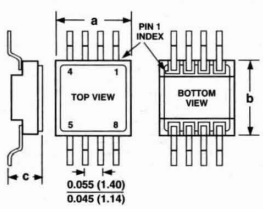
Through-Hole SIP With Staggered Leads

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
Y-15		15-Lead	0.778 (19.76)	0.798 (20.27)	0.684 (17.37)	0.694 (17.63)	0.172 (4.37)	0.182 (4.62)

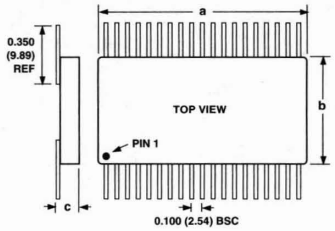
*For complete package dimensions see data sheet.

Package Information–Outline Dimensions

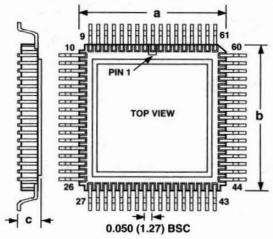
Z-8A, Z-16, Z-16A/B/C, Z-28



Z-40



Z-68



Leaded Chip Carrier (Ceramic)

ADI Letter Designator	PMI Letter Designator	Product Description	a*		b*		c*	
			Min	Max	Min	Max	Min	Max
Z-8A		8-Lead	0.250 (6.35)	0.260 (6.60)	0.250 (6.35)	0.260 (6.60)	0.018 (0.46)	0.098 (2.49)
Z-16		16-Lead	0.391 (9.93)	0.405 (10.29)	0.250 (6.35)	0.260 (6.60)		0.103 (2.62)
Z-16A		16-Lead	0.442 (11.23)	0.458 (11.63)	0.442 (11.23)	0.458 (11.63)	0.103 (2.62)	0.133 (3.38)
Z-16B		16-Lead	0.542 (13.77)	0.558 (14.17)	0.542 (13.77)	0.558 (14.17)	0.113 (2.87)	0.143 (3.63)
Z-16C		16-Lead	0.391 (9.93)	0.405 (10.29)	0.250 (6.35)	0.260 (6.60)	0.018 (0.46)	0.098 (2.49)
Z-28		28-Lead	0.710 (18.03)	0.730 (18.54)	0.490 (12.45)	0.510 (12.95)		
Z-40		40-Lead	2.074 (52.68)	2.116 (53.75)	1.079 (27.41)	1.101 (10.67)		0.217 (5.51)
Z-68		68-Lead	0.940 (23.88)	0.960 (24.38)	0.940 (23.88)	0.960 (24.38)	0.092 (2.34)	0.118 (2.997)

*For complete package dimensions see data sheet.

Appendix
Contents

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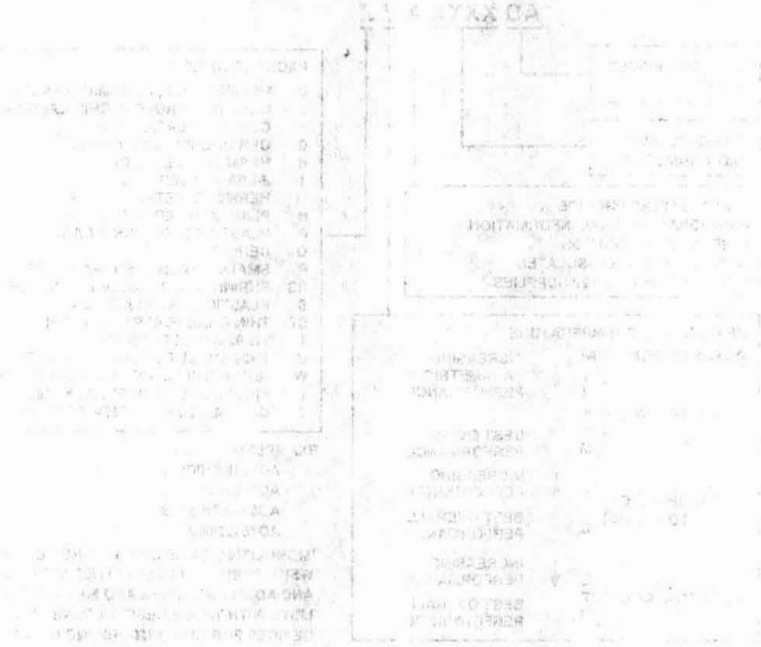
Product Families Still Available	30–4
Substitution Guide	30–5
Technical Publications	30–7
Worldwide Sales Directory	30–14
Faxcode Directory	30–16



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Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us, or one of our authorized distributors.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed on pages 30–14 and 30–15).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. This manual contains two model numbering schemes. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Santa Clara division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number,* an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Santa Clara division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

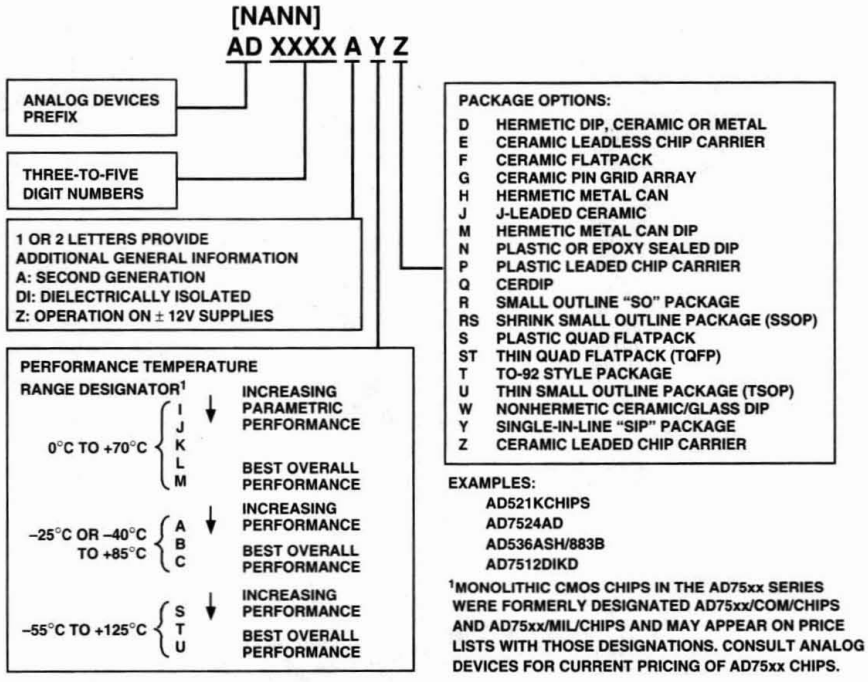
[NANN]
AD XXXX A Y Z
ANALOG DEVICES PREFIX
THREE-TO-FIVE DIGIT NUMBERS
1 OR 2 LETTERS PROVIDE ADDITIONAL GENERAL INFORMATION
A: SECOND GENERATION
DI: DIELECTRICALLY ISOLATED
Z: OPERATION ON ± 12V SUPPLIES
PERFORMANCE TEMPERATURE RANGE DESIGNATOR[1]
0°C TO +70°C
I J K L M
INCREASING PARAMETRIC PERFORMANCE
BEST OVERALL PERFORMANCE
–25°C OR –40°C TO +85°C
A B C
INCREASING PERFORMANCE
BEST OVERALL PERFORMANCE
–55°C TO +125°C
S T U
INCREASING PERFORMANCE
BEST OVERALL PERFORMANCE
PACKAGE OPTIONS:
D HERMETIC DIP, CERAMIC OR METAL
E CERAMIC LEADLESS CHIP CARRIER
F CERAMIC FLATPACK
G CERAMIC PIN GRID ARRAY
H HERMETIC METAL CAN
J J-LEADED CERAMIC
M HERMETIC METAL CAN DIP
N PLASTIC OR EPOXY SEALED DIP
P PLASTIC LEADED CHIP CARRIER
Q CERDIP
R SMALL OUTLINE "SO" PACKAGE
RS SHRINK SMALL OUTLINE PACKAGE (SSOP)
S PLASTIC QUAD FLATPACK
ST THIN QUAD FLATPACK (TQFP)
T TO-92 STYLE PACKAGE
U THIN SMALL OUTLINE PACKAGE (TSOP)
W NONHERMETIC CERAMIC/GLASS DIP
Y SINGLE-IN-LINE "SIP" PACKAGE
Z CERAMIC LEADED CHIP CARRIER
EXAMPLES:
AD521KCHIPS
AD7524AD
AD536ASH/883B
AD7512DIKD
[1]MONOLITHIC CMOS CHIPS IN THE AD75xx SERIES WERE FORMERLY DESIGNATED AD75xx/COM/CHIPS AND AD75xx/MIL/CHIPS AND MAY APPEAR ON PRICE LISTS WITH THOSE DESIGNATIONS. CONSULT ANALOG DEVICES FOR CURRENT PRICING OF AD75xx CHIPS.

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades Have the Added Suffix /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

*For some models, the combination [digit] [letter] [two or three digits] is used instead of ADXXXX, e.g. 2S80.

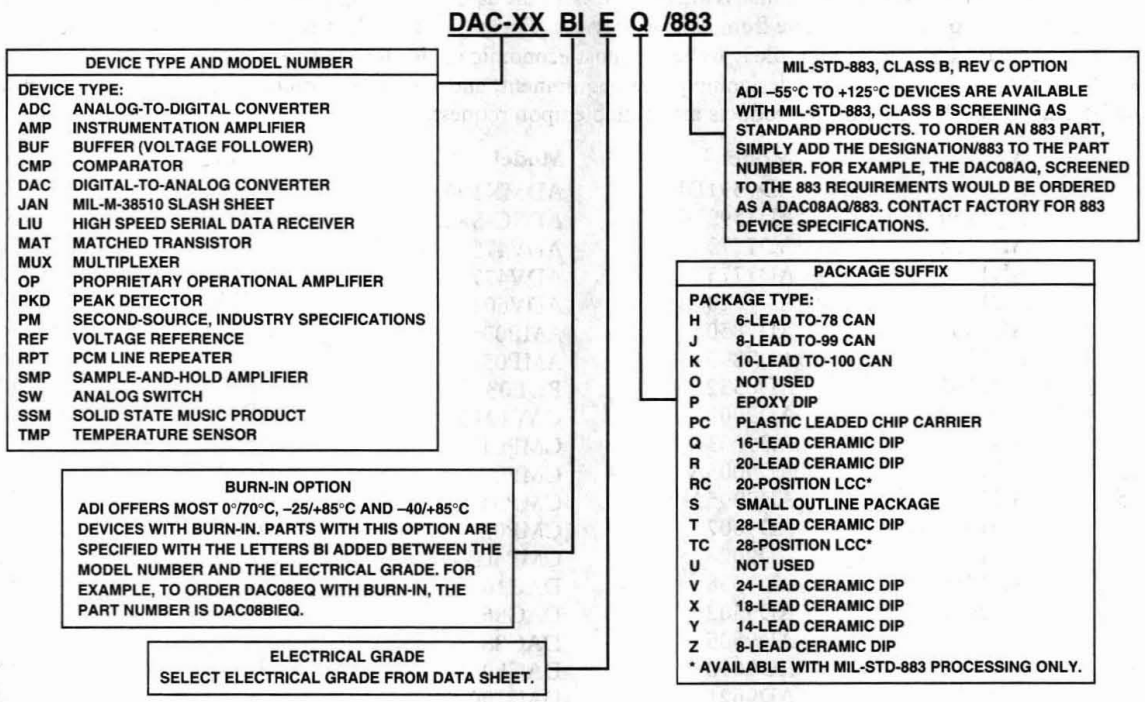
DAC-XX BI E Q /883
DEVICE TYPE AND MODEL NUMBER
DEVICE TYPE:
ADC ANALOG-TO-DIGITAL CONVERTER
AMP INSTRUMENTATION AMPLIFIER
BUF BUFFER (VOLTAGE FOLLOWER)
CMP COMPARATOR
DAC DIGITAL-TO-ANALOG CONVERTER
JAN MIL-M-38510 SLASH SHEET
LIU HIGH SPEED SERIAL DATA RECEIVER
MAT MATCHED TRANSISTOR
MUX MULTIPLEXER
OP PROPRIETARY OPERATIONAL AMPLIFIER
PKD PEAK DETECTOR
PM SECOND-SOURCE, INDUSTRY SPECIFICATIONS
REF VOLTAGE REFERENCE
RPT PCM LINE REPEATER
SMP SAMPLE-AND-HOLD AMPLIFIER
SW ANALOG SWITCH
SSM SOLID STATE MUSIC PRODUCT
TMP TEMPERATURE SENSOR
MIL-STD-883, CLASS B, REV C OPTION
ADI –55°C TO +125°C DEVICES ARE AVAILABLE WITH MIL-STD-883, CLASS B SCREENING AS STANDARD PRODUCTS. TO ORDER AN 883 PART, SIMPLY ADD THE DESIGNATION/883 TO THE PART NUMBER. FOR EXAMPLE, THE DAC08AQ, SCREENED TO THE 883 REQUIREMENTS WOULD BE ORDERED AS A DAC08AQ/883. CONTACT FACTORY FOR 883 DEVICE SPECIFICATIONS.
PACKAGE SUFFIX
PACKAGE TYPE:
H 6-LEAD TO-78 CAN
J 8-LEAD TO-99 CAN
K 10-LEAD TO-100 CAN
O NOT USED
P EPOXY DIP
PC PLASTIC LEADED CHIP CARRIER
Q 16-LEAD CERAMIC DIP
R 20-LEAD CERAMIC DIP
RC 20-POSITION LCC*
S SMALL OUTLINE PACKAGE
T 28-LEAD CERAMIC DIP
TC 28-POSITION LCC*
U NOT USED
V 24-LEAD CERAMIC DIP
X 18-LEAD CERAMIC DIP
Y 14-LEAD CERAMIC DIP
Z 8-LEAD CERAMIC DIP
* AVAILABLE WITH MIL-STD-883 PROCESSING ONLY.
BURN-IN OPTION
ADI OFFERS MOST 0°/70°C, –25/+85°C AND –40/+85°C DEVICES WITH BURN-IN. PARTS WITH THIS OPTION ARE SPECIFIED WITH THE LETTERS BI ADDED BETWEEN THE MODEL NUMBER AND THE ELECTRICAL GRADE. FOR EXAMPLE, TO ORDER DAC08EQ WITH BURN-IN, THE PART NUMBER IS DAC08BIEQ.
ELECTRICAL GRADE
SELECT ELECTRICAL GRADE FROM DATA SHEET.

Figure 2. Santa Clara Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory.

Eligible customers may place their orders through our regional customer service centers by dialing 1-800-262-5645 (U.S.A. only) or through our representatives or authorized distributors. (The telephone numbers for our representatives or authorized distributors are listed on pages 30–14 and 30–15.) Analog Devices' minimum order value is $1,000.00.

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Still Available

The information published in this Reference Manual is intended to assist the user in choosing components for the design of new equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are not likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model	Model	Model
AC1226	AD897	AD7591DI	ADMK100	OP09	RDC1741
AC2626	AD1139	AD7592DI	ADSC-SKD1	OP10	RDC1742
AD1B60	AD1154	AD7773	ADV475	OP11	REF05
AD2S34	AD1170	AD7775	ADV477	OP12	REF08
AD2S44	AD1175	AD7820	ADV601	OP14	REF10
AD2S46	AD1334	AD7850	AMP03	OP15	RPT82
AD2S65	AD1341	AD7895	AMP05	OP16	RPT83
AD2S66	AD1362	AD8532	BUF03	OP17	RPT85
AD2S75	AD1376	AD9000	CAV1210	OP20	RPT86
AD20msp511	AD1377	AD9003	CMP01	OP21	RPT87
AD20msp512	AD1378	AD9003A	CMP02	OP22	SDC1740
AD20msp815	AD1846	AD9005A	CMP05	OP32	SDC1741
AD246	AD1848	AD9007	CMP08	OP41	SDC1742
AD346	AD1856	AD9028	CMP404	OP43	SMP10
AD363	AD1860	AD9038	DAC10	OP44	SMP11
AD364	AD2010	AD9502	DAC86	OP50	SMP81
AD365	AD2700	AD9505	DAC88	OP61	SSM2013
AD380	AD2701	AD9610	DAC89	OP64	SSM2014
AD386	AD2702	AD9621	DAC100	OP80	SSM2015
AD389	AD2710	AD9622	DAC210	OP160	SSM2016
AD390	AD2712	AD9623	DAC888	OP207	SSM2018
AD394	AD5210 Series	AD9624	DAC1136	OP215	SSM2100
AD395	AD5254	AD9701	DAC1138	OP260	SSM2110
AD396	AD5539	AD9760	DAC1146	OP420	SSM2131
AD503	AD7001	AD9762	DAC1408A	OP421	SSM2132
AD504	AD7110	AD75062	DAS1152	OSC1758	SSM2134
AD506	AD7228	AD75068	DAS1153	PKD01	SSM2139
AD507	AD7240	AD79015	DAS1157	PM108/208/308	SSM2300
AD510	AD7245	AD ADC71	DAS1158	PM111	SW01/02
AD517	AD7248	AD ADC72	DAS1159	PM119	SW06
AD518	AD7341	AD ADC80	DRC1745	PM139	SW201
AD521	AD7371	AD ADC84	DRC1746	PM139A	SW202
AD522	AD7501	AD ADC85	HDS1240E	PM155	1S74
AD532	AD7502	ADC910	HDS1250	PM155A	281
AD533	AD7503	ADC912A	HOS050/050A/050C	PM156	284J
AD535	AD7506	ADC1130	HOS060	PM156A	286J
AD545	AD7507	ADC1131	HTC0300A	PM157	289
AD562	AD7520	ADC1140	HTS0010	PM157A	290A
AD563	AD7522	ADC1143	HTS0025	PM211	292A
AD567	AD7523	AD DAC71	IPA1764	PM219	2B20
AD572	AD7525	AD DAC72	JM38510/11301/11302	PM239	2B22
AD578	AD7541A	AD DAC80	LIU01	PM355	2B23
AD579	AD7542	AD DAC85	MUX08	PM356	2B30
AD582	AD7543	AD DAC86	MUX16	PM1012	2B31
AD611	AD7545	AD DAC87	MUX24	PM6012	2B50
AD671	AD7545A	ADDG815	MUX28	PM7524	2B54
AD744	AD7546	ADEB770	MUX88	PM7528	2B55
AD796	AD7548	ADG506A	OP01	PM7533	2S50
AD875	AD7572	ADG507A	OP02	PM7541A	2S54
AD890	AD7574	ADG529A	OP04	PM7543	2S56
AD891	AD7576	ADG529F	OP05	PM7545	2S58
AD892E	AD7586	ADM210	OP06	PM7548	755
AD892T	AD7590DI	ADM212E	OP08	PM7574	759

Substitution Guide

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD28msp01	AD1843/45	AD528	OP42	AD7544	AD7548
AD28msp02	None	AD530	AD633	AD7550	AD7713
AD101A	OP176	AD531	AD532	AD7552	AD7713
AD108/208/308	AD705	AD540	AD711	AD7555	AD7713
AD108A/208A/308A	AD705	AD559	AD557/AD558	AD7560	ADM660/8660
AD111/211/311	AD790	AD565	AD565A	AD7570	AD7776
AD201A	OP176	AD566	AD566A	AD7571	AD7896
AD206	None	AD575	AD573	AD7583	AD7890
AD230	ADM230L	AD583	AD585	AD7591	AD7590/92
AD231	ADM201A	AD612	AD524	AD7772	AD7776
AD232	ADM232A	AD614	AD524	AD7775	None
AD233	None	AD651	AD650/AD654	AD9006	None
AD234	ADM204A	AD674A	AD674B	AD9011	AD9002
AD235	None	AD682	AD684	AD9016	None
AD236	ADM206A	AD689	AD589	AD9521	AD640
AD237	ADM207A	AD707	OP177	AD9611	AD9632
AD238	ADM208A	AD770	AD9002	AD9686	AD9696
AD239	ADM209A	AD801	AD711	AD9615	AD9617
AD241	ADM241L	AD1145	AD7846	AD9685	AD96685
AD293	AD210	AD1147/48	AD669	AD9687	AD96686
AD294	AD210	AD1175	AD7713	AD9688	AD9002/AD9028
AD295	AD210	AD1321	AD1324	AD9703	None
AD301A	OP176	AD1322	AD1324	AD9950	None
AD301AL	OP176	AD1332	None	AD9955	None
AD345	AD1321/1324	AD1408	AD558	AD ADC816	AD7820/AD7821
AD351	AD790	AD1508	AD558	AD DAC08	DAC08
AD362	AD1362	AD1678	AD678	AD DAC100	DAC100
AD367	None	AD1679	AD679	ADC908	None
AD368	None	AD1779	AD779	ADG200	None
AD369	None	AD1885	None	ADG201	ADG201A
AD370/371	AD767	AD2006	None	ADLH0032G/CG	AD843
AD376	AD1376	AD2020	None	ADLH0033G/CG	BUF04
AD381	AD744	AD3554	AD843/AD845	ADM501	AD843
AD382	AD744/AD845	AD3860	AD567	ADM203A	None
AD392	AD664	AD5010/6020	AD9000	ADM205A	None
AD395/883B	AD394/883B	AD5201	AD1672	ADM233L	None
AD501	AD711	AD5202	AD5212	ADM235L	None
AD502	AD711	AD5204	AD5214	ADP501	None
AD505	AD817	AD5205	AD5215	ADREF01	REF01
AD506SH/883B	OP42AJ/883	AD5211	AD578	ADREF02	REF02
AD507	AD841	AD5240	AD ADC85	ADSHC85	AD585
AD507SH/883B	AD841	AD6012	AD565A	ADSHM5	HTC0300A
AD508	OP177	AD7005	AD7011/AD7013	ADSP-1008A	None
AD509	AD841	AD7115	AD7111	ADSP-1009A	None
AD511	AD711	AD7513	ADG201A	ADSP-1010A	None
AD512	OP97	AD7516	AD7510DI	ADSP-1010B	None
AD513	AD711	AD7519	None	ADSP-1012A	None
AD514	AD711	AD7521	AD7541A	ADSP-1016A	None
AD516	AD711	AD7527	AD7548	ADSP-1024A	None
AD520	AD524	AD7530	AD7533	ADSP-1080A	None
AD523	AD549A	AD7531	AD7541A	ADSP-1081A	None

Model	Closest Recommended Equivalent
ADSP-1101	None
ADSP-1110A	None
ADSP-1401	None
ADSP-1402	None
ADSP-1410	None
ADSP-2102	None
ADSP-2106	None
ADSP-2112	None
ADSP-3128A	None
ADSP-3201	None
ADSP-3202	None
ADSP-3210	None
ADSP-3211	None
ADSP-3212	None
ADSP-3220	None
ADSP-3221	None
ADSP-3222	None
ADSP-21msp50	ADSP-21msp58/59
ADSP-21msp51	None
ADSP-21msp55	ADSP-21msp58/59
ADSP-21msp56	ADSP-21msp58/59
ADSP-21010	ADSP-21020
ADV7141	None
ADV7146	None
ADV7148	None
AMP01BX	AMP01AX
AMP01BX/883C	AMP01AX/883C
AMP05BX	AMP05AX
AMP05BX/883C	AMP05Z/883C
BUF03BJ/883C	BUF03AJ/883C
CAV0920/1020	AD9020/9060
CAV1202	AD9223
CAV1205	AD871
CMP01Z	CMP01J
CMP05BJ	CMP05CJ
CMP05BZ	CMP05CZ
CMP05GJ	CMP05CJ
CMP404BY	CMP404AY
CMP404BY/883C	CMP404AY/883C
DAC01	None
DAC02/03	None
DAC05/06	None
DAC10BX	DAC10FX
DAC10CX	DAC10GX
DAC20	None
DAC100AAQ7	DAC100ACQ7
DAC100AAQ8	DAC100ACQ8
DAC100ABQ7	DAC100ACQ7
DAC100ABQ8	DAC100ACQ8
DAC100BBQ5/883C	DAC100ACQ5/883C
DAC100BCQ7	DAC100BBQ7
DAC100DDQ7	DAC100CCQ7
DAC312BR	DAC312ER
DAC888AX	DAC888EX
DAC888BX	DAC888EX
DAC1408-6P	DAC1408-8P
DAC1408-7P	DAC1408-8P
DAC1408-7Q	DAC1408-8Q
DAC1408-GQ	DAC1408-8Q
DAC1420	None
DAC1422	None
DAC1423	None
DAC1508A	DAC1408A
DAC1508A-8Q	DAC1408-8Q
DAC8012	AD7945
DAC8212	AD7247
HAS0802	AD7821
HAS1002	AD1672
HAS1202	AD1672
HDD1015	AD9720
HDD1409	AD768
HDG0805	AD7128
HDH0802	AD9720
HDH1003	AD9720
HDH1205	AD9713B
HDL3805	ADV453/ADV478
HDL3806	ADV453/ADV478
HDM1210	AD668/AD9713B
HDS0810E	ADV7128
HDS0820	ADV7128
HDS1015E	ADV7128
HDS1025	ADV7128
HOS100AH/SH	BUF04
HOS200	AD9620/30
HTC0300	HTC0300A
HTC0500	HTC0300A
IRDC1730-33	AD2S80A/82A
MAH0801	AD9005
MAH1001	AD9005
MAS0801	AD9005
MAS1001	AD9005
MAS1202	AD9005
MAT01/883C	MAT01AH/883C
MAT02BH	MAT02AH
MAT02BH/883C	MAT02AH/883C
MUX08AQ	MUX08BQ
MUX24AQ	MUX24EQ
MUX24BQ	MUX24FQ
MUX16AT	MUX16ET
MUX16BT	MUX16FT
OP01HJ	OP01J
OP01HZ	OP01HP
OP02BJ	OP02AJ
OP02BJ/883C	OP02AJ/883C
OP02EJ	OP07DJ
OP02EP	OP177GP
OP02EZ	OP177GZ
OP02J	OP02AJ
OP02/883C	OP02AZ/883C
OP04DY	OP04CY
OP04GBC	OP04NBC
OP04Y/883C	OP04AY/883C
OP05Z	OP05AZ
OP05/883C	OP05AZ/883C
OP06BJ/883C	OP06AJ/883C
OP06EZ	OP06GZ
OP06FZ	OP06GZ
OP08AJ	PM1008AJ
OP08AJ/883C	PM1008AJ/883C
OP08AZ/883C	PM1008AZ/883C
OP08CZ/883C	PM1008AZ/883C
OP08EJ	PM1008EJ
OP08EZ	PM1008EZ
OP09ARC/883C	OP11ARC/883C
OP09FY	OP09EY
OP12BZ	OP12AZ
OP12CZ	OP12AZ
OP12GZ	OP12FZ
OP14DZ	OP14CZ
OP14GRBC	OP14GBC
OP14J/883C	OP14AJ/883C
OP15BJ	OP15AJ
OP15BZ	OP15AZ
OP16BJ	OP16AJ
OP17BZ/883C	OP17AZ/883C
OP17CJ	OP17AJ
OP17FJ	OP17EJ
OP17FZ	OP17EZ
OP20CJ	OP20BJ
OP21GRBC	OP21GBC
OP215BJ	OP215AJ
OP215BJ/883C	OP215AJ/883C
OP215BZ	OP215AZ
OP215CZ/883C	OP215BZ/883C
OP21BJ	OP21AJ
OP21BZ	OP21AZ
OP21EJ	OP21AJ
OP220BJ	OP220AJ
OP22AJ	OP22AJ/883C
OP22EJ	OP22AJ/883C
OP32	OP193/OP196
OP65	AD817
OP111	AD795
OP147	AD817
OP160	AD811
OP166	AD811
PM148/248	OP495
PM562	AD565A/566A
PM725	OP177
PM741	OP195
PM0820	None
PM6012	AD568/668
PM7224	AD7224
PM7541	AD7541A
PM7542	AD7542
PM7645	AD7545A
SHA1144	None
SSM2044	None
SSM2045	None
SSM2047	None
SW7510/7511	AD7510/11

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In addition to the free publications, a group of technical reference books are available at reasonable cost. Subsystem products are supported with hardware, software, and user documentation, at prices related to content.

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DSP/MSP PRODUCTS REFERENCE MANUAL—1995. A 622-page databook on products for digital- and mixed-signal processing. Includes General Information, Signal-Processing Products, Sound-Processing Products (Computer Audio), Sound-Processing Products (Digital Audio), Technical Support, Application Notes.

DESIGN-IN REFERENCE MANUAL—1994. The sixth volume in ADI's reference manual series. Comprising 2400 pages of selection trees, selection guides and data sheets to all new ADI products introduced after the publication of Amplifier, Special Linear, and Data Converter Reference Manuals.

APPLICATIONS REFERENCE MANUAL—1993. A 1,344-page collection of 210 application notes, technical articles, and other design tutorials on such topics as audio and video circuits, A/D and D/A conversion, data acquisition and signal conditioning, digital signal processing, sigma-delta conversion, and much more. Cross-indexed by topic, product, subject, and application note number.

AMPLIFIER REFERENCE MANUAL—1992. Data sheets and selection guides to Operational Amplifiers, Comparators, Instrumentation Amplifiers, Isolation Amplifiers, Mixed-Signal ASICs, Power Supplies.

SPECIAL LINEAR REFERENCE MANUAL—1992. Data sheets and selection guides to Analog Multipliers/Dividers, Signal Compression Components, RMS-to-DC Converters, Mass Storage Components, ATE Components, Special Function Components, Matched Transistors, Temperature Sensors, Signal Conditioning Components, Automotive Components, Digital Signal Processing Products, Mixed-Signal ASICs, Power Supplies.

DATA CONVERTER REFERENCE MANUAL—1992: Volumes I and II. Data sheets and selection guides on A/D and D/A Converters, V/F and F/V Converters, Synchro/Resolver-to-Digital Converters, Sample/Track-Hold Amplifiers, Switches and Multiplexers, Voltage References, Data-Acquisition Subsystems, Analog I/O Ports, Communications Products, Bus Interface and I/O Products, Application-Specific ICs, Digital Panel Meters, Power Supplies.

*POWER SUPPLIES**—Linear Supplies •DC-DC Converters. 12-page Short Form Catalog listing AC/DC Power Supplies, Modular DC/DC Converters, Power-Supply Test Procedures, Transients, Thermal Derating, Mechanical Outlines of Packages and Sockets.

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"Embedded Shock and Temperature Recorder" [AN-383]
"Increasing the Frequency Response of the ADXL Series Accelerometers" [AN-377]
"Make Wide Temperature Range, Ultralow Drift Accelerometers Using Low Cost Crystal Ovens" [AN-385]
"Mounting Considerations for the ADXL Series Accelerometers" [AN-379]
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"Evaluation Board for the AD7701/AD7703 Sigma-Delta A/D Converters" [AN-368]
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"FIFO Operation and Boundary Conditions in the AD1332 and AD1334" [E1355]
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"Applications of the SSM2120 Dynamic Range Processor" [AN-382]
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"8th Order Programmable Low-Pass Filter Using Dual 12-Bit DACs" [AN-209]
"Exploring the AD667 12-Bit Analog Output Port" [E875]
"Gain Error and Tempco of CMOS Multiplying DACs" [E630C]
"Generate 4 Channels of Analog Output Using AD7542 12-Bit D/A Converters and Control the Lot with Only Two Wires" [AN-328]
"Interfacing the AD7549 Dual 12-Bit DAC to the MCS-48 and MCS-51 Microcomputer Families" [E941]
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Instrumentation Amplifier Application Guide, by Charles Kitchin and Lew Counts. Its 44-pages include basic instrumentation-amplifier ("in-amp") theory, design considerations, applications, specifications, and products—plus a brief bibliography and two indexes (by topic and by device model number).

Key Products Overview–Standard Linear Products. A 102-page brochure.

Low-Power Analog-to-Digital Converters. An 8-page reference guide to power-saving ADCs.

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Personal Sound Architecture. An 8-page brochure describing a programmable architecture for integrating sound into personal computers using software-based technologies and IC chipsets (including Analog Devices' DSPs, codecs, and other peripherals) for sound cards.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Sampling Analog-to-Digital Converter Integrated Circuits—1992 Short Form Selection Guide. Its 28 pages cover 35 different models with resolutions from 8 to 16 bits, and 12-bit resolution up to 20 MSPS. Besides block diagrams and key specs of each product, the booklet includes a detailed discussion of selection issues and a selection table sorted by resolution and speed.

A Selection Guide for Serial DACs. Eight pages of Serial 8-/16-bit DACs for supplies from +3 to ±15 V.

Single Supply Amplifier Guide. A card summarizing single-supply amplifiers available from ADI in Fall '95.

Signal Chain Guide, Volume 1, 1996. A 56-page brochure providing a means for selecting all of the appropriate Analog Devices Standard Linear Products from the Signal Chain System perspective.

Solutions for GSM/DCS–1800/DCS–1900. A 12-page brochure on chips and chipsets for wireless. Includes a glossary of wireless "buzzwords," such as TCH-HS.

Surface Mount IC. * A 28-page guide to ICs in SO and PLCC packages. Products include op amps, rms-to-dc converters, DACs, ADCs, VFCs, sample-holds and CMOS switches.

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ADSP-21020 USER'S MANUAL. [Floating-point processor] Introduction; Computational Units; Program Sequencing; Data Addressing; Timer; Memory Interface; Instruction Summary; Assembly Programmer's Tutorial; Hardware System Configuration; Appendixes; Index. Contains 394 pages.

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